Development of a Radiation Hard, Fully Depleted CMOS Monolithic Active Pixel Sensor (MAPS) on 50micron thick High Resistivity Silicon Using SBIR Funding

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LBNL Project Presentation, October 1 2015
• About SCI
• SCI’ deep depletion process
• Overview of SBIR Project
• SCI camera
About Sensor Creations, Inc. (SCI)

• Founded by Stefan Lauxtermann in 2010
• Located in Southern California
• Affordable, ROIC and image sensor design
  – Design (in house)
  – Fabrication (through CMOS fab partner)
  – Test (in house)
  – Prototype and low volume packaging (in house)
• Extensive suite of silicon proven IP blocks available today
  – Low noise snapshot shutter pixels with multi frame storage
  – Low noise readout chain programmable
  – Serial interface (SPI)
  – 14bit high speed, low power column parallel ADC (measured)
  – High speed I/O port with 1Gbit/sec (measured)
• Fully depleted backside illuminated CMOS imagers
  – Custom designs
  – Products
• Prototype Cameras
SCI’s Custom Pixels Typically Provide Functionality Beyond Classical Intensity Measurement

Examples of added functionality:
- Binning
- Multi Frame Sampling
- Signal discrimination
- <100nsec exposure time control
SCI uses Tanner EDA Design System

1. Schematic entry
2. Simulation
3. Layout
4. Block level verification
5. 2D/3D parasitic extraction
6. Top level verification

8” wafer with large format ROIC designed by SCI, (MacDougal et al, DSS 2012)

Designs with > 45M Transistors and Layout Area >22 x 32 mm² have been realized successfully
Advantages of Deep Depletion CMOS Technology

- High NIR response
  - Up to 40% at $\lambda = 1069$ nm (with 500μm thick silicon)
- High UV response
  - > 30% at $\lambda = 300$nm
- High broad band response
  - peak QE > 90%
- Direct detection of high energy radiation
  - X-ray < 20k eV
  - MIP (Minimum Ionizing Particle) for tracking
- Suited for very large format arrays
  - High yield compared to Hybrid FPAs
  - High data rate compared to CCD
  - Small pixel pitch (Nyquist MTF: 200μm thick silicon, 100V bias: 4.5μm)
- High Snapshot Shutter Efficiency
- Manufactural in standard CMOS foundry

Deep depletion CMOS Imagers Provide Scientific Sensor Performance with a Fabrication Price of a Mobile Phone Camera
Application for Deep Depletion CMOS Imagers

Hyperspectral Imaging in Remote Sensing Applications

NIR Laser Ranging

Direct X-Ray Detection

Benefits of DD-CMOS

- High NiR sensitivity
- nsec response time
- High X-ray sensitivity
- Low noise at high speed

NIR Night Vision

Nsec Fluorescence Lifetime imaging
Charge Collection Region Defined by Lateral and Vertical Depletion
Comparison of Deep Depletion MAPS Technology

- hybrid FPA
- 3D-IC
- Custom EPI layer (no backside contact)
- monolithic CMOS on high rho silicon
Comparison of Deep Depletion MAPS Technology

SCI’s Approach Combines Excellent Performance with Highest Manufacturability
## Comparison Summary of MAPS Technologies

<table>
<thead>
<tr>
<th></th>
<th>Hybrid FPA (a)</th>
<th>3D-IC (b)</th>
<th>EPI on SOI (c)</th>
<th>SCI technology (d)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Detector material</strong></td>
<td>high $\rho_{\text{Si}}$ wafer</td>
<td>high $\rho_{\text{Si}}$ wafer</td>
<td>high $\rho_{\text{Si}}$ EPI</td>
<td>high $\rho_{\text{Si}}$ wafer</td>
</tr>
<tr>
<td><strong>Detector thickness</strong></td>
<td>&lt;500 $\mu$m</td>
<td>&lt;500 $\mu$m</td>
<td>~ 25$\mu$m</td>
<td>&lt;500 $\mu$m</td>
</tr>
<tr>
<td><strong>Backside Electrode</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Photodiode speed</strong></td>
<td>high</td>
<td>high</td>
<td>medium</td>
<td>high</td>
</tr>
<tr>
<td><strong>Volume fabrication</strong></td>
<td>poor</td>
<td>good</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td><strong>CMOS fab compatibility</strong></td>
<td>poor</td>
<td>medium</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td><strong>Achievable noise</strong></td>
<td>medium</td>
<td>low</td>
<td>low</td>
<td>low</td>
</tr>
<tr>
<td><strong>Volume fabrication cost</strong></td>
<td>high</td>
<td>high</td>
<td>medium</td>
<td>low</td>
</tr>
</tbody>
</table>

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**Monolithic MAPS on High Resistivity Bulk Silicon Promise Best Overall Performance but is the Least Developed Technology**
Deep Depletion Sensor Development

1. Selection of silicon material
2. Development of Process Recipe
3. Verification of Device Functionality
4. IC Design
5. CMOS Fabrication and wafer thinning
6. Definition of AR coating layers on backside

Deep Depletion CMOS Development is a Very Interdisciplinary Effort
SBIR Project Objectives

• Develop active Minimum Ionizing Particle (MIP) detector using one of SCI’s Existing Monolithic Deep Depletion Sensors
  – This is the equivalent of a MAPS

• Develop passive MIP detector array in SCI’s deep depletion CMOS technology
  – Will be connected to FE-I4 readout for independent verification

• Characterize Detection Efficiency of active and passive detector arrays
  – To be done with 10GeV e\(^-\) from SLAC test beam facility (LBNL)

• Propose full size MAPS detector arrays to be developed in phase 2 of the SBIR project
Functionality of Monolithic MAPS

- Charge amplification
- Signal discrimination

MAPS Demonstrator will Provide Functionality of Classical MIP Detector
• SCI technology demonstration camera with deep depletion sensor (left) will be converted into particle detection system

All Hard- and Software Required for Technology Characterization will be Developed during phase 1 of the SBIR project
• Independent verification of SCI’s deep depletion technology for MIP particle tracking applications using the well characterized FE-I4 readout system.
What are the Challenges?

- Thick bulk detector layer must be completed depleted without punch through to backside
- Photodiodes must not short out laterally
  - Note: Electrons are collected in N type material
A single deep pwell is used to isolate circuitry from the high resistivity silicon sensing membrane. Electrons are collected very fast by lateral and vertical drift fields.

Deep Depletion Sensor is 3D structure with vertical and lateral Parasitic Bipolar Transistors.
Detection Efficiency for a collection time of 10nsec as a function of accumulated neutron irradiation for a 20μm thick detector. Charge Collection decreases with increasing radiation damage but can be compensated in high rho silicon by increasing detector backside bias.
Reverse bias IV characteristic measured on one of our 50 µm thick, 1mm² large test structures fabricated in SCI’s high rho silicon CMOS process.

Monolithic Detectors Can Be Reverse Biased with < -25V
How to Collect electrons in N-- Substrate?

- Neighboring N⁺ regions with different potential can easily short in high rho silicon

N⁺ regions must be Sufficiently Isolated Through Implants or/and Bias to Avoid Lateral Breakdown
• Current on IPD decreases when VB is decreased
  – Stronger reverse bias decrease of VB is also required to compensate for radiation damage
**SCI Deep Depletion BSI Camera**

- GigE or WiFi Interface
- C- or F- mount
- CameraLink available upon request
- Internet browser for display and camera control
  - No driver installation required

**Camera provides easy access to this new image sensor technology for early adopters**

*Sample image taken with this camera (raw data)*
First Images, 50um thick sensor – Example 1

- Correction: 2 point NUC
- Integration time: 15.11 msec (66Hz frame rate)
- F/#: 5.6
Curved line pattern under flat field illumination
  - Reported before in deep depletion CCDs → tree rings
    - Steve Holland et al., LBNL
Caused by inhomogeneity in silicon resistivity during crystal growth
  - Phenomenon in all deep depletion sensors

Tree Rings Disappear when Reverse Bias is Increased
# Deep Depletion Sensor Camera Performance Targets

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Format</td>
<td>640 X 512</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>15 µm</td>
</tr>
<tr>
<td>Die Size</td>
<td>11.2 X 12.2 mm²</td>
</tr>
<tr>
<td>Die Thickness</td>
<td>50 µm, 100 µm, 200 µm</td>
</tr>
<tr>
<td>Exposure time control</td>
<td>snapshot shutter: ITR, IWR, NDR</td>
</tr>
<tr>
<td>Charge Capacity</td>
<td>programmable</td>
</tr>
<tr>
<td>minimum</td>
<td>10k e⁻ (high gain)</td>
</tr>
<tr>
<td>medium</td>
<td>60k e⁻ (high gain)</td>
</tr>
<tr>
<td>maximum</td>
<td>500Ke (low gain)</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td></td>
</tr>
<tr>
<td>high gain</td>
<td>10e⁻</td>
</tr>
<tr>
<td>medium gain</td>
<td>30e⁻</td>
</tr>
<tr>
<td>low gain</td>
<td>130e⁻</td>
</tr>
<tr>
<td>Windowing</td>
<td>horizontal center to outsides, bottom to top</td>
</tr>
<tr>
<td>minimum</td>
<td>1 rows x 24 columns minimum</td>
</tr>
<tr>
<td>increments</td>
<td>1 rows, 24 columns</td>
</tr>
<tr>
<td>Integration Time range</td>
<td>100nsec to 30 msec</td>
</tr>
<tr>
<td>Output</td>
<td>analog (through 1,2, 4 or 8 output ports)</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>1000 Hz (when using all 8 output ports)</td>
</tr>
<tr>
<td>Output data rate</td>
<td>5MPixel/sec - 41MPixel/sec</td>
</tr>
<tr>
<td>Number of output channels</td>
<td>1, 2, 4 or 8 (programmable)</td>
</tr>
<tr>
<td>Master Clock</td>
<td>2.5 - 20.5 MHz</td>
</tr>
<tr>
<td>Binning</td>
<td>2x2, 2x1, 1x2</td>
</tr>
<tr>
<td>Power (120Hz, 60Hz, 30Hz)</td>
<td>60mW @ 60Hz frame rate</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.3/1.8</td>
</tr>
<tr>
<td>Logic I/O levels</td>
<td>0.0V/3.3V</td>
</tr>
<tr>
<td>Serial Interface</td>
<td>3 wire (multiple long word of different length)</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>300K</td>
</tr>
</tbody>
</table>
Thank You for your attention!
Potential Underneath 50 micron thick Photodiode Array

- Full Depletion and Pixel isolation on front side achieved
### Summary of specifications for the proposed SBIR phase 1 MAPS demonstrator

<table>
<thead>
<tr>
<th>#</th>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Type of Detector</td>
<td>high rho MAPS</td>
<td>Monolithic Active Pixel Sensor (MAPS on high resistivity silicon)</td>
</tr>
<tr>
<td>2</td>
<td>CMOS process</td>
<td>180nm</td>
<td>this is the technology node but a modified process flow applies</td>
</tr>
<tr>
<td>3</td>
<td>Silicon material</td>
<td>FZ</td>
<td>FZ - Float Zone silicon</td>
</tr>
<tr>
<td>4</td>
<td>Pixel resolution</td>
<td>50 x 60</td>
<td>equidistant in x and y direction</td>
</tr>
<tr>
<td>5</td>
<td>Pixel pitch [(\mu)m]</td>
<td>50</td>
<td>this is the pixel to pixel spacing</td>
</tr>
<tr>
<td>6</td>
<td>Detector thickness [(\mu)m]</td>
<td>50</td>
<td>no support substrate</td>
</tr>
<tr>
<td>7</td>
<td>Frame rate [Hz]</td>
<td>100,000</td>
<td>all pixel will be read out, no token based readout</td>
</tr>
<tr>
<td>8</td>
<td>Chip size [(\mu)m]</td>
<td>3000 x 6600</td>
<td>size is defined by our existing test chip dimensions</td>
</tr>
<tr>
<td>9</td>
<td>Output data rate [MPix/sec]</td>
<td>300</td>
<td>data from all pixels will be transferred off-chip, data stream not sparse</td>
</tr>
<tr>
<td>10</td>
<td>Clock rate [MHz]</td>
<td>150</td>
<td>output is double data rate (DDR)</td>
</tr>
<tr>
<td>11</td>
<td>Supply voltages [V]</td>
<td>1.8, 3.3</td>
<td>CMOS logic at 1.8V; analog circuits and CCD at 3.3V</td>
</tr>
<tr>
<td>12</td>
<td>Backside bias voltage [V]</td>
<td>-20</td>
<td>only ~-10 V is required to achieve full depletion</td>
</tr>
<tr>
<td>13</td>
<td>Output format</td>
<td>single bit data stream</td>
<td>data from all pixels will be transferred off-chip, data stream not sparse</td>
</tr>
<tr>
<td>14</td>
<td>Number of digital output pins</td>
<td>1</td>
<td>CMOS</td>
</tr>
<tr>
<td>15</td>
<td>I/O frame</td>
<td>single sided</td>
<td>all pads are arranged along bottom edge of chip over distance of 3000 (\mu)m</td>
</tr>
</tbody>
</table>
• Screen shot of top level schematic (left) and layout (middle) of SCI’s 640x512 deep depletion CMOS imager. A photograph of the chip cell comprising this imager, a test chip for evaluation of novel pixel designs (top in blue boundary box) and 12 1mm² large test
Thank You for your attention!
SCI Packaging Approach

- Wire bonding
- Chip on board
- Cold finger attached
  - Also guarantees planarity
- Backfill or vacuum seal
  - With ceramic board

Package 1: Cold finger directly attached against CMOS circuits

Package 2: Sensor freely suspended with support on sides only
  (⇒ only 50µm thick silicon membrane in beam path)

Low cost Package for High End Applications with Low Volume

October 1, 2015
High Resistivity Silicon Must be Used to Achieve Deep Depletion

For best performance a backside bias must be applied

Our 6.5 kOhm x cm material can be depleted to a thickness of 50um with a backside bias of less than 5V
Predicted FD PIN Diode Response Time

Transit time of photo generated charge carriers in 100um FD CMOS imager with 100V backside bias < 1nsec, corresponding to a 3dB bandwidth > 1GHz

Fully Depleted Imager is Suited to Support Nanosecond Integration Time Windows
For a 200um thick FD CMOS imager with 100V backside bias, photo generated charge carriers can spread up to 4.5 um before reaching the front side collection junction.
Quantum Efficiency

- High Broadband response
- High and stable UV response
- Peak QE > 90% can be customized with AR coating

Quantum Efficiency Comparable to that of Fully Depleted BSI CCDs
• Measured on 1mm² large test pixel arrays, on wafer level, at room temperature
• 1V back bias was applied

Measured Dark Current is Close to Predicted Depletion Current
>120dB Extinction Ratio in Visible Domain for $\lambda \leq 640\text{nm}$
High rho silicon wafer with completed CMOS process

Backside Process defines Optoelectronic Device Characteristics and can be Optimized for Different Applications

in-house backside processing

Wafer thinned to 50um

Thin film simulation of AR coating

50um thick wafer with AR coating