



Pixels at the LHC

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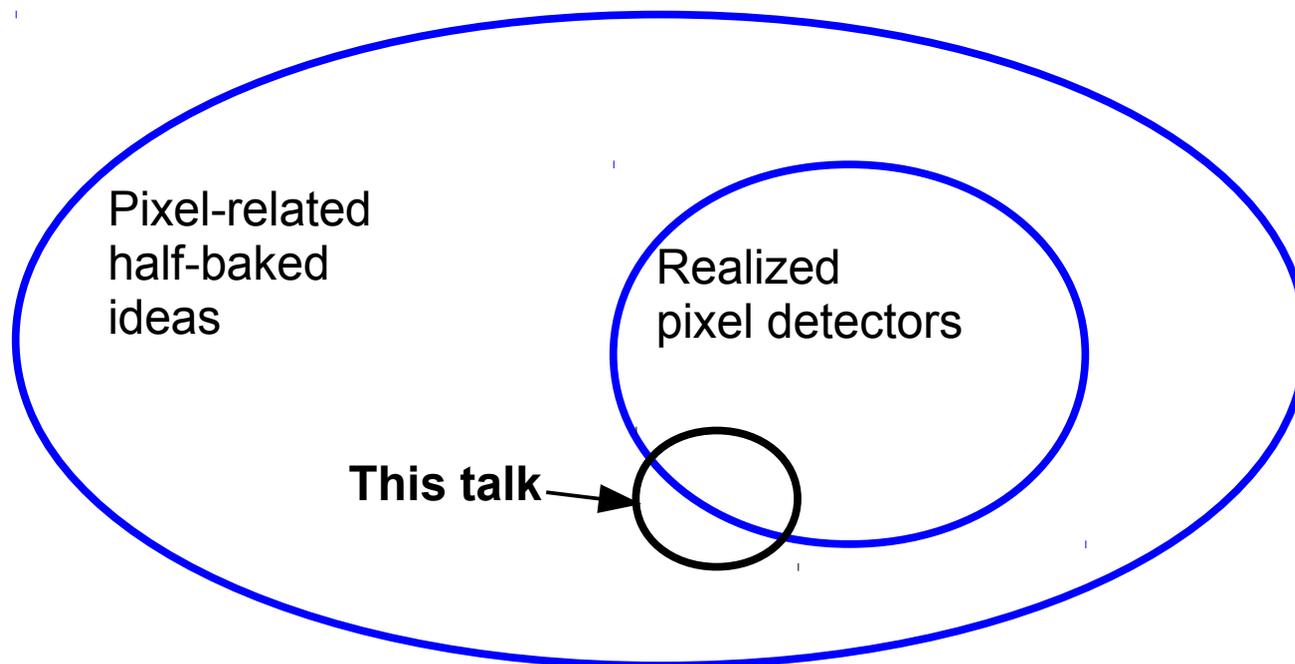
Close-up of ATLAS pixel detector, installed in 2007



?Experiment Artist? To-Do List

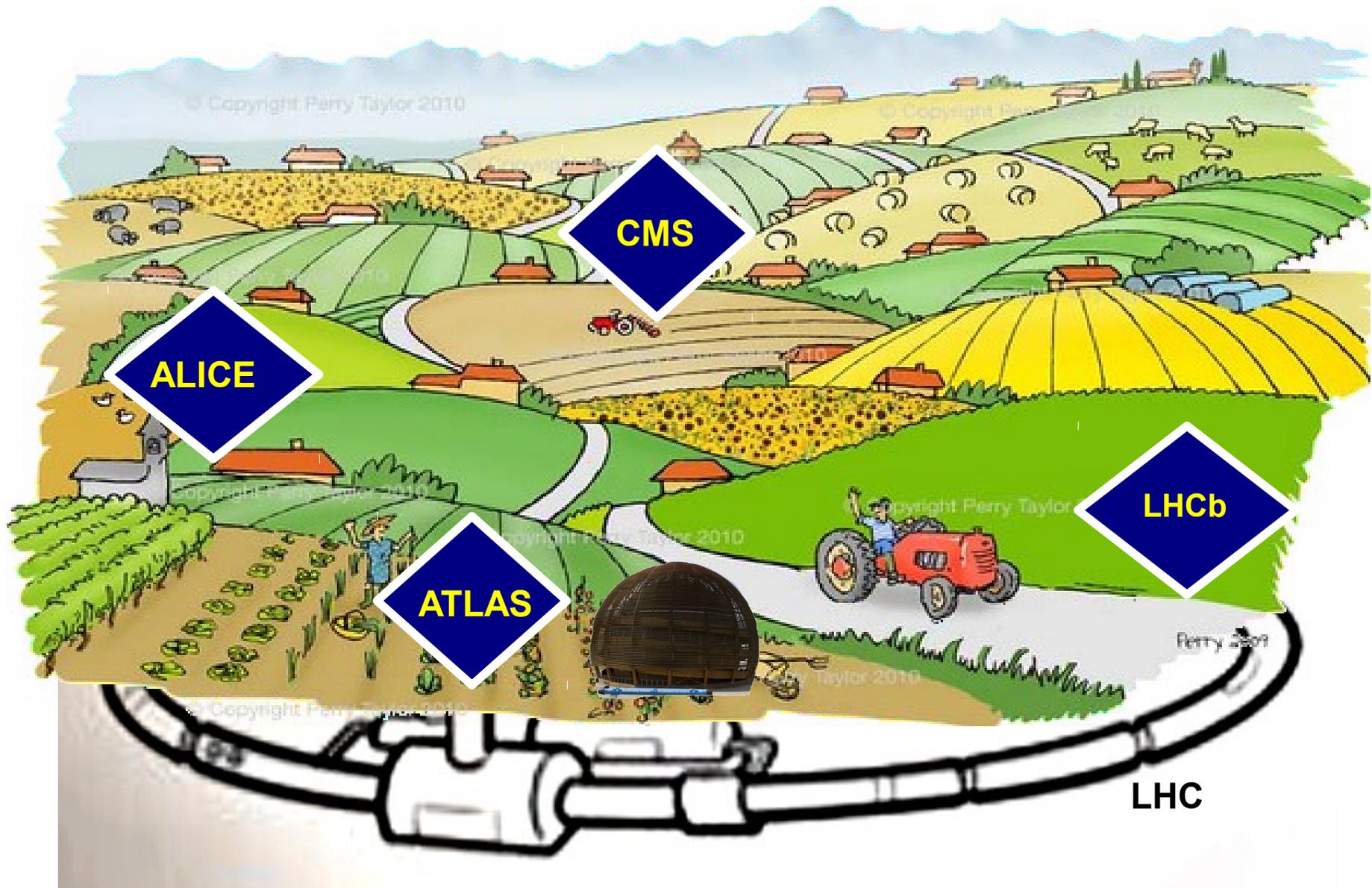


- Try to think up a “half-baked” idea each day
- *Meetings; email; budget sheets; travel, etc...*
- Find time to discuss half-baked ideas with others (yours and theirs)
 - Pixel detectors started as a half-baked concept



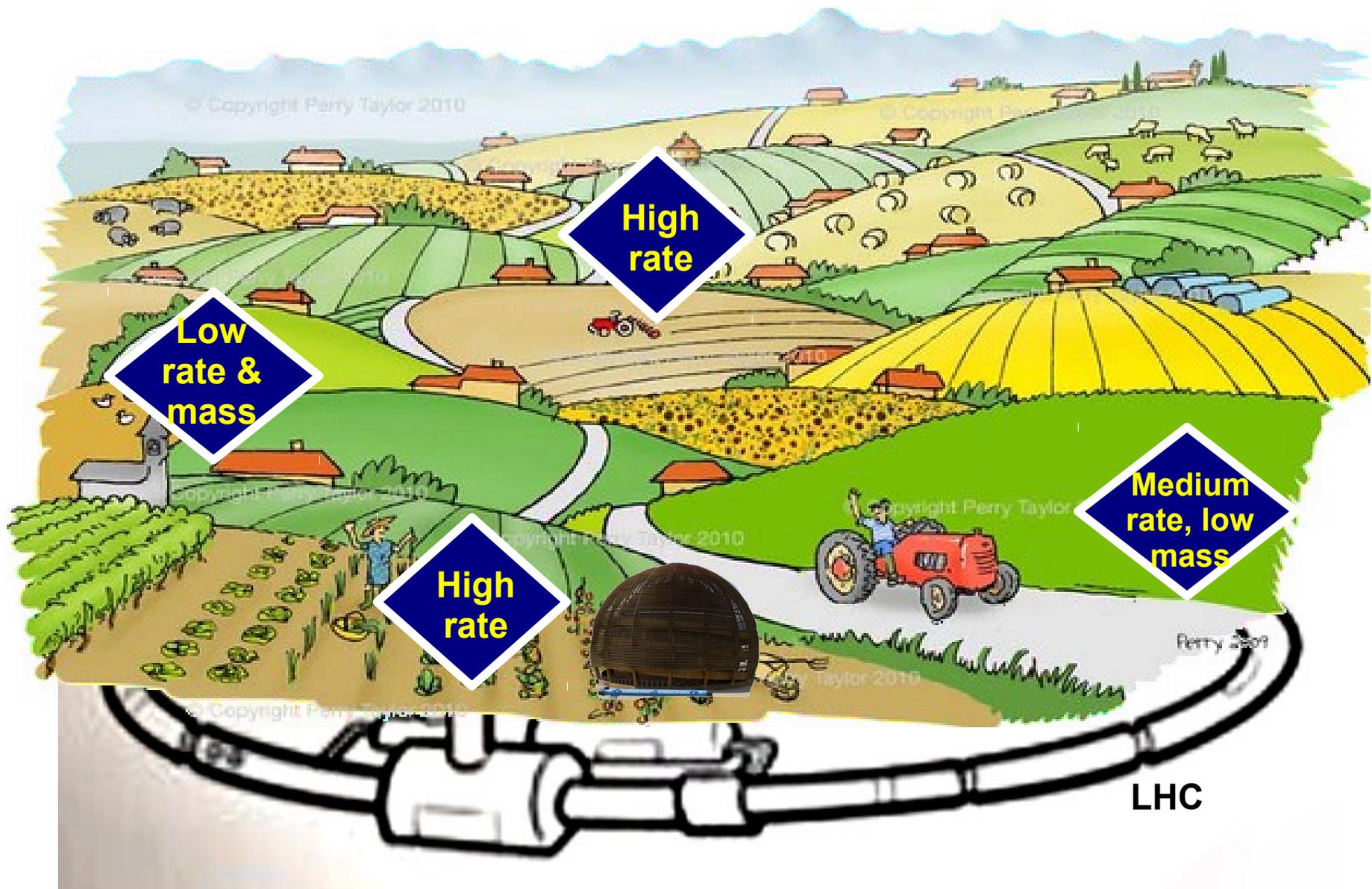


4 detectors around the LHC ring





Different requirements around the ring





Contents



- No time to talk about low mass
- Will focus on rate and readout technology
 - Hybrid pixels vs. monolithic pixels
- Futuristic concepts



Imaging analogy for rate

- Normal intensity image (present LHC rate and present detectors)



- To see finer details (precision Higgs physics, etc.), turn up the intensity (future high luminosity LHC)



Imaging analogy for rate 2

- Turn up the intensity--> need a faster camera



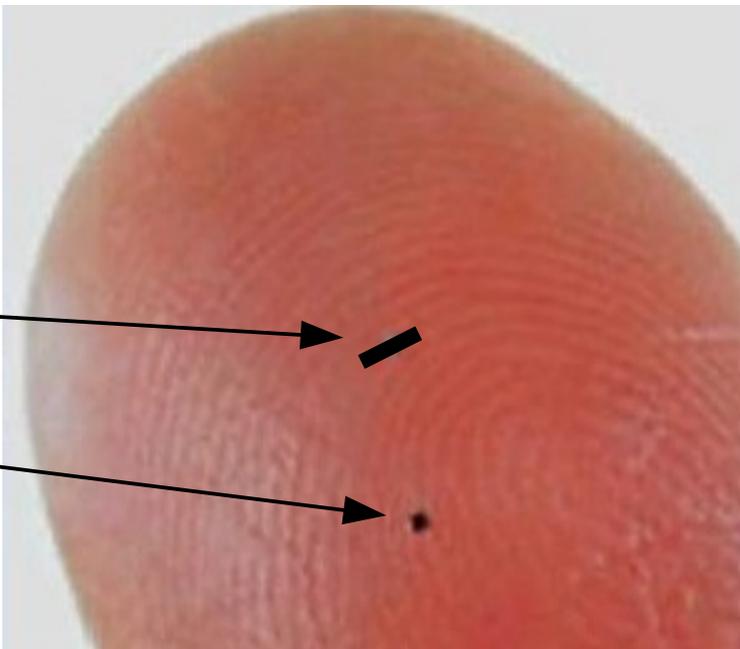
- As the rate goes, so goes the radiation dose (same source for both)



Single Pixel Details



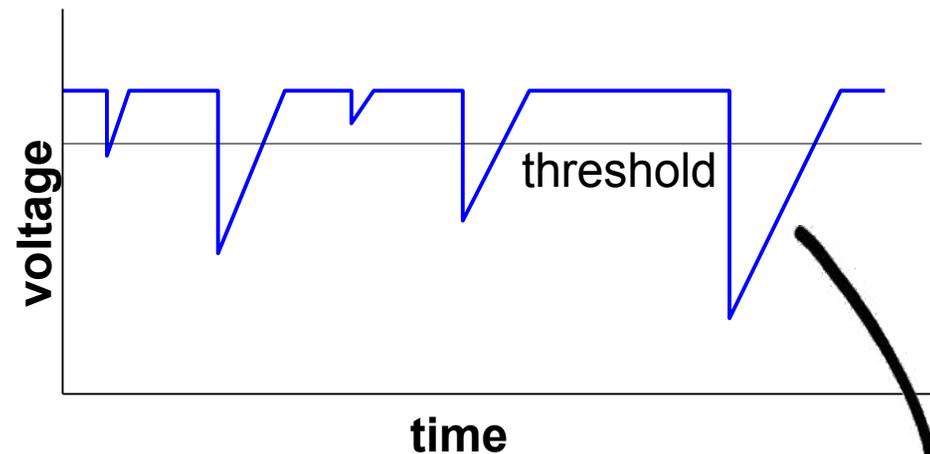
Pixel size



today →

future →

Pixel output

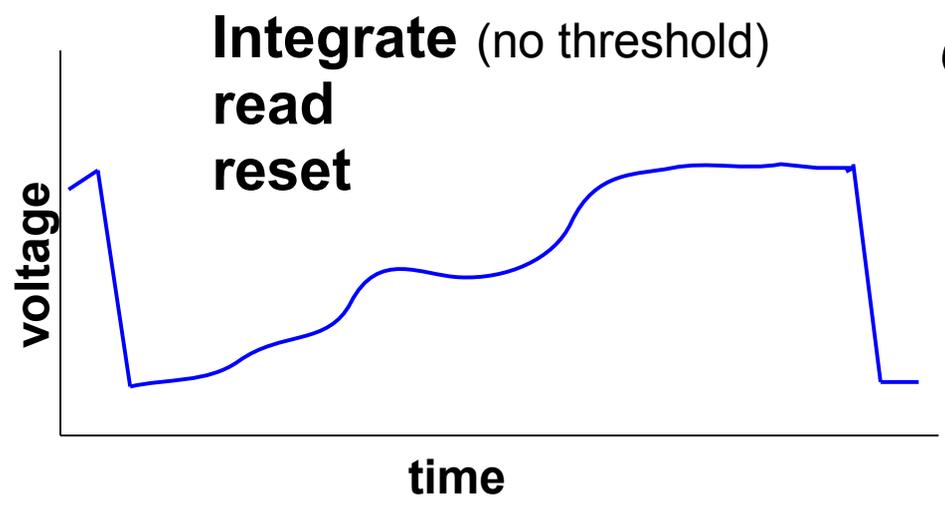
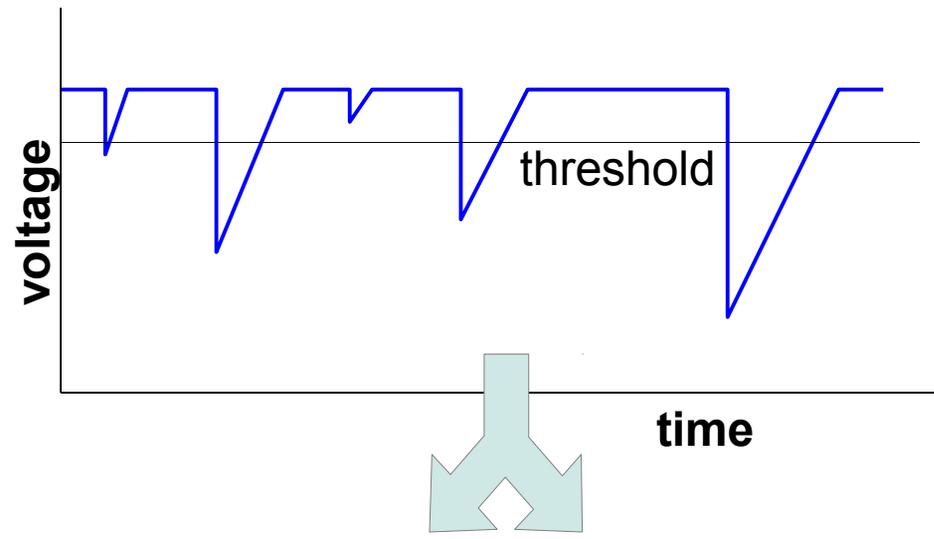


~50 kHz for ATLAS / CMS

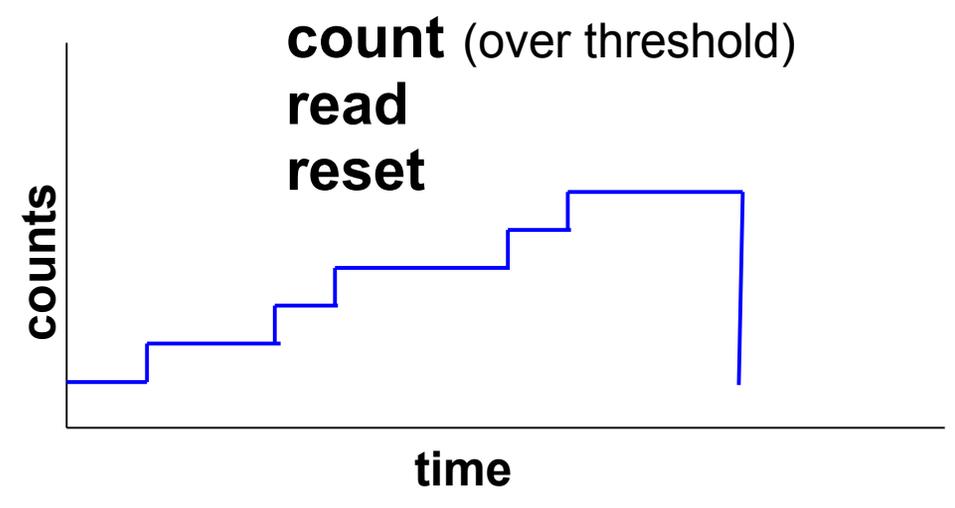
- For 50um x 50um (“future”) pixels, this is 2Ghz / sq. cm.

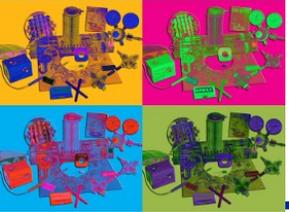


What imagers do with pixel output

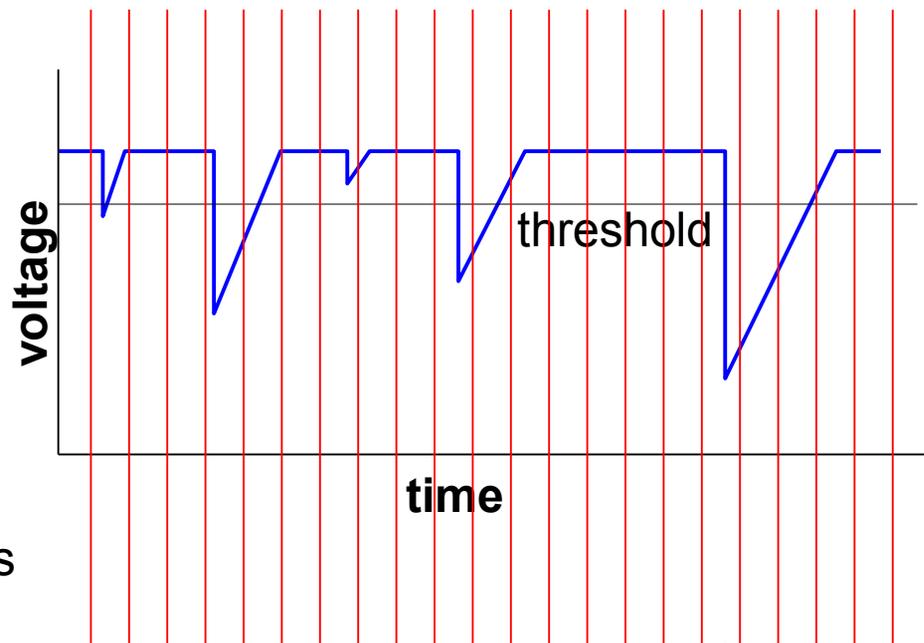


OR





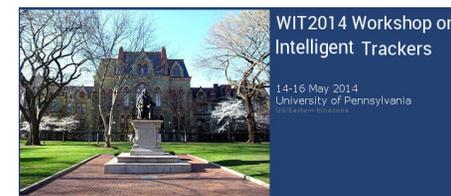
What LHC tracking detectors do



Record all 25ns time slices

Read out a few slices selected after the fact

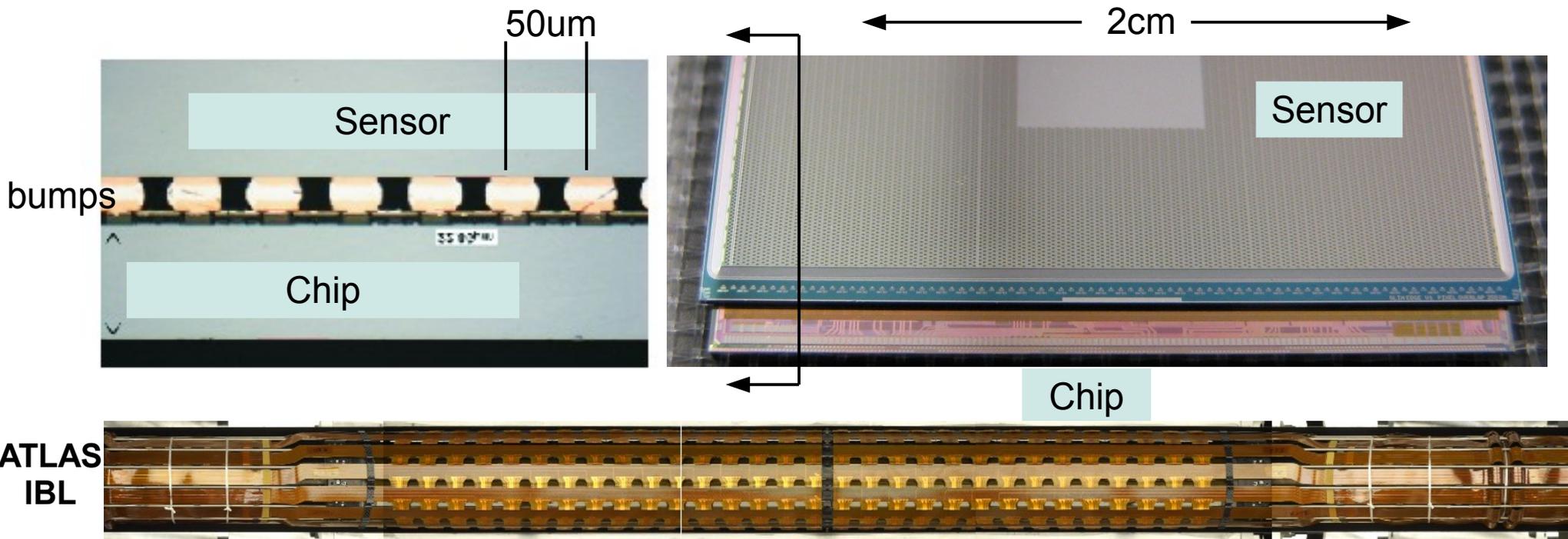
- Fraction of slices that can be read depends on the hit rate and readout bandwidth
- External trigger selects the time slices
- Half-baked ideas:
 - Read out all time slices (triggerless)
 - Decide locally which slices to read out (self-seeded trigger)





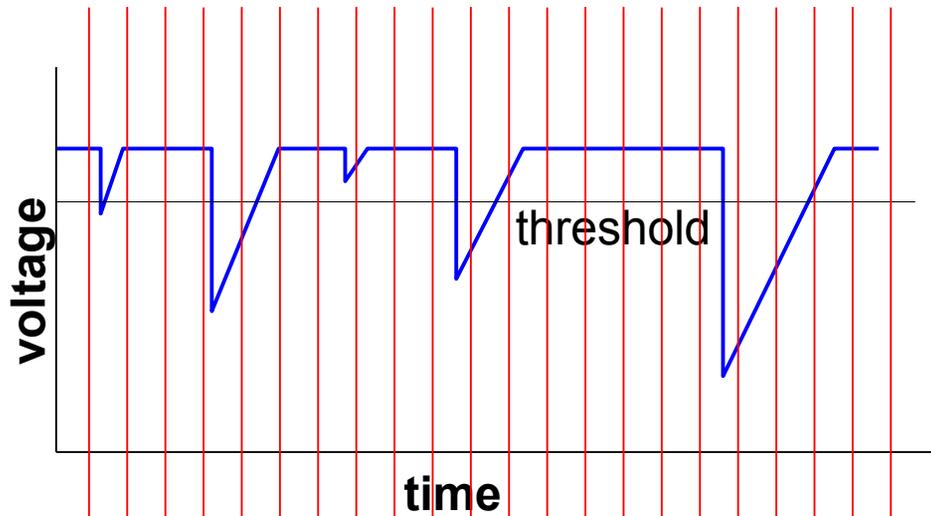
Hybrid Pixels

- Every pixel must be sampled at 40 MHz.
 - => Each pixel needs its own front end and digitizer
- Solution: a custom integrated circuit with one channel per pixel
- A separate sensor must be connected to this chip (one contact per pixel)
- Integrated circuit fabrication and area bump bonding are existing industrial technologies that made all this possible

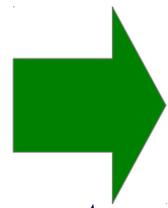




Digital perspective



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1100
1001
0011
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→ readout



Triggers (selected slice times)

What is this data rate per chip?



Data rate (simple analysis)

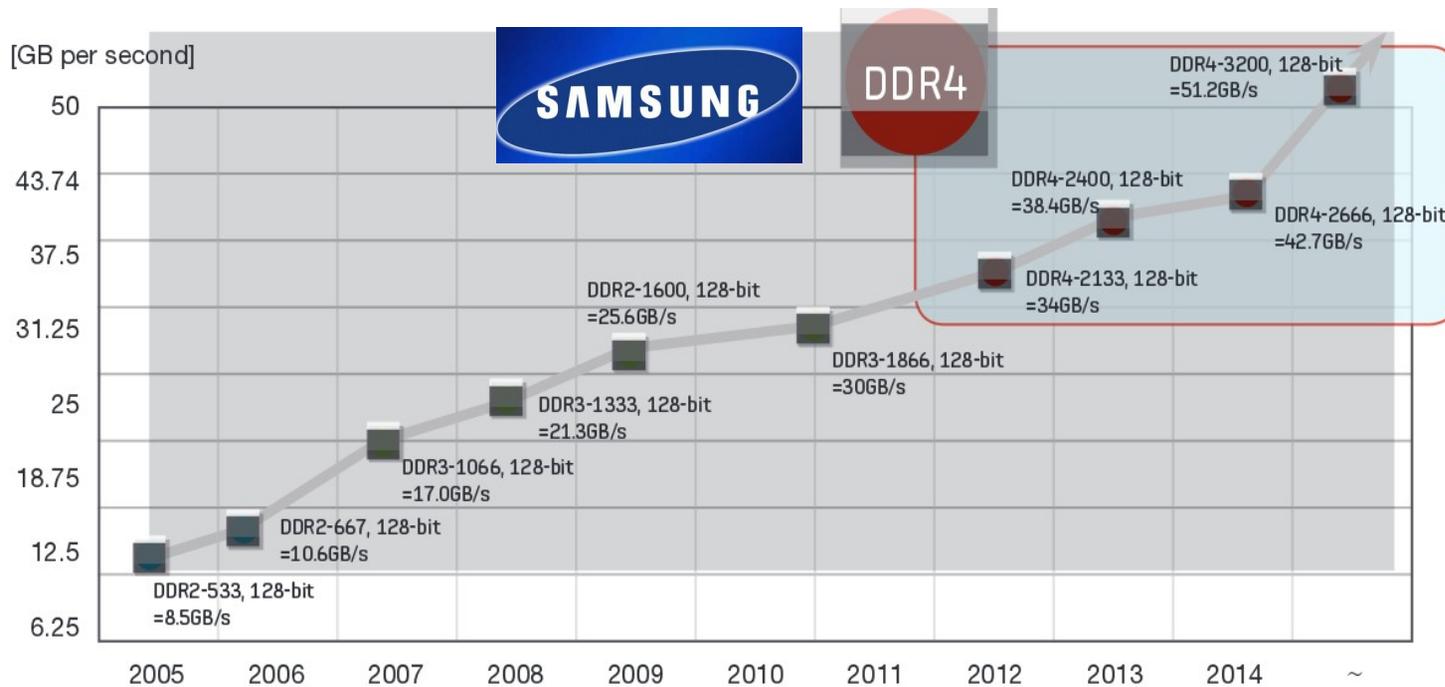


- If the total number of possible hit patterns in a chip is known:
 - and they are all equally likely, the information *entropy* is just the number of bits needed to count up to this number
- Can estimate the number of possible hit patterns by assuming all the hits are random (clusters change the answer, but won't discuss that here)
- For example, take $N=40k$ pixels per chip
- 50kHz / pixel gives 50 hits every 25ns
- Information entropy for picking 50 out of 40K is 550 bits
- This gives **22Gb/s** for the big green arrow.
- For 50um x 50um pixels that's per cm^2



Interesting comparison

- Are high rate pixel detectors memory chips?



This is for a memory module containing 8 silicon chips so $B = b$

Figure 2. DDR4 higher performance compared with DDR3L and DDR2

(and this is not rad hard)



Implications for experiments

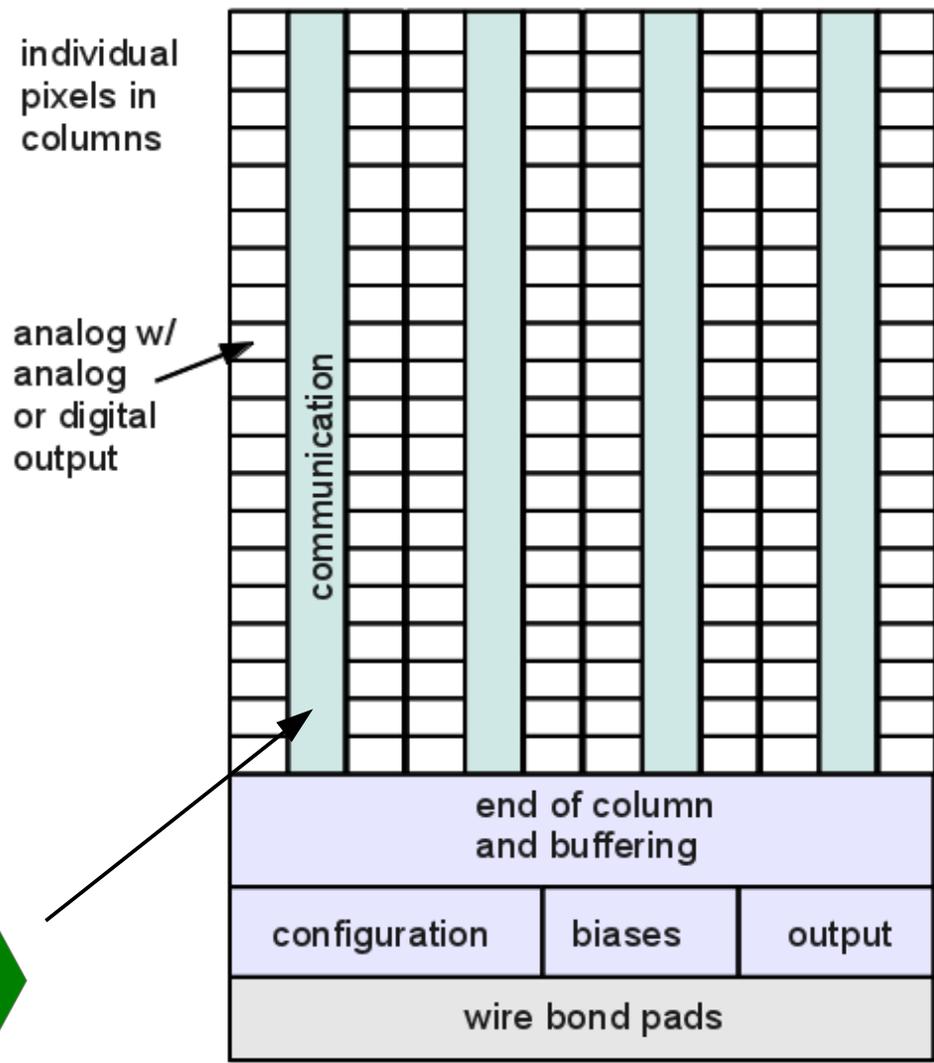
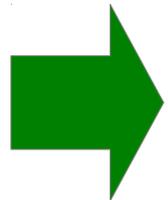


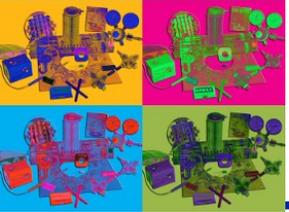
- ATLAS / CMS have 220Tb/s per m² of detector
 - Triggerless would need 500 data links with 400Gb/s each.
 - While 400Gb/s is the next generation commercial standard, those will not be rad hard, and need significant space.
 - => triggerless unlikely. Keep external trigger architecture
- LHCb has 10x lower data rate (lower luminosity)
 - Only 50 400Gb/s links (or 500 40Gb/s)
 - Plenty of space to put them due to fixed target geometry
 - Lower radiation.
 - => will attempt triggerless readout for 2019 upgrade
- ALICE has very low rate
 - Different considerations than rate



Classic Pixel Readout Chip Layout

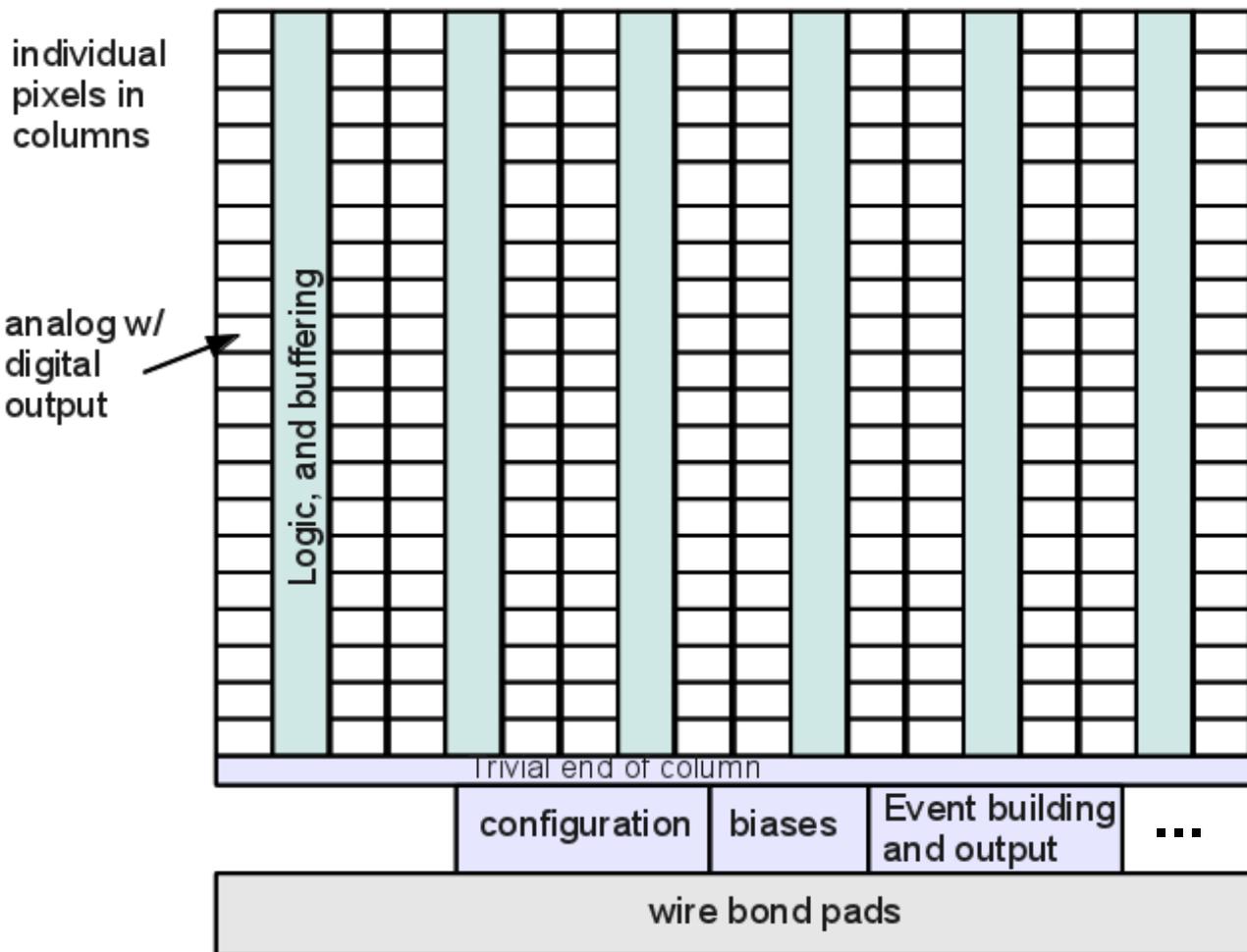
- **Array is primarily an analog circuit**
- **Try to keep clocks and digital activity out of array**
- **Limited intelligence in bottom of chip- mainly buffering and serialization**
- **Current generation already has gone beyond this classic picture**





Present generation readout chip

- Logic and buffering moved into array (a half-baked idea that worked!)
- Bottom of chip blocks shrank.
- Added system functions to bottom of chip

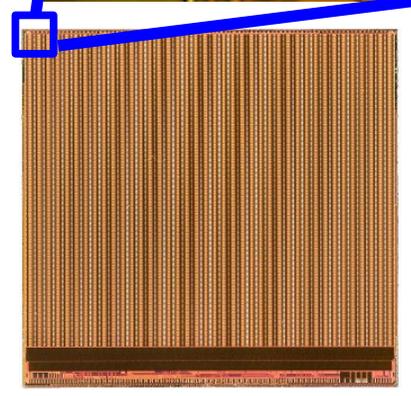
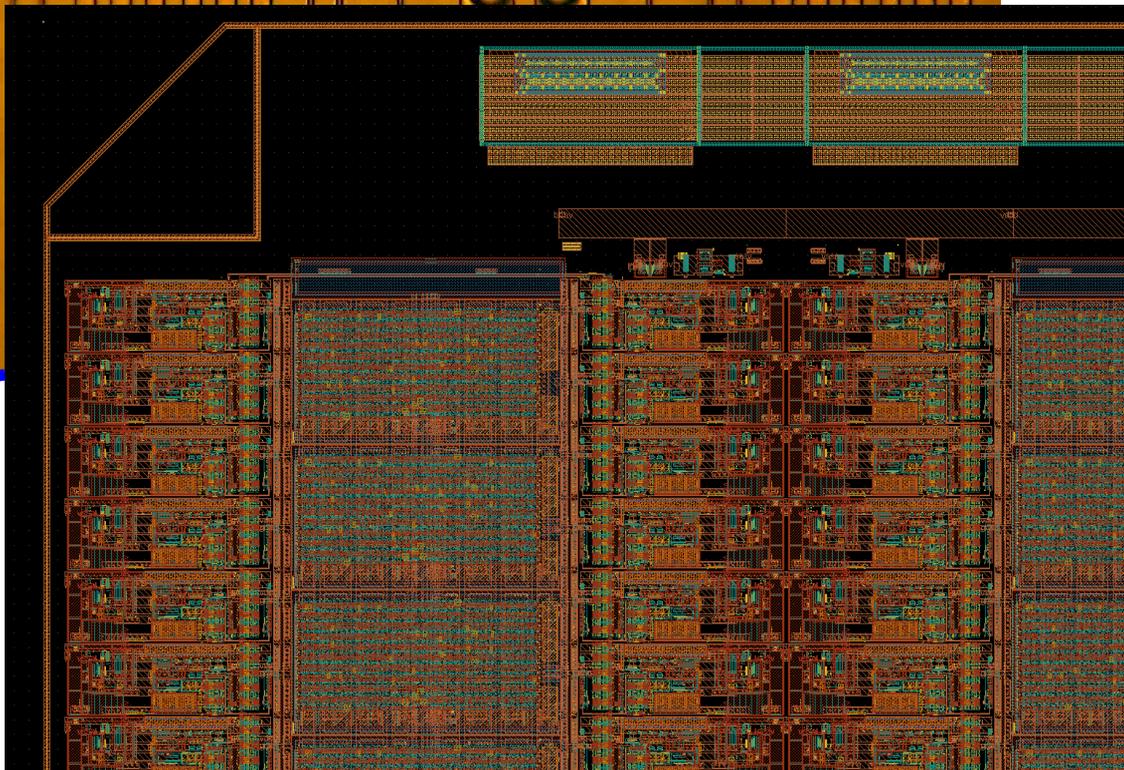


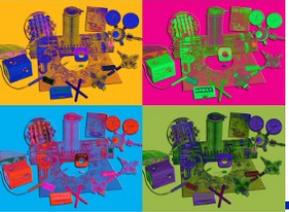


A look inside FE-I4



- Column composed of identical 4-pixel regions
- Each region logic is one synthesized block (10K gates)

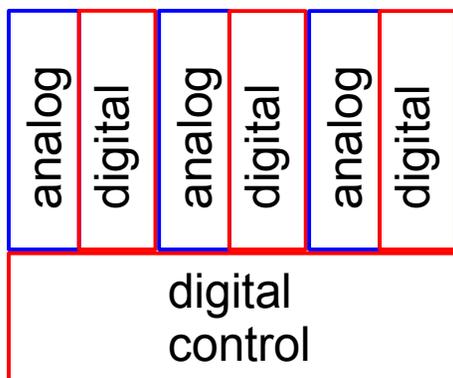
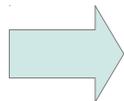




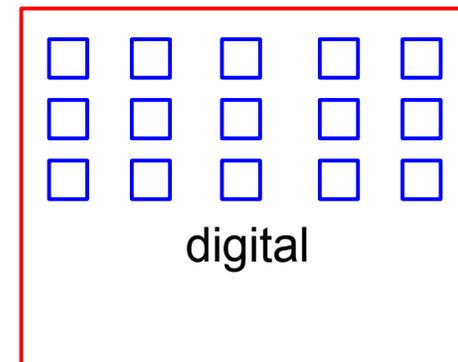
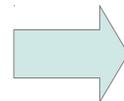
Trend is Clear



10 yrs ago

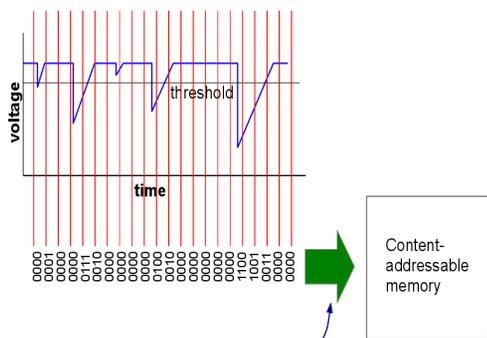


today

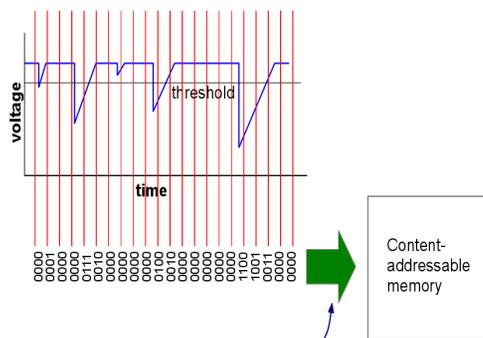


(looks like commercial chip)

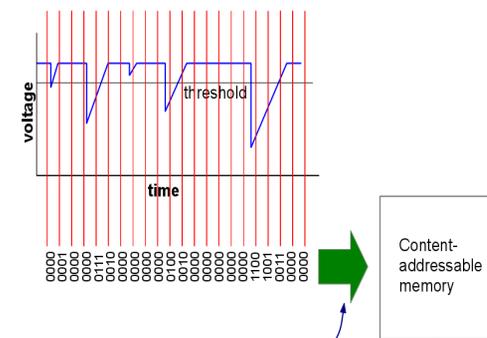
RD-53



<1Gb/s /cm²



5Gb/s /cm²



25Gb/s /cm²



RD-53



www.cern.ch/RD53



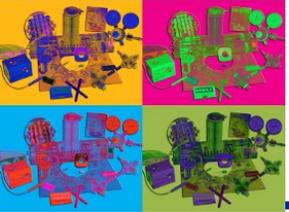
RD-53 Collaboration Home



RD-53 will develop the tools and designs needed to produce the next generation of pixel readout chips needed by [ATLAS](#) and [CMS](#) at the [HL-LHC](#). There is also interest and participation by [CLIC](#). More details can be found in the [collaboration proposal](#).

* [Meetings](#) * [Documents](#) (including papers) * [Press](#) * [Conferences](#) *





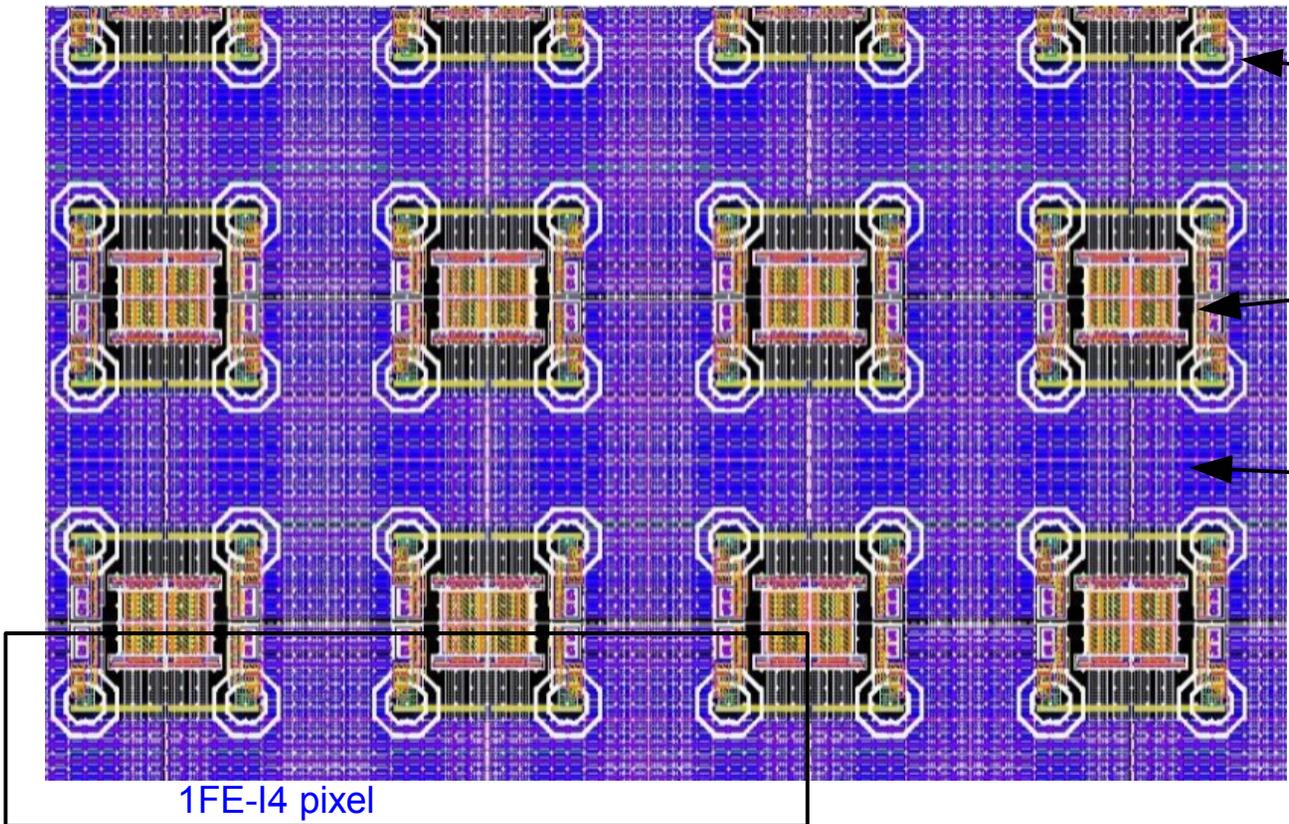
Next Generation Readout Chip



- **Designing in 65nm CMOS feature size**
- **A DIGITAL CHIP** containing embedded analog “sensing” circuits.
- **“Multi-core” architecture**
 - **Many “little chips” integrated into a reticle-size structure**
- **System on chip or “experiment on chip”**
 - **On-chip power management with no external components**
 - **Monitoring, control, interlock, self-test, etc.**
 - **Event level processing:**
 - DSP to run clustering algorithms now done off-line.
 - New trigger capabilities. For example could include an associative memory block with fast inputs (completely general and programmable- not specific to any experiment)
- **Configurable geometry. Configurable design?** (half baked)
 - **Would be nice if customization does not require re-fabrication (like an FPGA), but could also have customization of the design.**



Work in Progress Pixel Matrix Layout



Bump pads on 50um x 50um grid

Each of these front-end blocks produces 200kHz of hits

Synthesized logic few 1000 gates per pixel

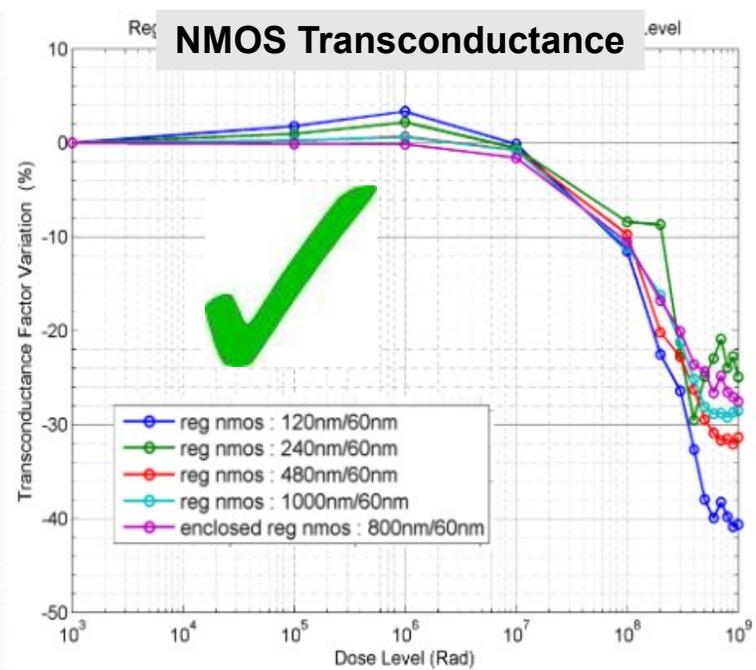
- 22Gb/s data “input” to this memory is highly distributed, unlike computer memory chip with 16 input pins
- Interesting: 2GHz/cm² hit rate >> dark count rate in cheap SiPM
- => half-baked idea: use SiPM as sensor feeding such a readout chip



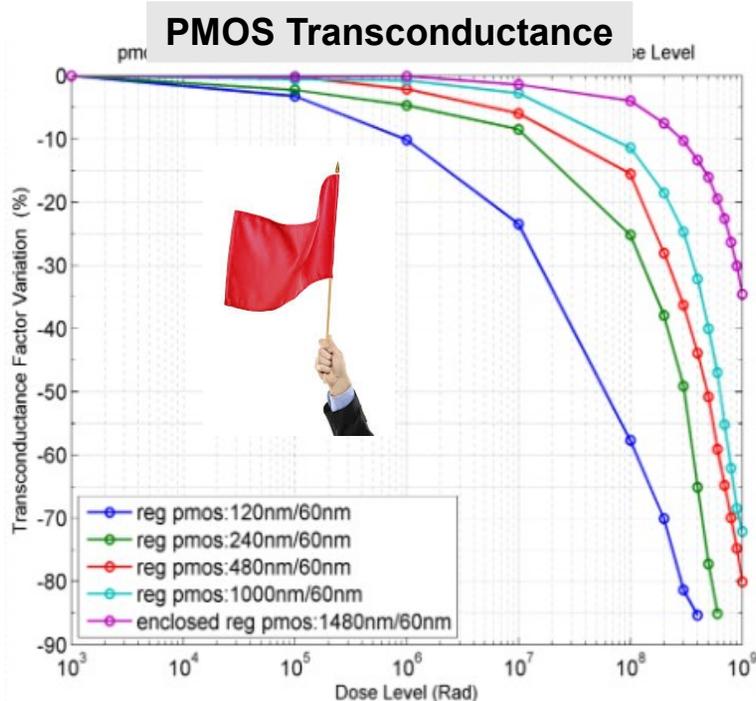
Work in progress rad hardness qualification



- Small feature size CMOS radiation hardness is something we get “for free”
- But different foundries with same feature size have shown different radiation response!
 - For example in 130nm, out of 4 foundries tested, one was good, one was bad and 2 in-between
- So far only one 65nm foundry being thoroughly tested to high dose, and it looks “in between” good and bad

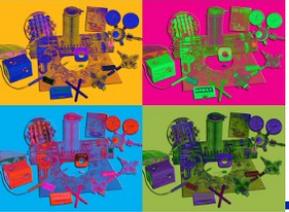


1Grad



Significant recovery after annealing

1Grad



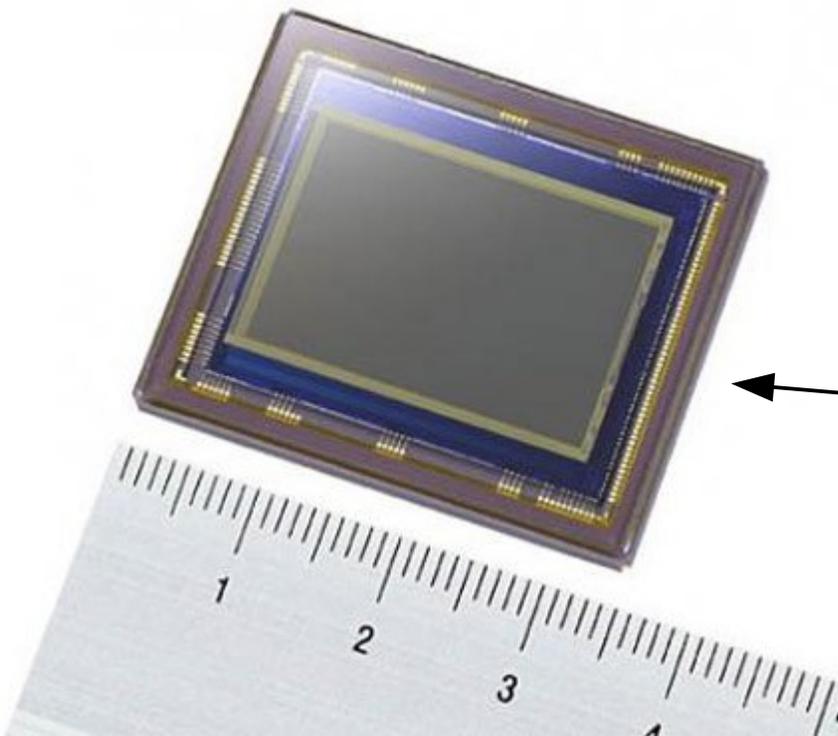
Back to imaging



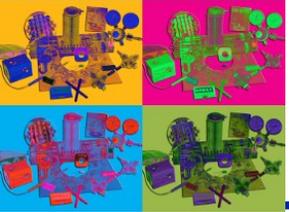


CMOS sensor technology

Cheap, ubiquitous, why aren't we using that instead of hybrid pixels?
This has been a half-baked idea for a long time: its time has finally come



$\sim 2 \text{ cm}^2$



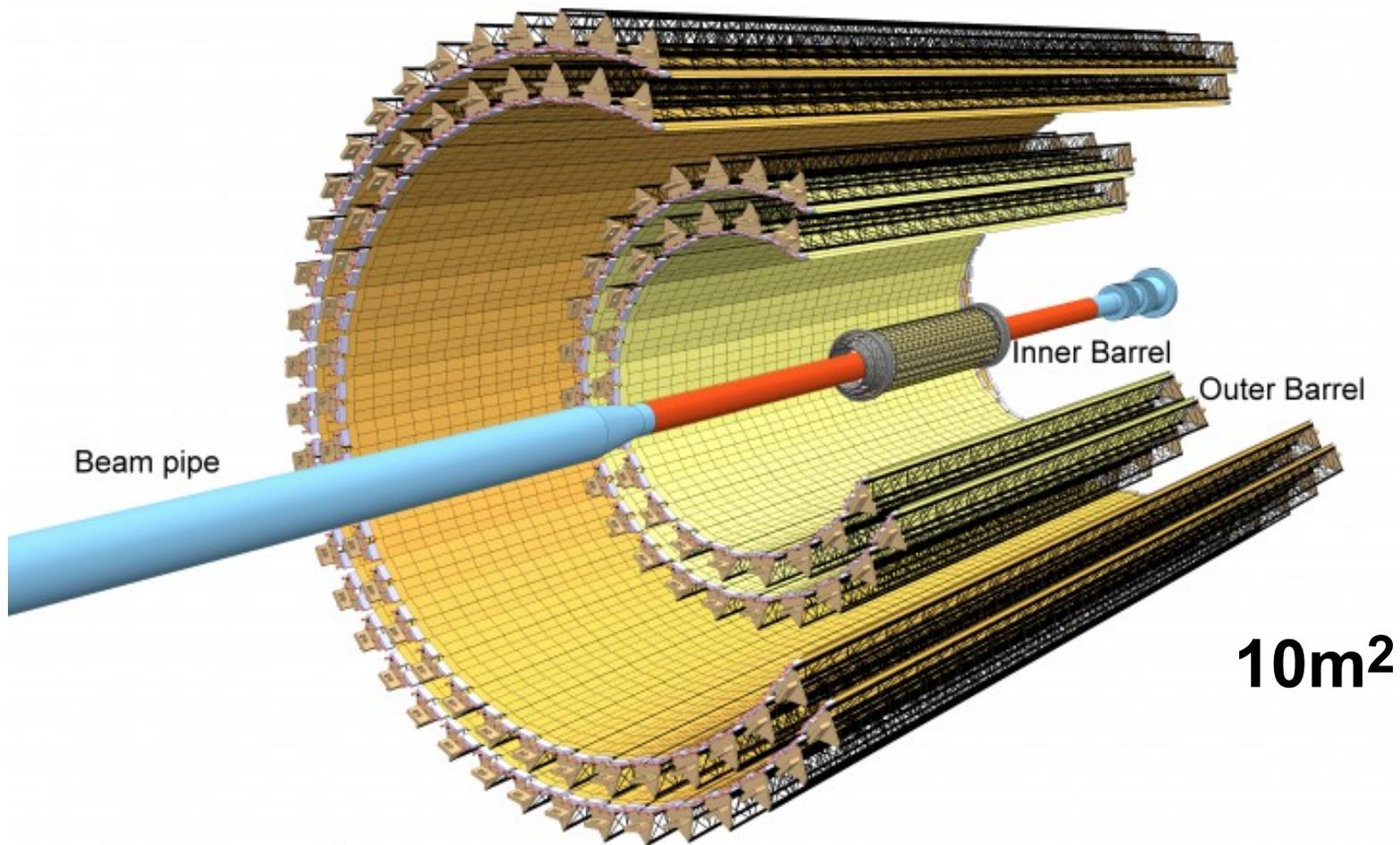
STAR Heavy Flavor Tracker

- Built downstairs in this building and in building 77A
- First collider pixel detector based on CMOS sensors





A whole tracker of CMOS Chips



Proposed ALICE tracker for 2019 upgrade.

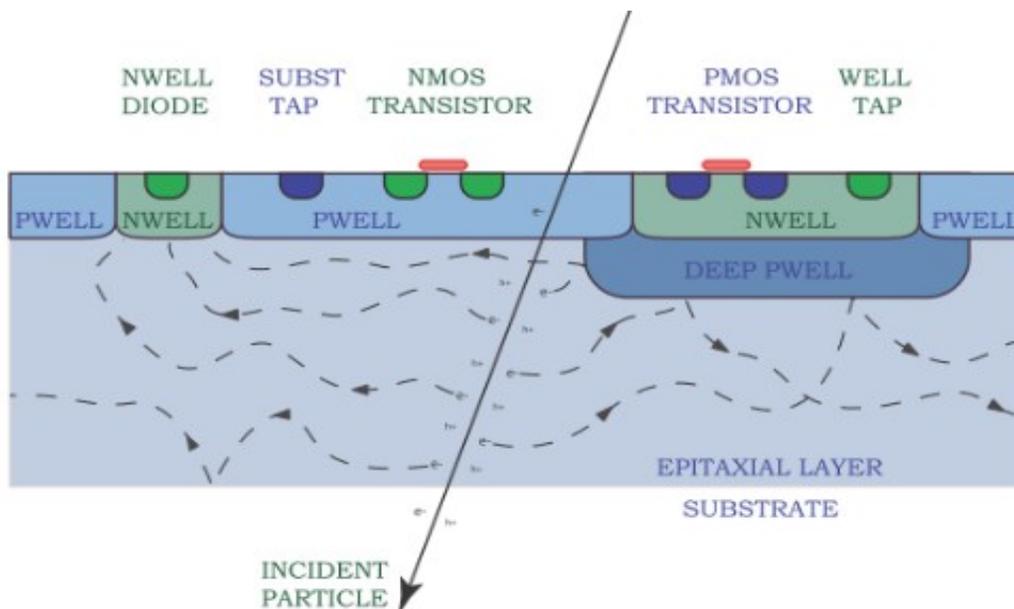


Traditional MAPS for STAR & ALICE

(monolithic active pixels)



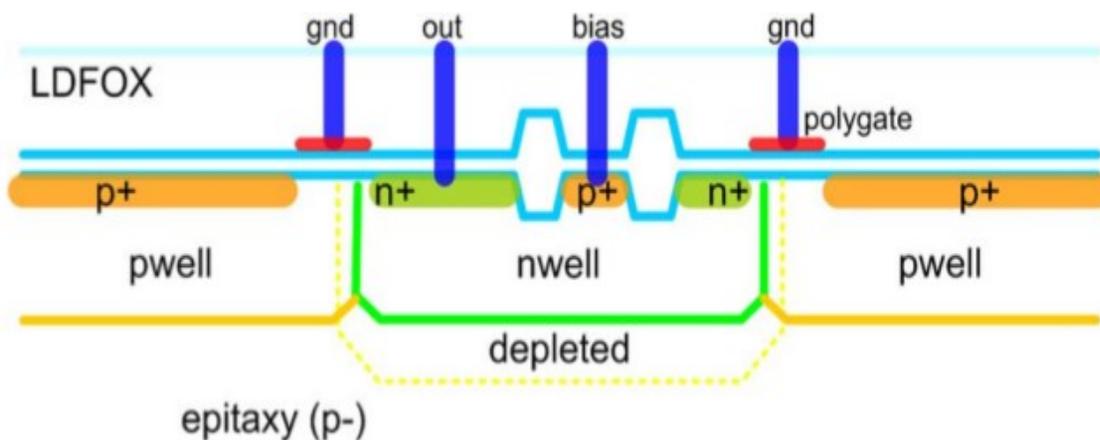
INMAPS
(RAL)



Tiny collection implant
 Tiny capacitance
 Collect by diffusion
 Slow
 Rolling shutter readout
 Not very rad hard

**WILL NOT WORK FOR
 ATLAS/CMS**

MIMOSTAR
(IPHC)

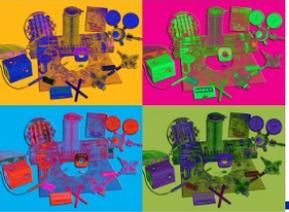




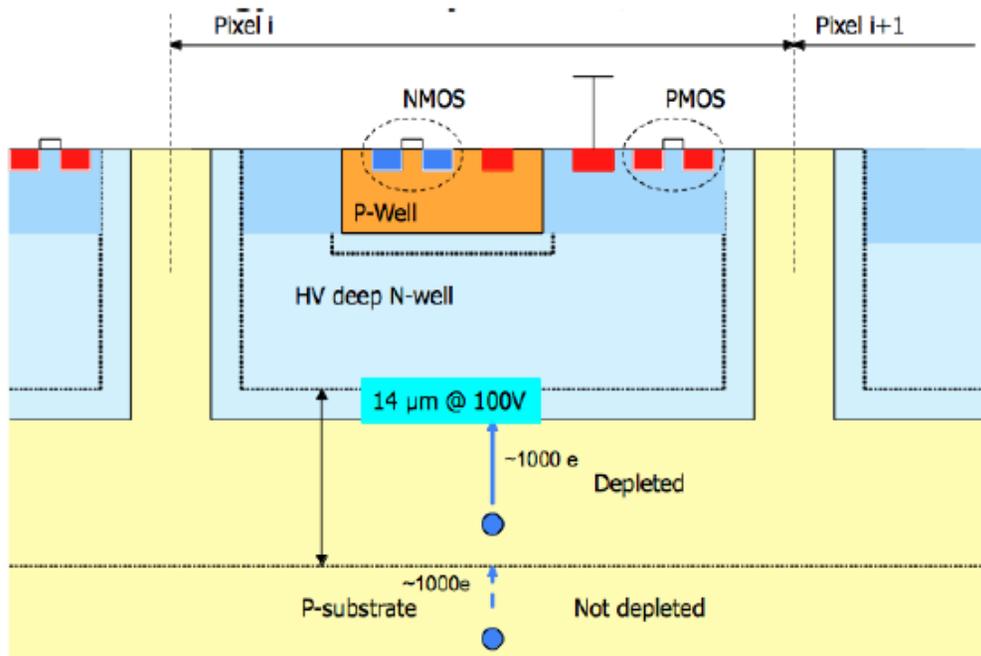
What might work for ATLAS / CMS?



- Must collect charge with a drift field in order to be faster
- Must be much more radiation hard
- Must read all pixels in parallel to cope with high event rate
 - (must handle the 22Gb/s input data rate)



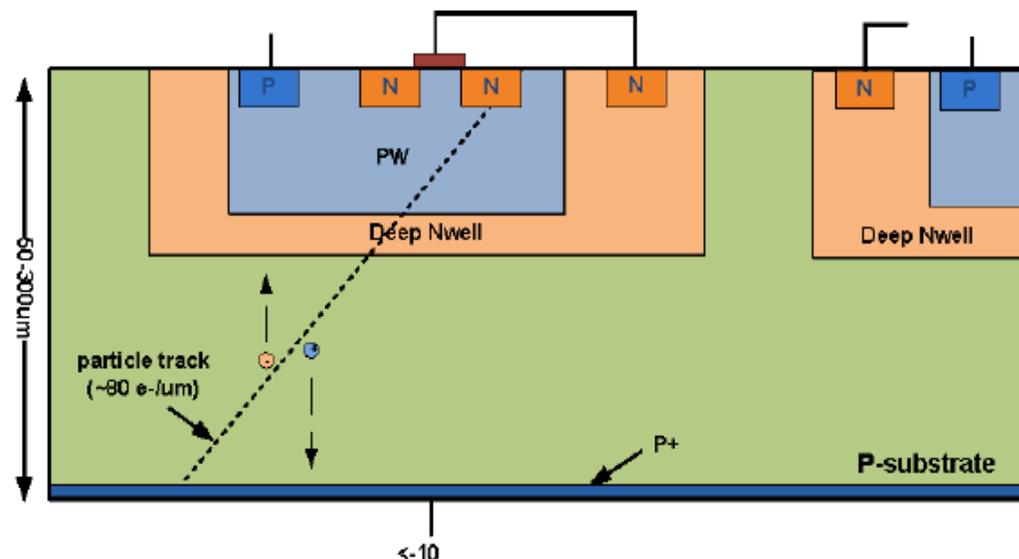
CMOS sensors with drift field and in-pixel discrimination



CMOS electronics placed inside the diode (inside the n-well)

HV-CMOS

Not much more signal than traditional MAPS, but more capacitance.
 Both signal and capacitance not well predicted in advance. Understanding via measurement
 Promising, but challenging



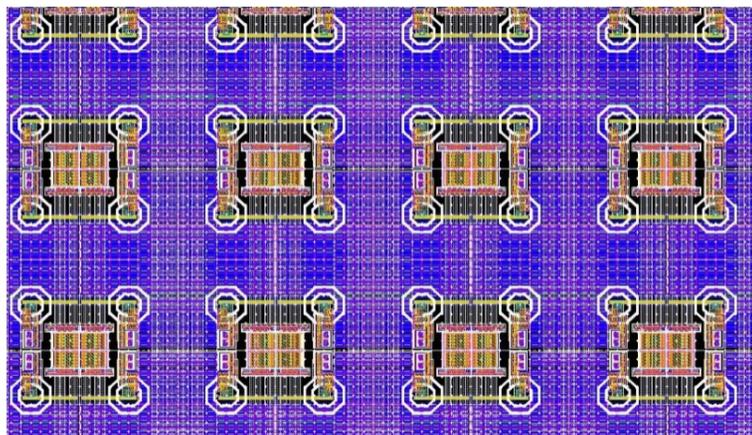
HR-CMOS

More signal from fully depleted bulk to overcome the capacitance.
 Starts to look like a sensor with some transistors inside the collection electrode (why not make sensors in this process? Trying that too)



CMOS sensors for high rate?

- High rate => too many hits to process them in periphery as in conventional MAPS. Recall the kind of circuitry needed:



- Must place all this circuitry in isolation implants and collect the charge from those implants.
- Very high capacitance and small signal. Very challenging, but nevertheless trying it.
- A less ambitious approach is to give up on truly monolithic and use a pixel readout chip with a CMOS sensor front end. Can save some cost relative to diode sensors. Also can potentially make smaller volume pixels (good for high track density)



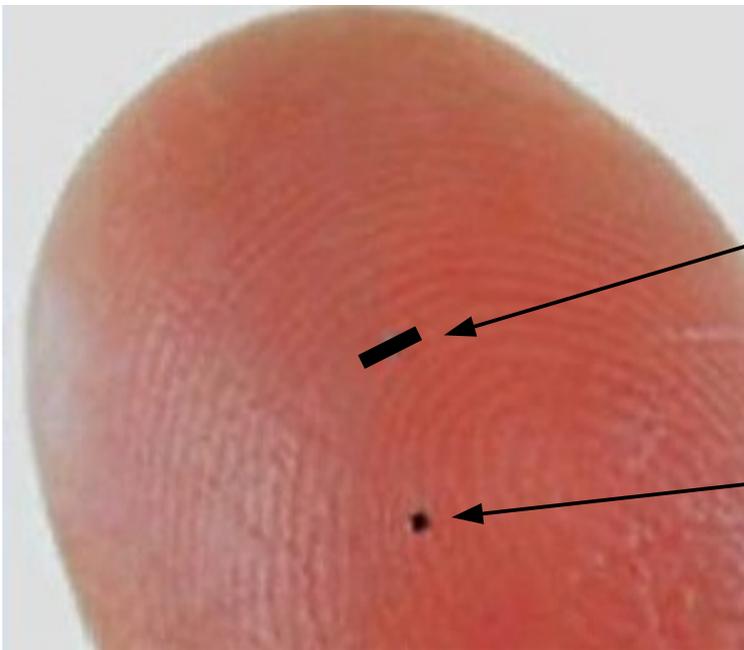
Back to half-baked

Remember this picture?





A single-pixel module

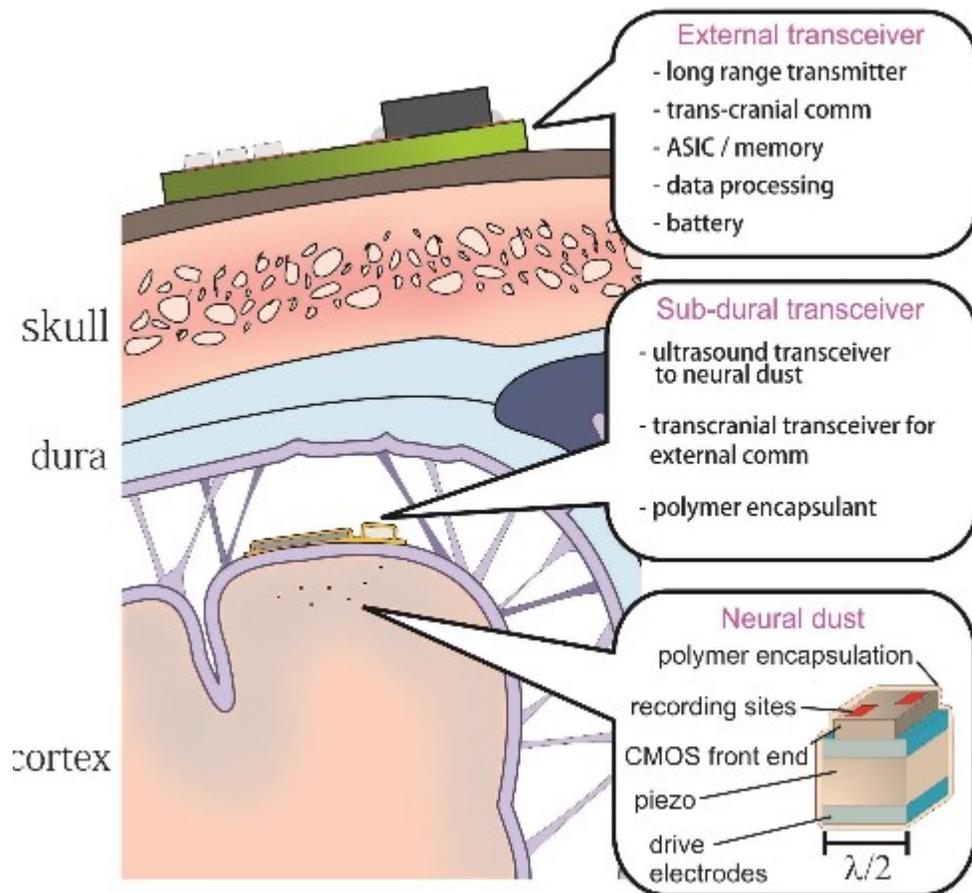


A black rectangle I drew on top of the picture

Part of the picture.
Hitachi μ -Chip RFID device
50 μ m x 50 μ m
a.k.a. Smart dust

What can we do with smart dust?

Some are trying to stick it in the brain



(arXiv 1307.2196)

Why not a single pixel CMOS sensor with wireless output?

Fill paint with this dust and brush onto surface to be made into a detector (need a few pickups to receive signals and triangulate hit positions)

(like a phosphor that you image with a camera, but single particle efficient and ns timing capable)



Conclusion



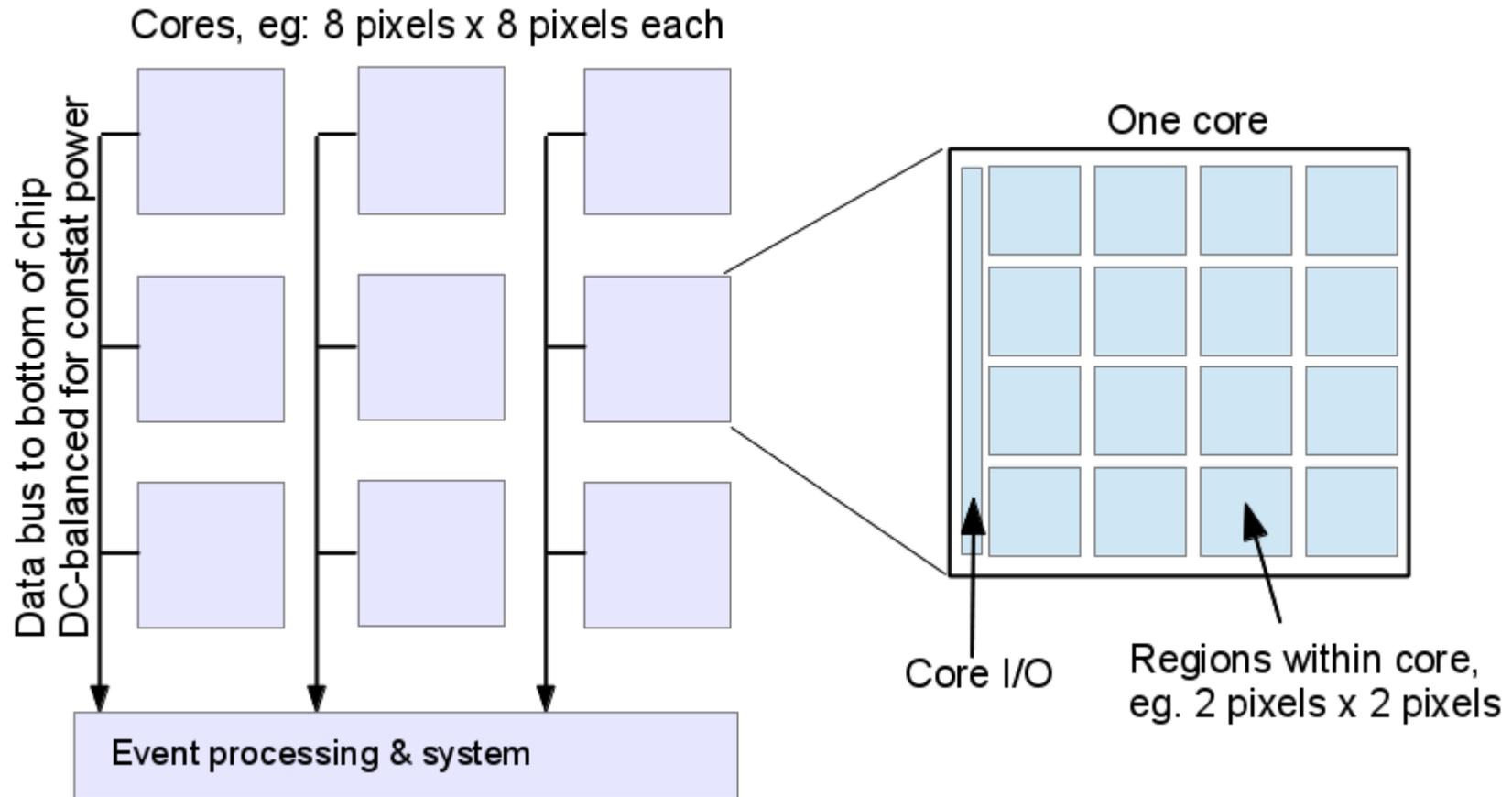
- Pixel detectors at the LHC have varying requirements around the ring
- High hit rate of order $2\text{GHz}/\text{cm}^2$ is the leading challenge for ATLAS and CMS. This drives
 - Readout electronics with high digital logic density, with bandwidths comparable to high speed computer memory chips
 - Extreme radiation tolerance
- At one order of magnitude lower hit rate, as for LHCb, triggerless readout appears feasible.
- Still a few more orders of magnitude lower hit rate (ALICE) allows the use of traditional MAPS
 - Efforts under way to try to extend MAPS technology to high hit rates and radiation
- Half-baked ideas have been a constant of pixel detector development and there is shortage of them today



BACKUP



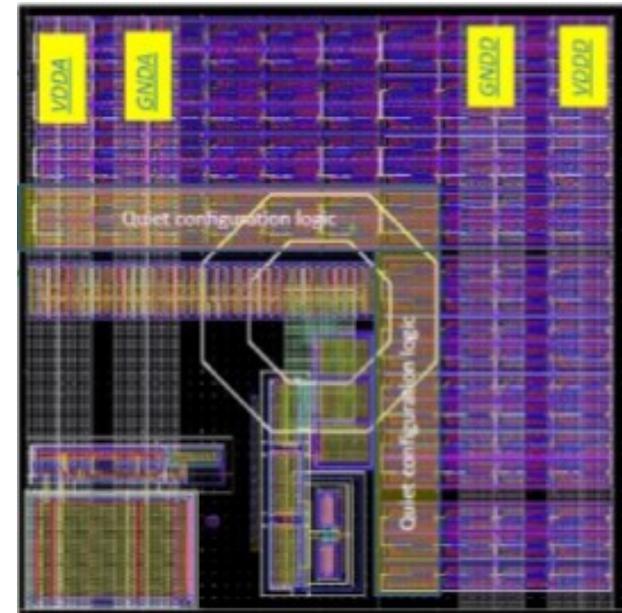
Multicore Concept





Analog/Digital Separation

- A key challenge is to prevent digital activity from affecting the analog threshold or coupling to the analog signal input
- There is going to be A LOT of digital activity, everywhere.
- Isolated routing as best as possible, obviously
- But it will not be perfect
- In fact, metal stack and isolation implants are WORSE in this process than in the FE-I4 process
- => Isolation will NOT be as good as in FE-I4

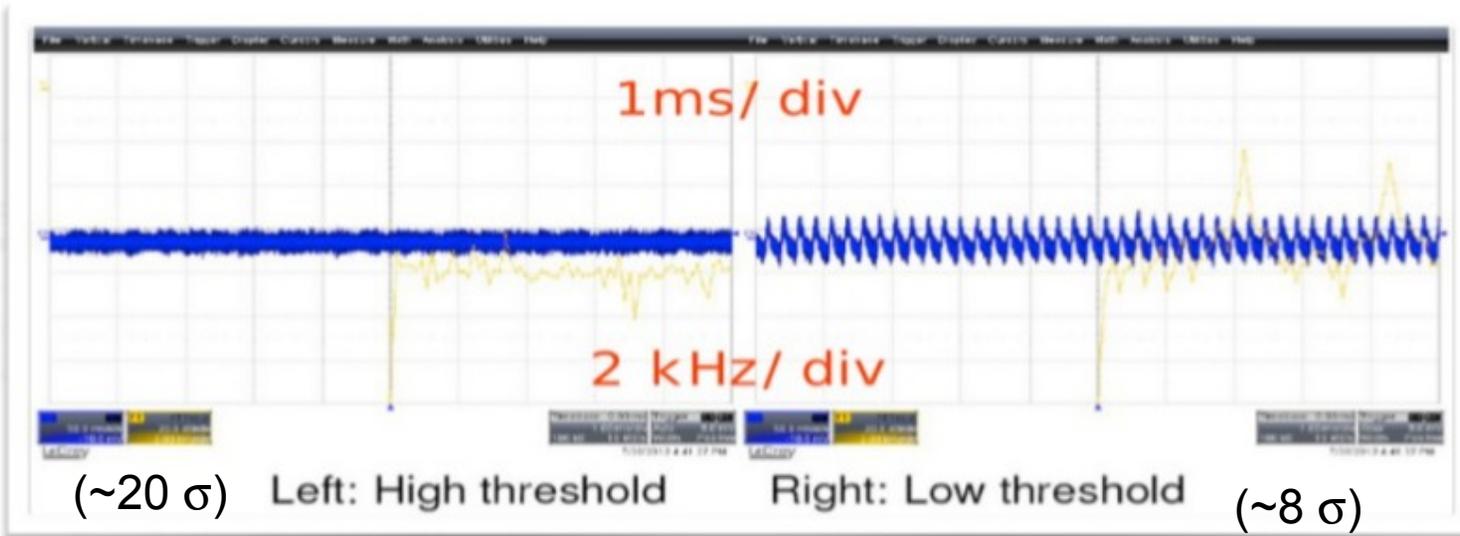




Limits of isolation in visible in FE-I4



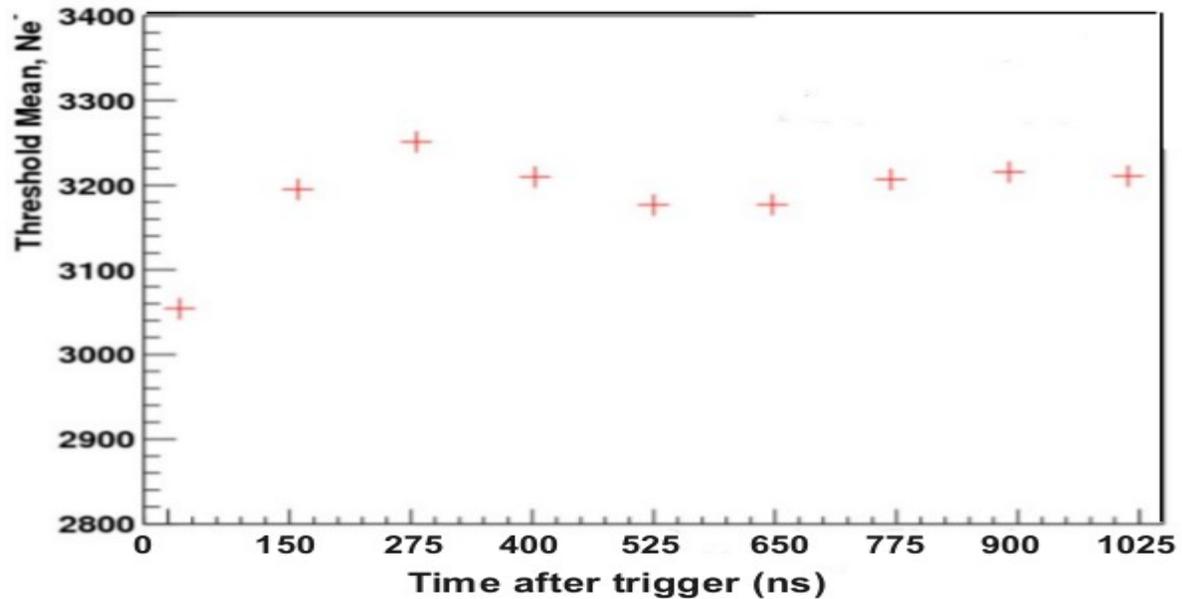
Impact of a large perturbation (make lots of pixels fire in phase) on chip power rail



Impact of triggers (to read out array) on measured threshold.

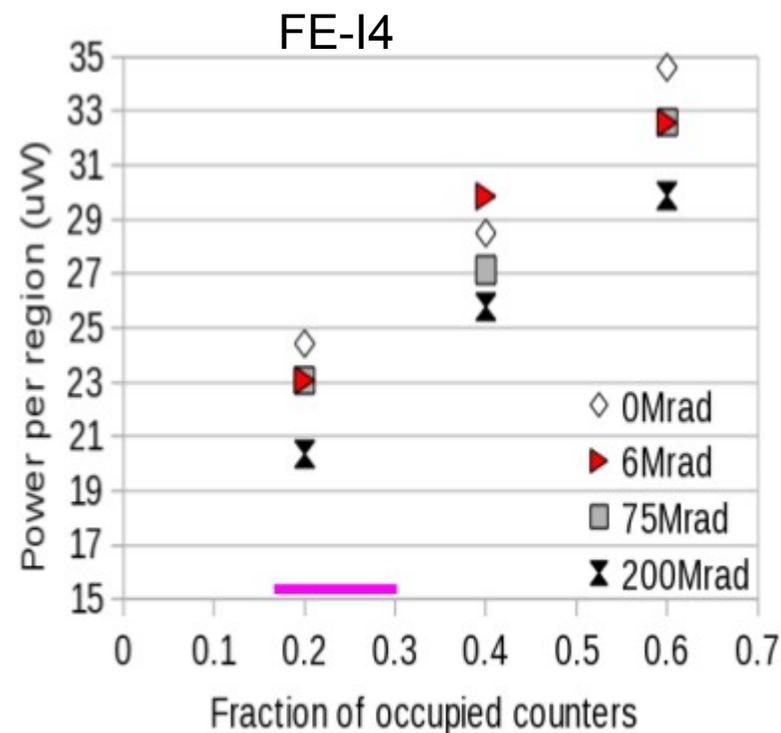
Plot shows effect of 16 consecutive triggers.

Effect is much smaller for a single trigger.



How to get better performance with worse isolation

- REMOVE THE ROOT CAUSE!
- The FE-I4 digital power consumption is a function of digital activity
- Changes in digital current will affect the chip ground potential
- Next time, make the digital current constant, independent of activity (=> maximum activity present all the time)
- This will result in higher average power, but same peak power.
- OK, because cooling is sized for peak power, not average.





Rad Hard logic lagged Moore's Law due to ELT, but now caught up



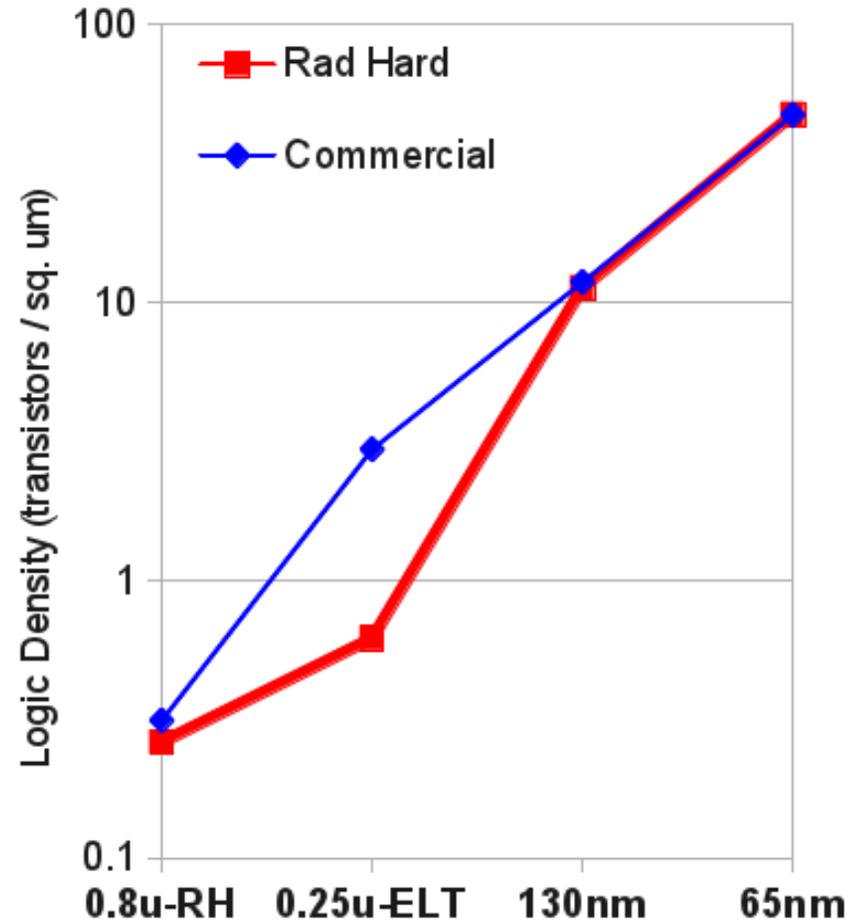
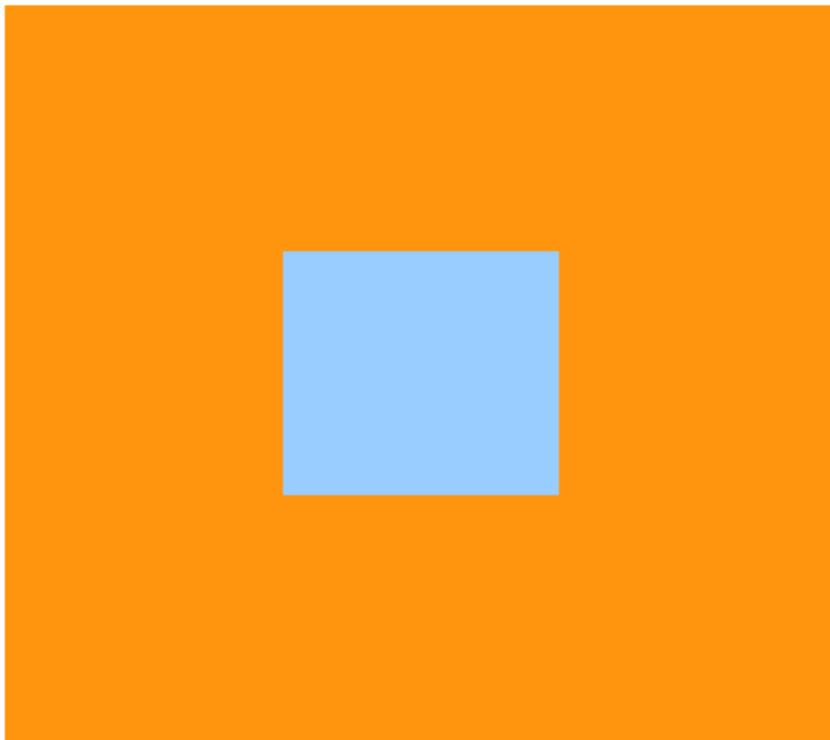
65nm



130nm



0.25um
ELT

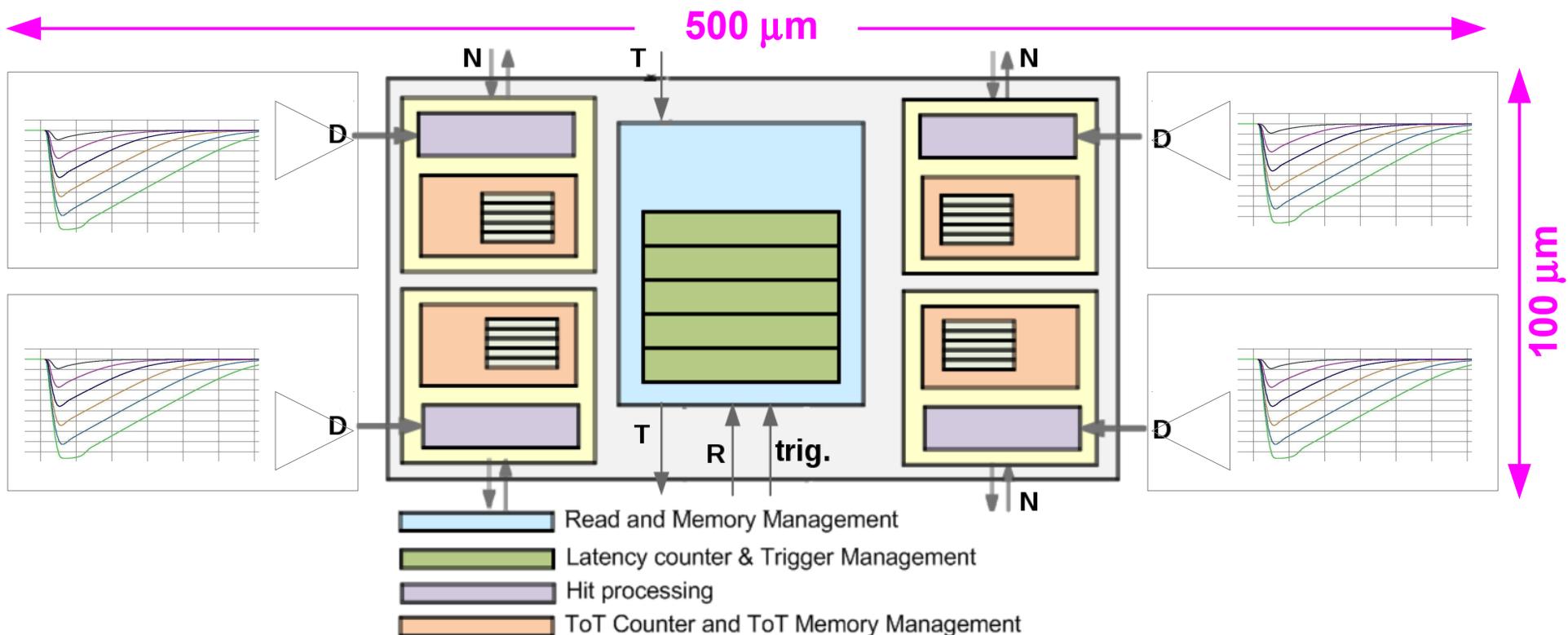




FE-I4 Digital Region

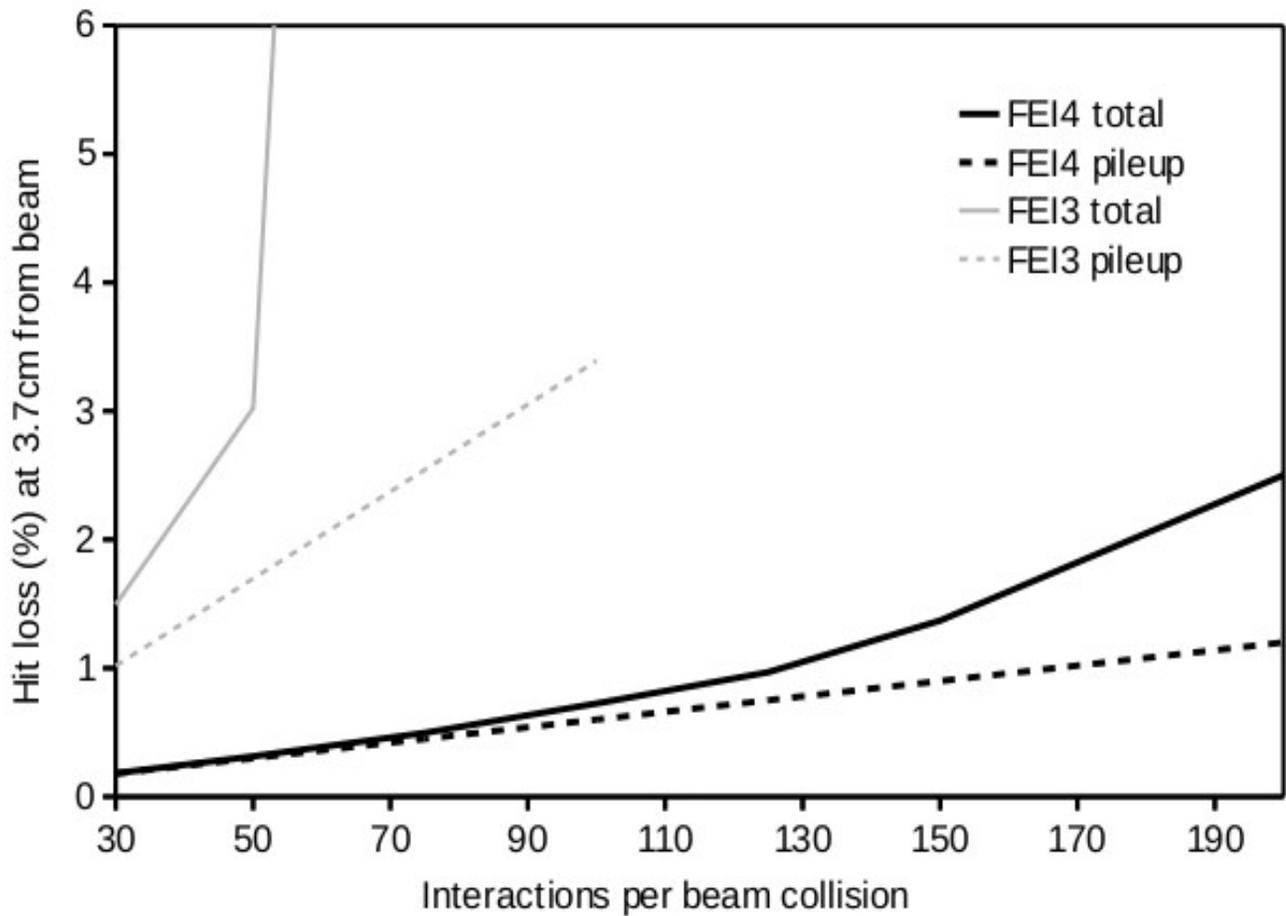


- Digital block is shared with 4 inputs- each form an identical analog pixel.
- A simple digital processing “core”





Impact of Pixel Size and Memory/Pixel

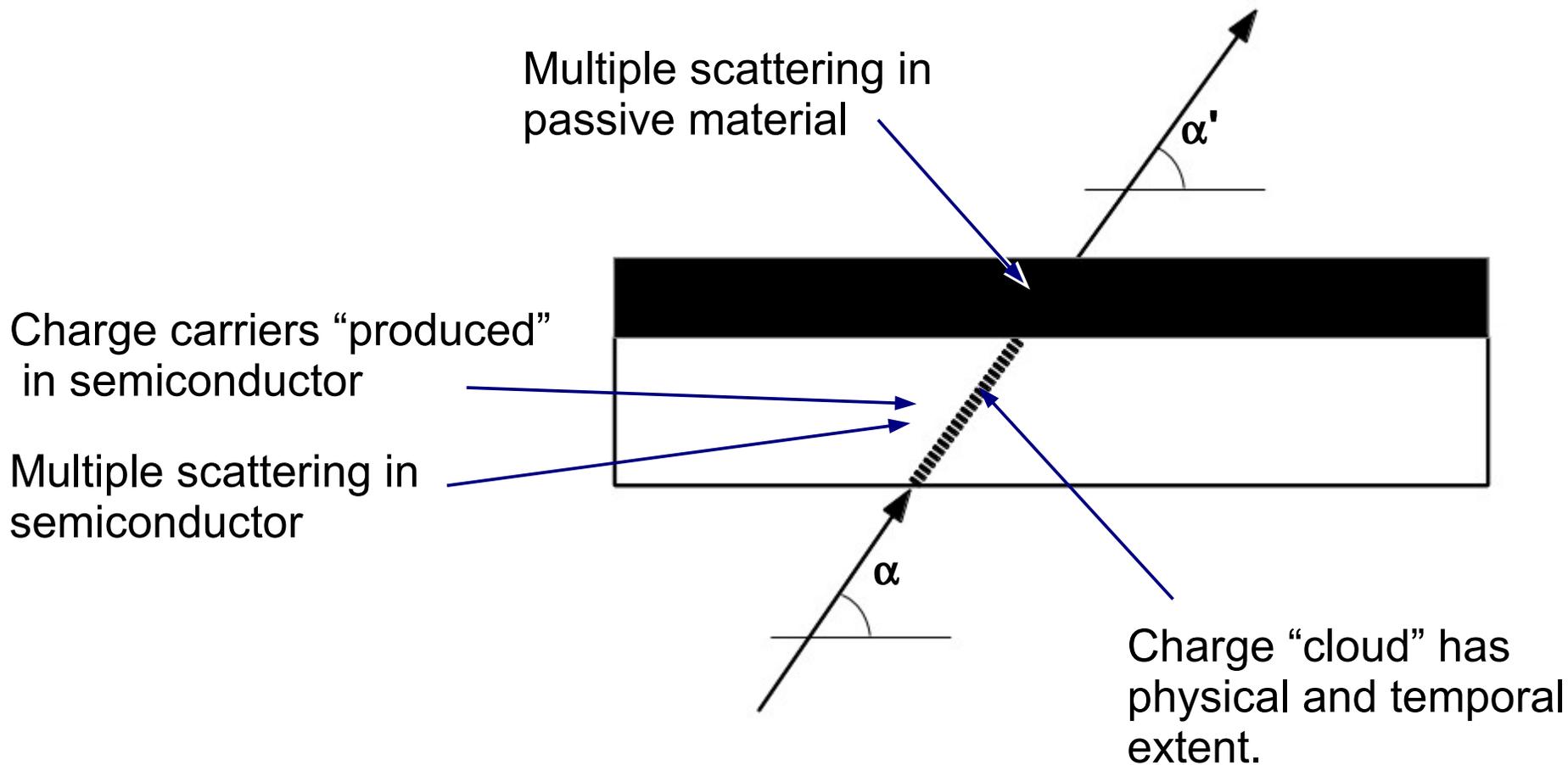


Architecture limit
wants higher circuit density

Occupancy limit
wants smaller/faster pixels
and thinner silicon



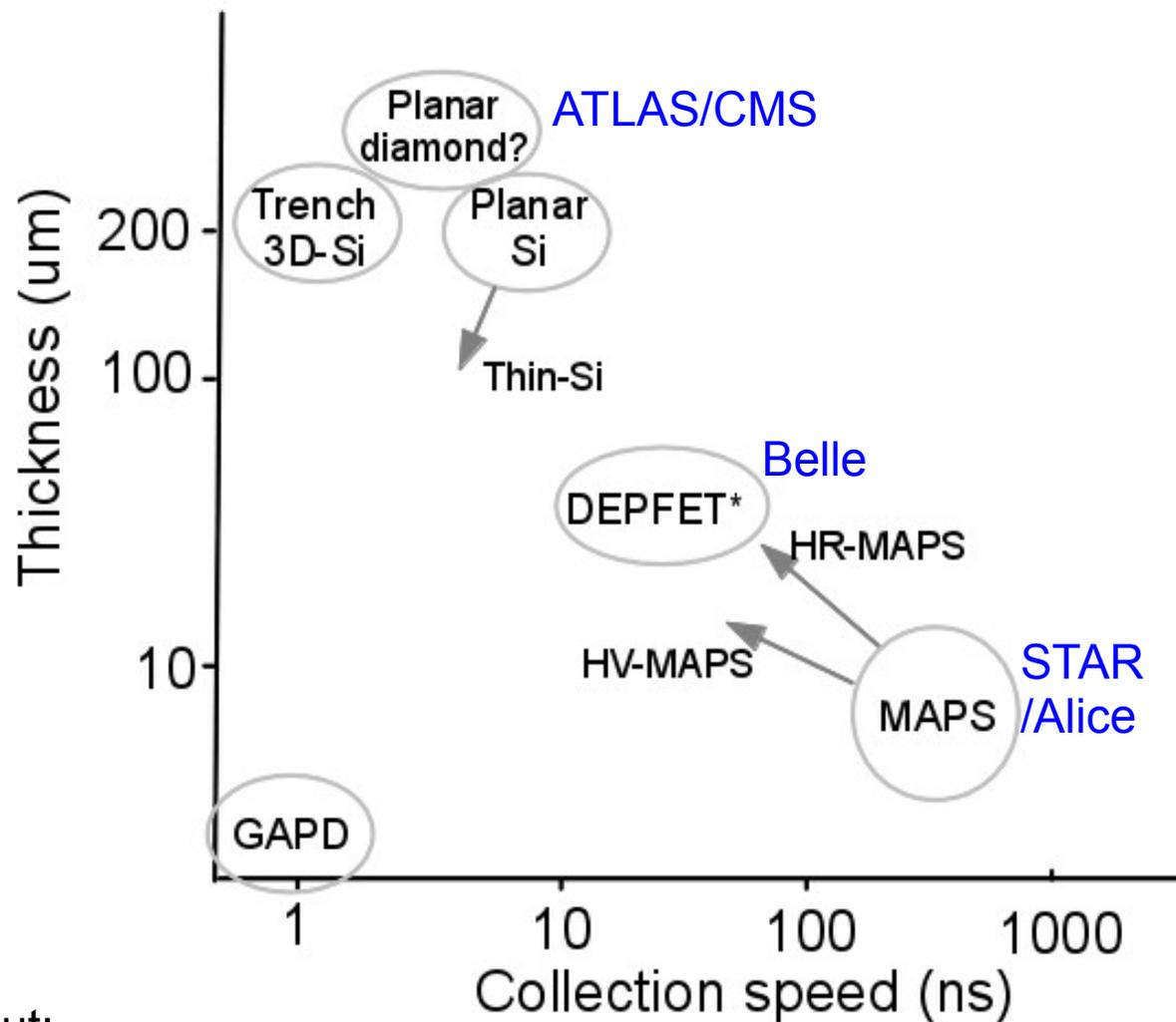
Charged particle sampling



Ideal pixellation: Collect the charge cloud without degrading time or spatial extent.



Charge Cloud Collection Status



(*) DEPFET use rolling shutter readout: much slower than charge collection



Charge Cloud Collection Goals

