RD53B Verification Update

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Building a Chip

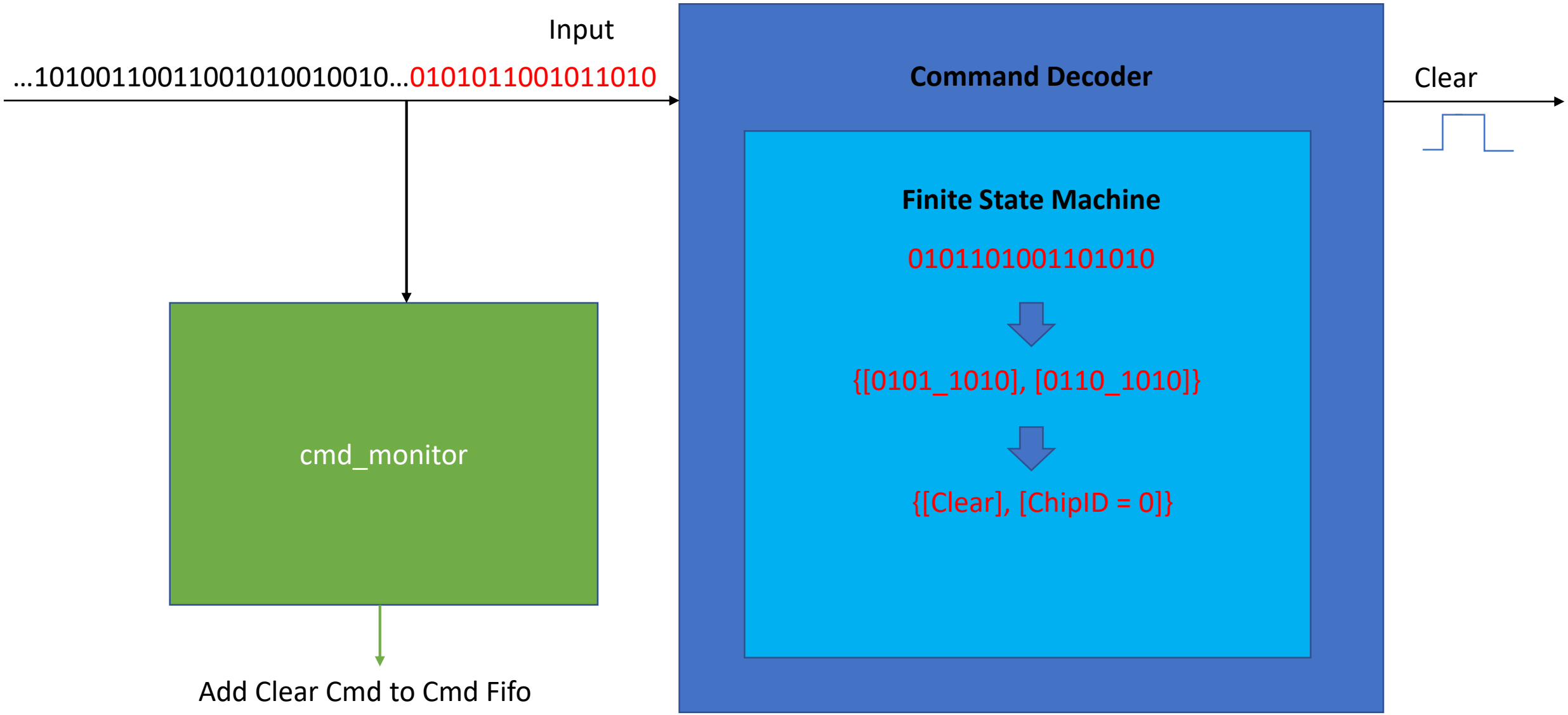
- Chip is designed by an IC Engineer and verified through a verification engineer.
- Need a way to model the physical blocks and logic of the chip using code.
- Verification done through modeling the chip using System Verilog and the Universal Verification Methodology (UVM).
- System Verilog is a hardware verification and description language similar to C++ but different in many ways.
- Through System Verilog & UVM you can:
  - Write up the logic and parts that make up the chip (DUT).
  - Write up the testbench to simulate the DUT and analyze the results.

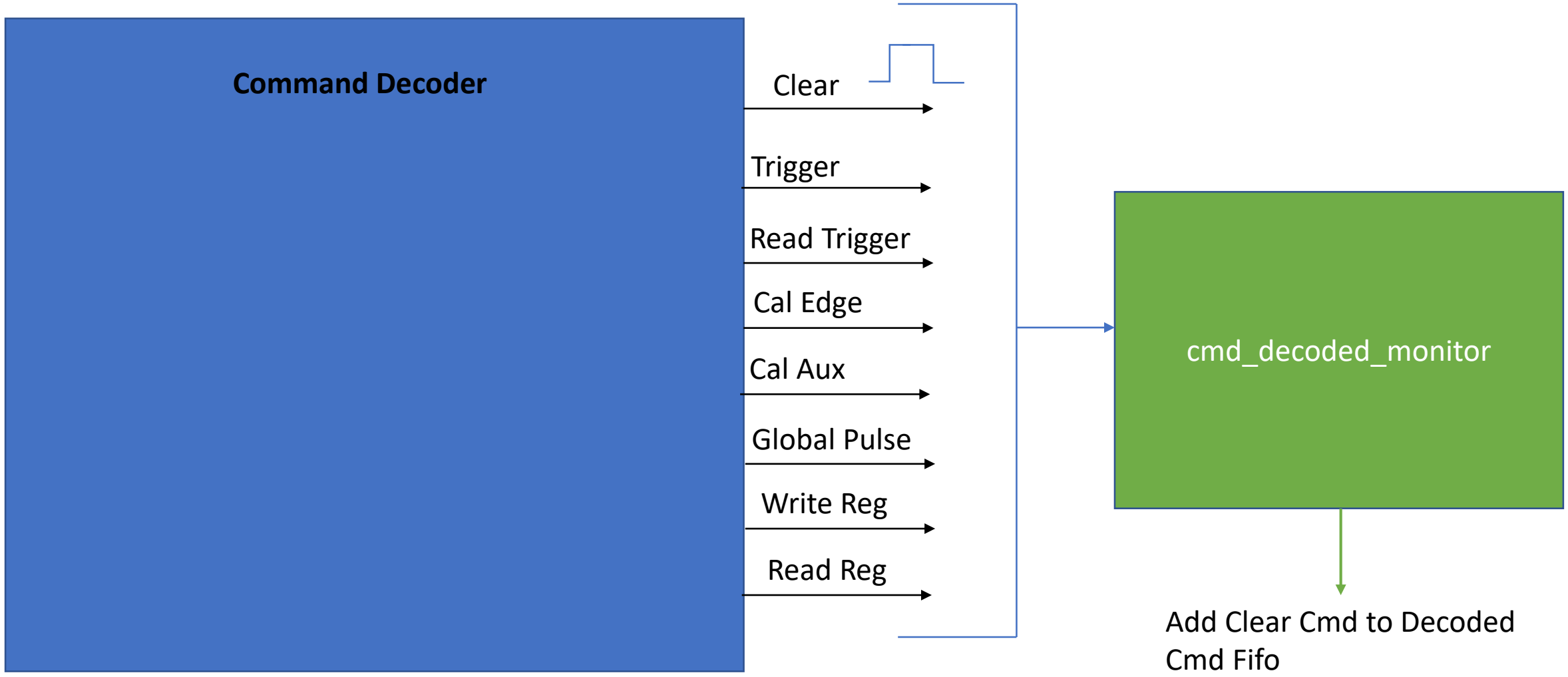
Command decoder verification

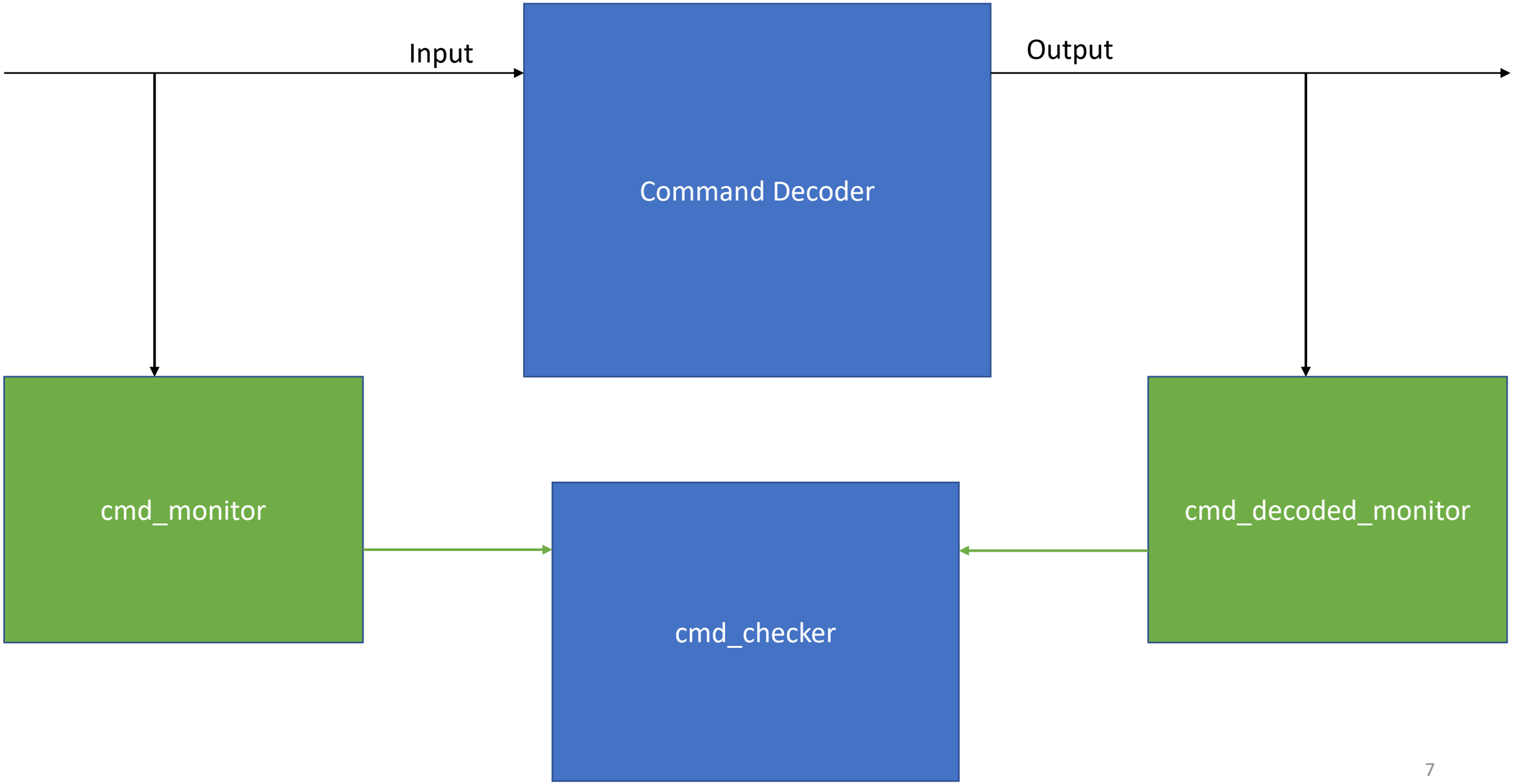
- [x] change position of ChipID in commands (after done at RTL @beccher , Manual: table 4)
- [x] extend multiple-write version of write register, to configure subsequently pixel pairs with 10 bits TDAC each (after done at RTL #102 (closed)) AND add test for this mode and for enable-bit-only write (3bits)
- [ ] automation of command decoding verification
  - [x] update command decoder reference model to include all commands in the command checker
    - timing of commands (Manual: executed 25ns after last frame, apart from Trigger, Cal and GP which dep. on delay and duration)
- [ ] constraint random test (with functional coverage?)
- [x] test for right/wrong chip ID - if wrong, expected to be processed (no error) but not executed
- [x] test for broadcast (all chip IDs)
- [x] test for recoverable bit flips - NO MORE recoverable
- [ ] test including readout of trigger tag with a bit flip with ReadTrigger
- [ ] test/assertions for remaining diagnostic counters (LockLoss count, BCIDcnt or any other if added)
- [ ] test for interleaving idles between a command and its data (X X C X D X D)
- [ ] test for interleaving a trigger between a command and its data (X X C T D D X)
- [ ] test for interleaving multiple triggers between a command and its data (X X C T T D D X)
- [ ] test for executing multiple commands consecutively (X X C D D C D D X)
  - in the past noticed interference between write/read regs , possibly only related to auto-row . Re-check.
- [x] tests for invalid conditions (Table 6 from Manual) should be re-checked
- [x] make list of tests in verification as part of regression - done for existent tests

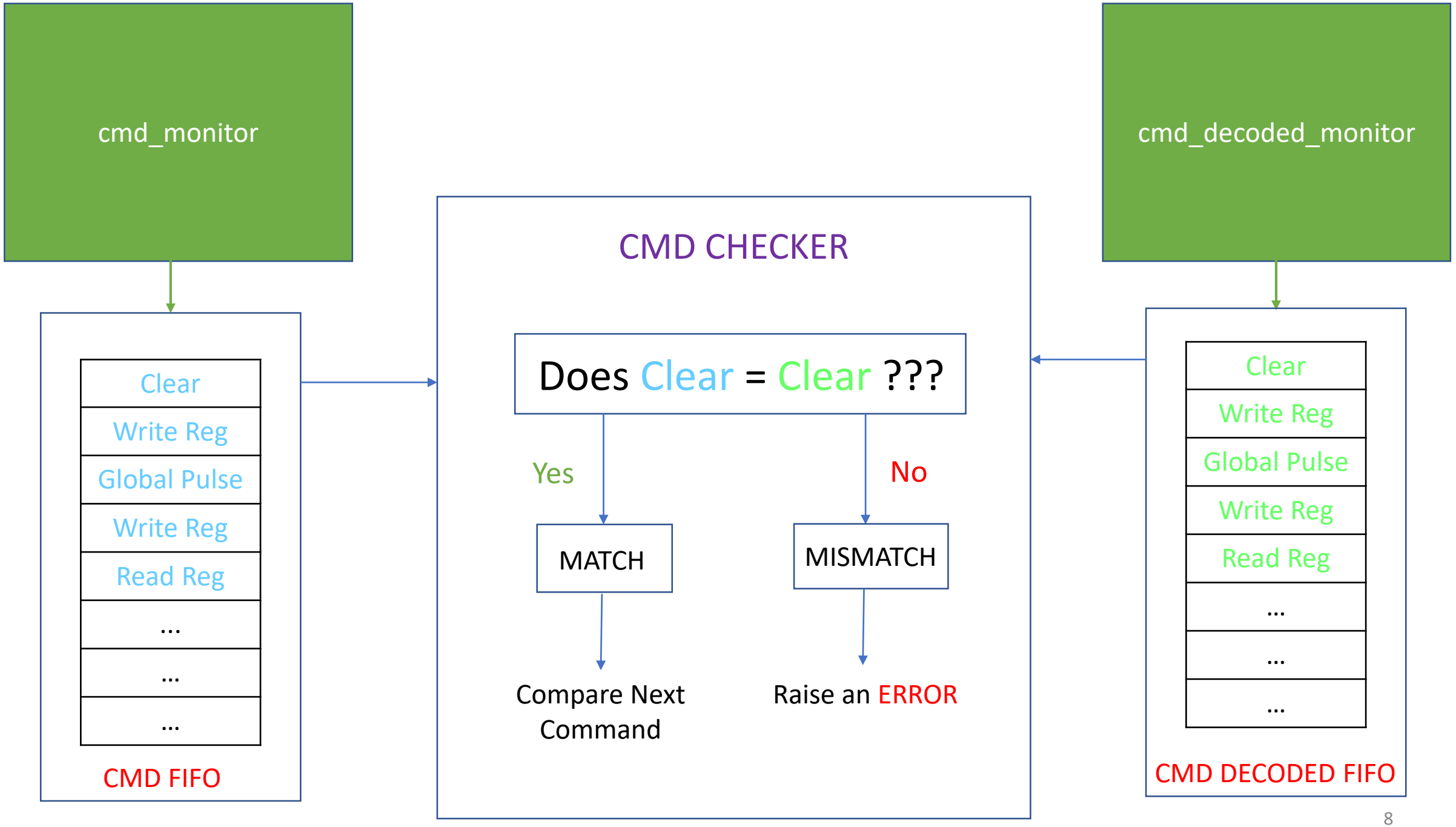
My Responsibilities

Command Decoder				
Correct command decoding	typical operation in standard tests. Old cmd_rand_stream for more randomized. TODO: re-use/write a randomized command generation and use/evolve cmd checker to verify correct command decoding. TODO: add new commands.	HIGH	Sara/Cesar	directed/random
second level trigger commands	WIP: Being added for all hit and trigs tests. Option to be configured (either from RefModel or parameter int est)	HIGH	Sara	
Right/wrong chip ID	test custom cmd with cmd_correct/wrong_chipID_seq.sv: very old (possibly with wrong address fields). TODO: revise/rewrite.	HIGH		directed
Broadcast (all chip IDs)	test custom cmd with cmd_broadcast_chipID_seq : very old (possibly with wrong address fields). TODO:revise/rewrite.	HIGH		directed
Recoverable bitflips	top_test_cmd_bitflip_recoverable. TODO: complete for all commands (ECR, BCR)	LOW	Cesar	directed (only
Bitflip warning counting	TODO: No test/sequence.	LOW	Cesar	directed (only
Response to any invalid/unexpected symbols.	TODO: No test/sequence.	LOW	Cesar	directed (only
Bitflip error counting	TODO: No test/sequence.	LOW	Cesar	directed (only
Command errors	TODO: No test/sequence.	LOW	Cesar	directed (only
Command error counting	TODO: No test/sequence.	LOW	Cesar	directed (only
Trigger position (4 BXs)	Custom cmd test with cmd_seq_triggers. But should be already checked by random triggers.	HIGH	Cesar	directed (only
Remaining diagnostic counters (LockLoss count, BCIDcnt or any other if added)	TODO: No test/sequence.	LOW		
Global pulse route	TODO: No dedicated test/sequence.	LOW		
No interference among subsequent commands unless they are time-consuming [i.e. global pulse and cal commands, special read reg (ring oscilaltors].	TODO (noticed subsequent write/read in sequence seem to interfere. maybe only related to the auto-increment).	MED		
Global configuration	General TODO: Register Model	HIGH	Joel	
Write valid data	top_test_global_conf_allones.sv,top_test_global_conf_allzeros, TODO: random data with Register Model.	HIGH	Peilian	directed
Write non valid data	TODO: No test/sequence.	HIGH	Peilian	
Write non valid address	TODO: No test/sequence.	HIGH	Peilian	
Register connections	No dedicated test.			

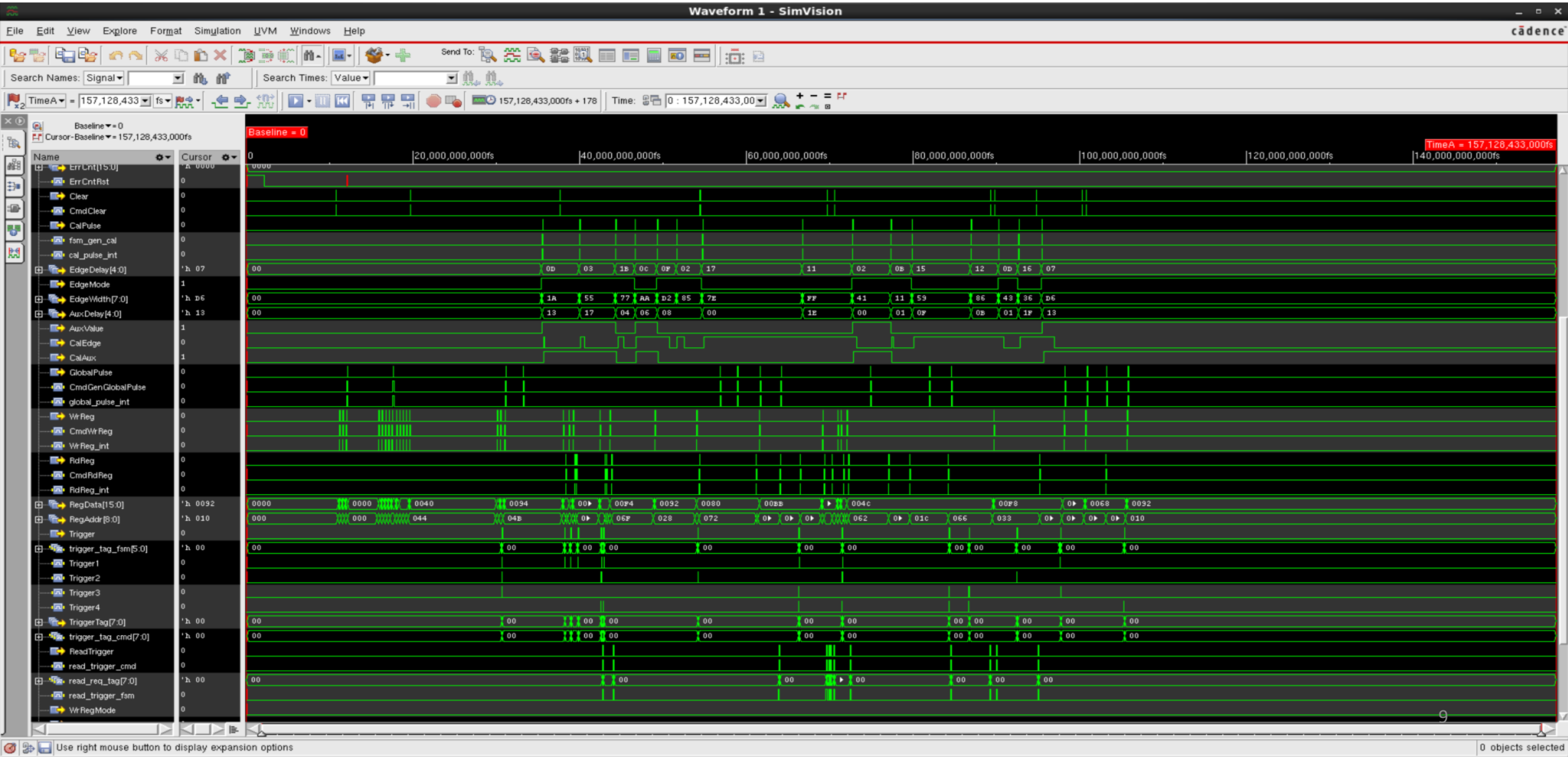

Input
…10100110011001010010010…0101011001011010
Command Decoder
Clear
Finite State Machine
0101101001101010
{[0101_1010], [0110_1010]}
{[Clear], [ChipID = 0]}
cmd_monitor
Add Clear Cmd to Cmd Fifo


Command Decoder
Clear
Trigger
Read Trigger
Cal Edge
Cal Aux
Global Pulse
Write Reg
Read Reg
cmd_decoded_monitor
Add Clear Cmd to Decoded Cmd Fifo


Input
Command Decoder
Output
cmd_monitor
cmd_checker
cmd_decoded_monitor

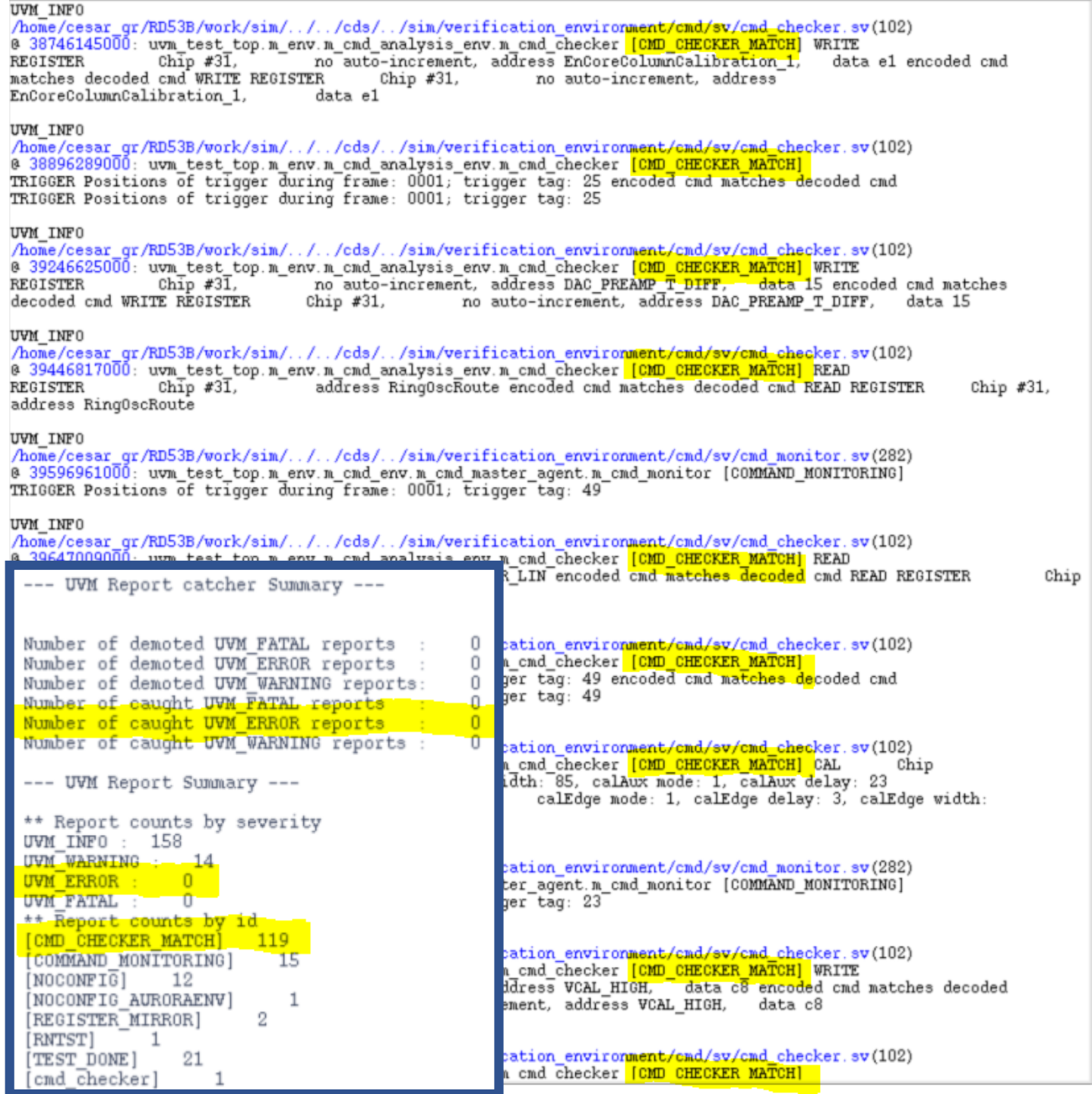

cmd_monitor
cmd_decoded_monitor
CMD CHECKER
Does Clear = Clear ???
Yes
No
MATCH
MISMATCH
Compare Next Command
Raise an ERROR
Clear
Write Reg
Global Pulse
Write Reg
Read Reg
...
...
...
CMD FIFO
Clear
Write Reg
Global Pulse
Write Reg
Read Reg
...
...
...
CMD DECODED FIFO

Command Checker Verification



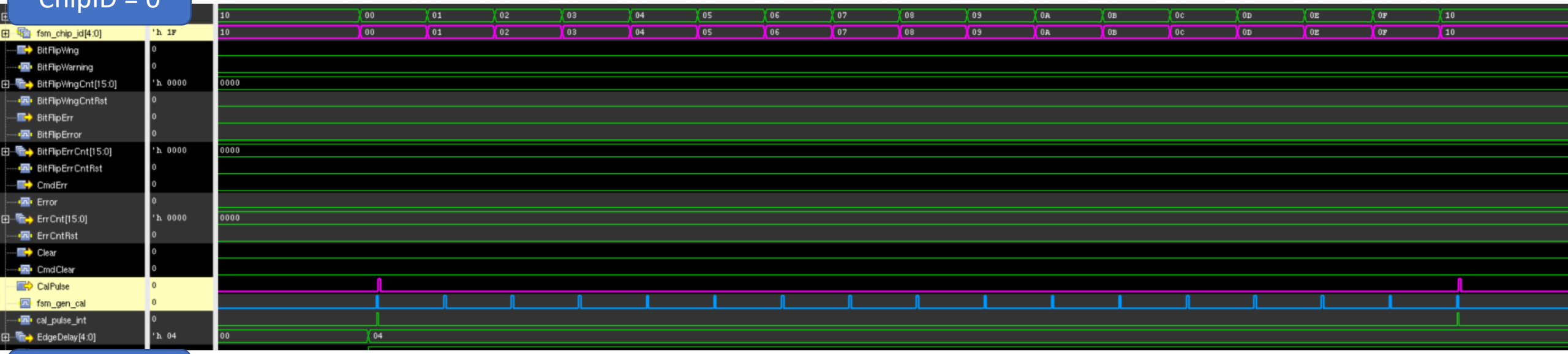
Command Checker Verification

- 100 Randomly generated commands sent.
- The data sent with each command is also randomly generated (within allowable values)
- Command Checker finds a match between Decoded and Encoded monitors for every command sent.



ChipID Test

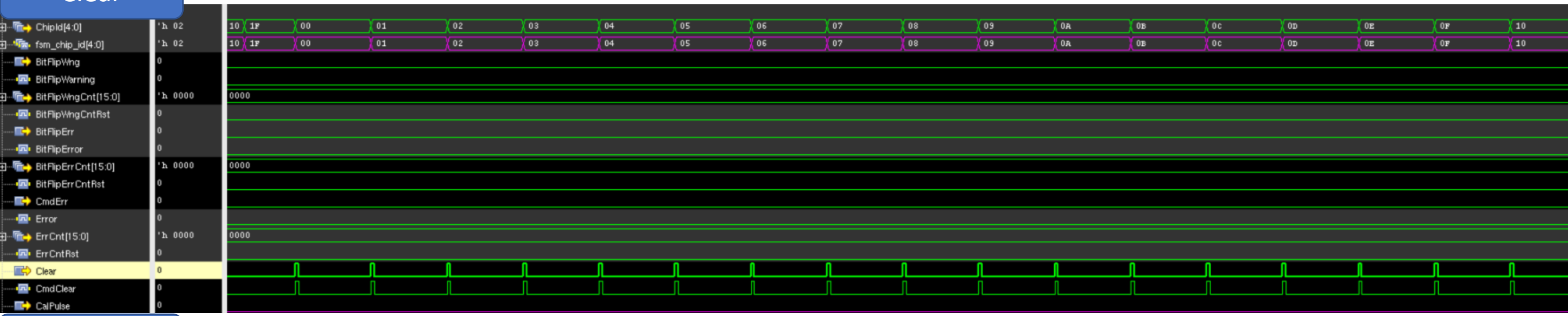
ChipID = 0



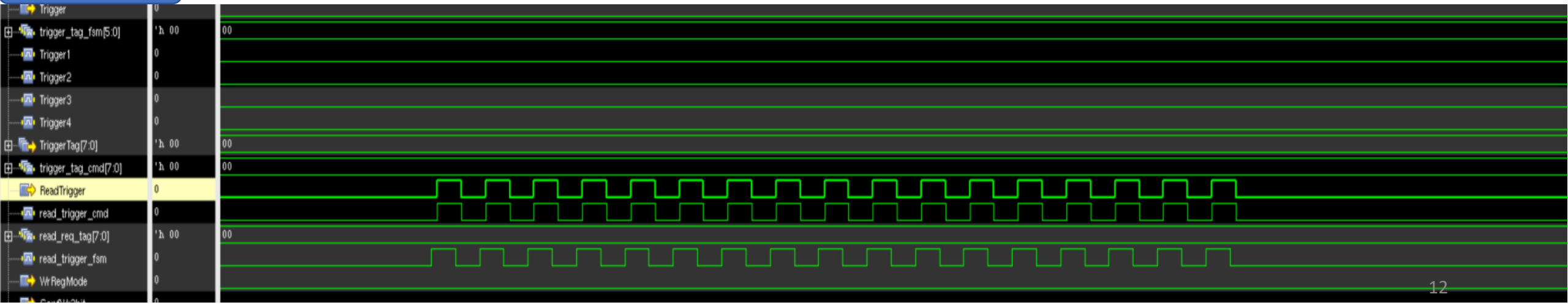
ChipID = 8

ChipID Issue

Clear

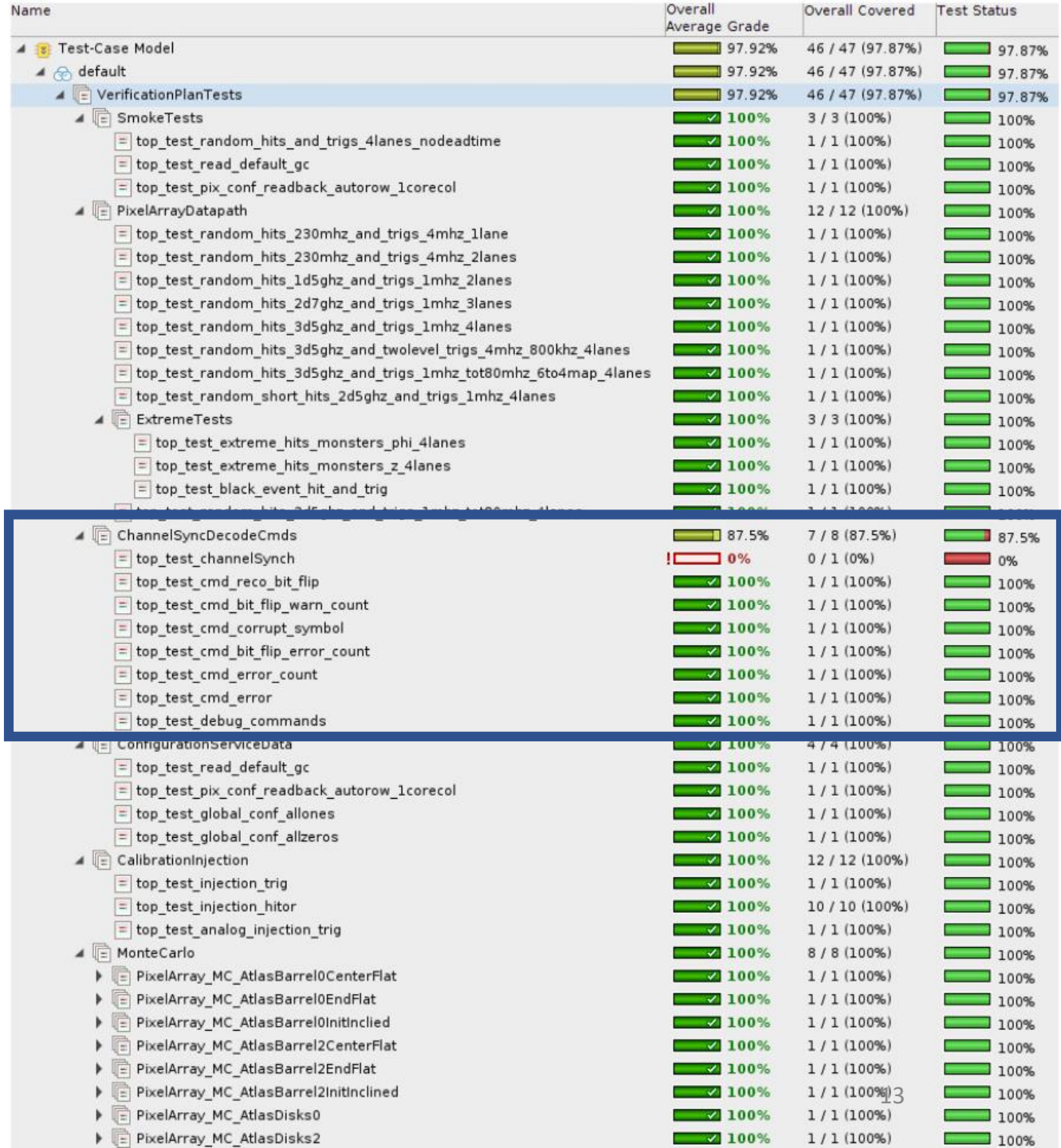


Read Trigger



Current Status

- Here you can see the tests I mentioned previously.
- Not seen here are tests for correct ChipID behavior or correct broadcast ChipID behavior



Issues with verification sub-tasks

Startup, Resets, Clocks verification 3 of 8 tasks completed
#95 · opened 6 months ago by Sara Marconi To Do Verification 0

Data merging verification 2 of 3 tasks completed
#93 · opened 6 months ago by Sara Marconi Doing Verification 0

Global configuration verification 5 of 10 tasks completed
#90 · opened 6 months ago by Sara Marconi Sep 30, 2019 Doing Verification 0

Command decoder verification 5 of 16 tasks completed
#89 · opened 6 months ago by Sara Marconi Doing Verification 0

Global pulse verification 2 of 4 tasks completed
#171 · opened 2 months ago by Sara Marconi To Do Verification 1

Verify all possible initialization states of ChannelSync
#154 · opened 3 months ago by Sara Marconi To Do Verification 1

ServiceData and Aurora verification 3 of 10 tasks completed
#92 · opened 6 months ago by Sara Marconi To Do Verification 1

Pixel configuration verification 6 of 13 tasks completed
#91 · opened 6 months ago by Sara Marconi Doing Verification 1

Digital Chip Bottom data flow verification 3 of 9 tasks completed
#87 · opened 6 months ago by Sara Marconi To Do Verification 1

PixelArrayReadout verification 8 of 12 tasks completed
#86 · opened 6 months ago by Sara Marconi To Do Verification 1

Verification of extreme cases 6 of 9 tasks completed
#85 · opened 6 months ago by Sara Marconi To Do Verification 1

Verify eFuses block
#191 · opened 1 month ago by Roberto Beccherle Sep 30, 2019 Simulation Verification 2

General Purpose IO verification
#173 · opened 2 months ago by Sara Marconi To Do Verification 2

Prev 1 2 Next

Label ~BUG

List of bugs open.

Clear command chipID ignored by command decoder
#205 · opened 1 week ago by Sara Marconi BUG Design Verification 0

Unexpected tag (249) readback in full chip top_test_analog_injection_trig
#195 · opened 3 weeks ago by Sara Marconi BUG Design Verification 0

Readback pixel configuration autorow , issue when switching to next col
#193 · opened 1 month ago by Sara Marconi BUG Design Verification 0

floating inputs
#196 · opened 3 weeks ago by Giuseppe De Robertis BUG

Aurora Output lane selection mismatch between LaneAlign and Aurora Block
#148 · opened 4 months ago by Timon Heim BUG RTL

updated 46 minutes ago

0

Verification Status

Sara Marconi

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Conclusion

- Apart from small hiccups here and there command decoder reference model is complete.
- Invalid command decoder input tests have been written, still need to report small issues.
- ChipID tests have been written, issues have been found and reported.
- Trigger tests have been written and proper trigger tag verified.
- Need to write tests for read trigger, WrReg/RdReg interference, and Interleaving Commands w/ trigger, syncs, etc.
- Any other test that comes up between now and submission (and beyond?)