

# RD53B Verification Update

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# Building a Chip

- Chip is designed by an IC Engineer and verified through a verification engineer.
- Need a way to model the physical blocks and logic of the chip using code.
- Verification done through modeling the chip using System Verilog and the Universal Verification Methodology (UVM).
- System Verilog is a hardware verification and description language similar to C++ but different in many ways.
- Through System Verilog & UVM you can:
  - Write up the logic and parts that make up the chip (DUT).
  - Write up the testbench to simulate the DUT and analyze the results.

# Command decoder verification

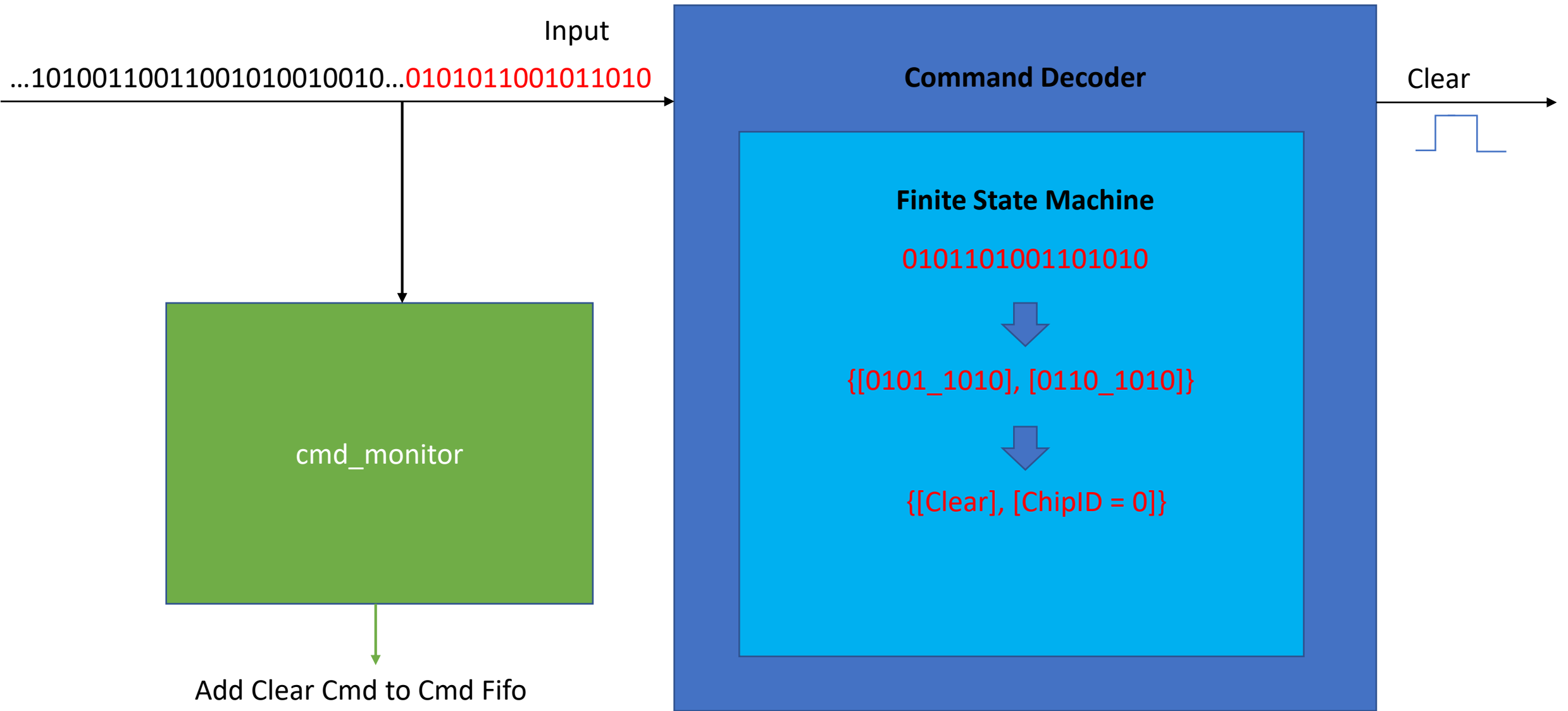


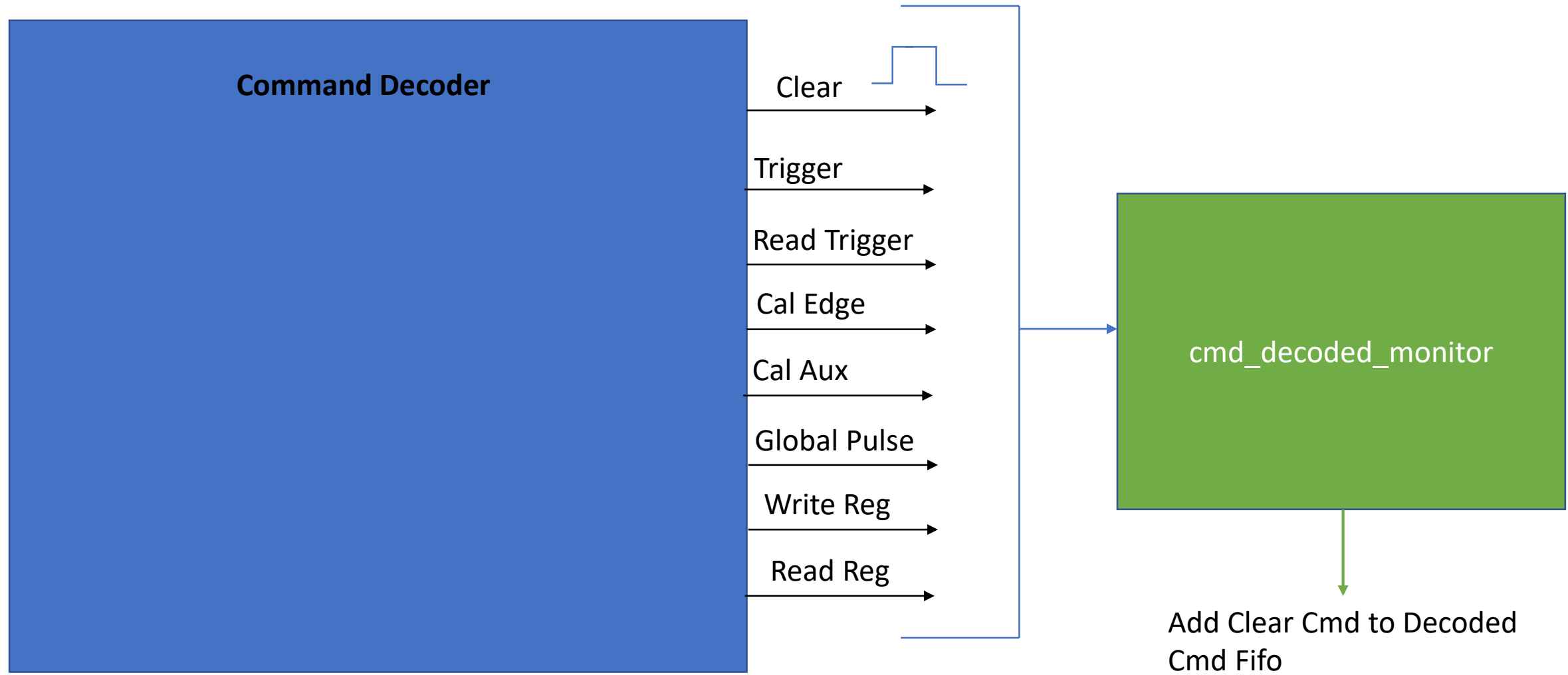
- ☒ change position of ChipID in commands (after done at RTL [@beccher](#) , Manual: table 4)
- ☒ extend multiple-write version of write register, to configure subsequently pixel pairs with 10 bits TDAC each (after done at RTL [#102 \(closed\)](#) ) AND add test for this mode and for enable-bit-only write (3bits)
- ☐ automation of command decoding verification
  - ☒ update command decoder reference model to include all commands in the command checker
    - timing of commands (Manual: executed 25ns after last frame, apart from Trigger, Cal and GP which dep. on delay and duration)
  - ☐ constraint random test (with functional coverage?)
- ☒ test for right/wrong chip ID - if wrong, expected to be processed (no error) but not executed
- ☒ test for broadcast (all chip IDs)
- ☒ test for recoverable bit flips - NO MORE recoverable
- ☐ test including readout of trigger tag with a bit flip with ReadTrigger
- ☐ test/assertions for remaining diagnostic counters (LockLoss count, BCIDcnt or any other if added)
- ☐ test for interleaving idles between a command and its data ( X X C X D X D )
- ☐ test for interleaving a trigger between a command and its data ( X X C T D D X )
- ☐ test for interleaving multiple triggers between a command and its data ( X X C T T D D X )
- ☐ test for executing multiple commands consecutively ( X X C D D C D D X )
  - in the past noticed interference between write/read regs , possibly only related to auto-row . Re-check.
- ☒ tests for invalid conditions (Table 6 from Manual) should be re-checked
- ☒ make list of tests in verification as part of regression - done for existent tests

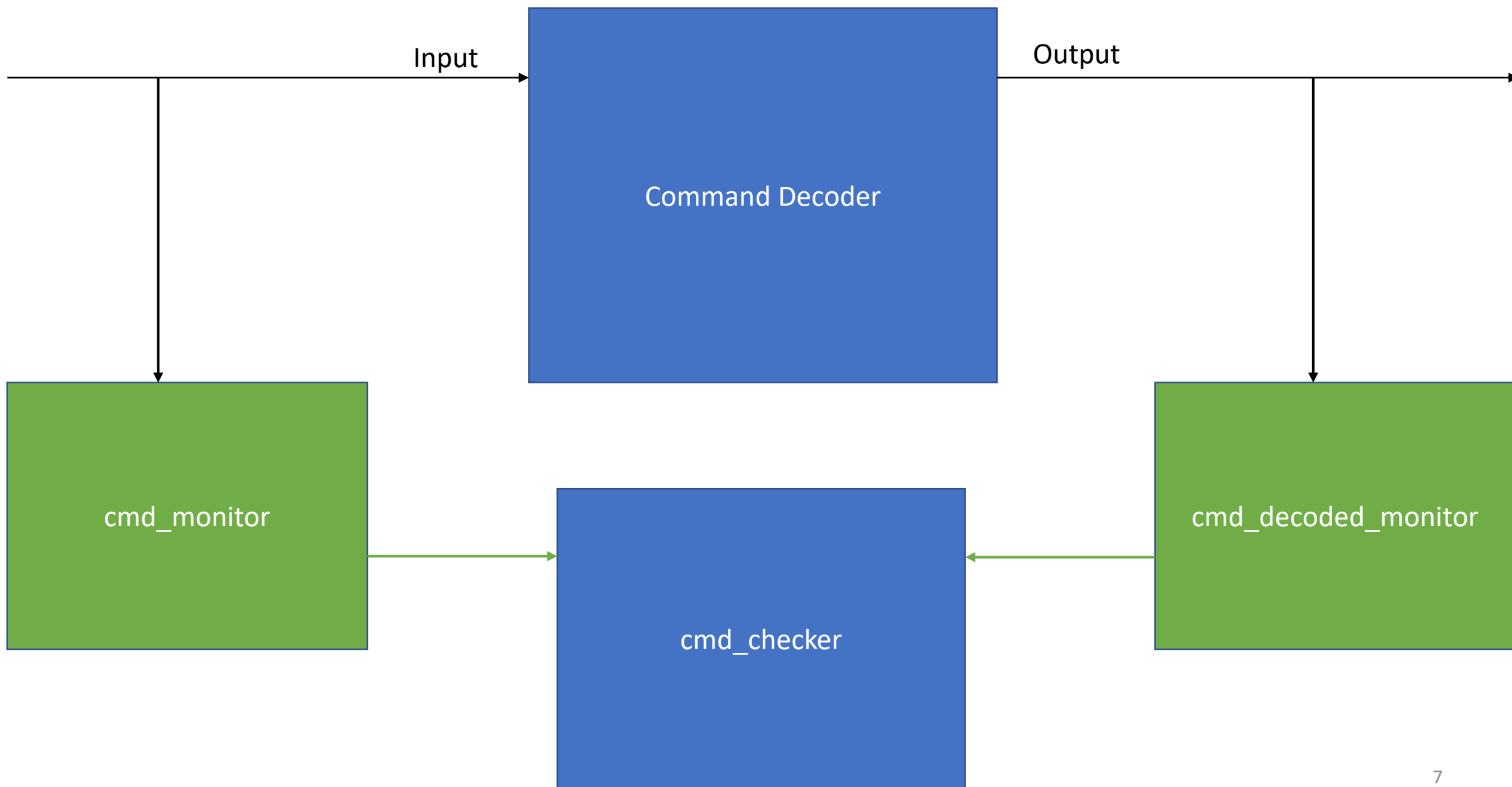
# My Responsibilities

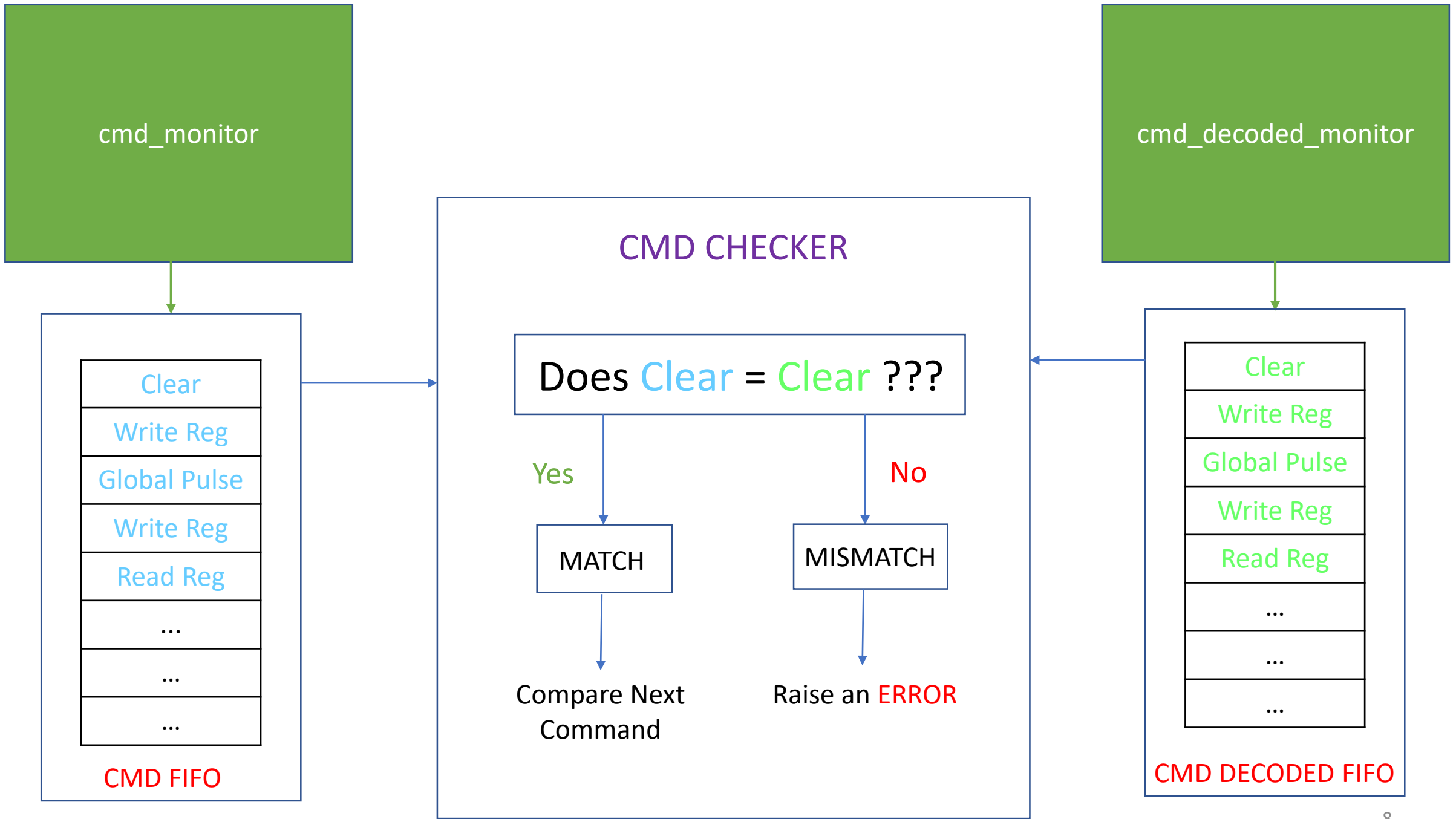
## Command Decoder

Correct command decoding	typical operation in standard tests. Old cmd_rand_stream for more randomized. TODO: re-use/write a randomized command generation and use/evolve cmd checker to verify correct command decoding. TODO: add new commands.	HIGH	Sara/Cesar	directed/random
second level trigger commands	WIP: Being added for all hit and trigs tests. Option to be configured (either from RefModel or parameter int est)	HIGH	Sara	
Right/wrong chip ID	test custom cmd with cmd_correct/wrong_chipID_seq.sv: very old (possibly with wrong address fields). TODO: revise/rewrite.	HIGH		directed
Broadcast (all chip IDs)	test custom cmd with cmd_broadcast_chipID_seq : very old (possibly with wrong address fields). TODO:revise/rewrite.	HIGH		directed
Recoverable bitflips	top_test_cmd_bitflip_recoverable. TODO: complete for all commands (ECR, BCR)	LOW	Cesar	directed (only
Bitflip warning counting	TODO: No test/sequence.	LOW	Cesar	directed (only
Response to any invalid/unexpected symbols.	TODO: No test/sequence.	LOW	Cesar	directed (only
Bitflip error counting	TODO: No test/sequence.	LOW	Cesar	directed (only
Command errors	TODO: No test/sequence.	LOW	Cesar	directed (only
Command error counting	TODO: No test/sequence.	LOW	Cesar	directed (only
Trigger position (4 BXs)	Custom cmd test with cmd_seq_triggers. But should be already checked by random triggers.	HIGH	Cesar	directed (only
Remaining diagnostic counters (LockLoss count, BCIDcnt or any other if added)	TODO: No test/sequence.	LOW		
Global pulse route	TODO: No dedicated test/sequence.	LOW		
No interference among subsequent commands unless they are time-consuming [ i.e. global pulse and cal commands, special read reg (ring oscillators)].	TODO (noticed subsequent write/read in sequence seem to interfere. maybe only related to the auto-increment).	MED		
<b>Global configuration</b>	General TODO: Register Model	HIGH	Joel	
Write valid data	top_test_global_conf_allones.sv,top_test_global_conf_allzeros, TODO: random data with Register Model.	HIGH	Peilian	directed
Write non valid data	TODO: No test/sequence.	HIGH	Peilian	
Write non valid address	TODO: No test/sequence.	HIGH	Peilian	
Register connections	No dedicated test.			



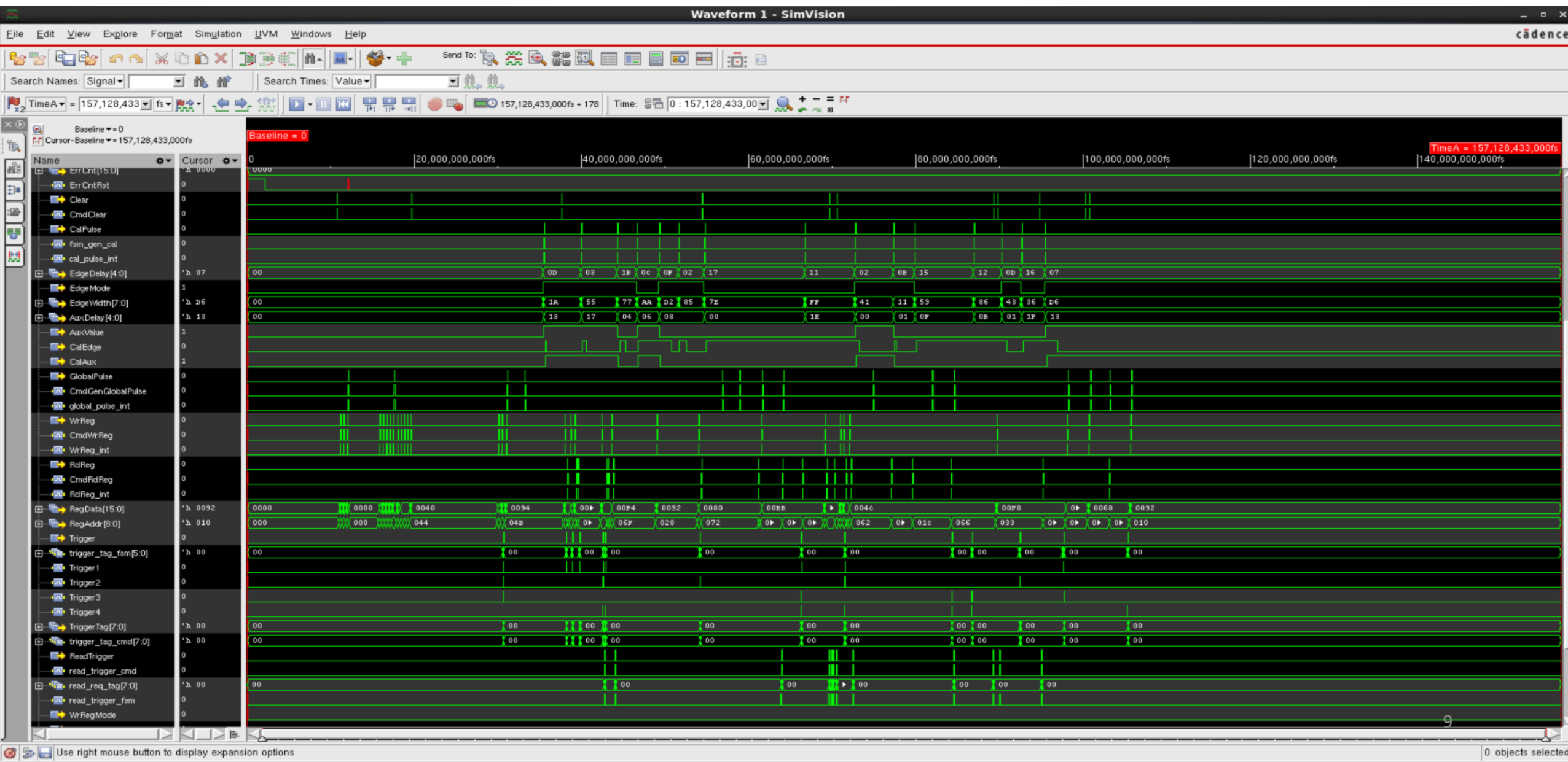








# Command Checker Verification



# Command Checker Verification

- 100 Randomly generated commands sent.
- The data sent with each command is also randomly generated (within allowable values)
- Command Checker finds a match between Decoded and Encoded monitors for every command sent.

```
UVM_INFO
/home/cesar_gr/RD53B/work/sim/../../../../cds/./sim/verification_environment/cmd/sv/cmd_checker.sv(102)
@ 38746145000: uvm_test_top.m_env.m_cmd_analysis_env.m_cmd_checker [CMD_CHECKER_MATCH] WRITE
REGISTER      Chip #31,      no auto-increment, address EnCoreColumnCalibration_1,      data e1 encoded cmd
matches decoded cmd WRITE REGISTER      Chip #31,      no auto-increment, address
EnCoreColumnCalibration_1,      data e1

UVM_INFO
/home/cesar_gr/RD53B/work/sim/../../../../cds/./sim/verification_environment/cmd/sv/cmd_checker.sv(102)
@ 38896289000: uvm_test_top.m_env.m_cmd_analysis_env.m_cmd_checker [CMD_CHECKER_MATCH]
TRIGGER Positions of trigger during frame: 0001; trigger tag: 25 encoded cmd matches decoded cmd
TRIGGER Positions of trigger during frame: 0001; trigger tag: 25

UVM_INFO
/home/cesar_gr/RD53B/work/sim/../../../../cds/./sim/verification_environment/cmd/sv/cmd_checker.sv(102)
@ 39246625000: uvm_test_top.m_env.m_cmd_analysis_env.m_cmd_checker [CMD_CHECKER_MATCH] WRITE
REGISTER      Chip #31,      no auto-increment, address DAC_PREAMP_T_DIFF,      data 15 encoded cmd matches
decoded cmd WRITE REGISTER      Chip #31,      no auto-increment, address DAC_PREAMP_T_DIFF,      data 15

UVM_INFO
/home/cesar_gr/RD53B/work/sim/../../../../cds/./sim/verification_environment/cmd/sv/cmd_checker.sv(102)
@ 39446817000: uvm_test_top.m_env.m_cmd_analysis_env.m_cmd_checker [CMD_CHECKER_MATCH] READ
REGISTER      Chip #31,      address RingOscRoute encoded cmd matches decoded cmd READ REGISTER      Chip #31,
address RingOscRoute

UVM_INFO
/home/cesar_gr/RD53B/work/sim/../../../../cds/./sim/verification_environment/cmd/sv/cmd_monitor.sv(282)
@ 39596961000: uvm_test_top.m_env.m_cmd_env.m_cmd_master_agent.m_cmd_monitor [COMMAND_MONITORING]
TRIGGER Positions of trigger during frame: 0001; trigger tag: 49

UVM_INFO
/home/cesar_gr/RD53B/work/sim/../../../../cds/./sim/verification_environment/cmd/sv/cmd_checker.sv(102)
@ 39647009000: uvm_test_top.m_env.m_cmd_analysis_env.m_cmd_checker [CMD_CHECKER_MATCH] READ
REGISTER      Chip #31,      address RingOscRoute encoded cmd matches decoded cmd READ REGISTER      Chip #31,
address RingOscRoute

--- UVM Report catcher Summary ---

Number of demoted UVM_FATAL reports : 0
Number of demoted UVM_ERROR reports : 0
Number of demoted UVM_WARNING reports: 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0

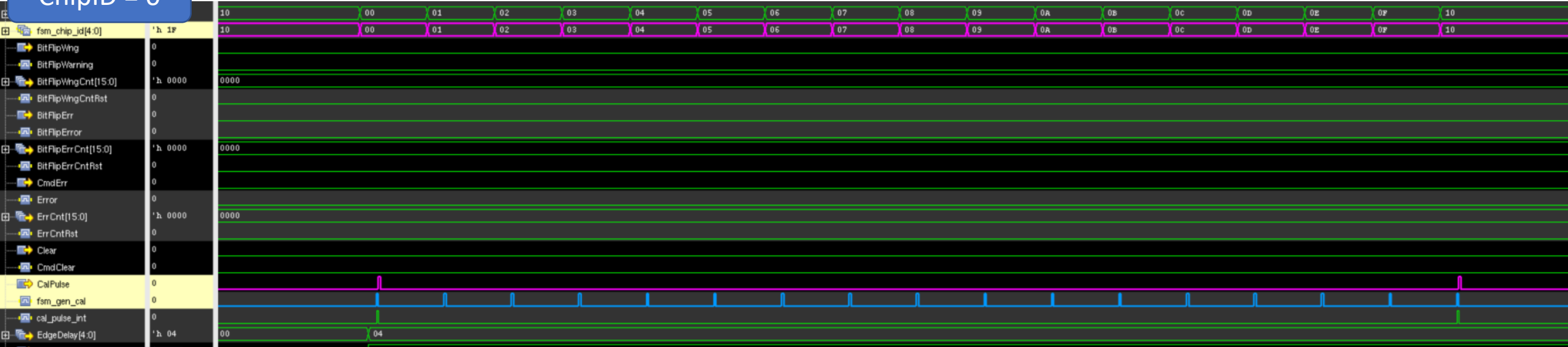
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 158
UVM_WARNING : 14
UVM_ERROR : 0
UVM_FATAL : 0

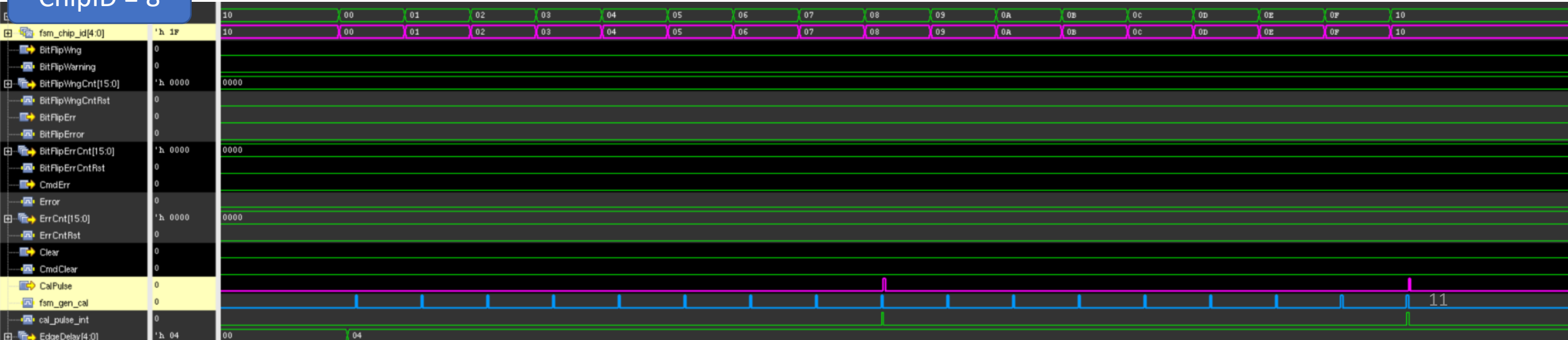
** Report counts by id
[CMD_CHECKER_MATCH] 119
[COMMAND_MONITORING] 15
[NOCONFIG] 12
[NOCONFIG_AURORAENV] 1
[REGISTER_MIRROR] 2
[RNTST] 1
[TEST_DONE] 21
[cmd_checker] 1
```

# ChipID Test

ChipID = 0

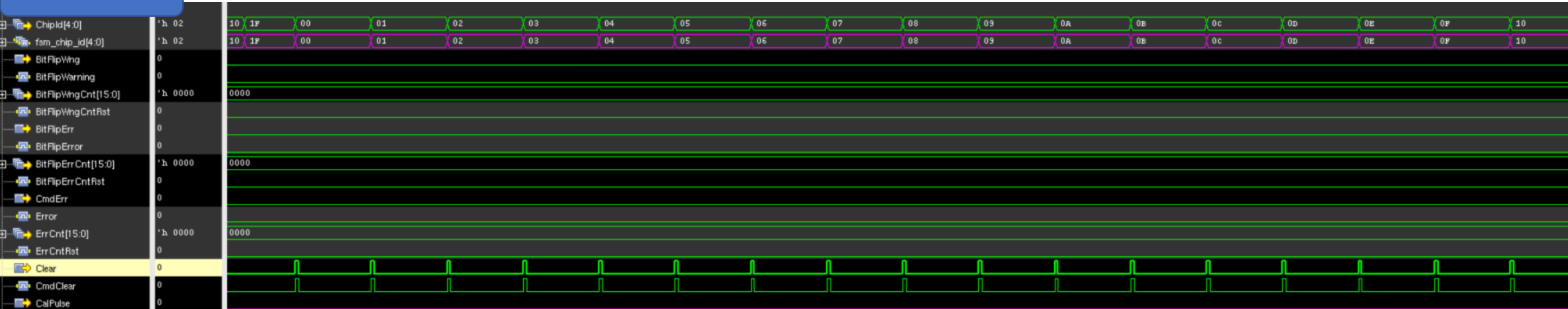


ChipID = 8

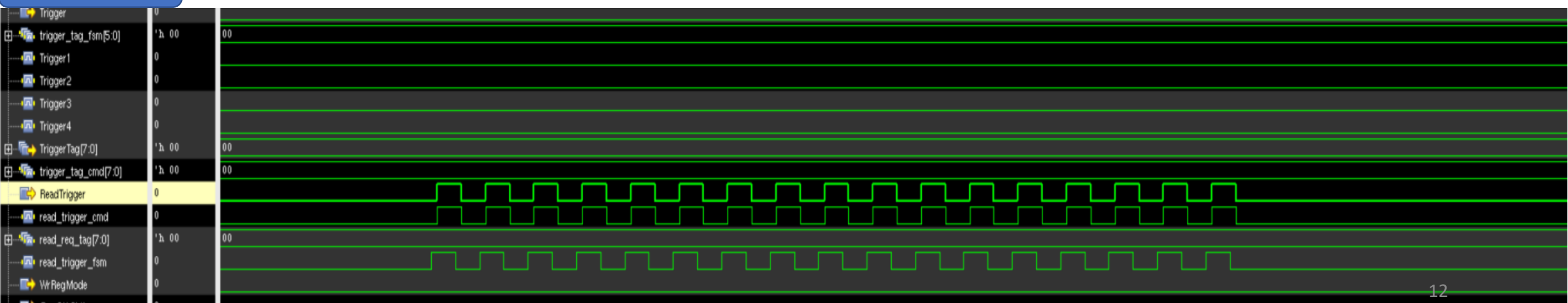


# ChipID Issue

Clear



Read Trigger



# Current Status

- Here you can see the tests I mentioned previously.
- Not seen here are tests for correct ChipID behavior or correct broadcast ChipID behavior

Name	Overall Average Grade	Overall Covered	Test Status
Test-Case Model	97.92%	46 / 47 (97.87%)	97.87%
default	97.92%	46 / 47 (97.87%)	97.87%
VerificationPlanTests	97.92%	46 / 47 (97.87%)	97.87%
SmokeTests	100%	3 / 3 (100%)	100%
top_test_random_hits_and_trigs_4lanes_nodetime	100%	1 / 1 (100%)	100%
top_test_read_default_gc	100%	1 / 1 (100%)	100%
top_test_pix_conf_readback_autorow_1corecol	100%	1 / 1 (100%)	100%
PixelFormatDatapath	100%	12 / 12 (100%)	100%
top_test_random_hits_230mhz_and_trigs_4mhz_1lane	100%	1 / 1 (100%)	100%
top_test_random_hits_230mhz_and_trigs_4mhz_2lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_1d5ghz_and_trigs_1mhz_2lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_2d7ghz_and_trigs_1mhz_3lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_3d5ghz_and_trigs_1mhz_4lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_3d5ghz_and_twolevel_trigs_4mhz_800khz_4lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_3d5ghz_and_trigs_1mhz_tot80mhz_6to4map_4lanes	100%	1 / 1 (100%)	100%
top_test_random_short_hits_2d5ghz_and_trigs_1mhz_4lanes	100%	1 / 1 (100%)	100%
ExtremeTests	100%	3 / 3 (100%)	100%
top_test_extreme_hits_monsters_phi_4lanes	100%	1 / 1 (100%)	100%
top_test_extreme_hits_monsters_z_4lanes	100%	1 / 1 (100%)	100%
top_test_black_event_hit_and_trig	100%	1 / 1 (100%)	100%
top_test_black_event_hit_and_trig_15ghz_1lane_3hits_4lanes	100%	1 / 1 (100%)	100%
ChannelSyncDecodeCmds	87.5%	7 / 8 (87.5%)	87.5%
top_test_channelSynch	0%	0 / 1 (0%)	0%
top_test_cmd_reco_bit_flip	100%	1 / 1 (100%)	100%
top_test_cmd_bit_flip_warn_count	100%	1 / 1 (100%)	100%
top_test_cmd_corrupt_symbol	100%	1 / 1 (100%)	100%
top_test_cmd_bit_flip_error_count	100%	1 / 1 (100%)	100%
top_test_cmd_error_count	100%	1 / 1 (100%)	100%
top_test_cmd_error	100%	1 / 1 (100%)	100%
top_test_debug_commands	100%	1 / 1 (100%)	100%
ConfigurationServiceData	100%	4 / 4 (100%)	100%
top_test_read_default_gc	100%	1 / 1 (100%)	100%
top_test_pix_conf_readback_autorow_1corecol	100%	1 / 1 (100%)	100%
top_test_global_conf_allones	100%	1 / 1 (100%)	100%
top_test_global_conf_allzeros	100%	1 / 1 (100%)	100%
CalibrationInjection	100%	12 / 12 (100%)	100%
top_test_injection_trig	100%	1 / 1 (100%)	100%
top_test_injection_hitor	100%	10 / 10 (100%)	100%
top_test_analog_injection_trig	100%	1 / 1 (100%)	100%
MonteCarlo	100%	8 / 8 (100%)	100%
PixelFormat_MC_AtlasBarrel0CenterFlat	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasBarrel0EndFlat	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasBarrel0InitInclined	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasBarrel2CenterFlat	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasBarrel2EndFlat	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasBarrel2InitInclined	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasDisks0	100%	1 / 1 (100%)	100%
PixelFormat_MC_AtlasDisks2	100%	1 / 1 (100%)	100%



## Issues with verification sub-tasks

Startup, Resets, Clocks verification 3 of 8 tasks completed

#95 · opened 6 months ago by Sara Marconi To Do Verification 0

Data merging verification 2 of 3 tasks completed

#93 · opened 6 months ago by Sara Marconi Doing Verification 0

Global configuration verification 5 of 10 tasks completed

#90 · opened 6 months ago by Sara Marconi Sep 30, 2019 Doing Verification 0

Command decoder verification 5 of 16 tasks completed

#89 · opened 6 months ago by Sara Marconi Doing Verification 0

Global pulse verification 2 of 4 tasks completed

#171 · opened 2 months ago by Sara Marconi To Do Verification 1

Verify all possible initialization states of ChannelSync

#154 · opened 3 months ago by Sara Marconi To Do Verification 1

ServiceData and Aurora verification 3 of 10 tasks completed

#92 · opened 6 months ago by Sara Marconi To Do Verification 1

Pixel configuration verification 6 of 13 tasks completed

#91 · opened 6 months ago by Sara Marconi Doing Verification 1

Digital Chip Bottom data flow verification 3 of 9 tasks completed

#87 · opened 6 months ago by Sara Marconi To Do Verification 1

PixelArrayReadout verification 8 of 12 tasks completed

#86 · opened 6 months ago by Sara Marconi To Do Verification 1

Verification of extreme cases 6 of 9 tasks completed

#85 · opened 6 months ago by Sara Marconi To Do Verification 1

Verify eFuses block

#191 · opened 1 month ago by Roberto Beccherle Sep 30, 2019 Simulation Verification 2

General Purpose IO verification

#173 · opened 2 months ago by Sara Marconi To Do Verification 2

### List of bugs open.

Clear command chipID ignored by command decoder

#205 · opened 1 week ago by Sara Marconi BUG Design Verification 0

Unexpected tag (249) readback in full chip top\_test\_analog\_injection\_trig

#195 · opened 3 weeks ago by Sara Marconi BUG Design Verification 0

Readback pixel configuration autorow , issue when switching to next col

#193 · opened 1 month ago by Sara Marconi BUG Design Verification 0

floating inputs

#196 · opened 3 weeks ago by Giuseppe De Robertis BUG

Aurora Output lane selection mismatch between LaneAlign and Aurora Block

#148 · opened 4 months ago by Timon Heim BUG RTL

updated 46 minutes ago

## Verification Status

Sara Marconi



# Conclusion

- Apart from small hiccups here and there command decoder reference model is complete.
- Invalid command decoder input tests have been written, still need to report small issues.
- ChipID tests have been written, issues have been found and reported.
- Trigger tests have been written and proper trigger tag verified.
- Need to write tests for read trigger, WrReg/RdReg interference, and Interleaving Commands w/ trigger, syncs, etc.
- Any other test that comes up between now and submission (and beyond?)