WG Wrap Up
RCE

Incomplete Participant List

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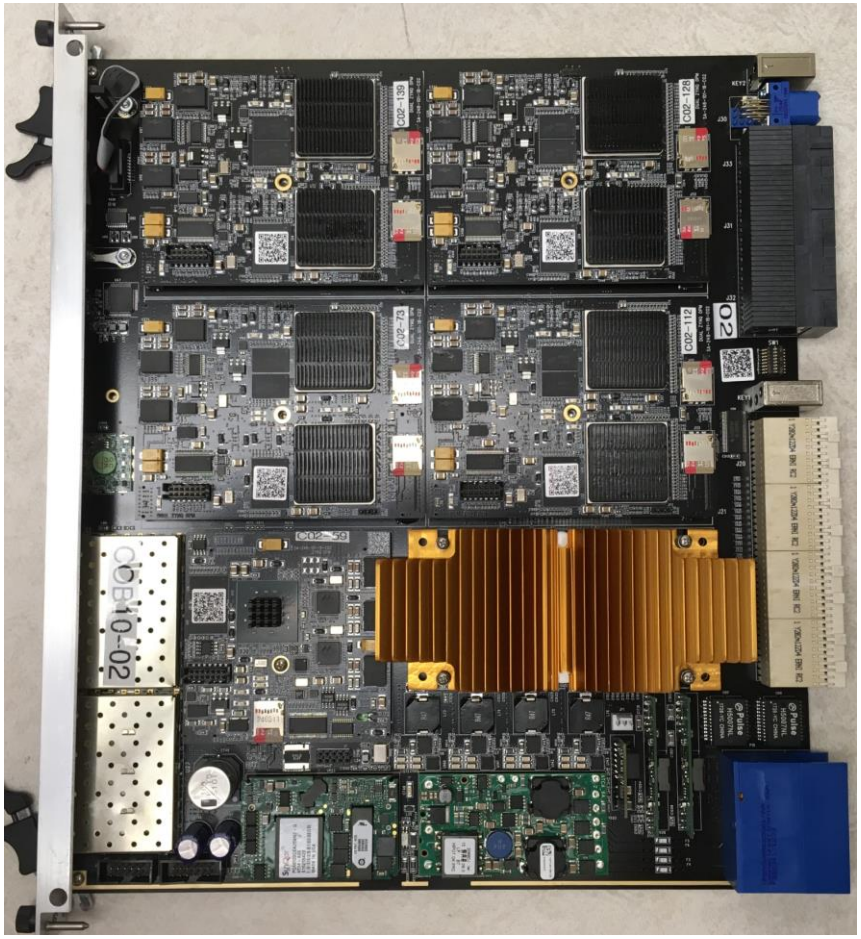
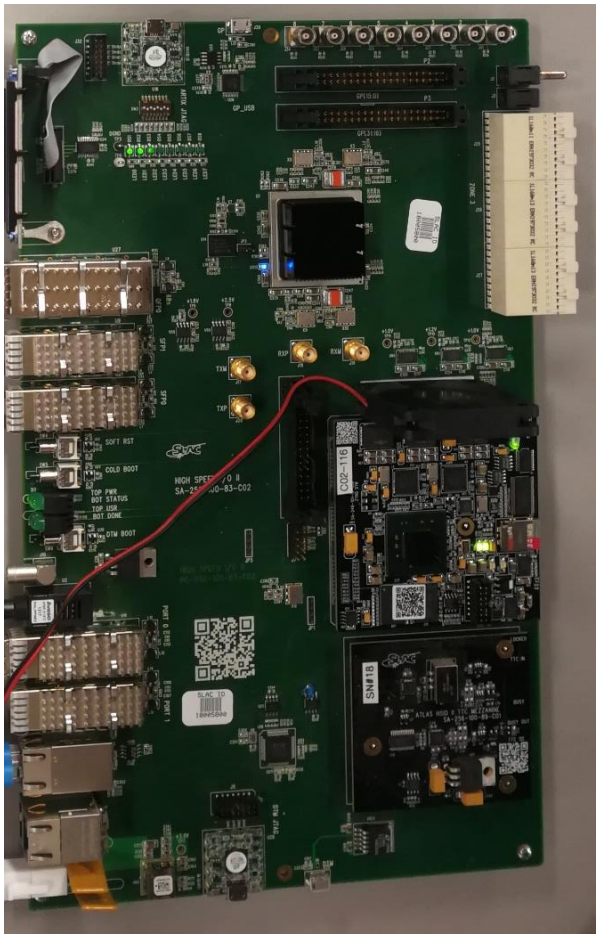
RCE (Reconfigurable Cluster Element)

SLAC

ATCA platform for detector running

HSIO platform for laboratory and testbeam



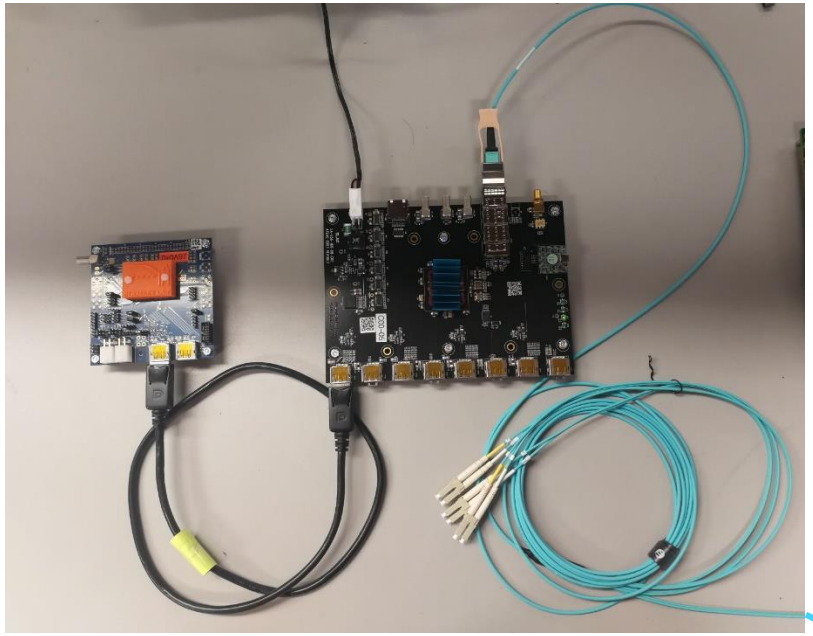


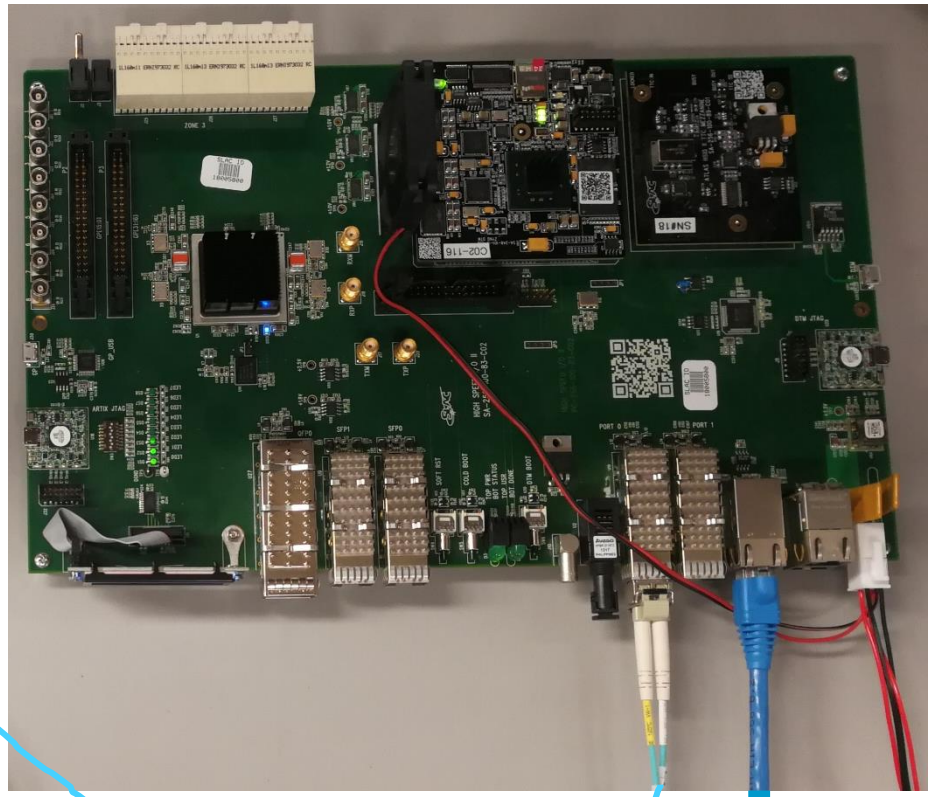
RCE for ITK

HSIO2/RCE

RD53A

FEB

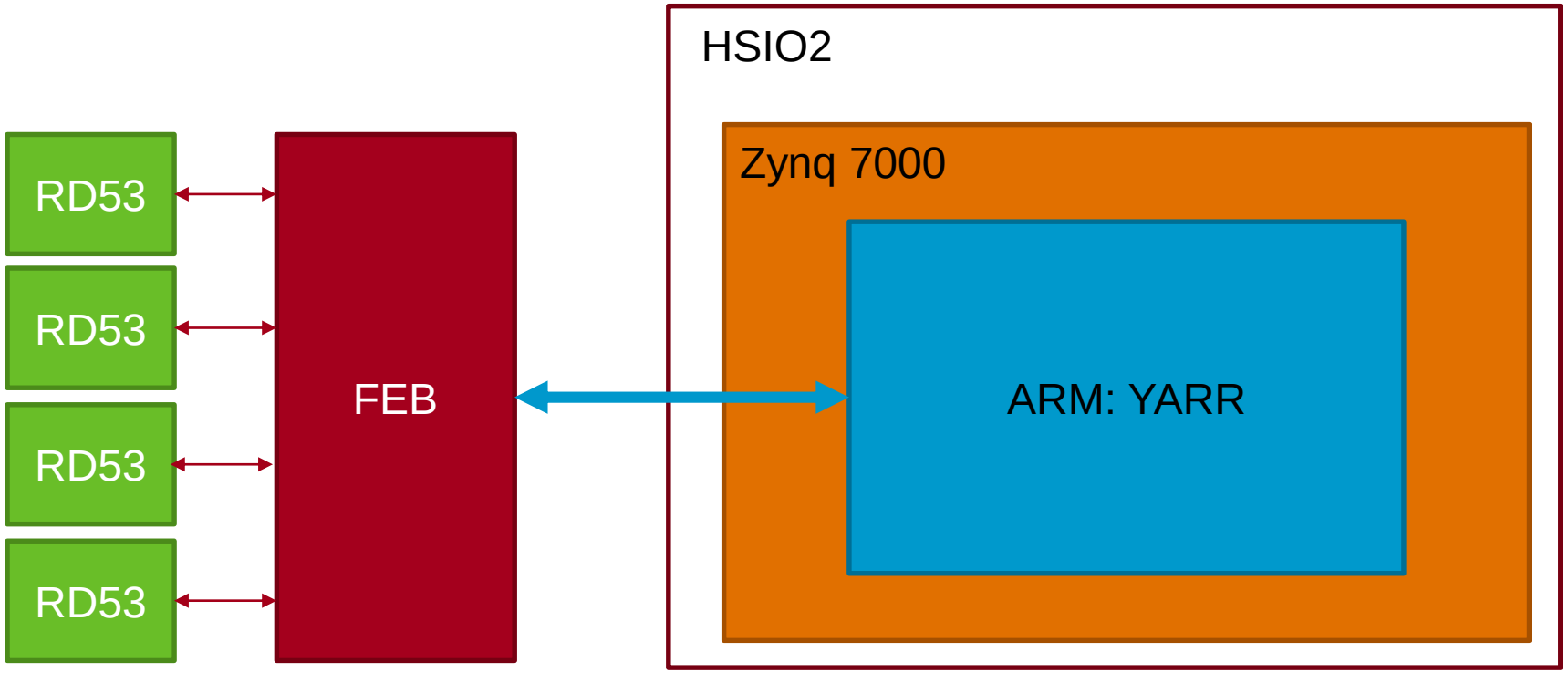




Ethernet

QSFP+ optical fiber cable

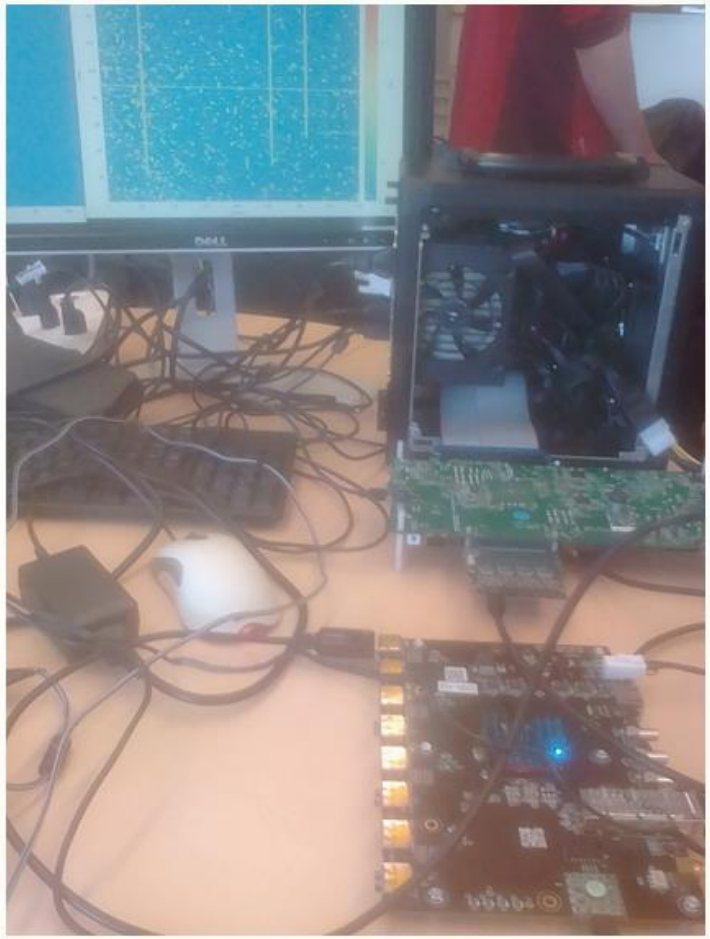
RCE for ITK



RD53 Emulator

Same FEB board is used as Emulator

- Emulator + YARR works fine
- Emulator + RCE still has issue, will continue to work on it



https://indico.physics.lbl.gov/indico/event/856/sessions/298/#20190529

System Test Readout Evolution

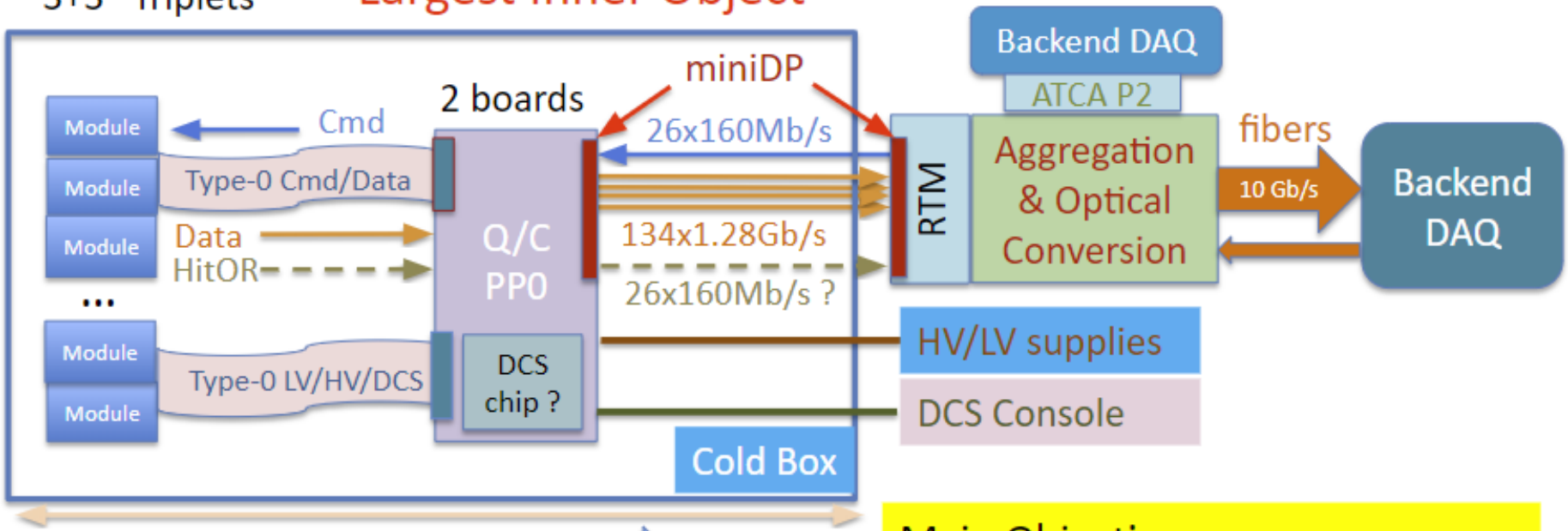
- Performant readout needed for Demonstrators/Prototype systems with ~100+ data links this year
- System tests much more valuable if data links can be driven at full speed of 1.28 Gb/s
- Will not have RD53B for some time. Have to do the best we can to drive RD53A with sub-optimal transmission control
- Compact/flexible solution needed with commercial or existing substitutes for electrical service and test readout, that can evolve, until production components are mature

Inner Coupled-Ring Disk Test Readout Model

SLAC

10+10 Quads
3+3 Triplets

Largest Inner Object



~1m

As realistic as possible on detector components

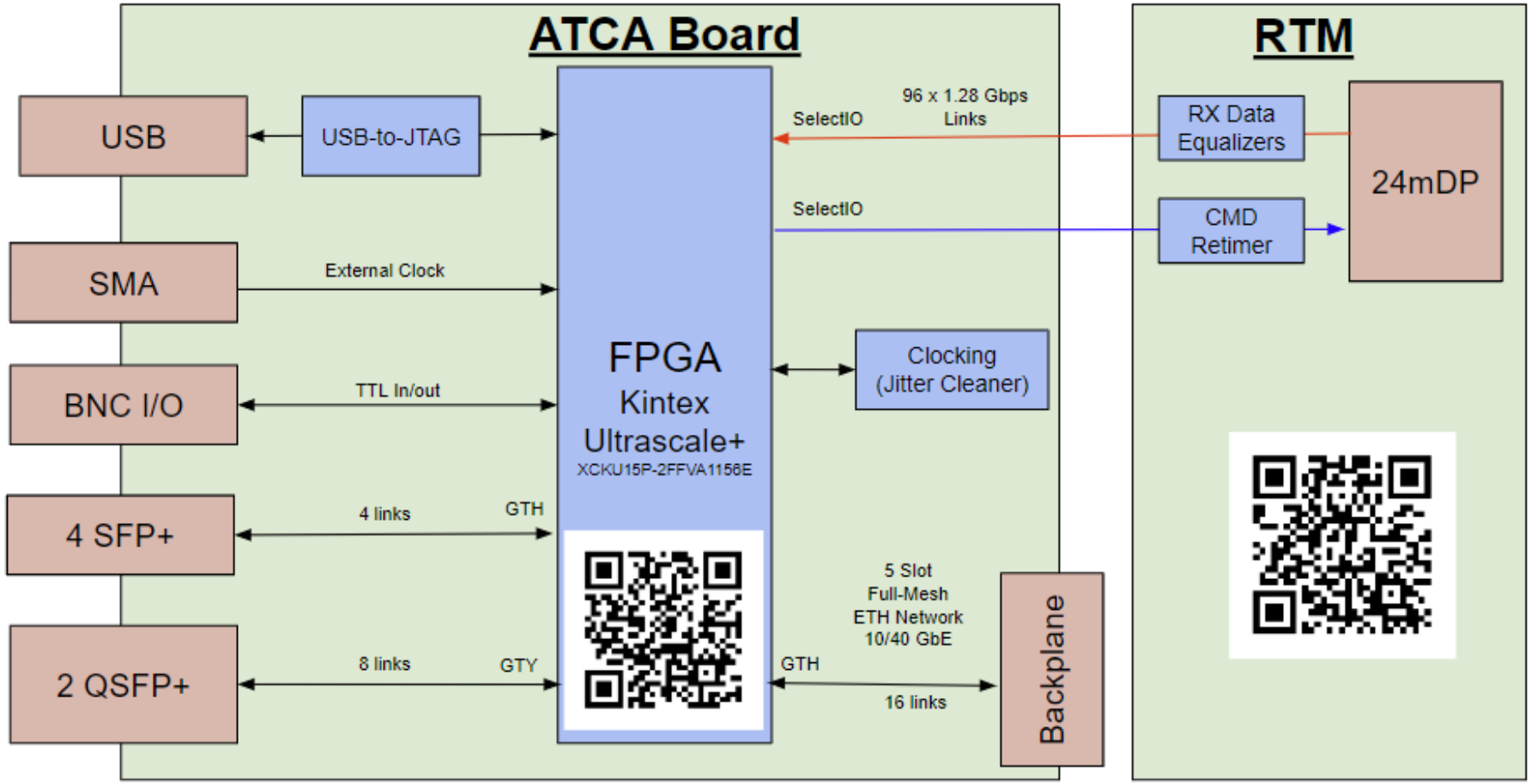
Commercial /existing substitutes whenever possible

Main Objective:
Tests of on detector components

- PP0-RTM: MiniDP cable/connection allow test DAQ connections
- Can substitute in real PP0/twinAx/OptoBoard when ready

https://confluence.slac.stanford.edu/display/AIRTRACK/ATLAS:+RD53

ATCA RD53 Link Aggregator Concept



https://docs.google.com/presentation/d/1RHsEeQzuOsGa87eaIiL5AMZswAfcKtoG_HHkYwLRNMo/edit#slide=id.g4ecf007e48_0_13

RCE for ITK

RD53A
- 4 lanes output
- 1.28Gbps

Xilinx Evaluation KCU105:
- FMC connect to HP bank, > 1.4Gbps

FMC adapter
- PLL, retimer, equalizer

RCE for ITK

4 x RD53A

https://github.com/slaclab/

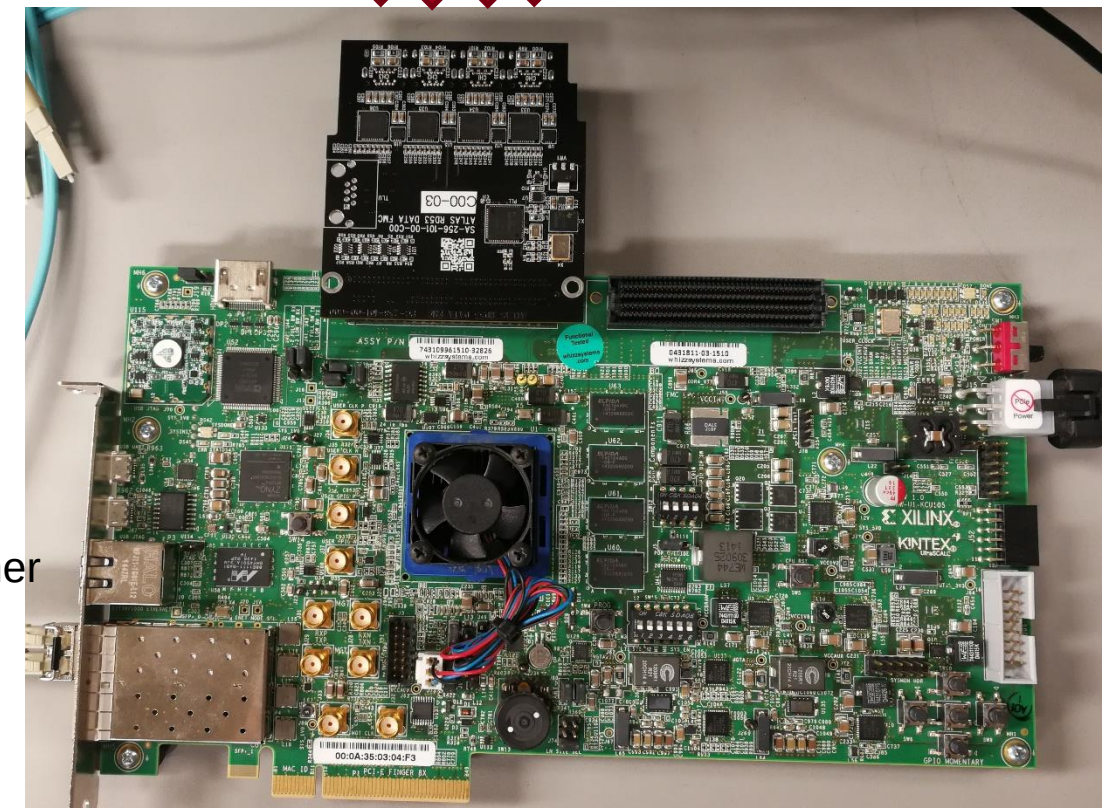
SLAC firmware/software lib to support

PC:

- SFF+ for 10G Ether
- 1G Ether
- PCIe

RCE:

- SFP+ for pgp3



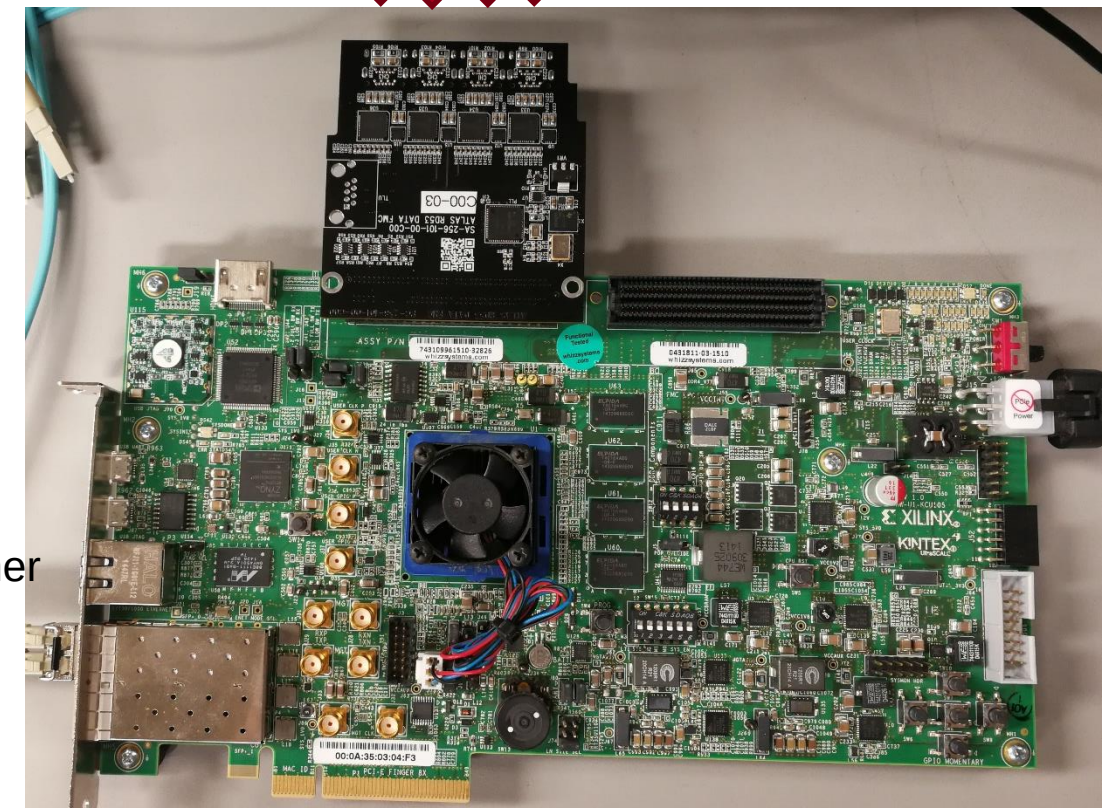
RCE for ITK

4 x RD53A

*revision in fabrication because of wrong pin mapping

A patched card is in tested

- 4 lane output could stabilized at 1.28Gbps
- seems like CMD line have some glitch



Backup

ATCA RD53 Link Aggregator Layout