Measurement of Single Event Upset rates in single pixels of ATLAS IBL

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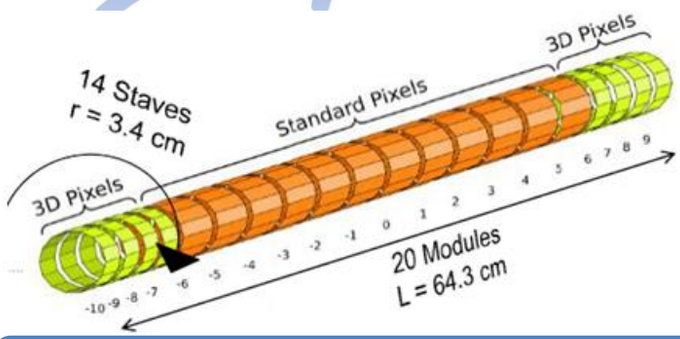


IBL

The Insertable B Layer (IBL) is a cylindrical silicon pixel detector that consists of 14 staves placed around the beam pipe. Each stave consists of 12 planar modules and 8 3D modules.

FE-I4B chip - 80×336 pixels
- pixel size: 250×50 μm^2

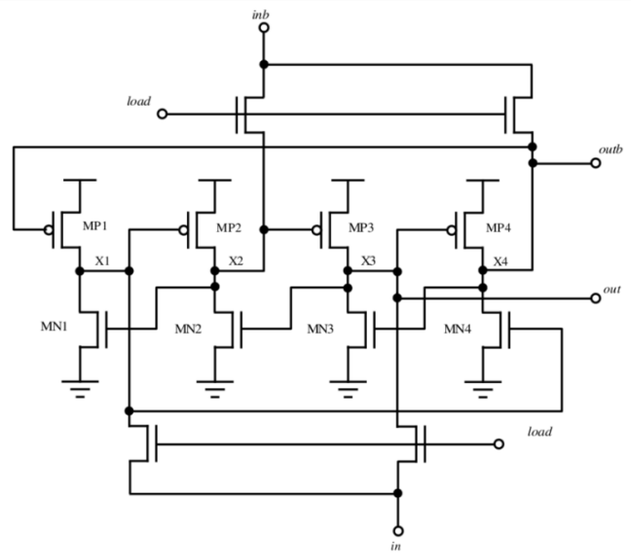
1. Introduction

a) Single Event Upset

- A flip-flop or latch is a circuit having two stable states
  To store state information
- **Single Event Upset (SEU): change of state caused by ionizing radiation**

b) Efforts to increase SEU tolerance of FE-I4

- Dual Interlocked CEll (**DICE**) latches based memories
  - **Redundant storage nodes** making SEU less likely (by ~1 order of magnitude from test beam studies)
  - **Reduction of charge sharing between critical nodes**
- DICE latch is upset if 2 nodes storing the same logic state (X1-X3) or (X2-X4) change the state due to the single particle impact effects
- **Single** DICE latches for memories of each **pixel** configuration
- **Triplet** DICE latches for memories of global chip configuration



- Cross coupled inverter latch structure

  Assume **X1 flipped from 0 to 1**

  → **MP2 and MN3 are blocked**

  → **X2 and X3 have conserved the true information**

2. SEU cross section

a) SEU cross section $\sigma = \frac{N_{\text{errors}}}{\Phi \cdot N_{\text{latches}}}$

- N_{errors}: the total number of errors obtained for the whole memory
- Φ: the total fluence achieved during the test
- N_{latches}: the number of the latches memories in the chip

Determined by beam testing in 2012: $1.1 \cdot 10^{-15}\text{cm}^2$, by disabling the enable bit of each pixel before the test beam [1]

b) Quiet-pixels-fraction

Quiet pixels : never fired in 20 pb^{-1} data (prob = 1.1×10^{-20} for normal pixels)

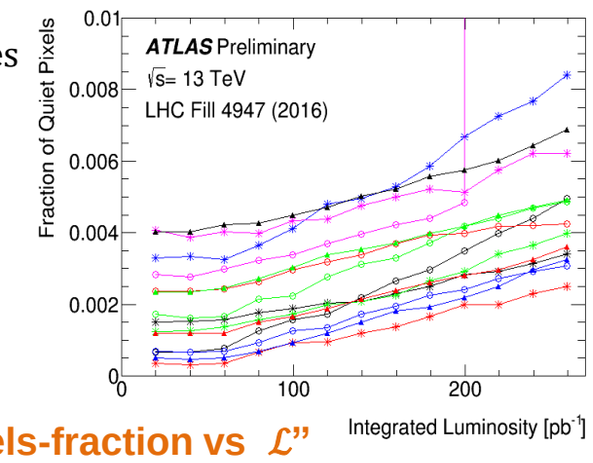
* *Average occupancy of one pixel~46 in one of the most forward 3D module in 20 pb^{-1} data*

* *Only clusters the length of which along beam direction is 1 are used due to the lack of the pixels information of other clusters*

Caused by SEU effects with flipping the pixel enable bit from 1 to 0

Similar behavior of the 14 3D modules in the most forward IBL ring

- **More pixels go to quiet** along the data taking due to the **accumulation of ionizing radiation**
- **Dead pixels in some modules**



c) Extraction of σ from "quiet-pixels-fraction vs $\mathcal{L}$"

Quiet-pixels-fraction which increases with $\mathcal{L}$: $p_0 + p_1 \cdot \mathcal{L}$ is actually $\frac{N_{\text{errors}}}{N_{\text{latches}}}$

→ $\sigma = \frac{p_1 \cdot \mathcal{L}}{\Phi}$ (Ideally $p_0 = 0$)

- p_1: $1\sim2 \cdot 10^{-5}$, 1 pb^{-1} data corresponds to a fluence of $\frac{5}{3} \cdot 10^{10} n_{eq}\text{cm}^{-2}$

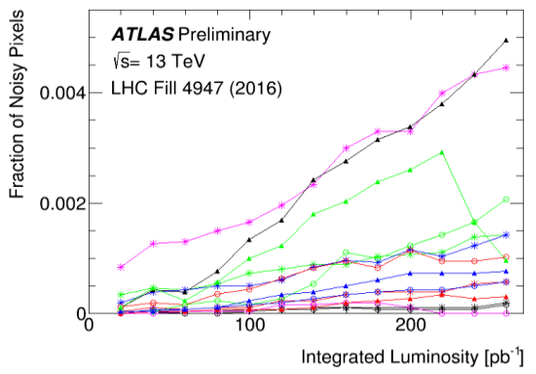
- **The SEU cross section is calculated to be $0.6\sim1.2 \cdot 10^{-15}\text{cm}^2$**
- This is at the same order of magnitude with the beam testing result

3. Noisy pixels by SEU

a) Noisy-pixels fraction

Noisy pixel: fired >300 times in 20pb^{-1} data (prob.= 2.3×10^{-136} for normal pixels)

Different behavior of the 14 3D modules in the most forward IBL ring



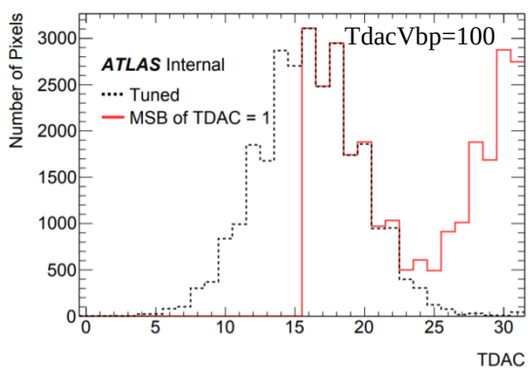
b) Production of noisy pixels are due to the threshold decrease caused by the bit flip of TDAC

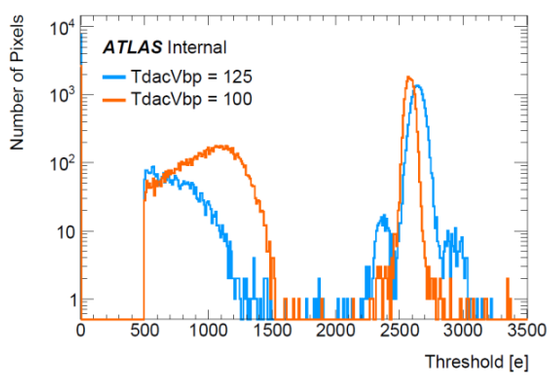
- **Threshold in each pixel** is determined by
  f (VthinAlt_Coarse) + f (VthinAlt_Fine) + f(TDAC*TdacVbp)

two 8-bit global register for adjustment of global threshold	in-pixel threshold tuning 5-bit DAC	8-bit global register sets the step size of TDAC

- Global registers are not easily flipped due to triple redundancy latches

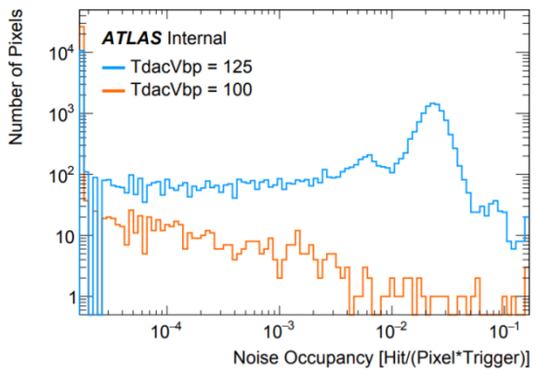
MSB of TDAC is flipped from 0 to 1 → **Lower threshold**





- The truncation at $500e$ is due to the lower limit of charge injection.
- The bias voltage of TdacVbp can be changed

- **Smaller TdacVbp value is better**
  - **but some pixels cannot be tuned**



4. Summary

- **The SEU cross section is estimated with "quiet-pixels-fraction vs $\mathcal{L}$"**
  - **The determined cross section of SEU (1→0) is at the same order of magnitude with the beam testing result**
  - **0→1 transition has been studied in LHC Fill 6356 by disabling the enable bit of each pixel at the beginning of this fill [2]**
- **The noisy pixels are due to the threshold decrease caused by the bit flip of TDAC.**

  Modules behave differently due to different values of TdacVbp. **Smaller TdacVbp value decreases the fraction of noisy pixels.**

[1] M. Menouni et al., SEU tolerant memory design for the ATLAS pixel readout chip, 2013 JINST 8 C02026.

[2] Pierfrancesco Butti, https://indico.cern.ch/event/695271/contributions/2956065/attachments/1637565/2614124/SEU_RadWorkshop.pdf