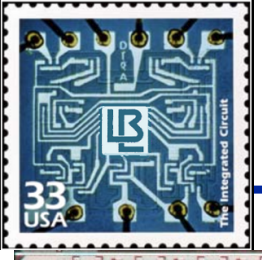

Integrated Circuits

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Lawrence Berkeley National Lab

Physics 290E
Jan. 31, 2018

Introduction

GOAL: Encourage you to learn more about integrated circuits
Exposure to some concepts and words
you'll hear IC designers speak.

- Where are integrated circuits used? ASICs
- History and HEP history
- Special place of Berkeley
- How are ICs made?
- How are ICs designed
- Special needs of physics experiments
- Lithographic fabrication beyond IC's enables many experiments

- ASIC = Application Specific Integrated Circuit

Introduction

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- ASIC = Application Specific Integrated Circuit

List of ASICs in ATLAS

Tracking detectors	ASIC	Technology	Functionality	Quantity & remarks
Pixel	FEI3	0.25 µ CMOS	Front-end	~28000
	Module Controller	0.25 µ CMOS	Control	~1800
	VDC	0.25 µ CMOS	VCSEL driver	~500
	DORIC	0.25 µ CMOS	Timing and control receiver	~400
Silicon Strips	ABCD	DMILL	Front-end	~50000 BiCMOS design
	DORIC	0.35µ BiCMOS	Timing and control	~4100
	VDC	0.35µ BiCMOS	VCSEL driver	~8200
TRT	ASDBLR	DMILL	Amplifier-shaper-discriminator	~38000 Bipolar design
	DTMROC	0.25 µ CMOS	Digitiser	~19000

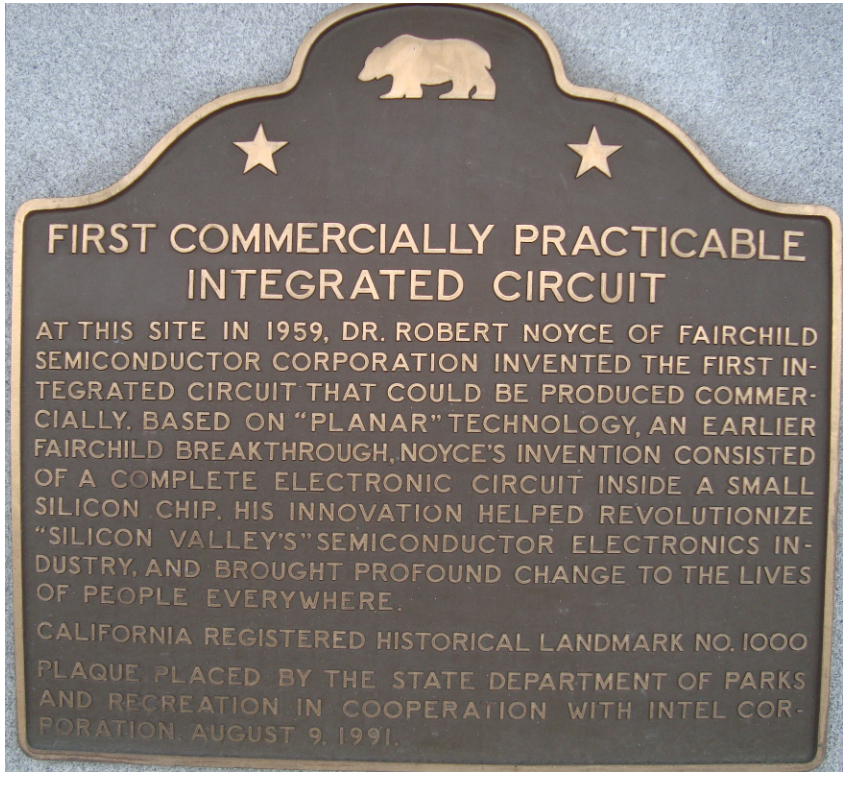
Muon	ASIC	Technology	Functionality	Quantity & remarks
MDT	ASD	0.5 µ CMOS	Amplifier-shaper	~5000
	AMT	0.3 µ CMOS	Time to digital conv.	~15000
CSC				
CSC	ASM1	0.5 µ CMOS	Preamplifier	~1300
	ASM2	0.5 µ CMOS	Multiplexor	~1300
	Clock driver	0.5 µ CMOS	Clock driver	~200
	HAMAC-SCA	DMILL	Analogue memory	~2600 Common with LAr
RPC				
RPC	ASD	GaAs	Amplifier-shaper	~47000
	CMA	0.18 µ CMOS	Coincidence matrix	~3300

Calorimeters	ASIC	Technology	Functionality	Quantity & remarks
LAr Calorimeter	HAMAC-SCA	DMILL	Analogue memory	~52000
	BiMUX	DMILL	Multiplexor	~8000 Bipolar design
	OpAmp	DMILL	Operational amplifier	~17000 Bipolar design
	DAC	DMILL	16-bit DAC	~130
	SPAC slave	DMILL	Control interface	~2000
	Configuration	DMILL	Control	~1600
	SMUX	DMILL	Digital multiplexer	~1600
	Calibration logic	DMILL	Glue logic	~800
	SCA controller	0.25 µ CMOS	Control	~3200
	Gain selector	0.25 µ CMOS	Control	~13000
	Clock fan-out	0.25 µ CMOS	Clock driver	~11000
	DCU	0.25 µ CMOS	Control	~3200 CMS design
	HEC	GaAs	Front-end amplifier	~700 Inside liquid argon
Tile Calorimeter	TileDMU	0.35 µ CMOS	Pipeline	~256 Gate Array

TGC				
TGC	ASD	Bipolar	Amplifier-shaper	~81000
	HpT	0.35 µ CMOS	Trigger	~800
	PP	0.35 µ CMOS	Trigger	~15000
	SLB	0.35 µ CMOS	Trigger	~3000
	JRC	0.35 µ CMOS	JTAG controller	~1400

History


Berkeley
San Francisco
580
680
880
580
Daly City
101
82
Pleasanton
San Mateo
680
84
1
101
92
844 East Charleston Road
Mountain View
880
280
San Jose


FIRST COMMERCIALLY PRACTICABLE INTEGRATED CIRCUIT
AT THIS SITE IN 1959, DR. ROBERT NOYCE OF FAIRCHILD SEMICONDUCTOR CORPORATION INVENTED THE FIRST INTEGRATED CIRCUIT THAT COULD BE PRODUCED COMMERCIALLY. BASED ON "PLANAR" TECHNOLOGY, AN EARLIER FAIRCHILD BREAKTHROUGH, NOYCE'S INVENTION CONSISTED OF A COMPLETE ELECTRONIC CIRCUIT INSIDE A SMALL SILICON CHIP. HIS INNOVATION HELPED REVOLUTIONIZE "SILICON VALLEY'S" SEMICONDUCTOR ELECTRONICS INDUSTRY, AND BROUGHT PROFOUND CHANGE TO THE LIVES OF PEOPLE EVERYWHERE.
CALIFORNIA REGISTERED HISTORICAL LANDMARK NO. 1000
PLAQUE PLACED BY THE STATE DEPARTMENT OF PARKS AND RECREATION IN COOPERATION WITH INTEL CORPORATION, AUGUST 9, 1991.

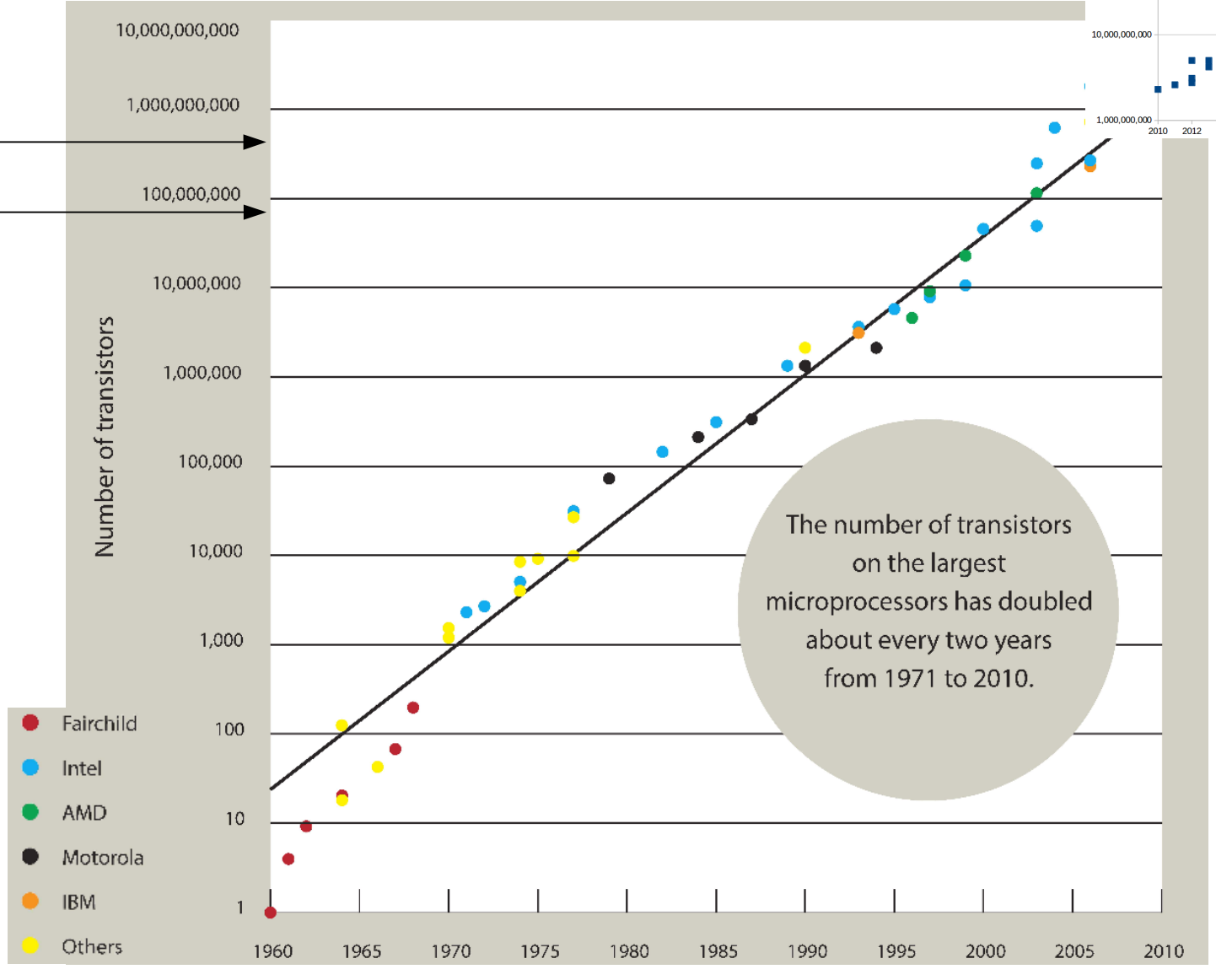
What else happened in 1959?

- Here: Segre, Chamberlain get Nobel prize to antiproton discovery
- There: The CERN PS produced first beam (28 GeV)

Obligatory Mention of Moore's Law

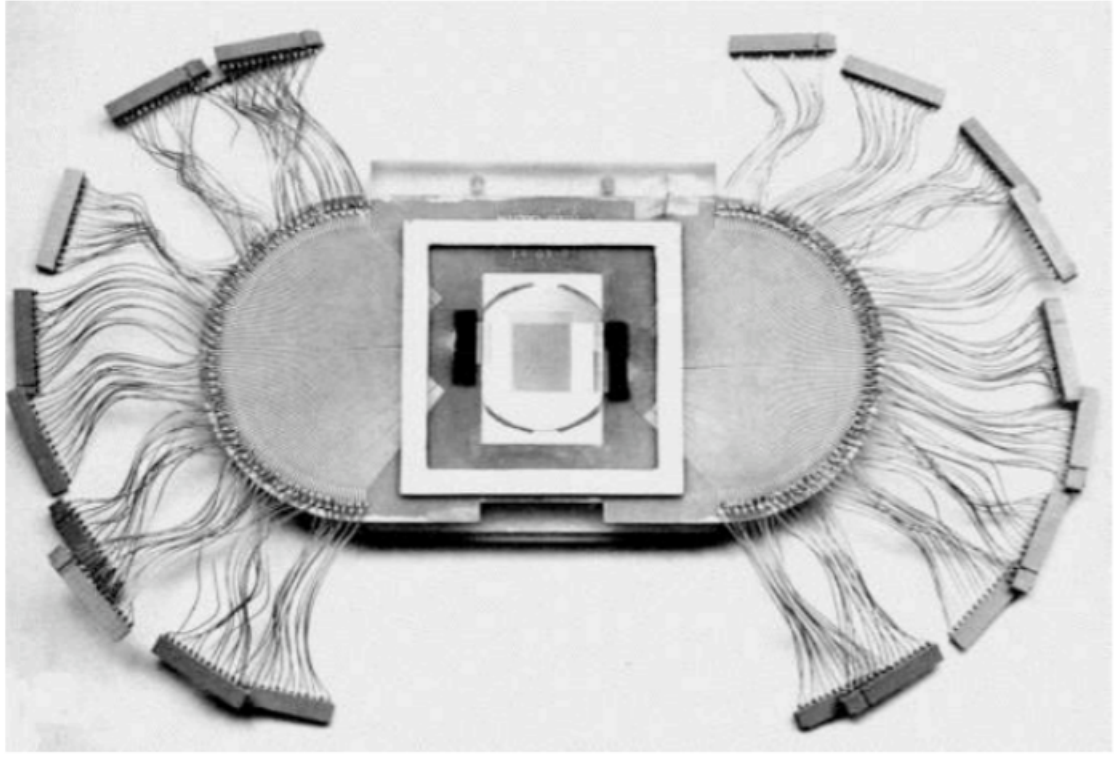
RD53A

FE-I4



HEP need for ASICs

NA11, CERN 1981. Silicon strip sensor with discrete readout

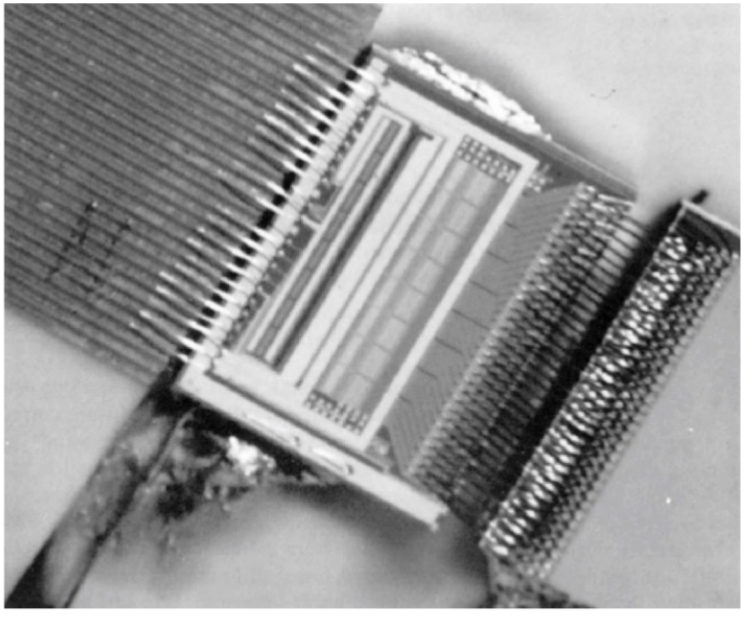


NIM205 (1983) 99

=> Special connection between silicon detectors and ASICs

HEP IC beginnings -pre CMOS

- Stanford / SLAC's NMOS Microplex (left) and Microstore (right)
- Walker, Parker, Hyams, Shapiro, "Development of High Density Readout for Silicon Strip Detectors," NIM 226 (1984).
- Walker, Chae, Shapiro, Larsen, "Microstore – the Stanford Analog Memory Unit," IEEE TNS NS-32, No 1. Feb. 1985



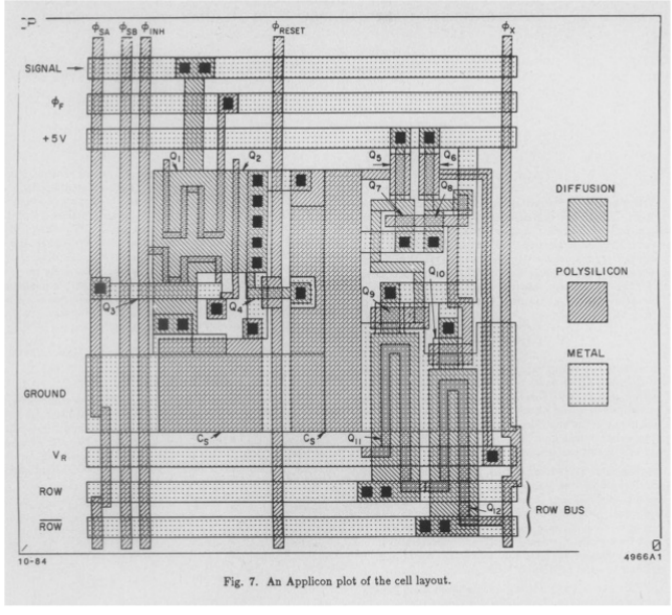
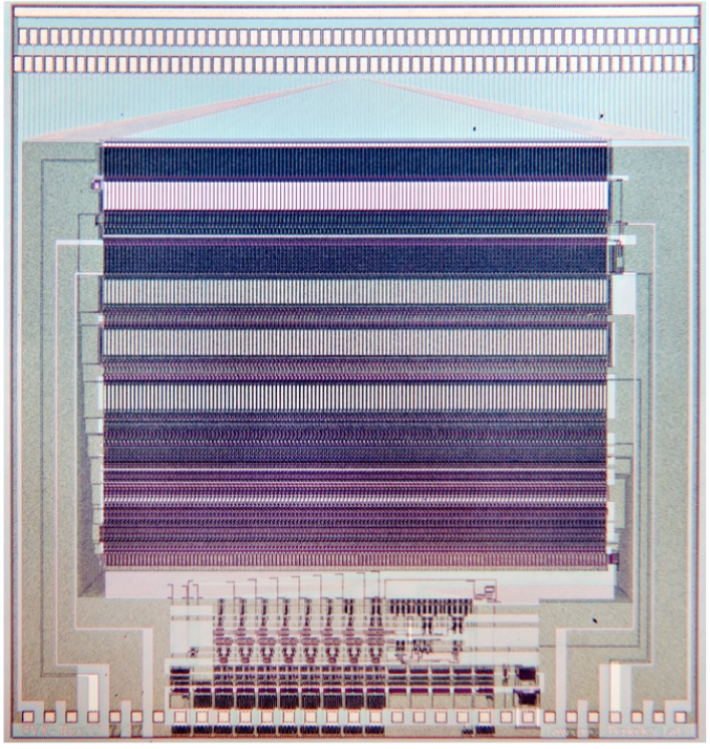


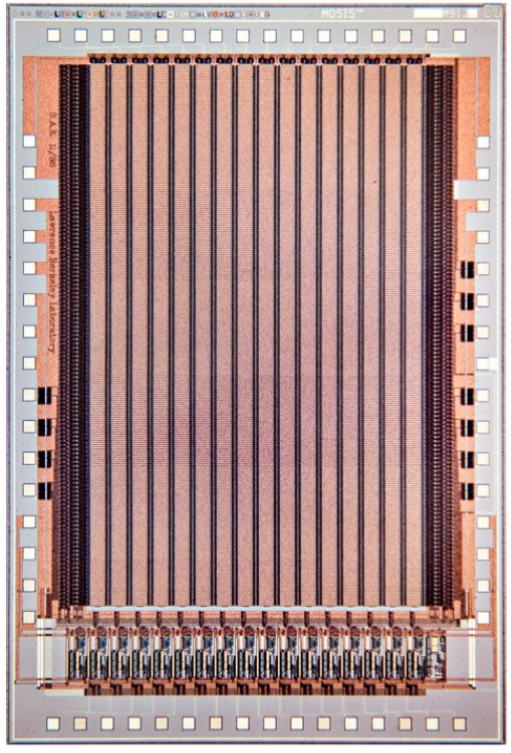
Fig. 7. An Applicon plot of the cell layout.

Sherwood's IEEE outstanding achievement award in 2015

HEP CMOS beginning

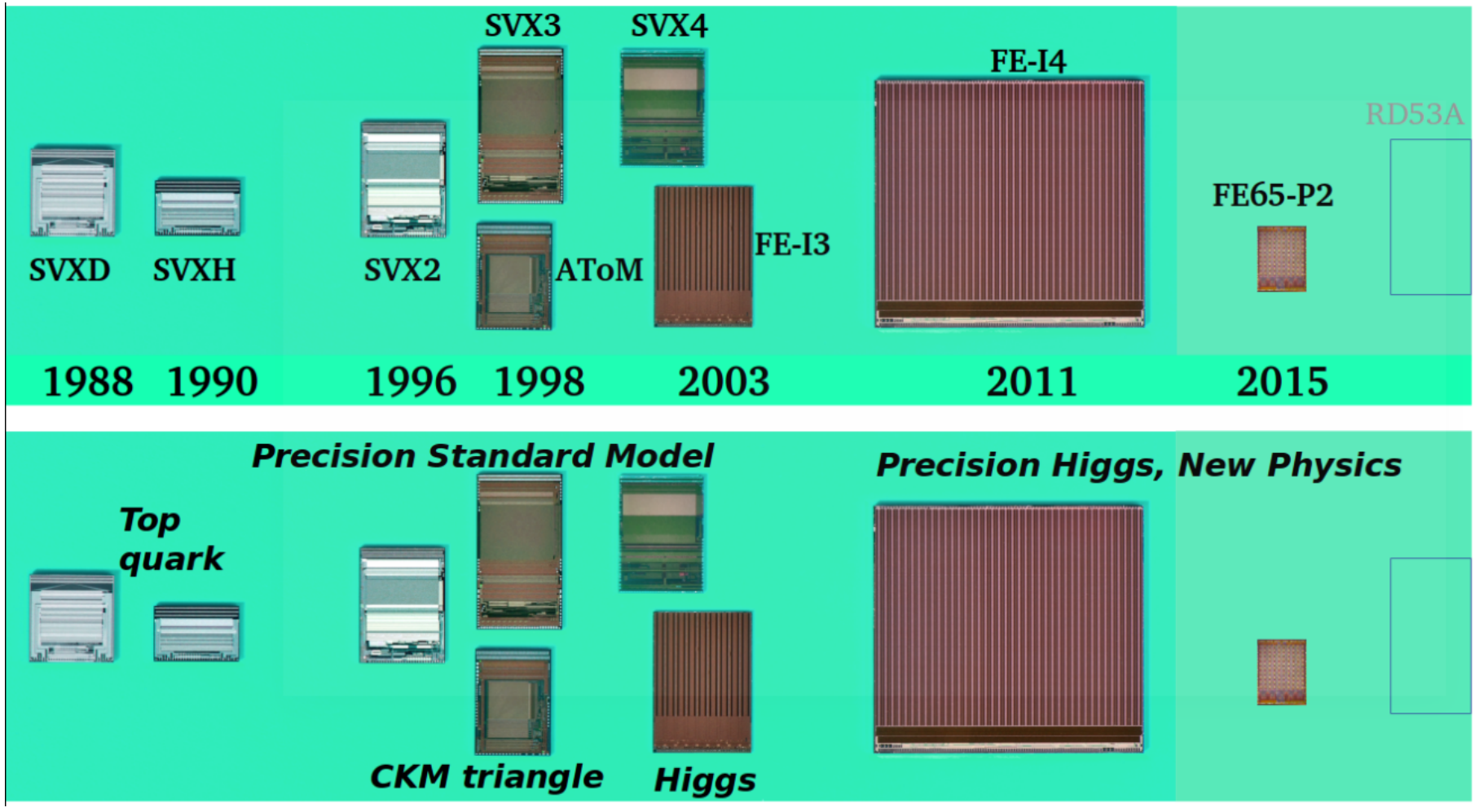
- The SVX chip was likely the first CMOS ASIC for physics. It offered improved amplification, auto-zeroed offset and leakage, sparse data scanning + nearest-neighbor logic, etc. (Kleinfelder, 1988).
- The SCA Switched Capacitor Array introduced a DRAM-like architecture for high density and low power, with rail-to-rail operation (Kleinfelder, 1988).





Stuart holding microplex wafers at HEPIC 2017

Silicon detector chips at LBL



Special Place of Berkeley

A few snippets

The 1970s-pioneered contributions to computer-aided design for microelectronics, the best-known being the SPICE program, were led by Professors D. O. Pederson, E. S. Kuh, and R. A. Rohrer. Industry-leading firms, including Cadence and Synopsys, were founded by graduates to commercialize design tools for microelectronics. A Berkeley team led by Profs. R. W. Brodersen, P. R. Gray, and D. A. Hodges invented mixed-signal MOS integrated circuits, combining precision analog-digital conversion and switched-C filters with high-density digital circuits.

2012

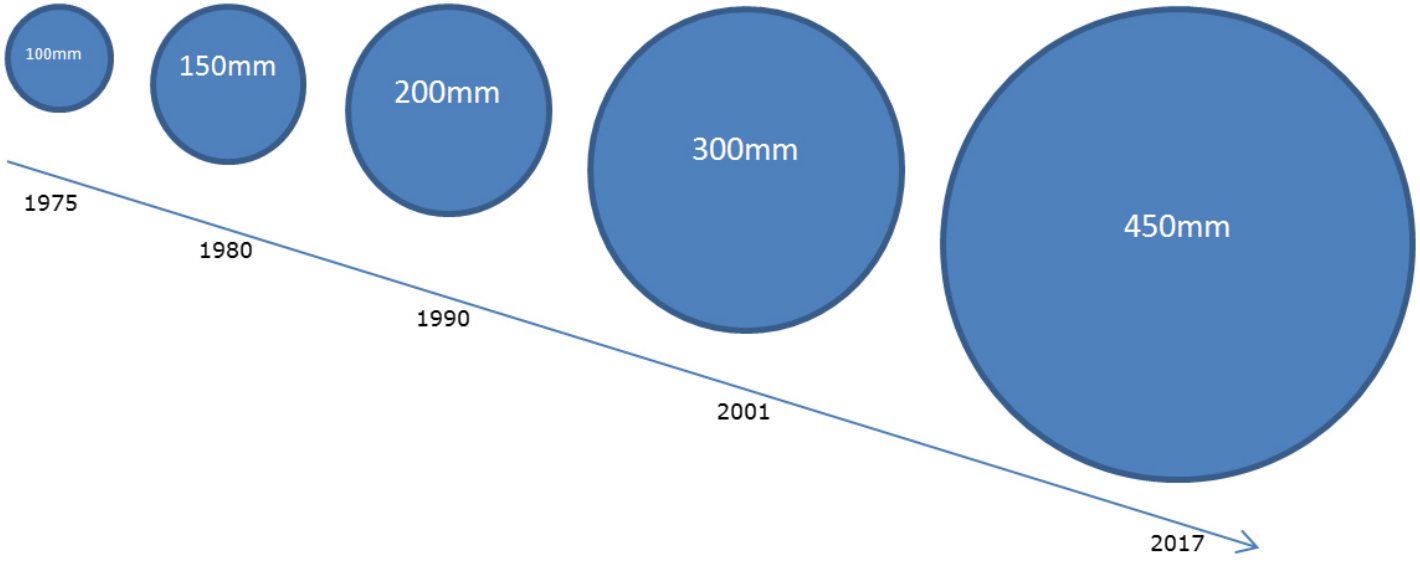
Dr. Chenming Hu has been called the Father of 3D Transistor for developing the FinFET in 1999.
(Steve Holland's thesis advisor)

Steve Holland developed fully depleted CCD's in the 90's. following a suggestion from Dave Nygren
This used the Microsystems Lab in bldg. 70A, which is an on-site IC fab.

In the late 80's Dave Nygren initiated research aimed at developing "smart-pixel arrays" for SSC. This work led to the ATLAS pixel readout system based on the column drain architecture

How are IC's made?

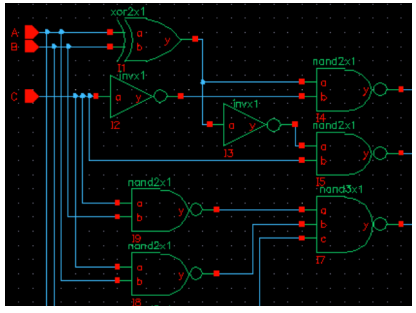
- https://www.youtube.com/watch?v=JDROPMoNZpk
- https://www.youtube.com/watch?v=3m4WmYObxzY
-

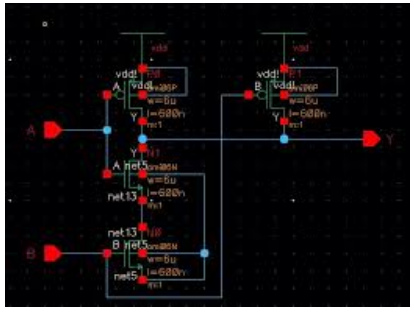


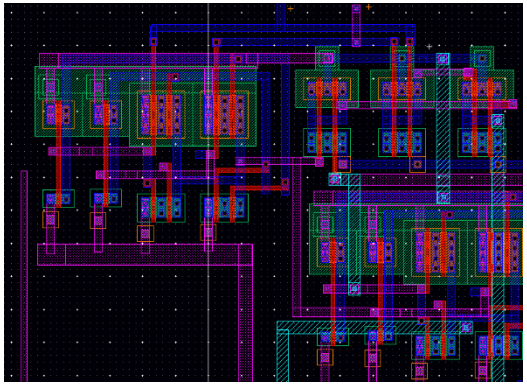
How are IC' are designed?

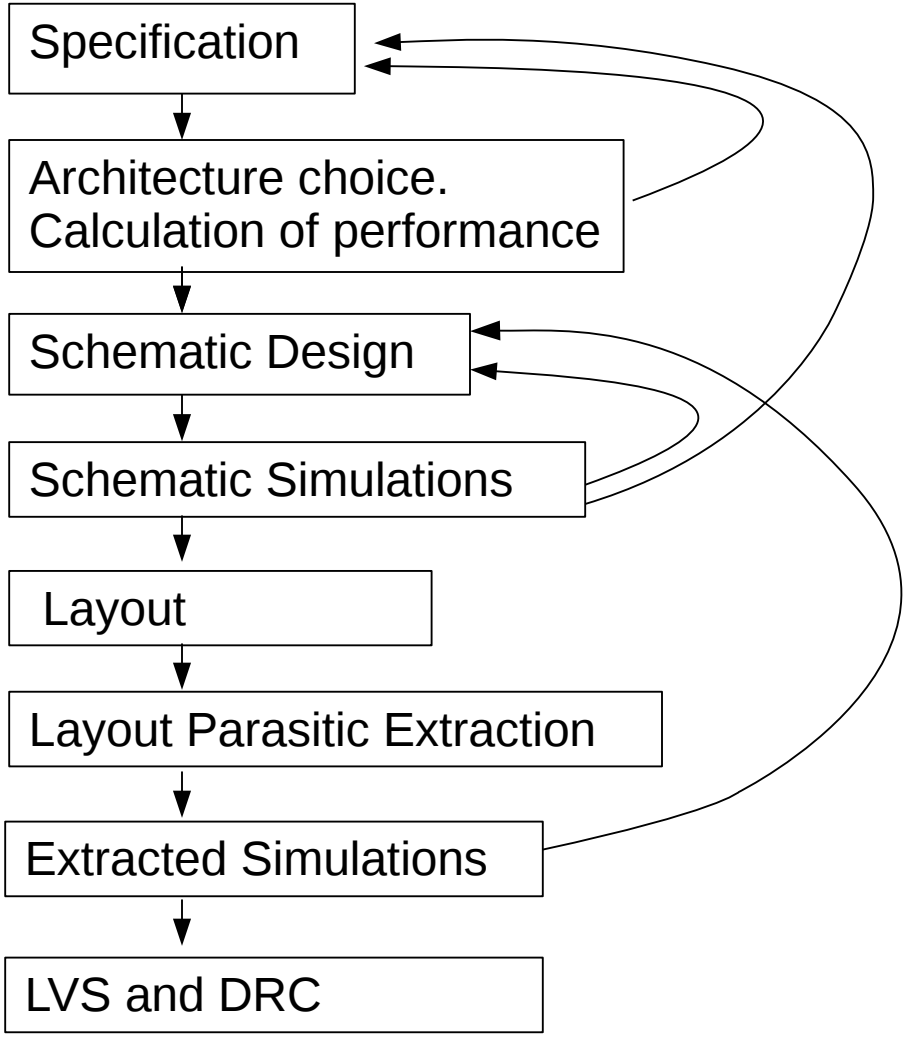
Flow, Methodology.

Full Custom Flow









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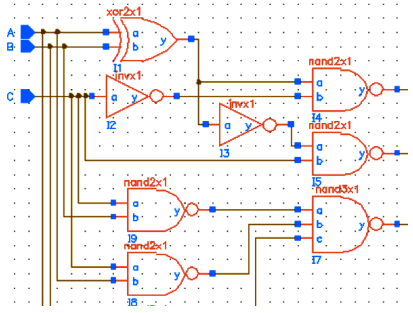
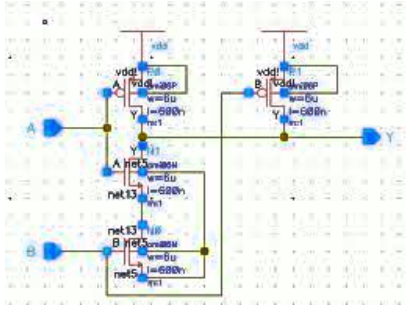
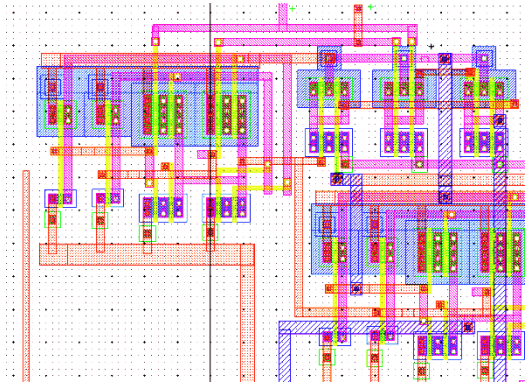
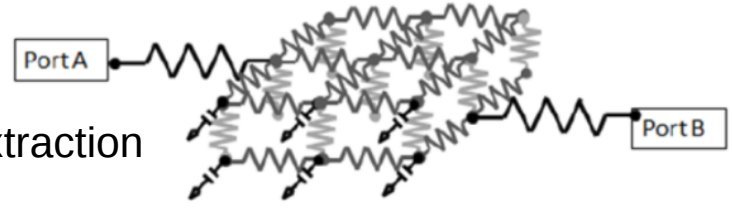






- Specification
- Architecture choice. Calculation of performance
- Schematic Design
- Schematic Simulations
- Layout
- Layout Parasitic Extraction
- Extracted Simulations
- LVS and DRC



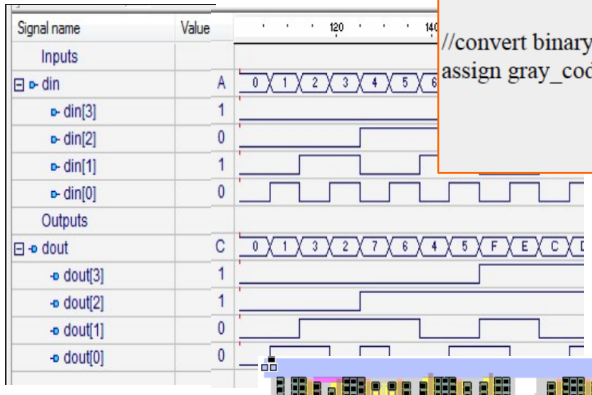
Parasitic extraction

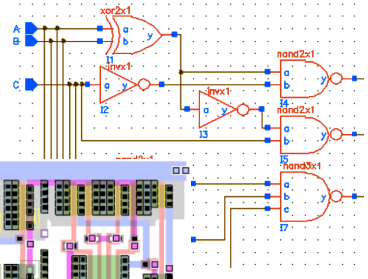
How are IC' are designed?

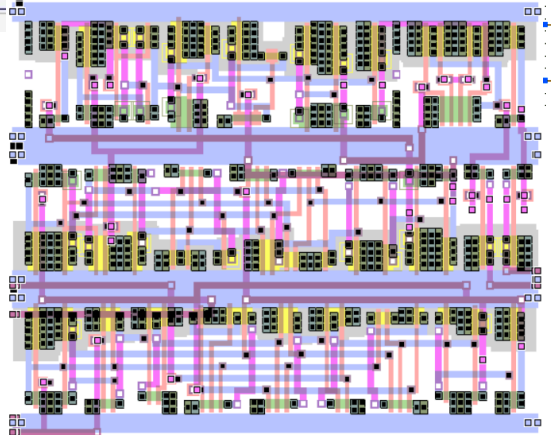
Flow, Methodology.

Digital Flow

```
always @(posedge clk or negedge rst)
  if (!rst)
    bcd_counter <= #1 4'b0000;
  else
    bcd_counter <= #1 bcd_counter + 1; // binary counter
end

//convert binary to gray code
assign gray_code = { bcd_counter[3] ,
                     bcd_counter[3] ^ bcd_counter[2],
                     bcd_counter[2] ^ bcd_counter[1],
                     bcd_counter[1] ^ bcd_counter[0]}
```



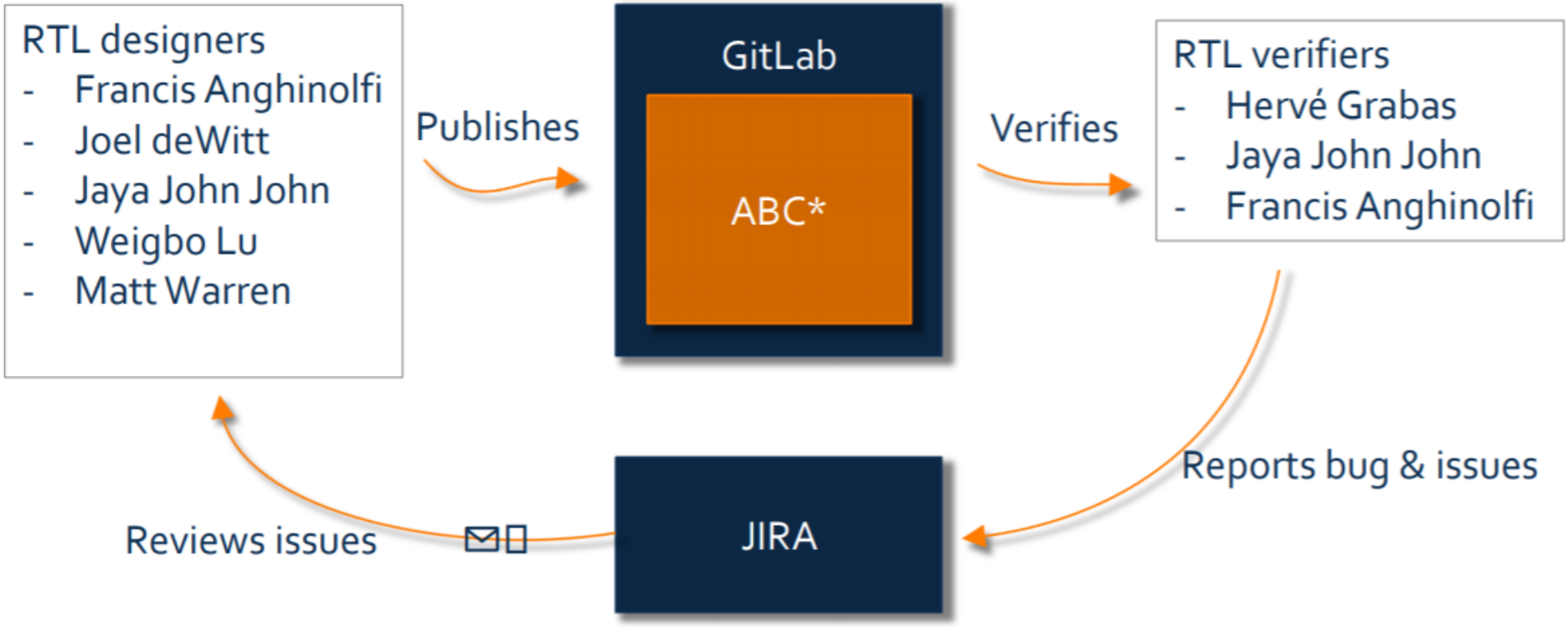




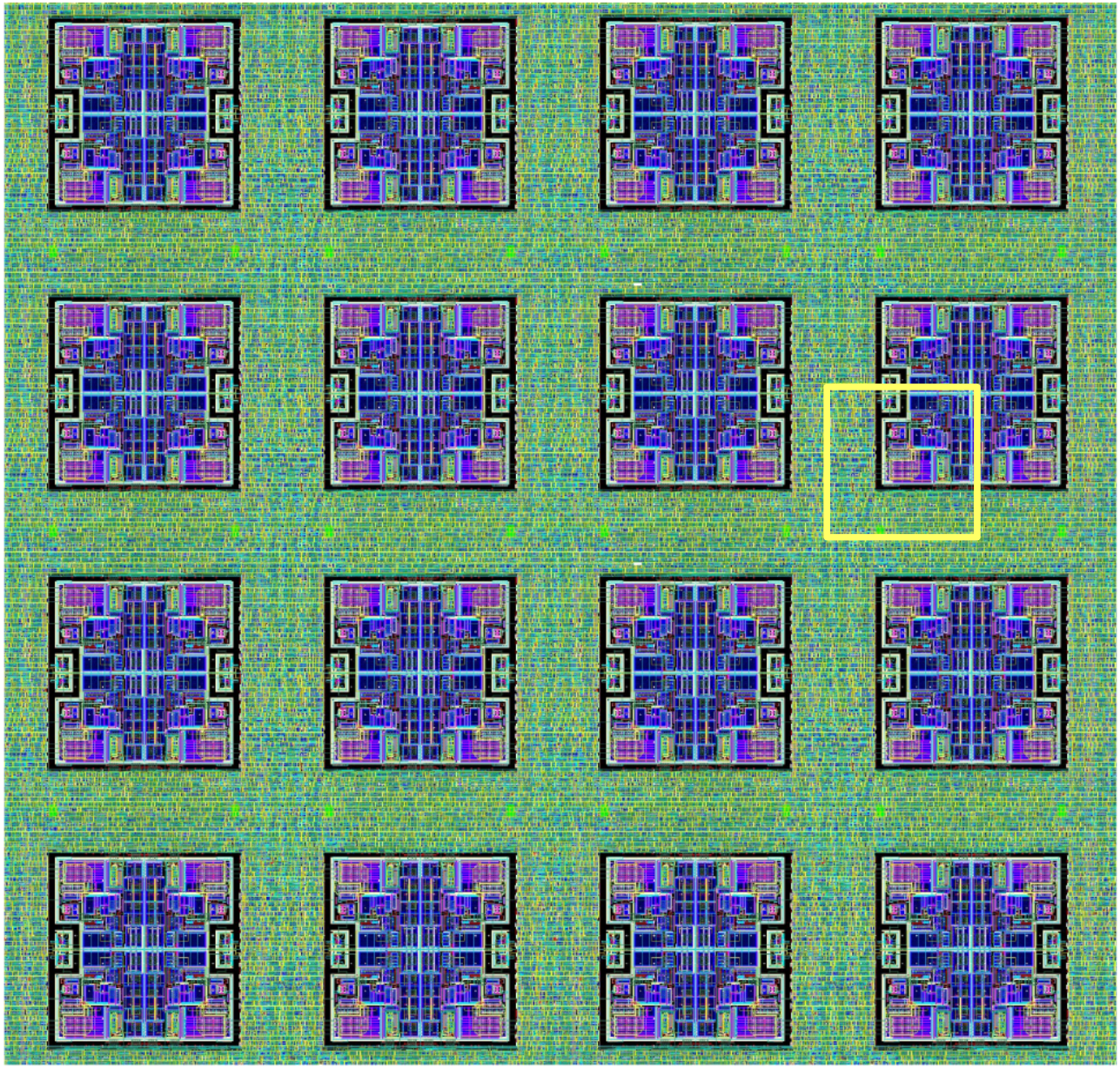
- Specification
- Write RTL code
- Simulation
- Synthesize schematic
- Auto place and route
- Layout Extraction
- Timing back-annotated Simulations
- LVS and DRC

RTL = Register Transfer Level. Written in a high level description language VHDL, Verilog.

ATLAS ABC* example



One RD53A Chip Core



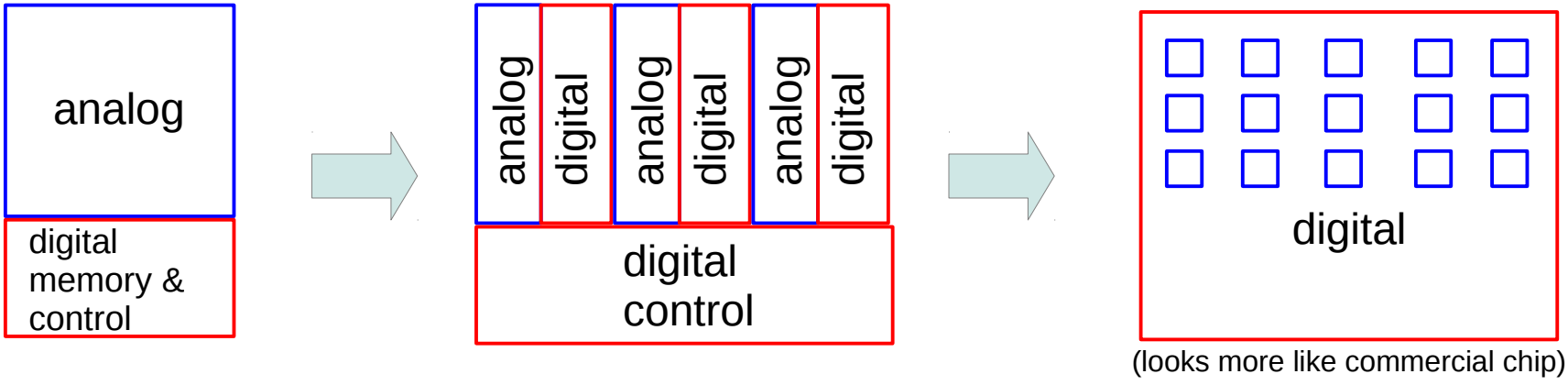
One flat synthesized circuit
Each pixel is different !

Whole block is stepped and repeated

~ 200k transistors
Size chosen so it CAN be SPICE simulated

(routing dominated re: metal stack)

HEP Chip Evolution



16 yrs ago
Full custom
including logic

8 yrs ago
Full custom layout
With synthesized logic inserts

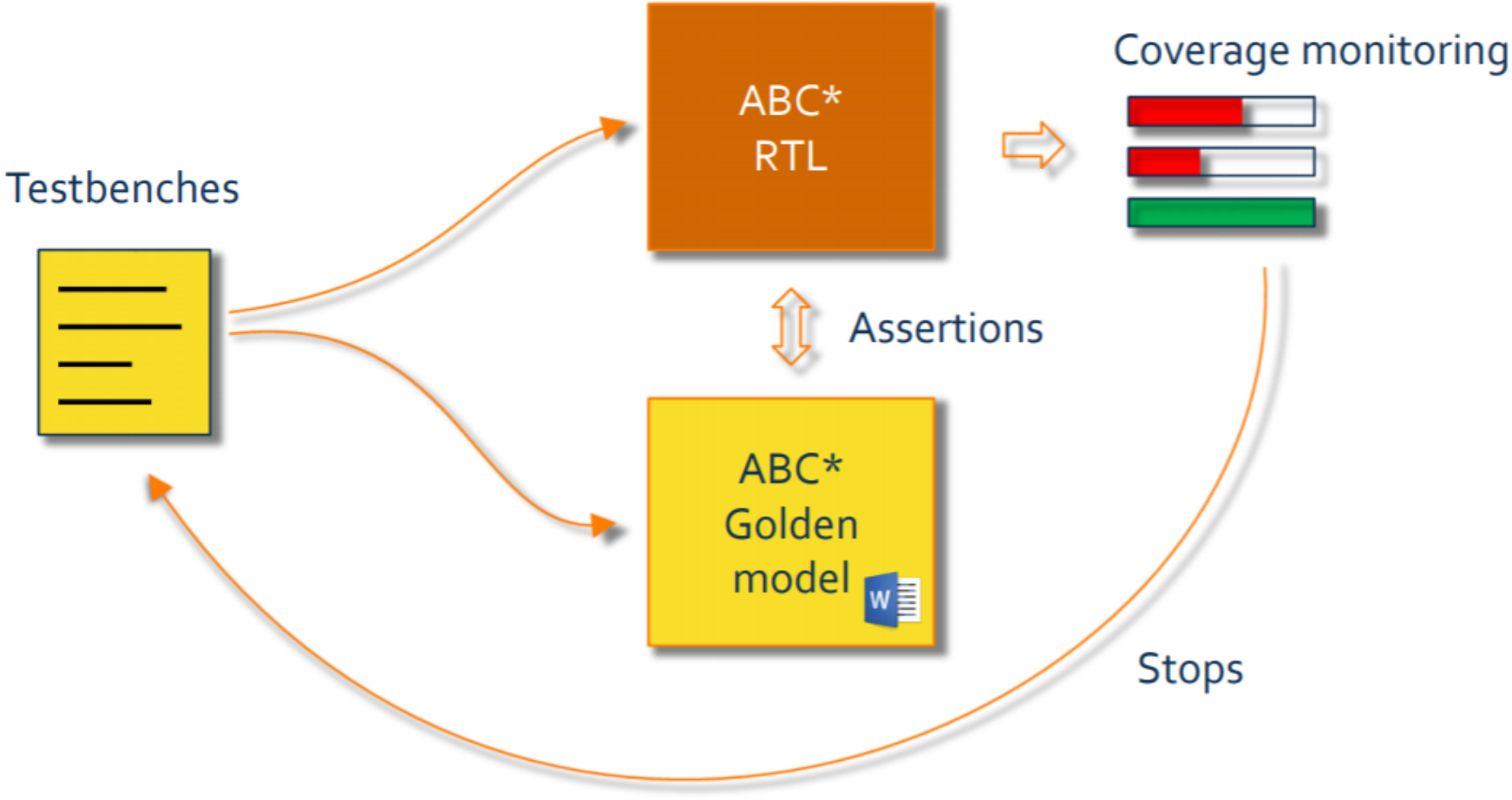
Now
Full digital flow
With analog inserts

Methodology, Verification

- Basically, how to ensure that an IC design sent to fabrication will result in a working chip.
- Integration of individual elements (circuits) into a full chip
- Validation that the full chip is bug free
- Goal: remove all possibility for human error
- Digital is compiled code
- Analog is hand drawn by a human

Which do you think can be more reliably automatically verified?

ABC* example


Testbenches
ABC*
RTL
Coverage monitoring
Assertions
ABC*
Golden
model
Stops

Code segment example: counters

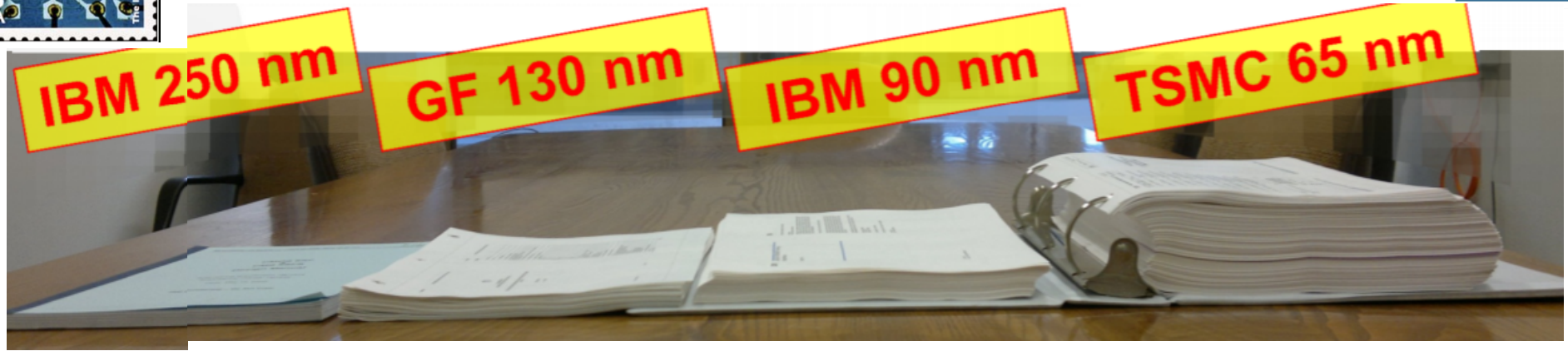
```
always @(AfterPreset) begin
  static real cov = 0;
  fork begin
    while (cov != 100) begin
      randsequence(main)
      //Sequence of counter start - stop - reset - enable - disable - l0 with weights
      main : cstart := 20 | cstop := 10 | crest :=2 | cenab :=10 | cdisa :=5 | l0str :=150 | l0sing := 250 | nothg :=200;
      cstart : {CountStart;};
      cstop  : {CountStop;};
      crest  : {CountReset;};
      cenab  : {EnableCounter;};
      cdisa  : {DisableCounter;};
      l0str  : repeat ($urandom_range(1,4)) l0sing;
      l0sing : {SendL0;};
      nothg  : {BCclockIt;};
      endsequence
      if (cov < hitc_cg.get_coverage()) begin
        cov = hitc_cg.get_coverage();
        $display("[Test.sv]Hit coverage is: %e", cov);
      end
    end
  end

  //Distribution of hits with 0 to 255 hits
  begin
    forever begin
      BCclockIt;
      number_of_hits = $urandom_range(0,255);  //White distribution from 0 to 255
      void'(randomize(stripData) with {$countones(stripData) == number_of_hits;});
    end
  end
```

Run until coverage = 100%

Random sequence

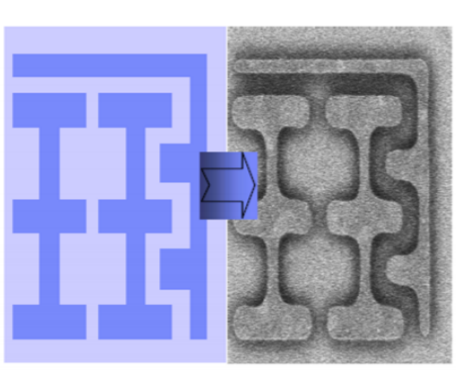
Task with weighted probability

Design Rules

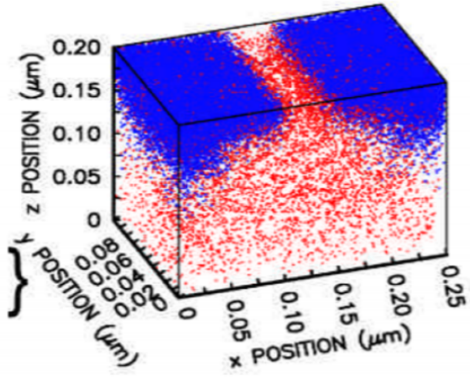


- Process is like a “build your own” sandwich:
  - Pre-defined as: bread, dressing, cheese, meat, veggies
  - You choose type of bread, dressing, cheese, meat, veggies, but not
    - order (bread goes outside and dressing goes on bread),
    - sizes and amounts, etc.
- Design rules specify layers, layer properties, restrictions, etc.

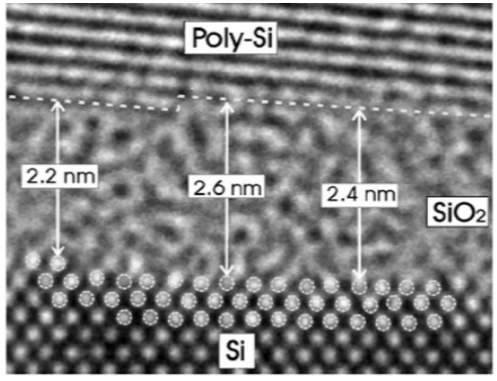
Variability (mismatch)



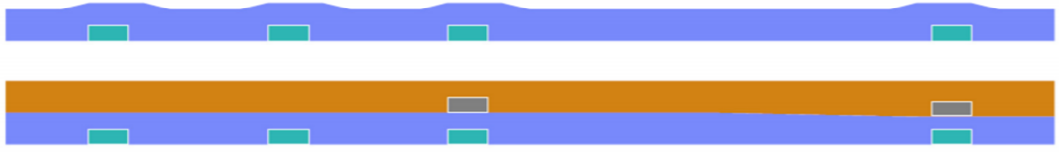
Litho-induced variability



Random dopant effects

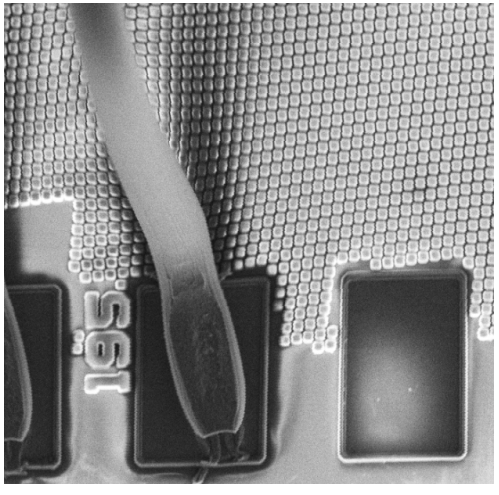


Oxide thickness

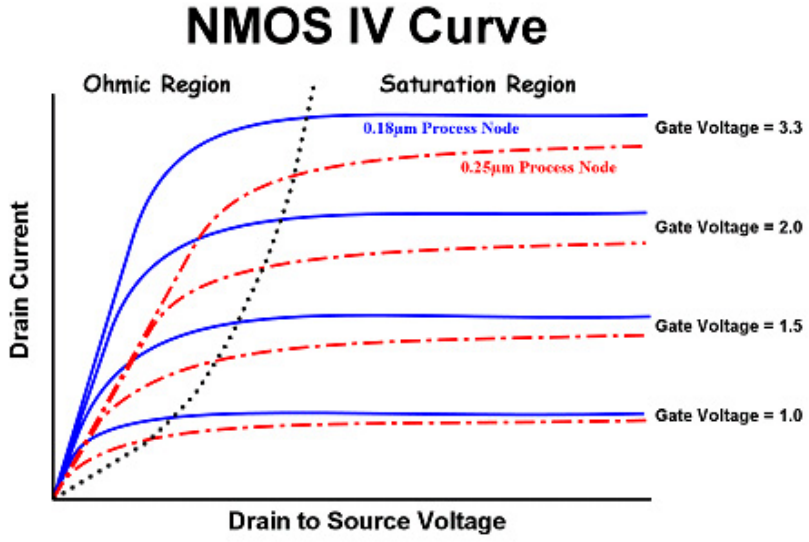


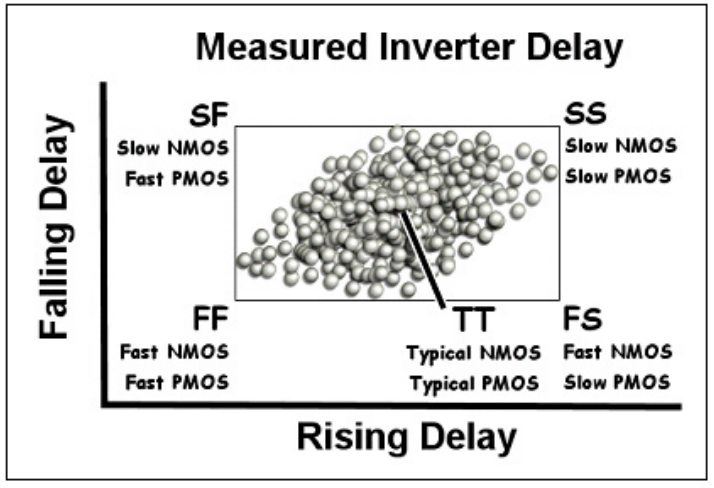
Interconnect CMP effects

Logically these get worse the smaller the feature size
Design rules mitigate them. Would be overwhelming without complex rules. Eg. Density :



Simulation Models and Corners





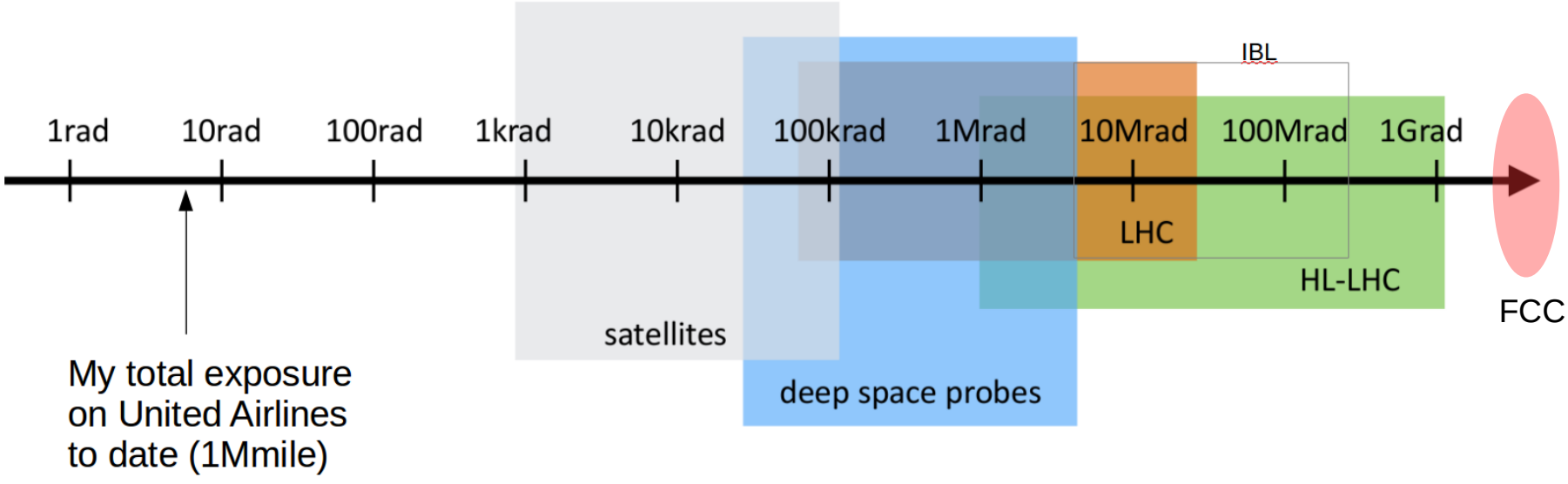
- Parametrized transistor response for analog simulation
- Parametrized gate delays & thresholds for digital simulation
- Parameters: size, voltage, temperature, process corners,…

- What about using transistors outside model parameters?

Outside of Model Parameters

- Two approaches:
  - De-rate existing parameters. For example model at lower voltage
  - Make your own corner models
- Second one is more work, but really the only way to take full advantage of very powerful digital design tools

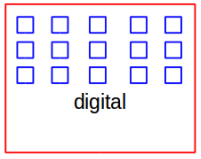
Radiation



We need to model its effect

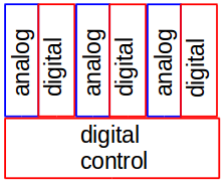
Rad Hard Logic Density Scaling

28nm ?



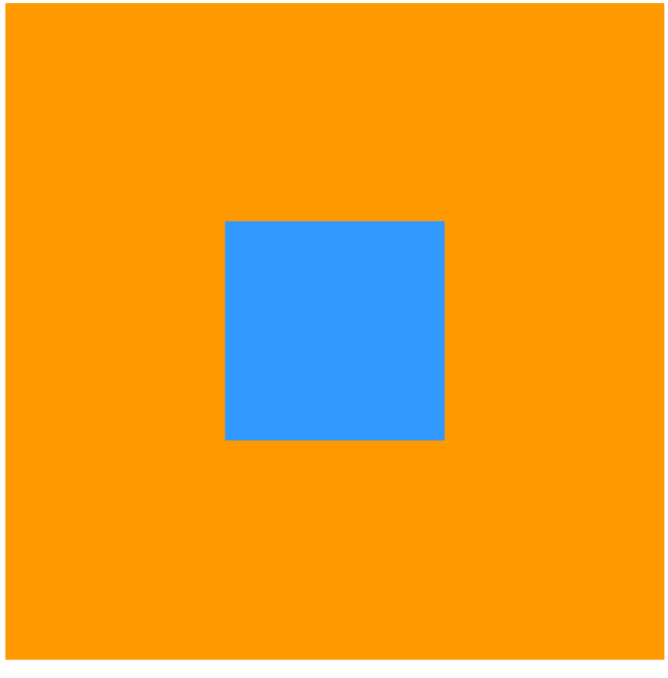
65nm

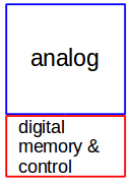
Not quite min. size due to pesky radiation damage.
But still 2-3x higher logic density than 130nm.



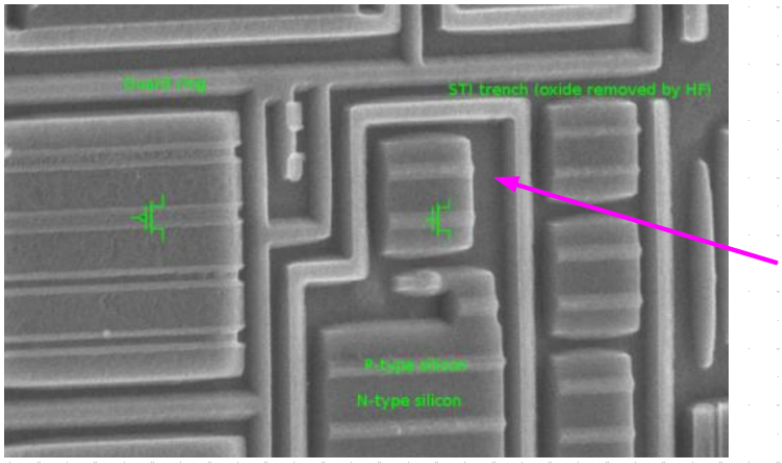
130nm

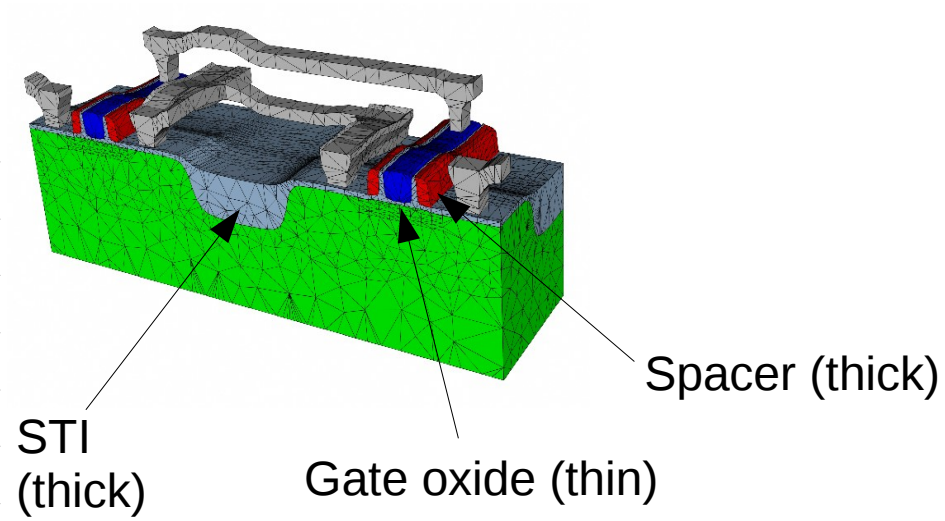
0.25um
ELT

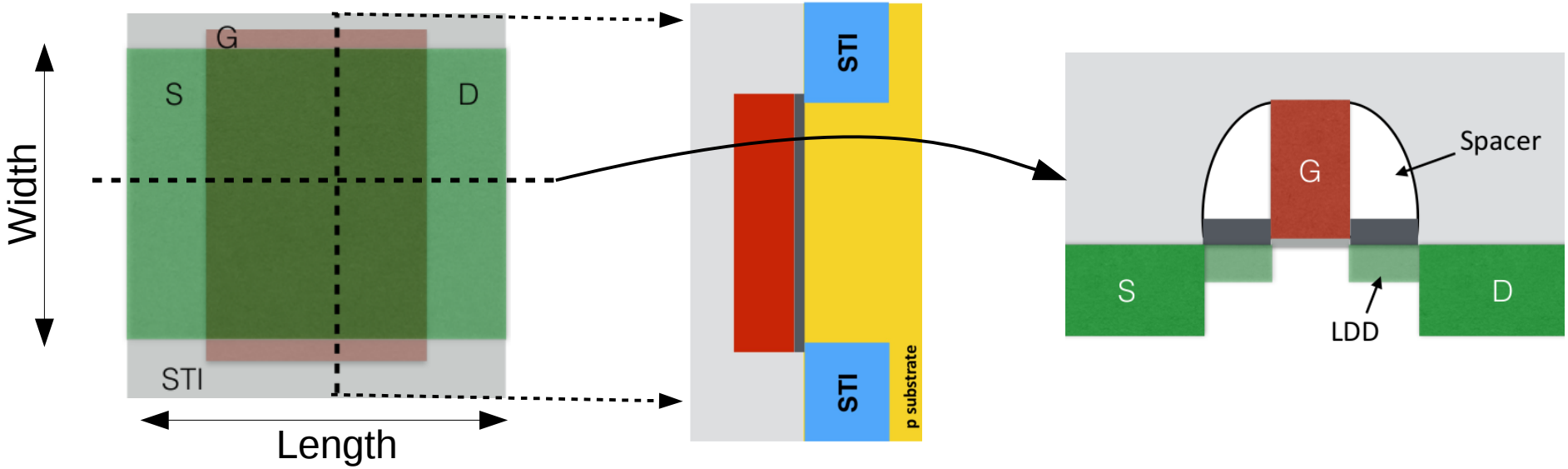




Radiation damage is an oxide affair
STI, Gate, Spacer





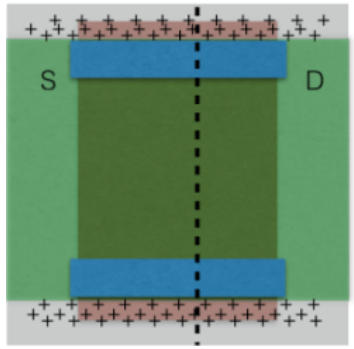


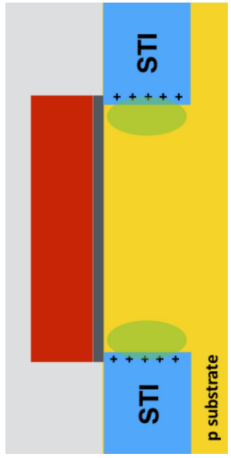
RINCE

Radiation Induced Narrow Channel Effect

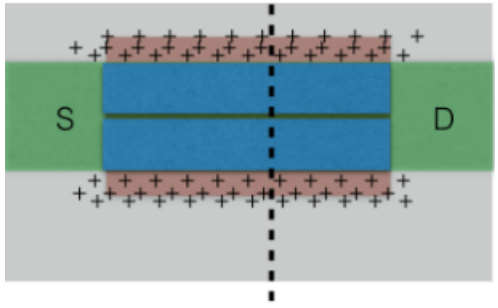
F. Faccio and G.Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Science, Vol.52, N.6 (2005) pp.2413-2420 http://dx.doi.org/10.1109/TNS.2005.860698

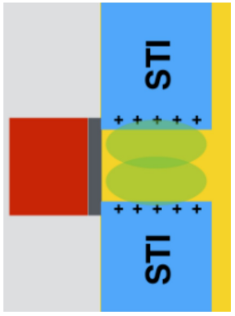
Wide Transistor

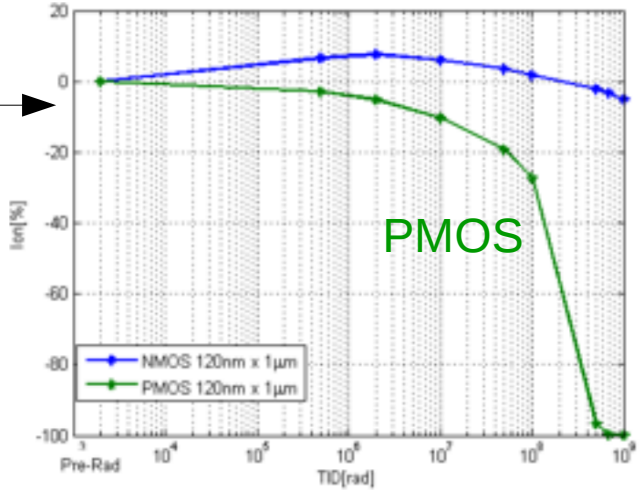




Narrowest Transistor







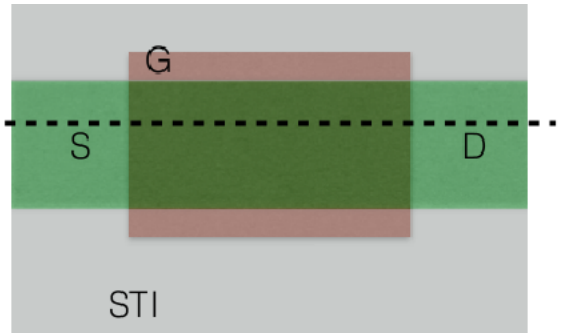
1Grad

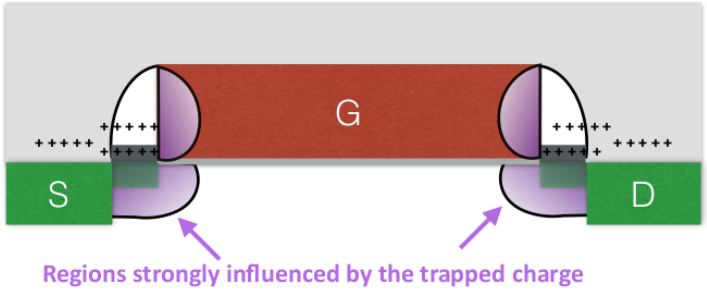
RISCE

Radiation Induced Short Channel Effect

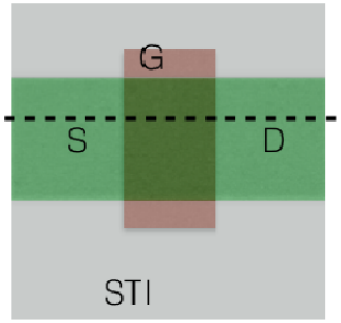
F. Faccio et al., "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," IEEE Trans. Nucl. Science, Vol.62 , N.6 (2015) http://dx.doi.org/10.1109/TNS.2015.2492778

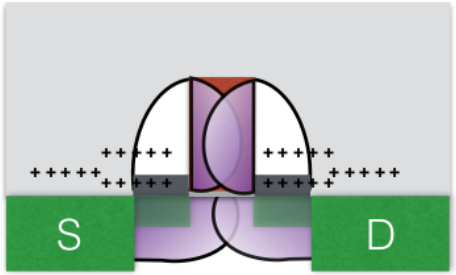
Long Transistor

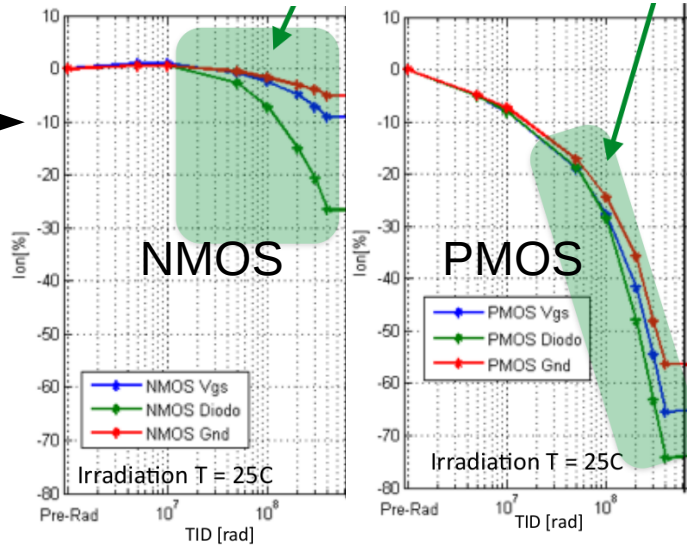




Shortest Transistor

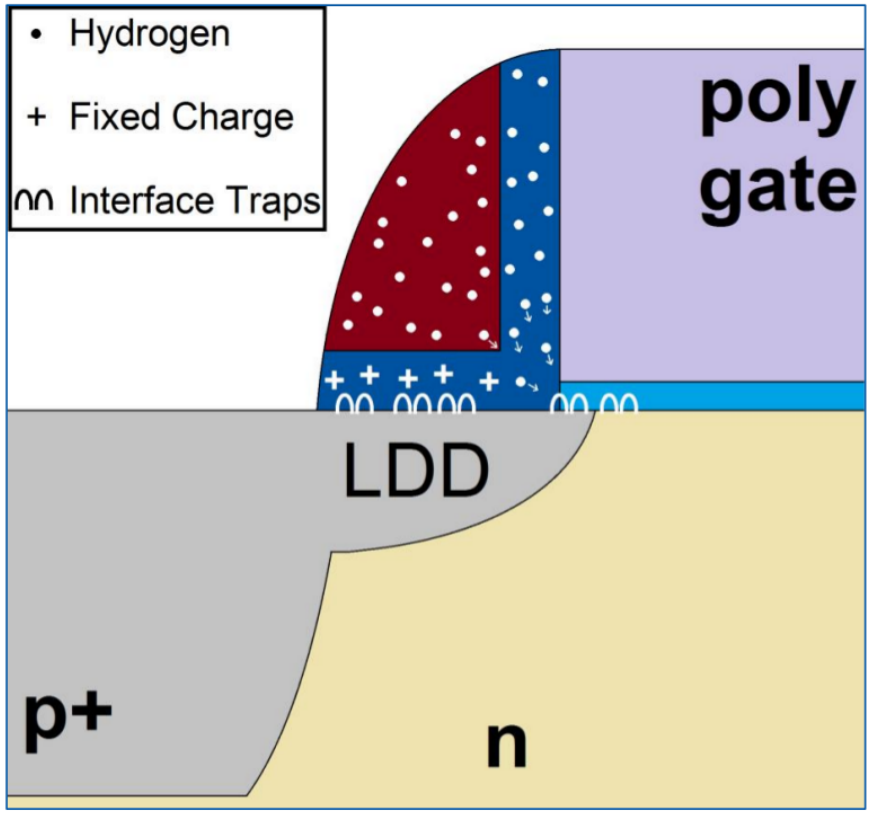






Bias matters!

Some understanding of complex mechanisms



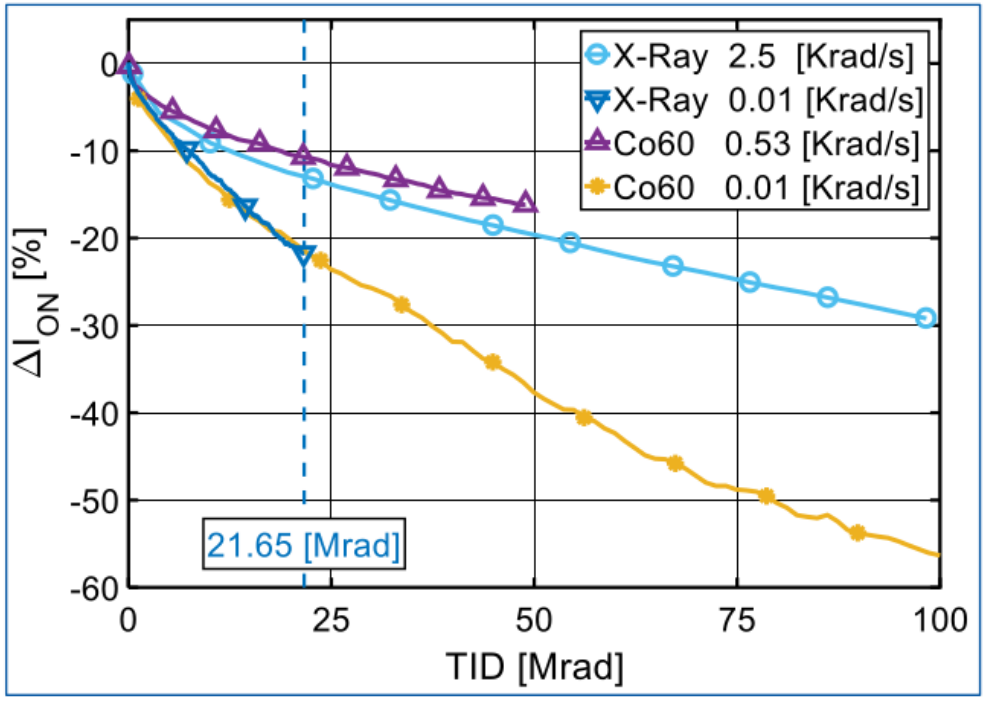
F. Faccio, et. al, "*Influence of LDD spacers and h+ transport on the total-ionizing-dose response of 65 nm mosfets irradiated to ultra-high doses*," Presented at the 2017 NSREC.

3-stage process:

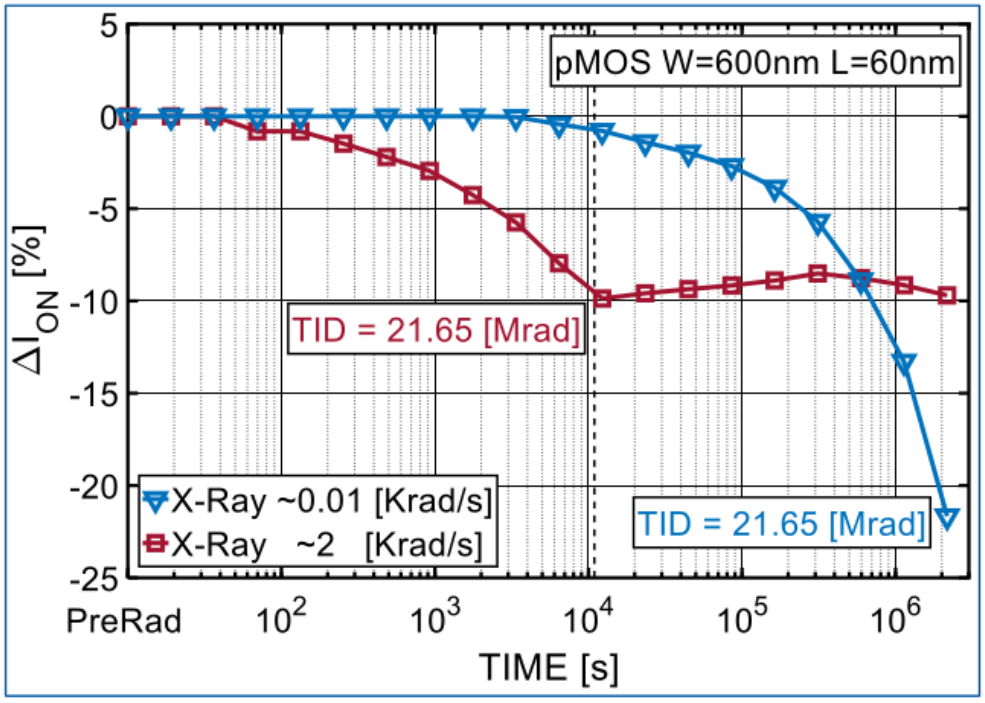
1. Ionization in the spacers.
2. Transport of H^+ from the spacers to the channel region.
3. De-passivation of Si-H bonds at the interface with the gate oxide.

✓ Large threshold voltage shift.

One more effect still to understand

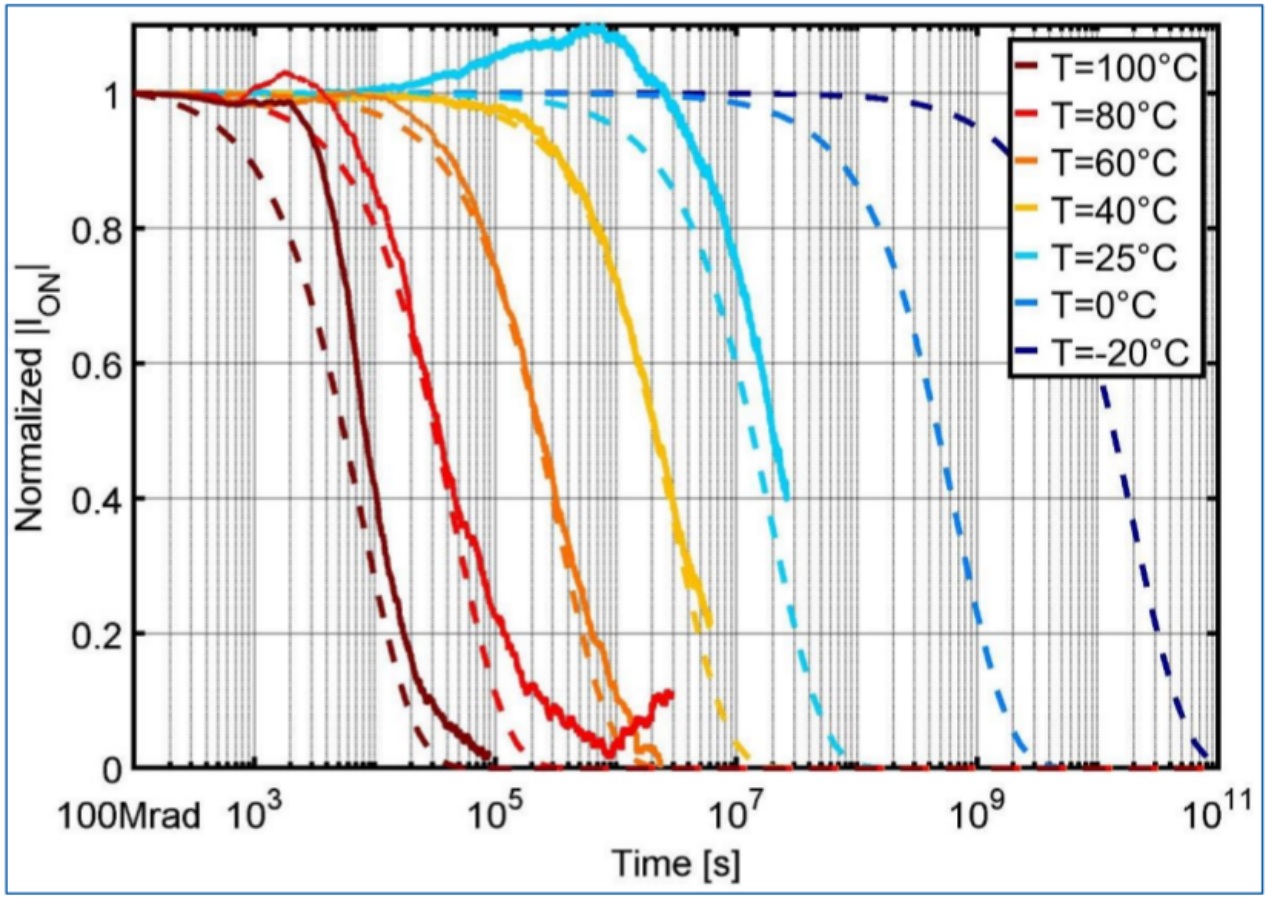


Larger current degradation at lower dose rates.



Not "time-dependent" effect – True enhanced LDR sensitivity.

Cold is safe (LDR aside)



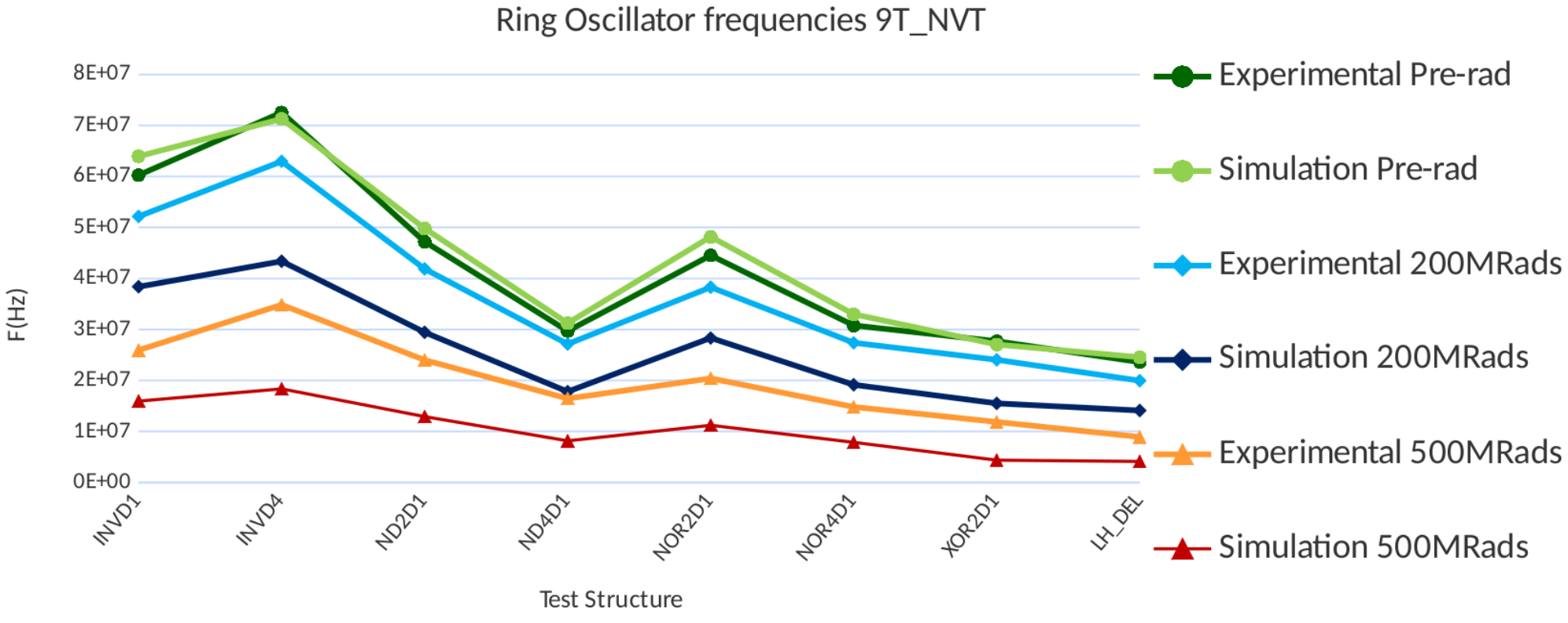
We estimated the evolution of the 2nd effect at low T.

Solid lines: measured
Dashed lines: estimated

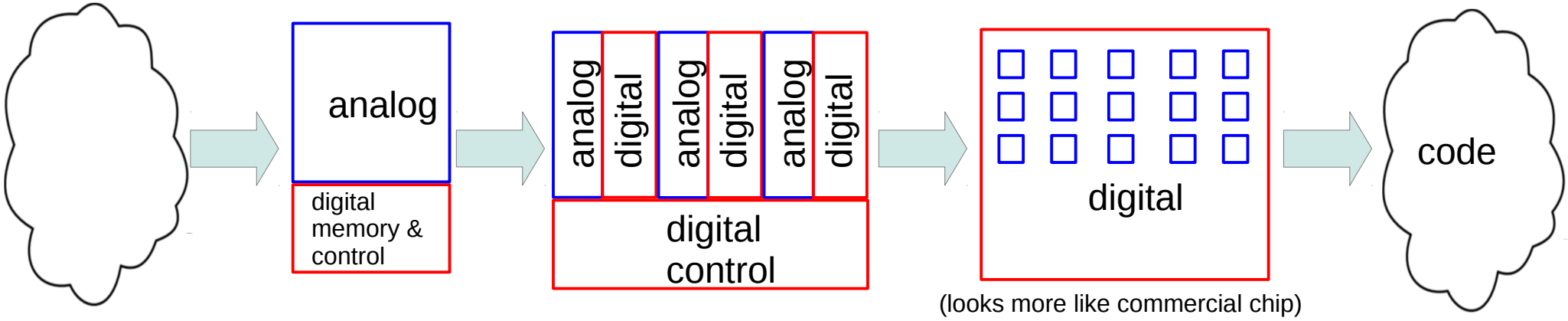
At -20°C it would take more than 400 years to halve the maximum drain current.

Digital switching is safe: Data-simulation comparison

- Comparison of models used in RD53A chip with test chip data.
- Ring oscillator frequency is sensitive to TID effects
- Different logic cells can be used to make ring oscillator test structures
- Models were built from single transistor data under DC worst case bias.
- A switching transistor is less vulnerable. We see 2x less damage.



Shift in IC Design Approach



(looks more like commercial chip)

Physicist drawing transistors

Single institute team

FE-I4

Participating institutes:

Bonn: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis.

CPPM: D. Fougeron, M. Menouni.

Genova: R. Beccherle, G. Darbo.

LBNL: S. Dube, D. Elledge, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui.

Nikhef: V. Gromov, R. Kluit, J.D. Schipper

Nov. 2017 RD53 meeting, CERN

Your pic here

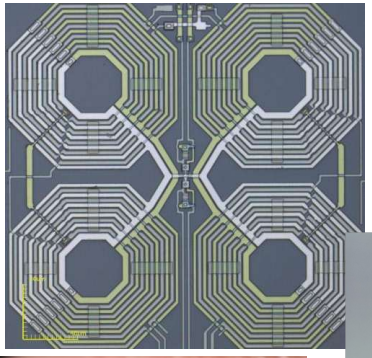
Commercial style design and validation
10^9 transistor Chips work the first time

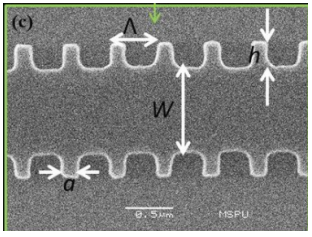
Lithographic Manufacture

IC invention → Develop Si lithographic manufacture → Make Si strip detectors → Need readout ASICs → pixels Etc.

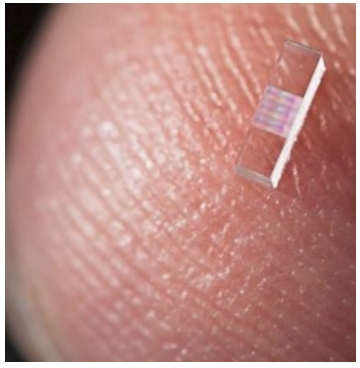
Other HEP instrumentation development

SQUIDs

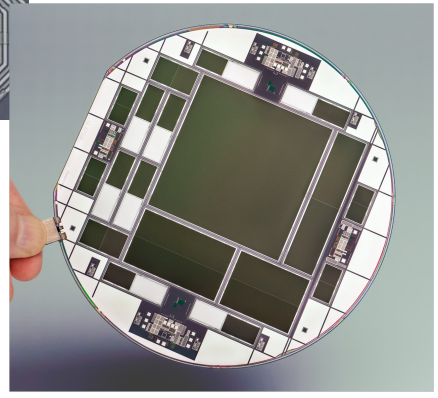




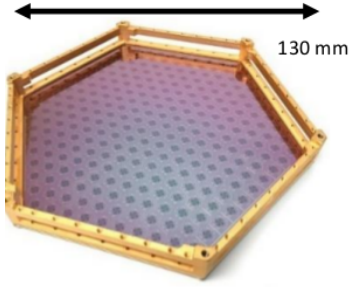
Silicon photonics



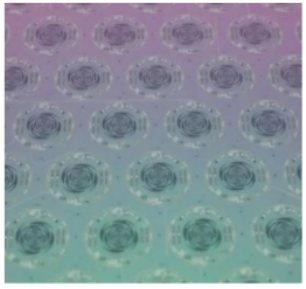
MEMS accelerators



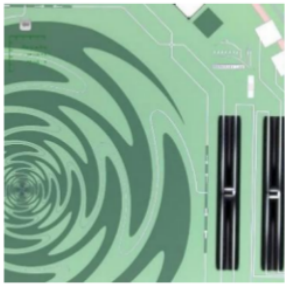
Fully depleted CCDs



Detector Array

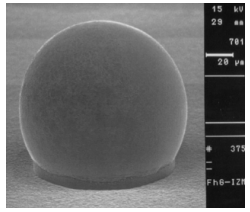


Array of Pixels (6mm)



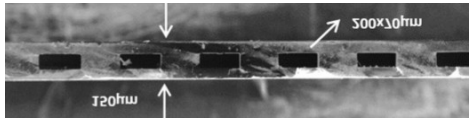
Pixel Overview

Superconducting bolometer arrays

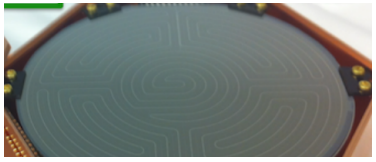


Bump bonding

Micro channel cooling



Micro-calorimeters

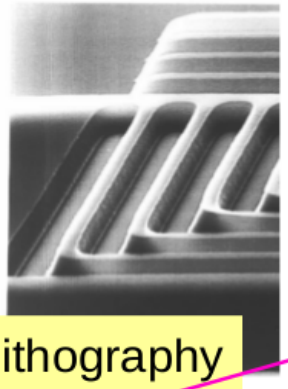


Conclusions

- This was not a practical or quantitative lecture on IC desing
- Presented a flavor of what you could learn more about
- ASIC's and/or microfabrication are essential to almost every experiment
  - Maybe one should know something about this
- Should there be a real IC design lab course for physics students?
  - (end product is a tape-out of your very own design IC)

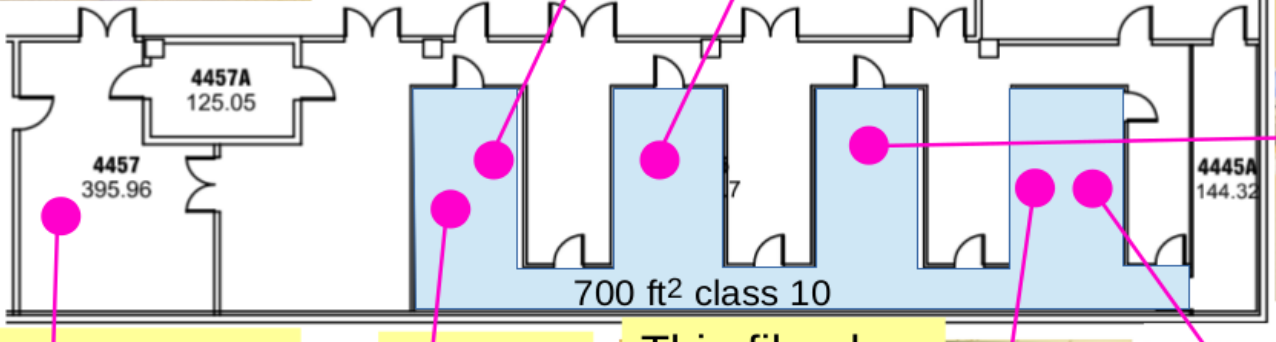
MSL Virtual tour

Thermal proc.



1.5µm Photolithography

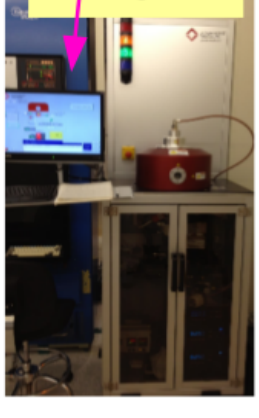
Purification



Wet Chemistry

CMB equipment

PE CVD



Thin film dep.

Dry Etching