ATLAS readout system from the current Pixel Detector to the Phase-I and Phase-II upgrade

Alessandro Gabrielli

Physics and Astronomy Department University of Bologna

alessandro.gabrielli@bo.infn.it http://www.bo.infn.it/~gabriell

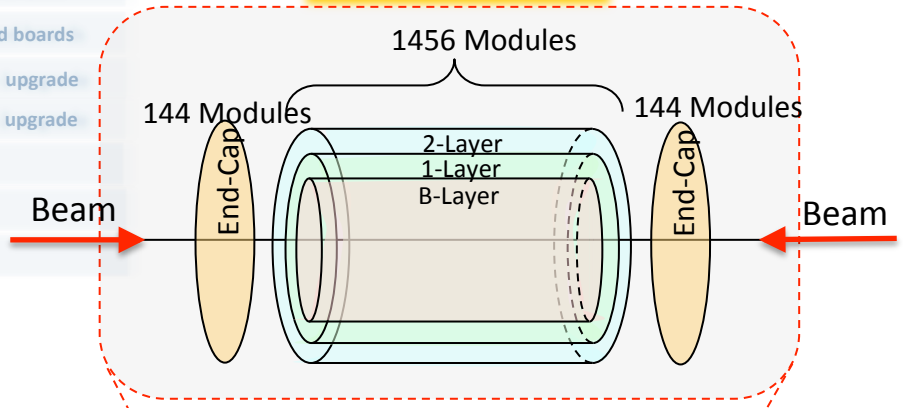
.. and F. Alfonsi, G. Balbi, G. D'Amen, D. Falchieri, N. Giangiacomi, G. Pellegrini, R. Travaglini

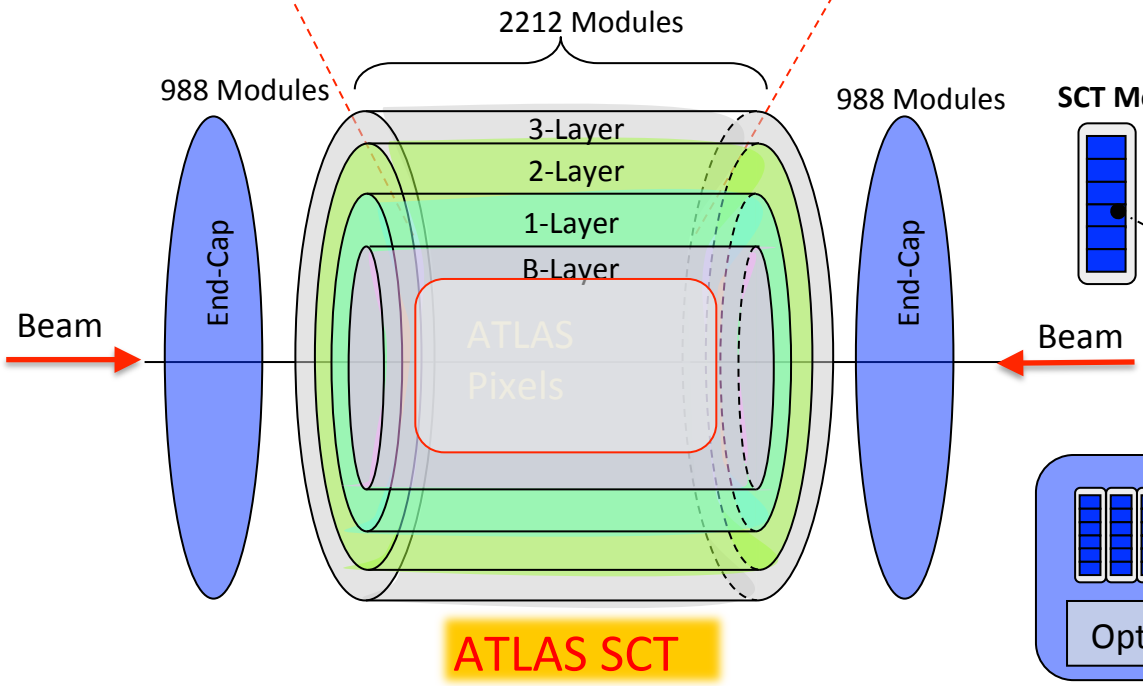
The presenter wishes to acknowledge A. Borga, G. Lehmann and M. G. Sciveres for their relevant contributes to this summary

Outline

- Pixel Readout System till 2009, before Phase 0 upgrade
- IBL Plan started in 2009
- IBL commissioned boards
- Towards Phase-1 upgrade
- Towards Phase-2 upgrade
- GBT and FELIX
- Pixel_ROD
- Future Plans

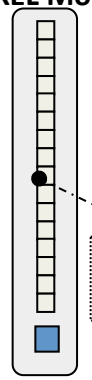
ATLAS Pixels





ATLAS SCT

PIXEL Module

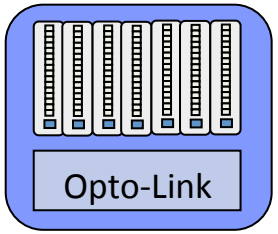


16 FE-I3

160 x 18 pixels
50 x 400 μm²

1 Module
Controller
Chip MCC

OptoBoard (2 versions) **2009**



7 Modules

Layer	EC	2	1	B
OptoBoard		4	2	1
Modules		32	16	8
Rate Mb/s	40	40	80	160
Ribbon Tx/Rx		4/4	2/2	1/2
Fibers Tx/Rx		32	16	8/16

SCT Module

6 ABCD3TA

128 strips
80 μm

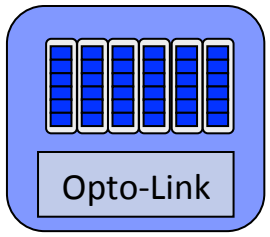
40 Mb/s

40÷160 Mb/s

Max
1 Gb/s

4 x 12-fiber ribbon = **48** TX-fibers

8 x 12-fiber ribbon = 96 RX-fibers



6 Modules

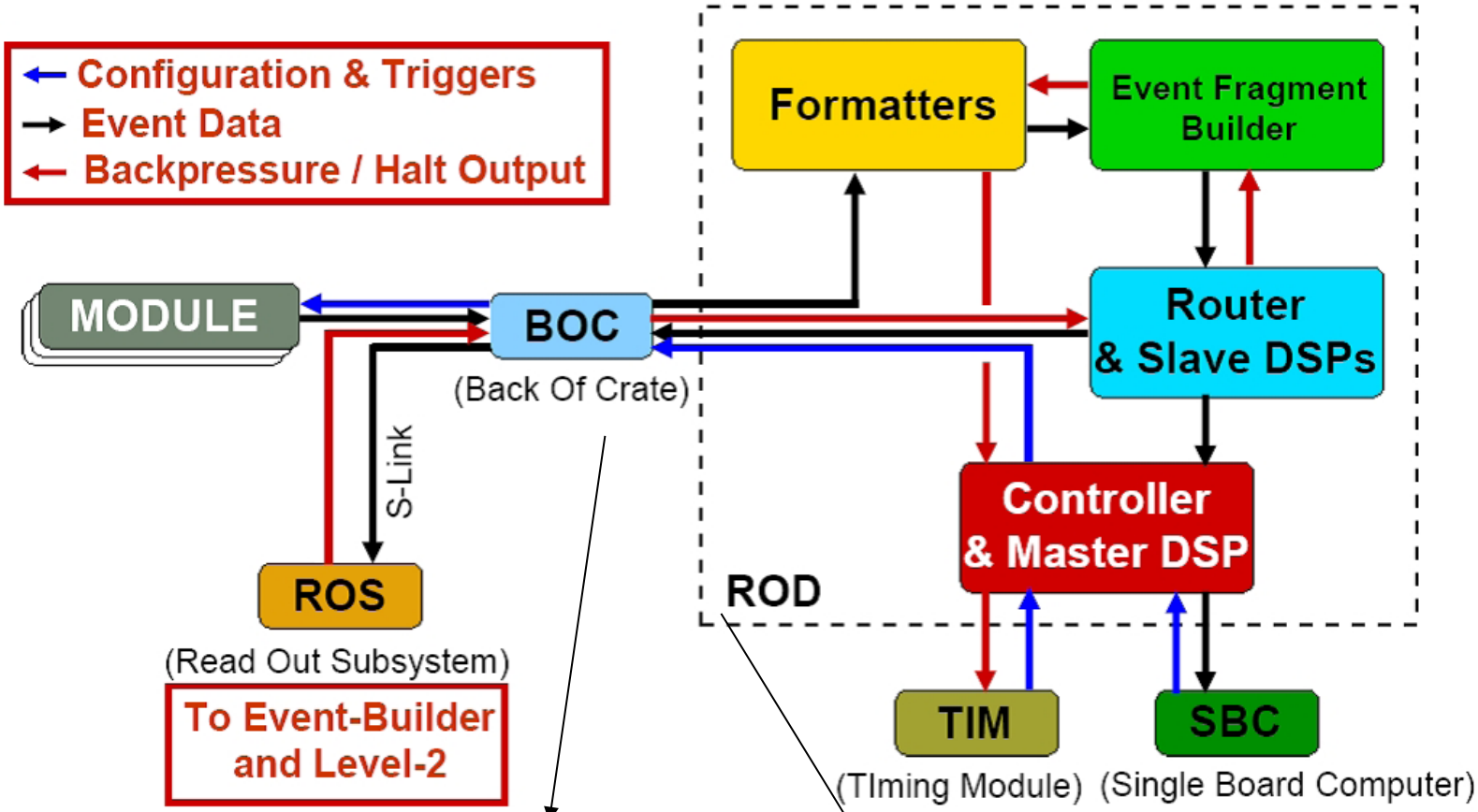
OptoBoard for SCT

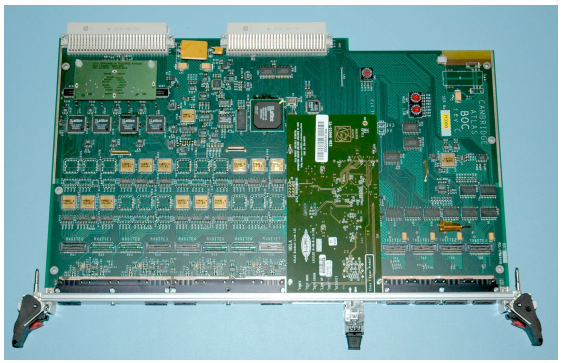
Back Of
Crate BOC

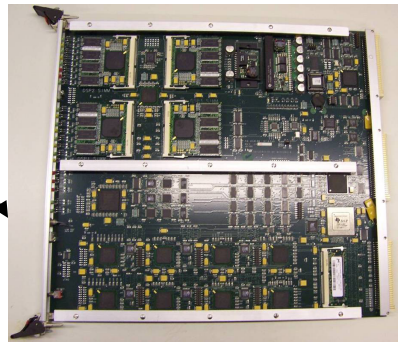
ReadOut
Driver ROD

1 S-Link

Old Pixel Readout Chain 2009







Some IBL Numbers

Item		Radial Extension [mm]	Length [mm]	Staves / Sectors	Modules	Pixels ($\times 10^6$)
Beam pipe (today)		$29 < R < 36$				
Beam pipe (with IBL)		$25 < R < 29$				
IBL	Envelope	$31.0 < R < 40.0$				
	Sensitive	$< R > = 25.7$	$\|Z\| < 332$	14	224	6.02
Pixel	Envelope	$45.5 < R < 241.0$	$\|Z\| < 3092$			
B-layer	Sensitive	$< R > = 50.5$	$\|Z\| < 400.5$	22	286	13.2
Layer 1	Sensitive	$< R > = 88.5$	$\|Z\| < 400.5$	38	494	22.8
Layer 2	Sensitive	$< R > = 122.5$	$\|Z\| < 400.5$	52	676	31.2
Disk 1	Sensitive	$88.8 < R < 149.6 = 88.5$	$< Z > = 495$	8×2	48×2	4.4
Disk 1	Sensitive	$88.8 < R < 149.6 = 88.5$	$< Z > = 580$	8×2	48×2	4.4
Disk 1	Sensitive	$88.8 < R < 149.6 = 88.5$	$< Z > = 650$	8×2	48×2	4.4
					Pixel Total	*80.4*

Table 1. Main parameters of the Pixel Detector system including the foreseen IBL.

Directly from ATLAS TDR 19 8 October 2010

IBL: Insertable B-Layer

Some Numbers

Pixel System $L = 10^{34}cm^{-2}s^{-1}$, *LVL1 rate = 100 kHZ*	**Col. pair occ.** hits/BC	**MCC** bandwidth	**ROD** bandwidth
B-layer *160 Mb/s MCC out* *6/7 modules/ROD, 44 RODs*	0.18	47 ± 3 %	52 ± 3 %
Layer 1 / Disks *80 Mb/s MCC out* *13 modules/ROD, 38 + 24 RODs*	0.06	39 ± 3 %	35 ± 3 %
Layer 2 *40 Mb/s MCC out* *26 modules/ROD, 26 RODs*	0.04	53 ± 3 %	43 ± 3 %

Layer 2 expected to be more critical than Layer 1

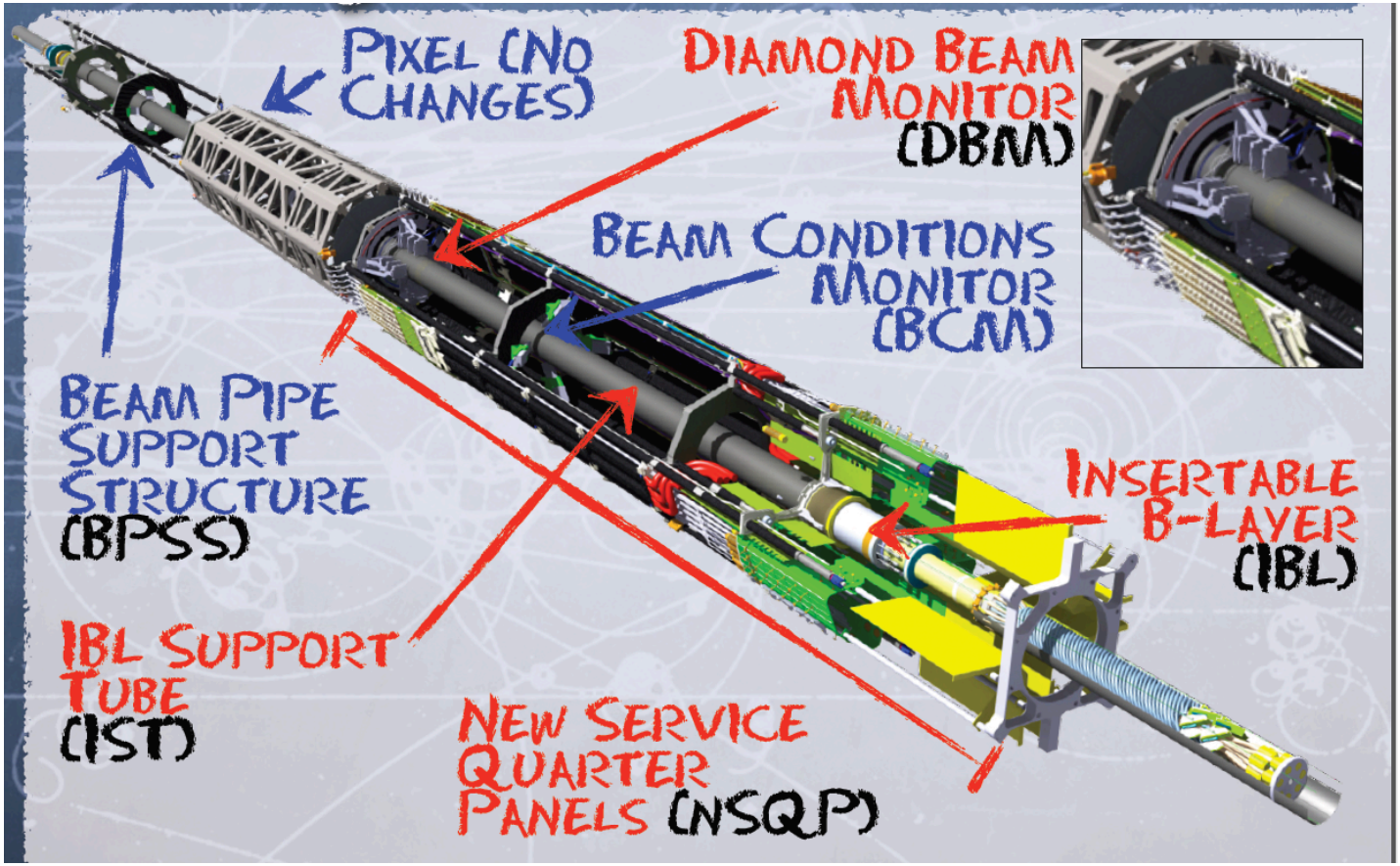
Table 2. Column pair occupancies and output bandwidths for single MCC and ROD for different Pixel subsystems. Values reported in the table have been simulated for nominal LHC luminosity of $10^{34}cm^{-2}s^{-1}$ and maximum design first level trigger (LVL1) rate of 100 kHz.

Directly from ATLAS TDR 19 8 October 2010

IBL: Insertable B-Layer

IBL plan

2009



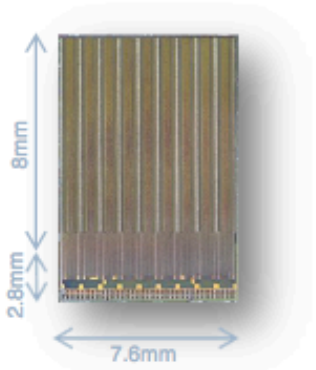
Insertable B-Layer (IBL) is a fourth layer added to the old Pixel detector between a new beam pipe and the old inner Pixel layer (B-layer).

MOTIVATIONS

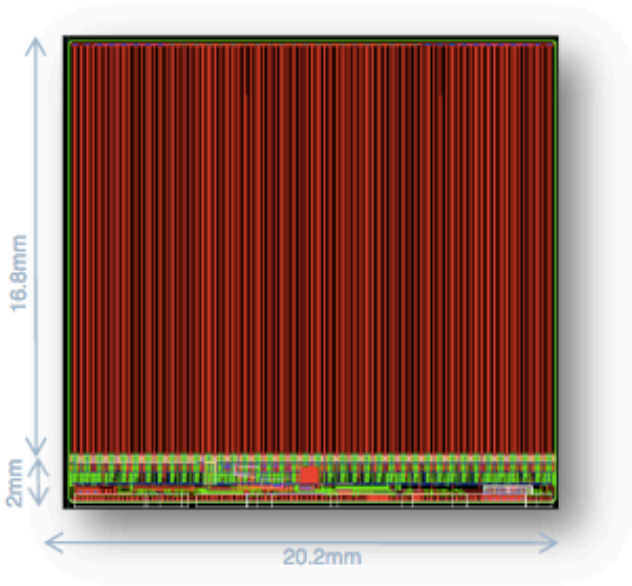
- **Peak luminosity was expected to increase from 1 to 2.2 x 10^{34} $cm^{-2}s^{-1}$**
- ***b* tagging efficiency, tracking precision**
- **Radiation hardness**

Readout Chips

FE-I3

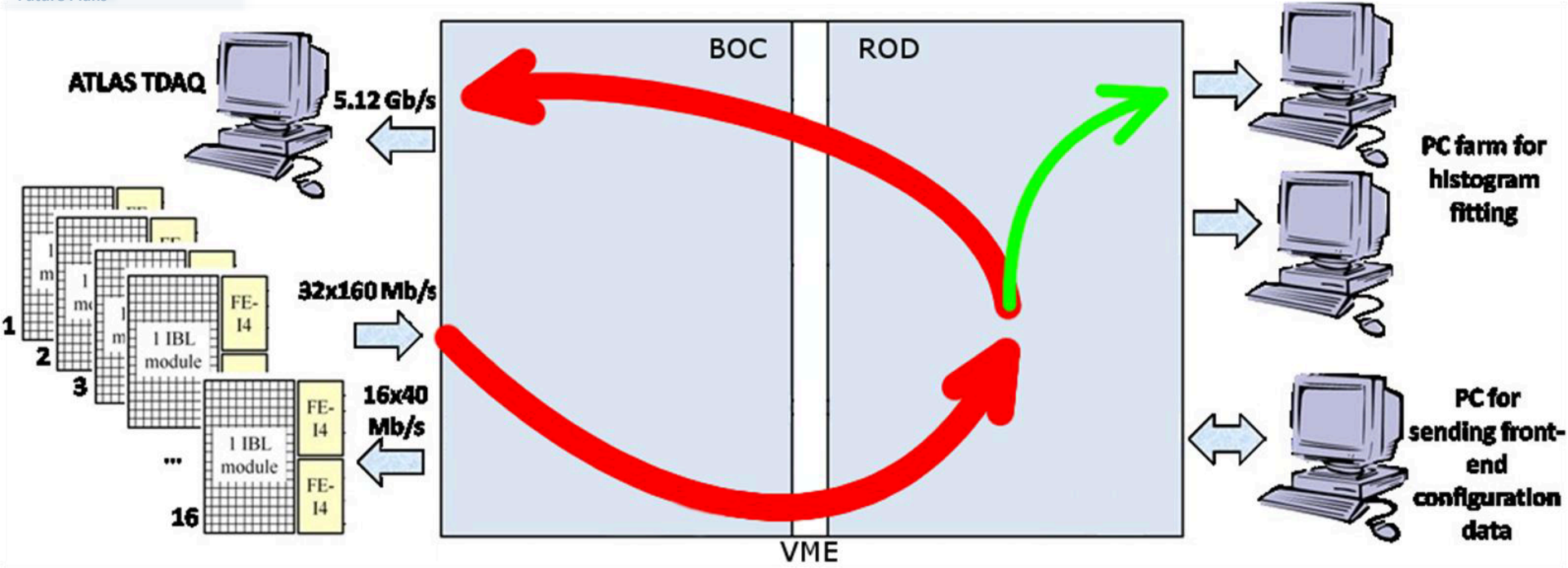


FE-I4

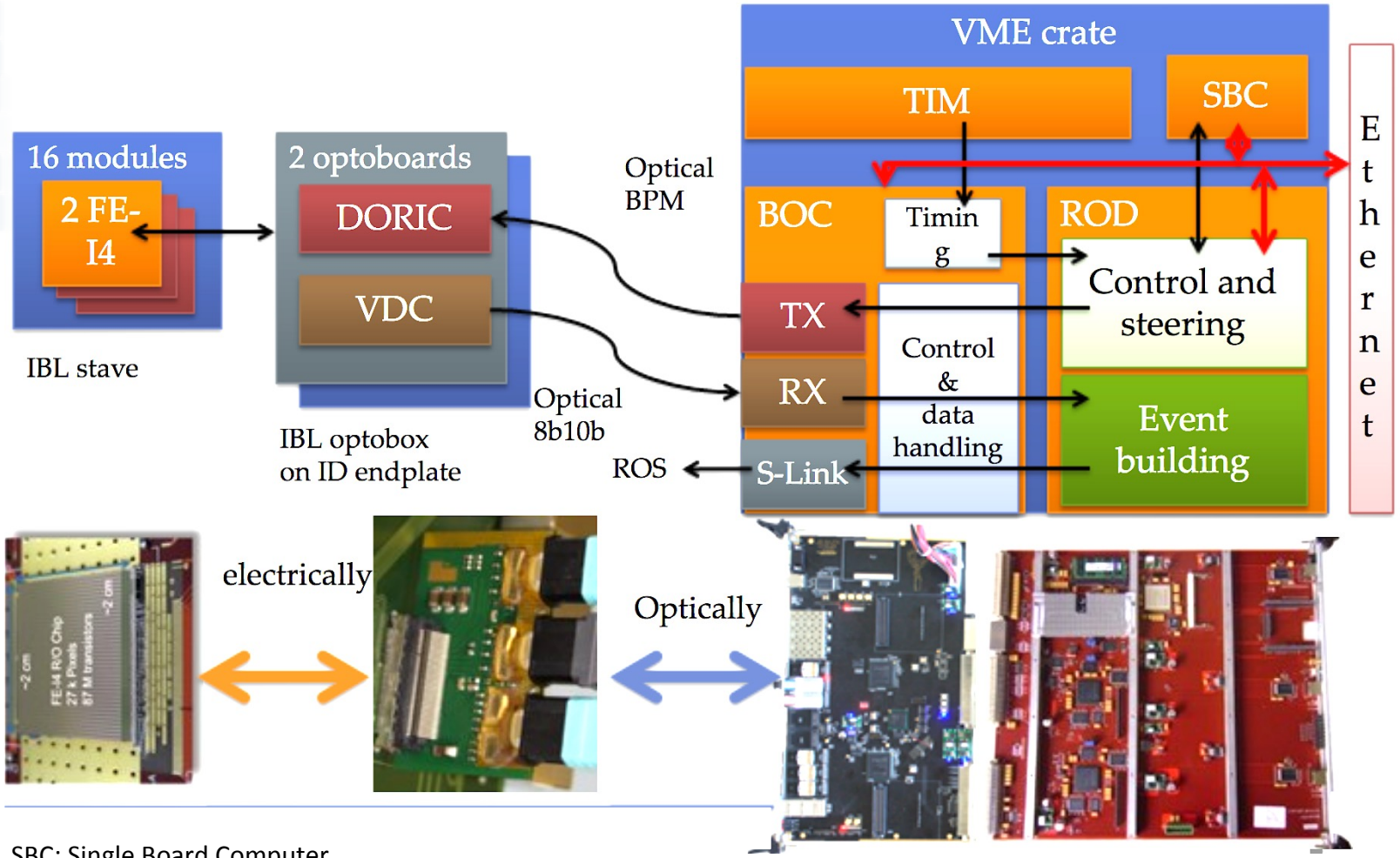


Pixel Size [μm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Output Data Rate [Mb/s]	40	160
Transistor Count [M]	-	~80

IBL BOC + ROD



IBL Pixel Readout Chain

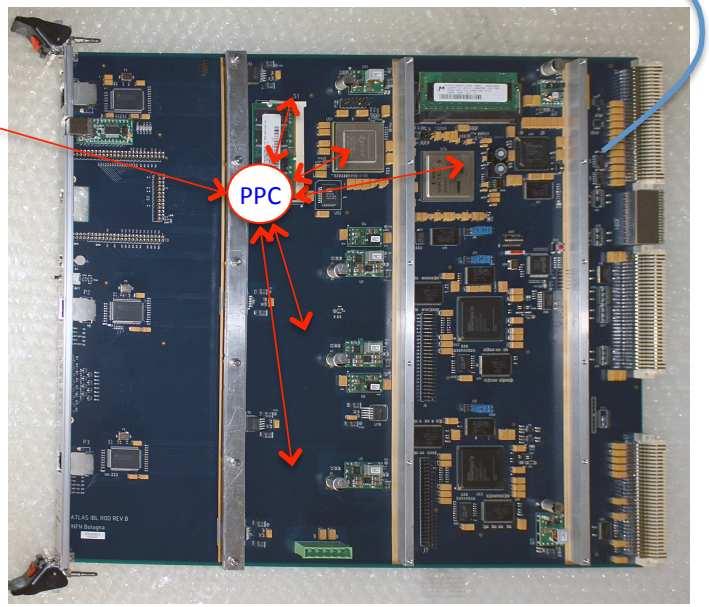


SBC: Single Board Computer
TIM: TTC (Timing, Trigger and Control) Interface Module
DORIC: Digital Optical Receiver Integrated Circuit
VDC: Voltage-to-Digital Converter
BPM: Bi-Phase Mark
ROS: ReadOut Server
S-Link: Simple Link Interface

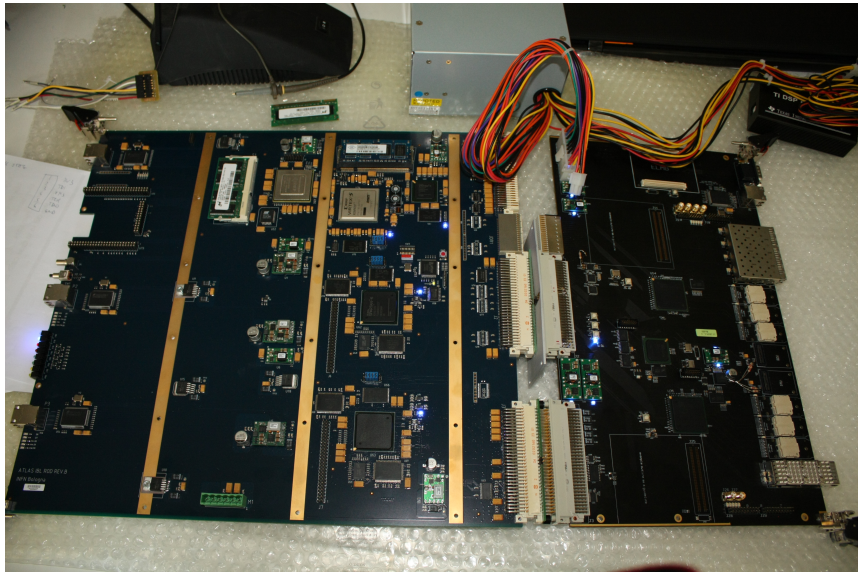
Mar. 2012 - IBL ROD (rev B) Bologna

FEI4 module

B
O
C

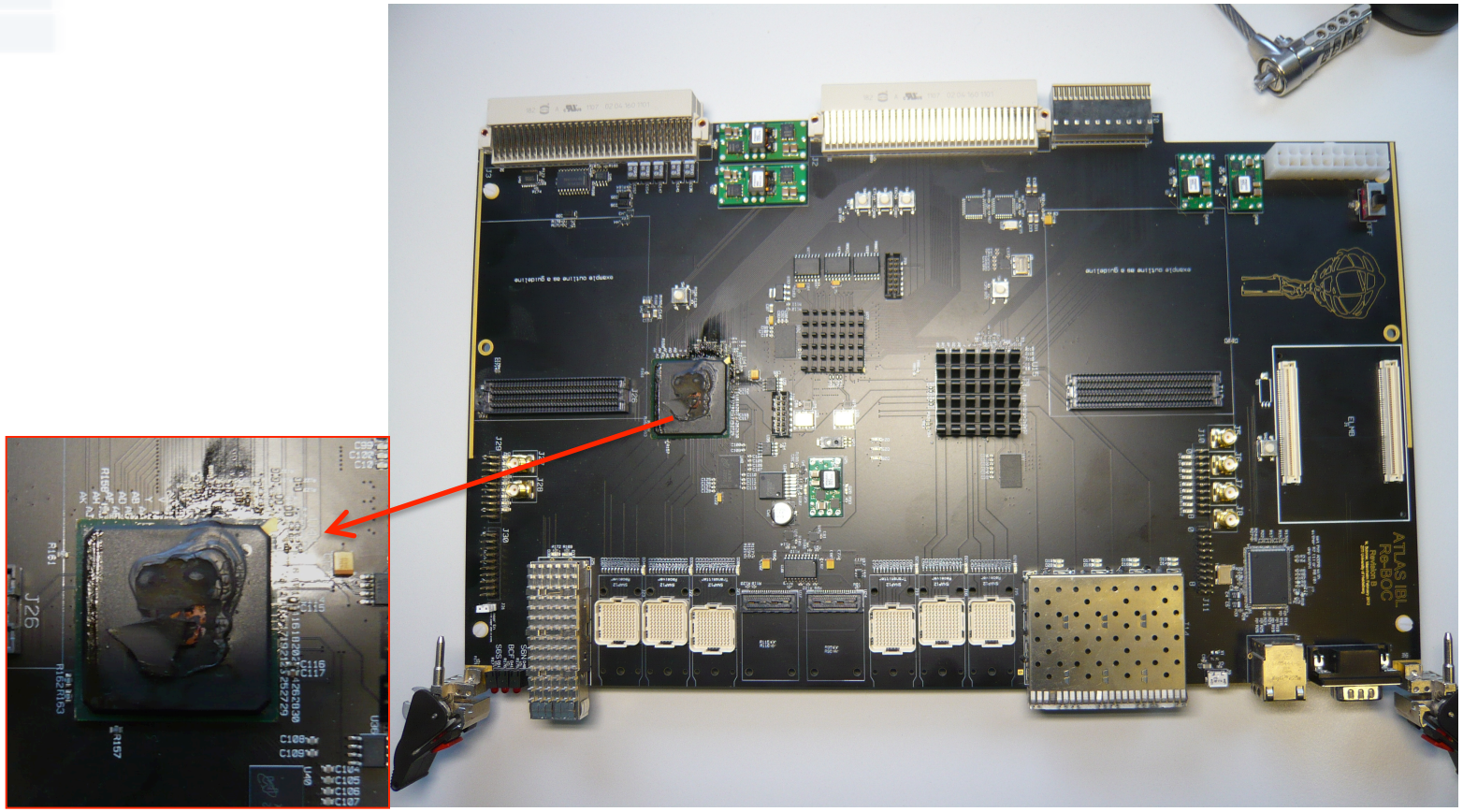


Virtex5 + PowerPC environment



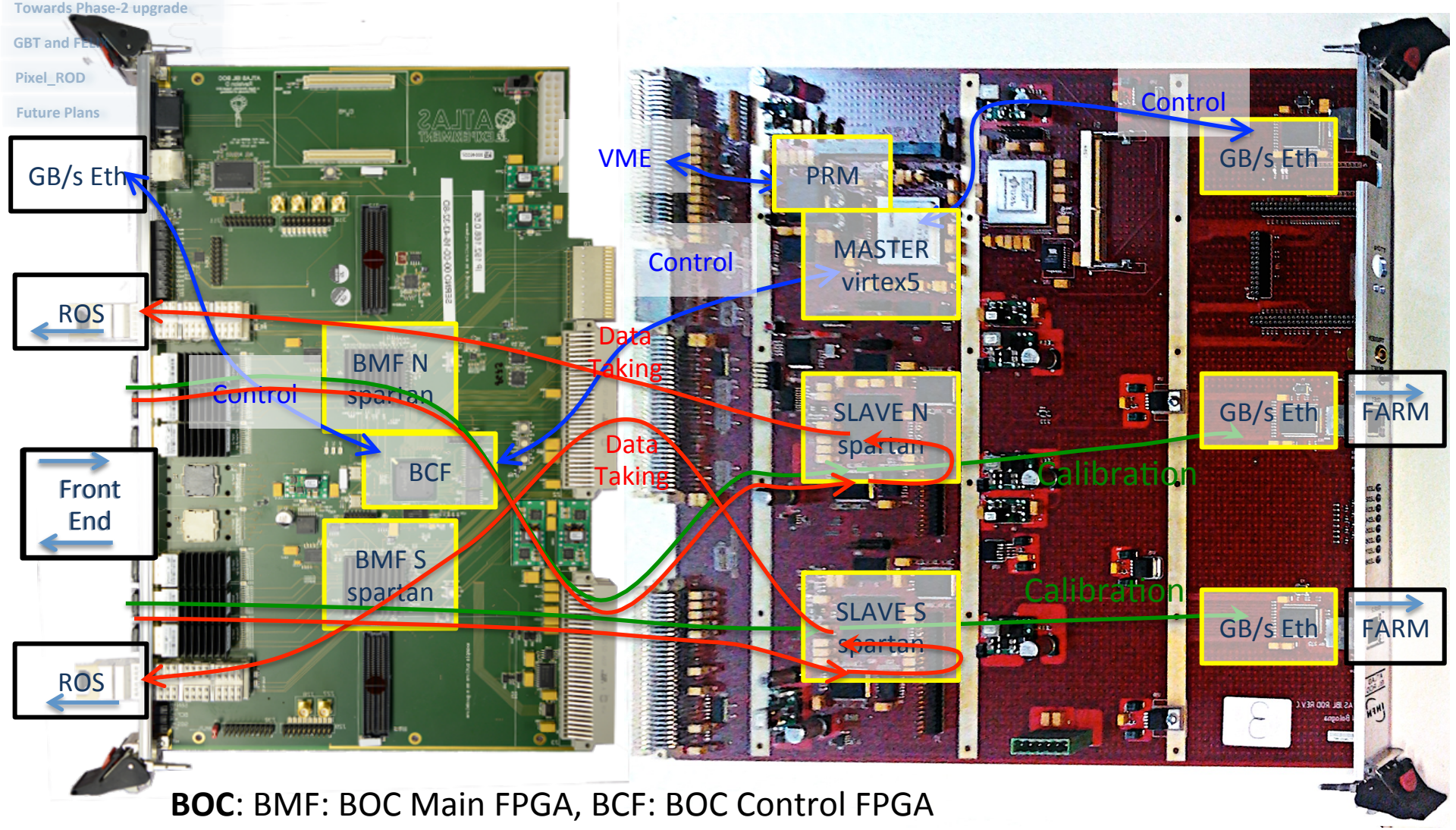
Patch for bugs on rev A
Tests in Bologna, Wuppertal, CERN from May 2012

Dec. 2012 - IBL BOC burnout at CERN



Reworking time 2 months

IBL/L2/L1/B-Layer/Disks
BOC ROD current features



BOC: BMF: BOC Main FPGA, BCF: BOC Control FPGA

ROD: PRM: Program Reset Manager, Master and 2 x Slaves

Occupancy extrapolation

Estimated Module Controller Chip MCC→IBL ROD **link occupancy** at **75** and **100** kHz level 1 (LVL1) rate:

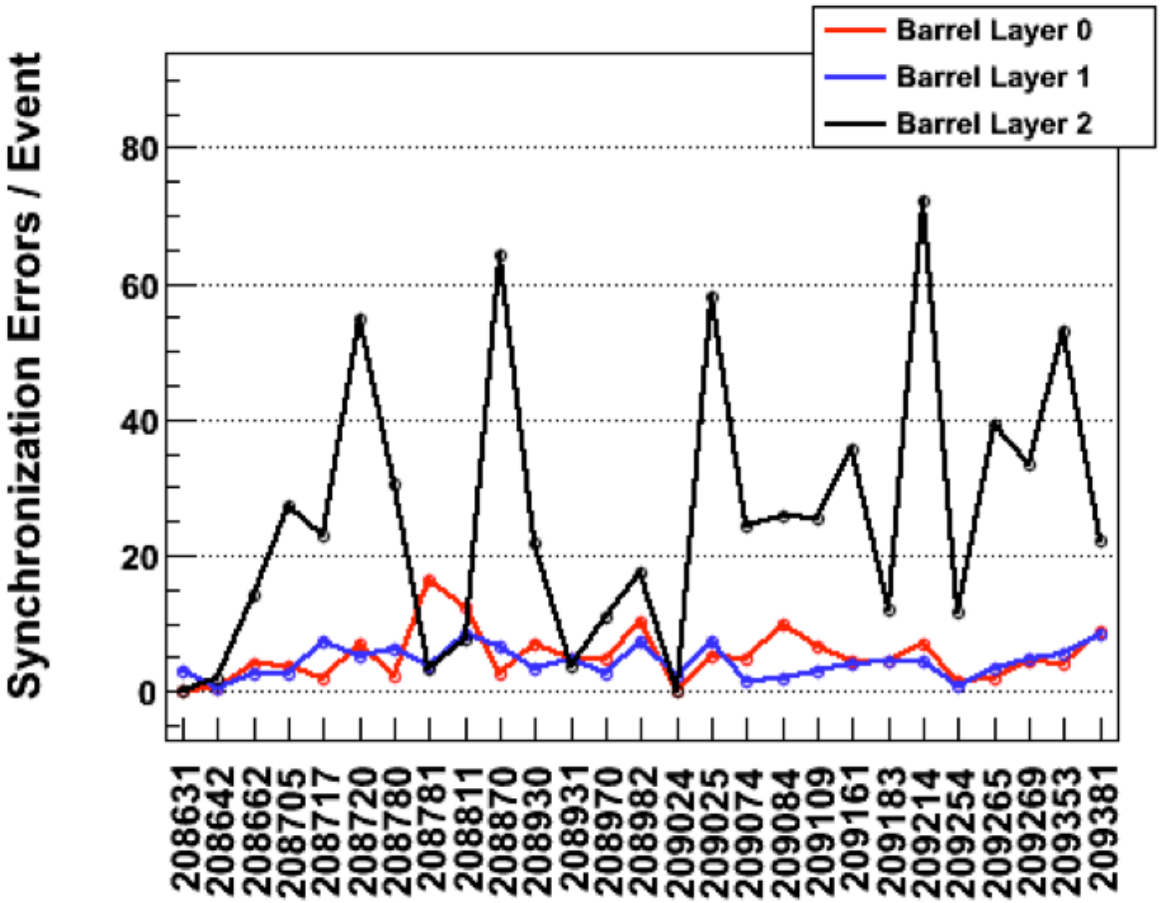
Link occupancy at 75 kHz L1 Trigger					
	μ	B-Layer	Layer 1	Layer 2	Disks
50 ns	37	39%	34%	52%	30%
25 ns; 13 TeV	25	35%	31%	48%	27%
	51	53%	59%	66%	39%
	76	71%	73%	111%	64%

Link occupancy at 100 kHz L1 Trigger					
	μ	B-Layer	Layer 1	Layer 2	Disks
50 ns	37	51%	45%	69%	40%
25 ns; 13 TeV	25	47%	42%	65%	37%
	51	71%	67%	88%	52%
	76	95%	97%	148%	75%

μ pile-up events

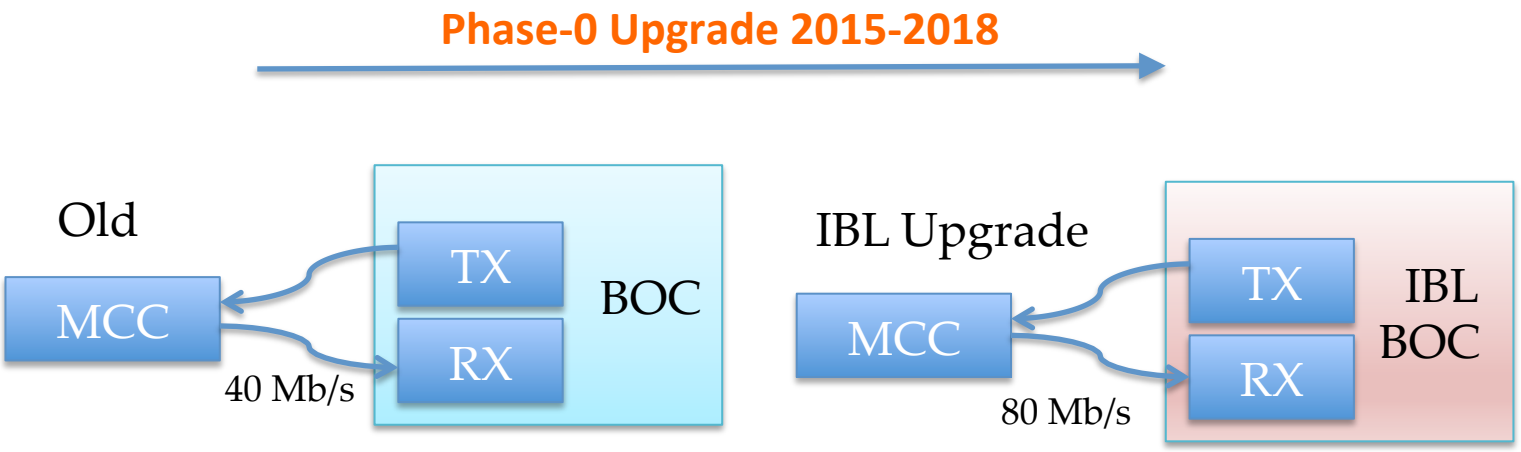
Layer 2 limitations at L=7x10^{33}cm^{-2}s^{-1}

Higher number of desynchronized modules in Layer 2



Layer 2 limitations at $L=7x10^{33}cm^{-2}s^{-1}$

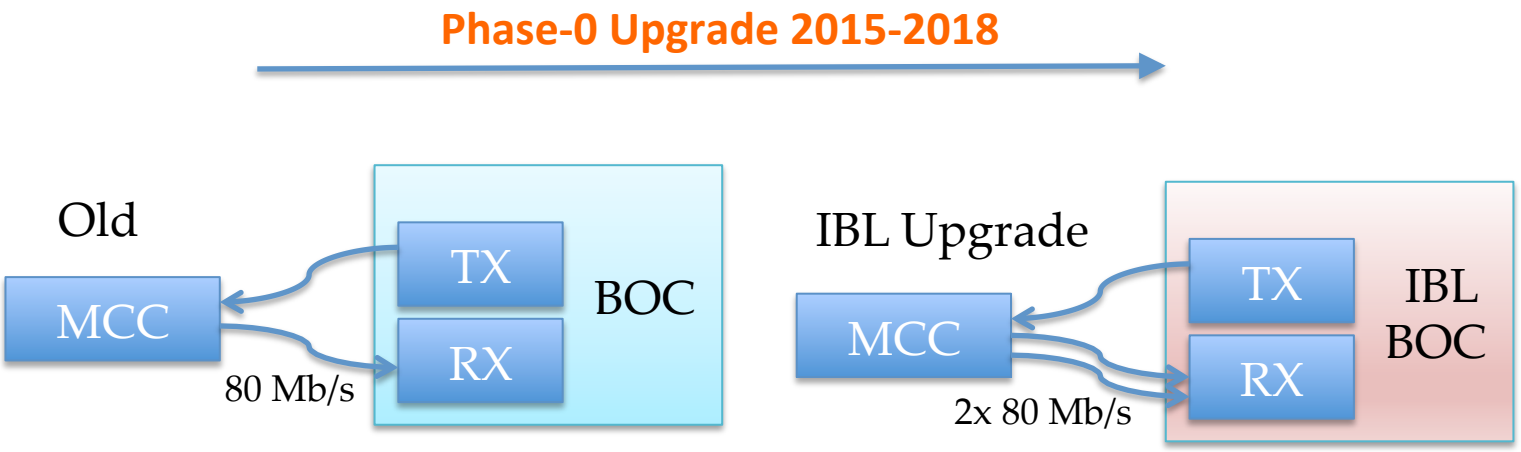
- Bandwidth limitations (@ 40 Mb/s) show up earlier as expected getting worse with increased luminosity
- **Increase link bandwidth to 80 Mb/s**



BOC: Back Of Crate. ROD: ReadOut Driver
MCC: Module Controller Chip

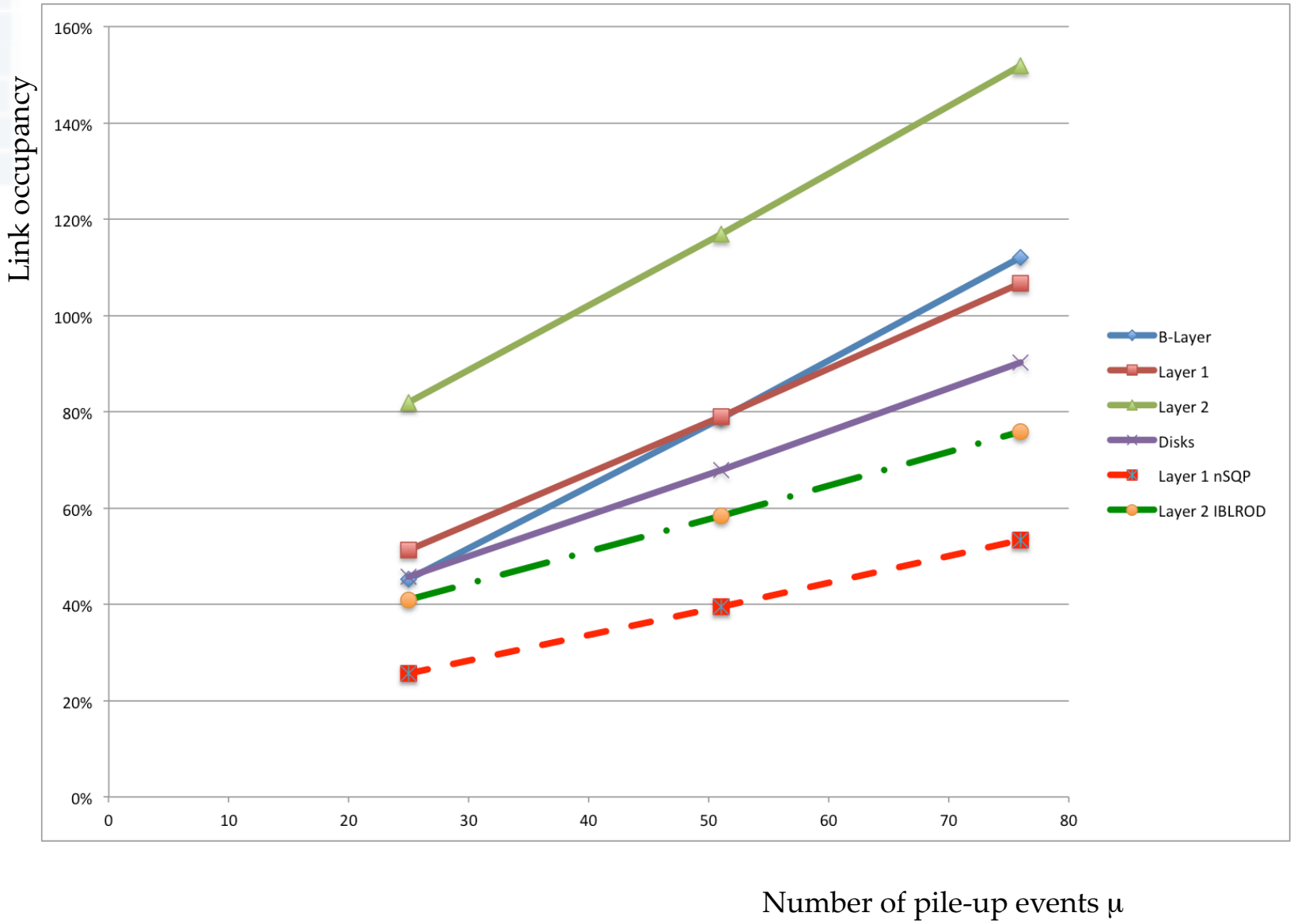
Layer 1 limitations at $L=7x10^{33}cm^{-2}s^{-1}$

- Layer 1 will hit a brick wall later, at ~$2x10^{34}$ luminosity
- Layer 1 is already read out at 80 Mb/s
- **Double the links per module and upgrade the bandwidth to 2x 80 Mb/s**
- The IBL BOC then receives 2 links per module back, same as for the B-Layer right now.



BOC: Back Of Crate. ROD: ReadOut Driver
MCC: Module Controller Chip

Bandwidth limitations MCC-> IBL-ROD



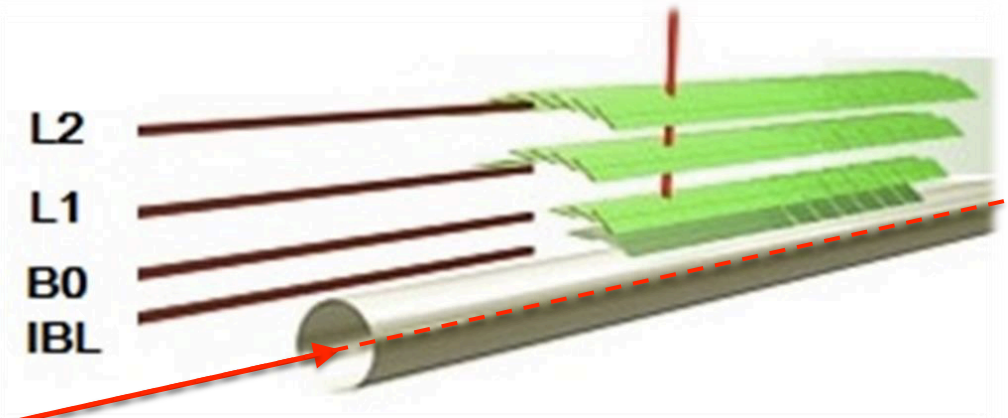
The way out 

- Plan to use the IBL ROD and BOC cards also for the Pixel upgrade to overcome the bandwidth limitations. **Still using VME cards**.
- Firmware of the IBL ROD needs modification to handle the Pixel module data.
- 26 card pairs for Layer2 and 38 card pairs for Layer1.
- **ATLAS CERN identifies:**
  - **Bologna for the IBL-RODs**
  - **Wuppertal for the IBL-BOCs**
- **Base Option**
  - **Same IBL BOC-ROD pairs** with fiber adapters and FW modifications

Bologna activity 2013-2017

Now Taking Data

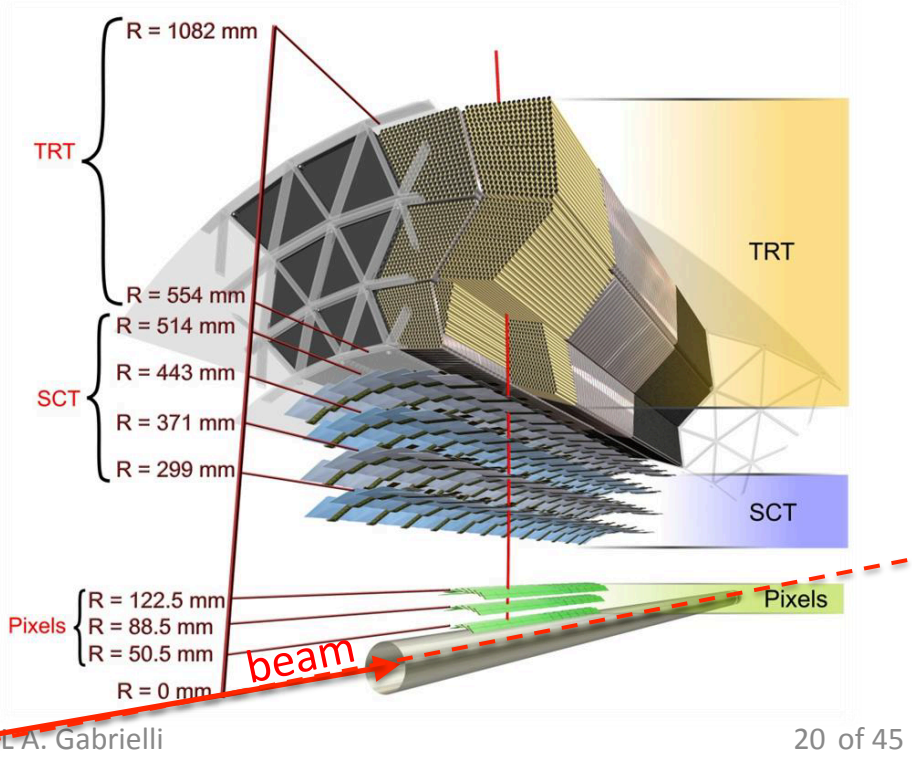
- ✓ **14+1** RODs for IBL (FEI4)
- ✓ **26** RODs for L2
- ✓ **38** RODs for L1



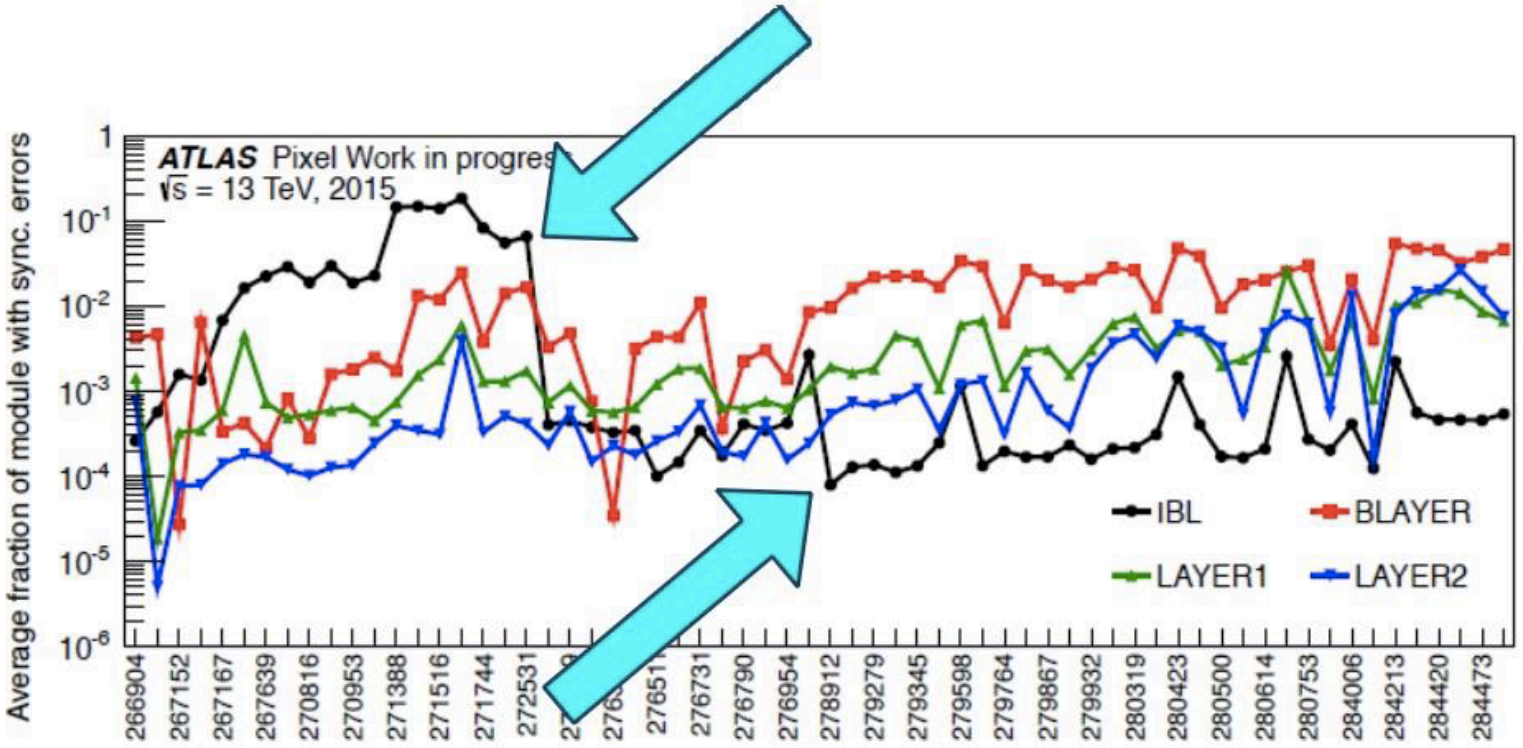
Under Commissioning

- ✓ 12 RODs for Disks
- ✓ 22 RODs for B0

Already Produced and tested



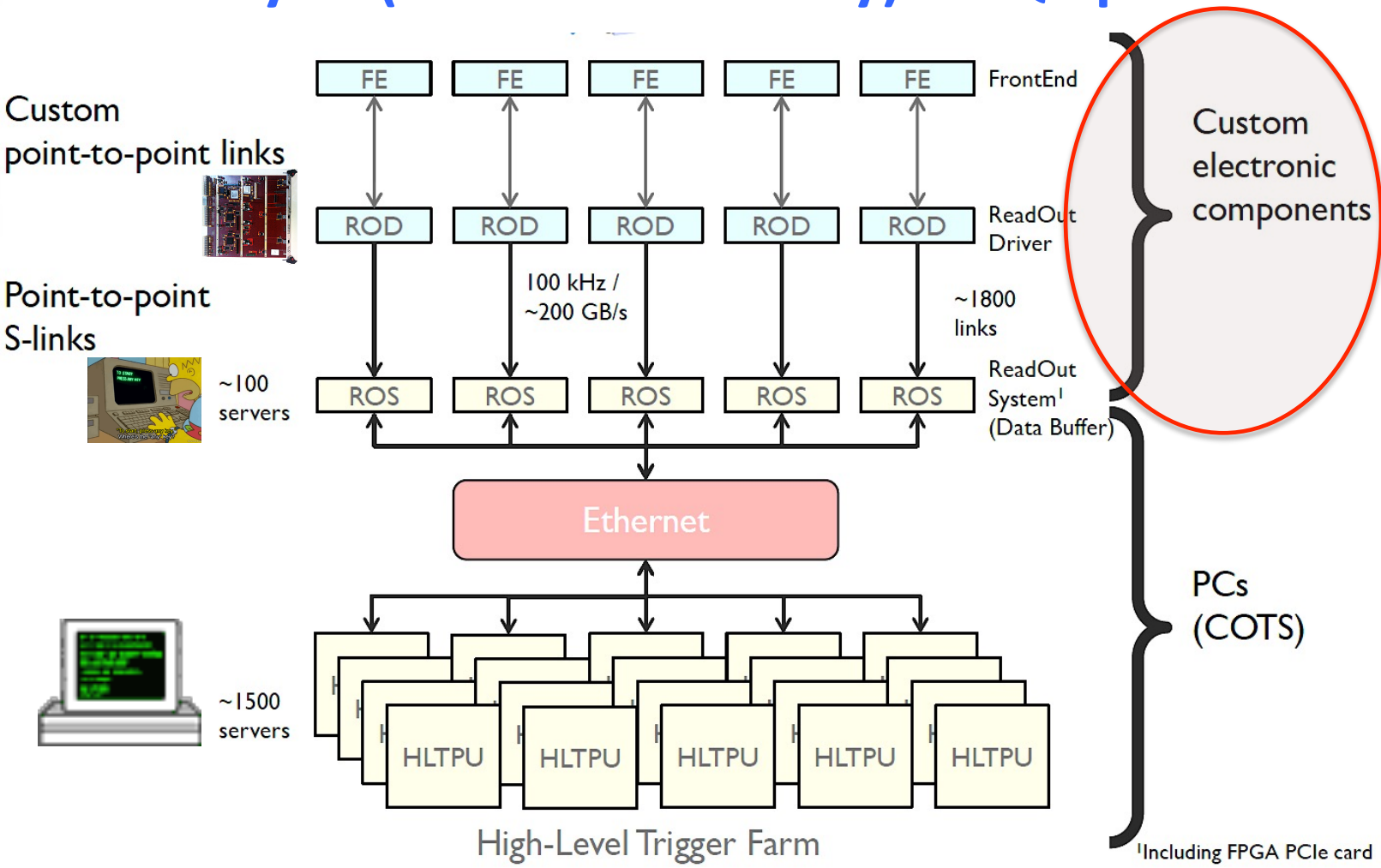
Data Taking at CERN in 2015



- Data Taking in 2015 before and after a firmware tuning on the IBL RODs (black-plot)
- Sync errors goes down and below the other pixel layers that were not yet upgraded

- **The RELEVANCE of the FIRMWARE**

Summary of (Pixel but not only) DAQ up to 2017

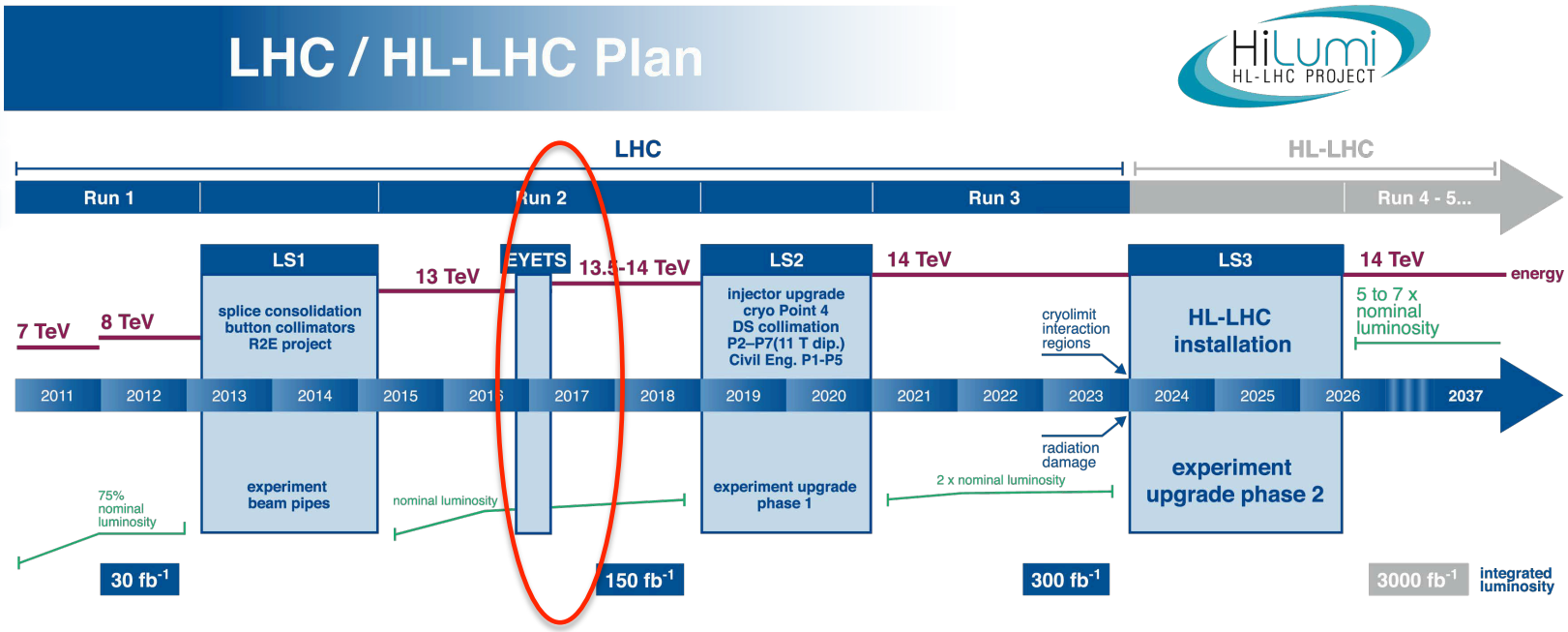


Courtesy of A. Borga

Points to be revised for the Upgrade of Phase-II

- Too much custom electronics
- Too rigid configuration (Detector Dependent)
- ReadOut Driver (ROD) card based on Firmware and Embedded Software

Towards Phase-2 Upgrade



We are here

- LHC Upgrade towards High Luminosity LHC (HL-LHC) in 2024-2026 (**Phase-2**)
- ATLAS will replace the inner detector completely
- New Pixel Front-End electronics
- **Readout architecture and data transmission scheme will also change completely**

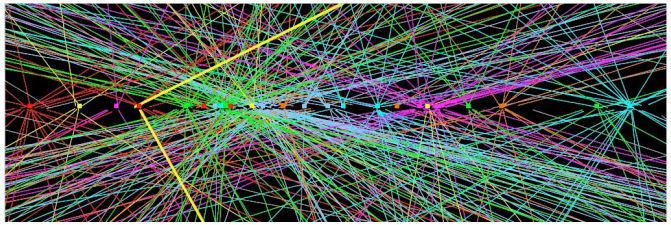
HL: high-Luminosity
LS: long shutdown
EYETS: Extended Year-End Technical Stop

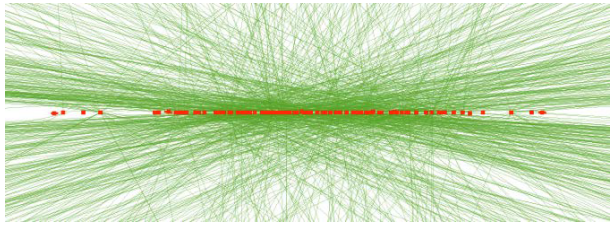
Towards Phase-2 Upgrade

MOTIVATIONS

- LHC will become High Luminosity-LHC to produce 3000 fb^{-1} integrated
- **Instantaneous luminosity increase by factor 5-7** up to $5*10^{34}cm^{-2}s^{-1}$
  - (not only a factor 2 of particle density)
- **Integrated luminosity increase by factor 10** (radiation damage)

LHC: 25 vertices ➟ HL-LHC: 200 vertices





ADVANTAGES vs DRAWBACKS

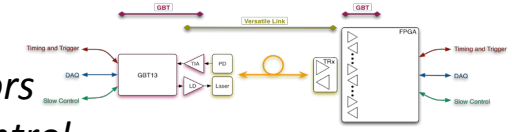
- Higher track density ➟ **better tracking granularity**
- Higher particle flow ➟ higher radiation damage
  - (current components already damaged by 2024)

HL: high-Luminosity
LS: long shutdown
EYETS: Extended Year-End Technical Stop

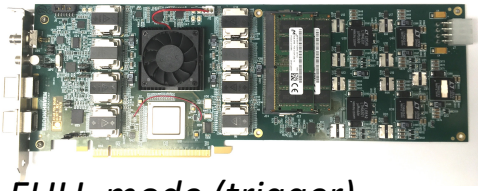
Towards Phase-2 Upgrade

Towards Phase-2 Upgrade, CERN (not only ATLAS) has developed some versatile components:

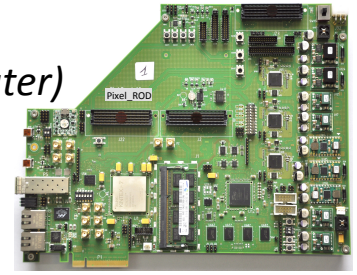
- A high-speed optical rad-hard link (**GBT project**) to interface any "compatible" front-end electronics (see later)
  - *independent from the experiments and the detectors*
  - *can be used for data-taking and front-end slow-control*



- ATLAS has developed the so-called **FELIX project** to upgrade the DAQ electronics
  - *independent from the detectors*
  - *GBT interface capability*
  - *dual operational mode: GBT-mode (data-taking) and FULL-mode (trigger)*

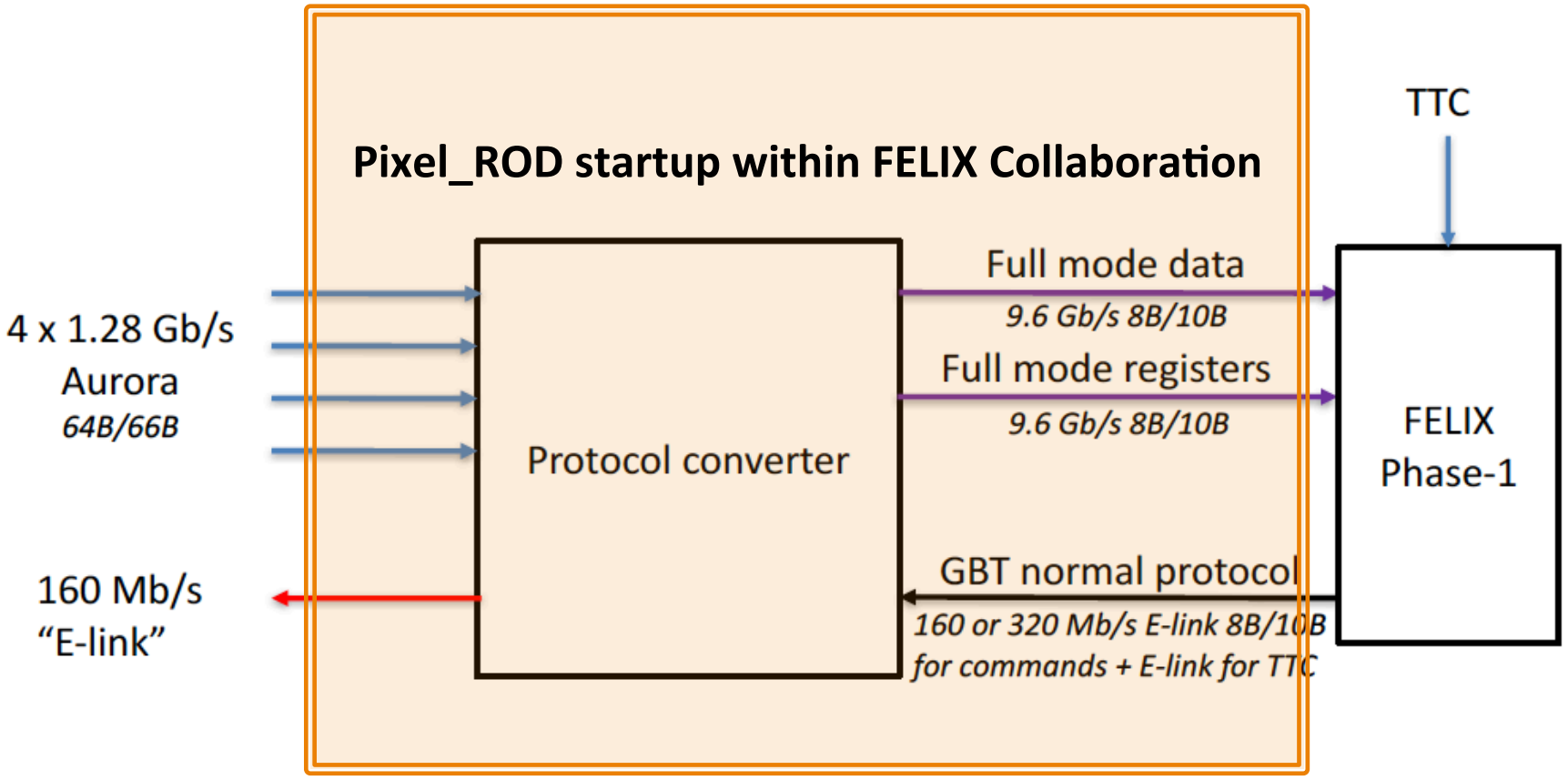


- Bologna, by following the ATLAS IBL ROD experience, has developed a PCI-express card (**Pixel_ROD**), which can be proposed within the FELIX project
  - *PCI-express ver-2 bus, 16 GTX transceivers at 10 Gb/s (see later)*
  - *GBT interface capability*

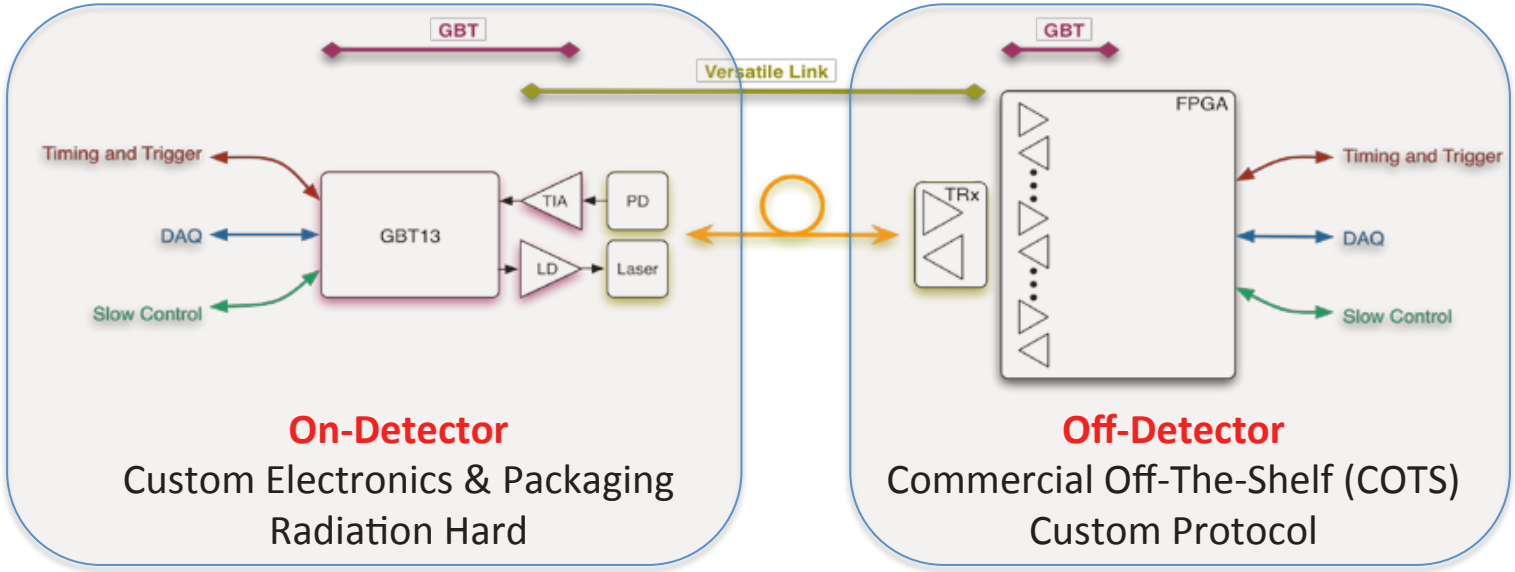


Case Study

This is a first proposal about how to integrate the Pixel_ROD board within the FELIX Collaboration: some tests already carried out (see later)



The GBT Project



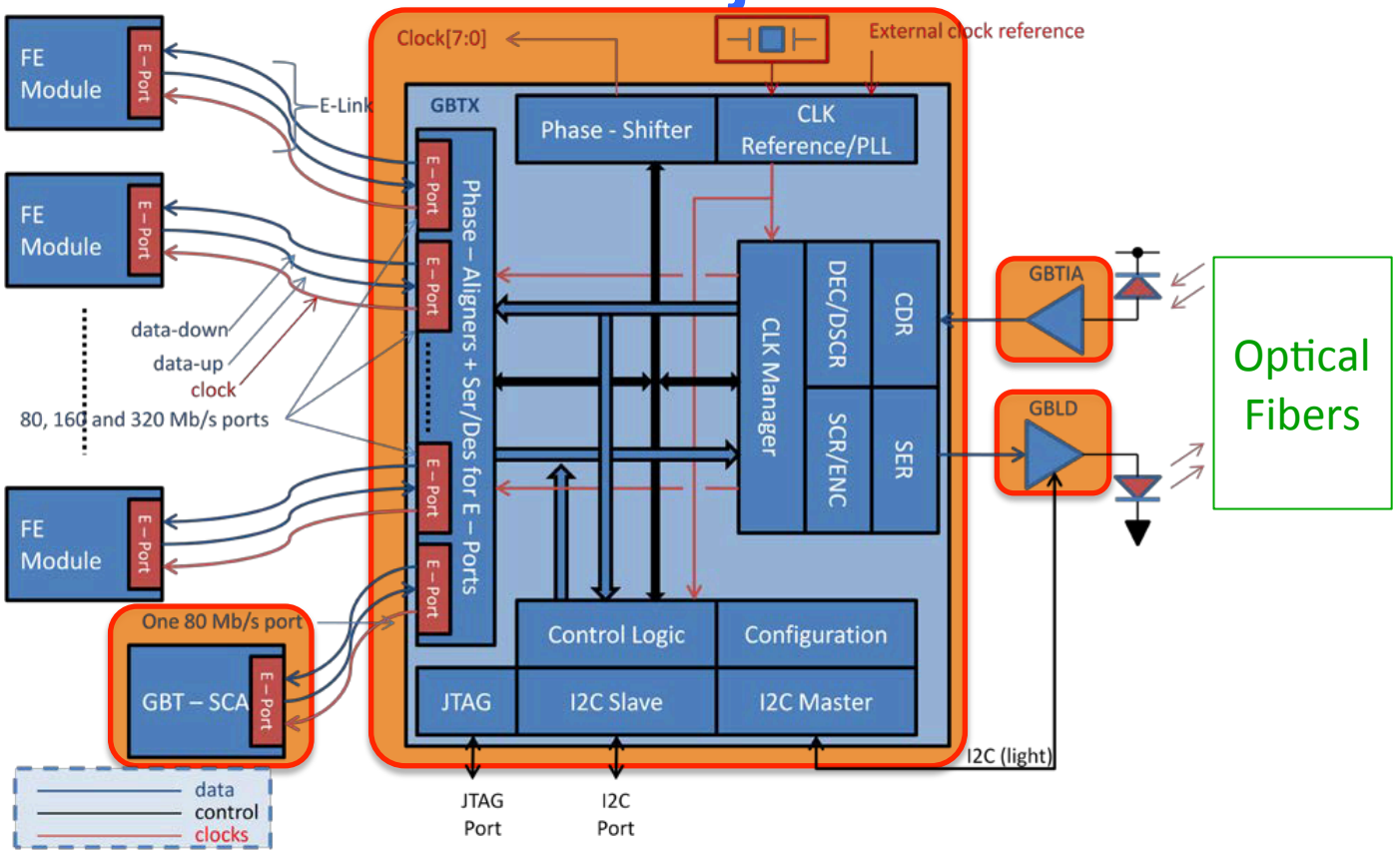
GBT (GigaBit Transceiver)

Optical link independent from the detector (type of Front-End)

- The **GBTx** (GBT13) is a radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links for high-energy physics experiments
- Logically the link provides three "distinct" data paths for **Timing and Trigger Control** (TTC), **Data Acquisition** (DAQ) and **Slow Control** (SC) information
- The link establishes a **point-to-point**, optical, **bidirectional**, constant latency **connection** that can function with very high reliability in the harsh radiation environment typical of high energy physics experiments at LHC

PD: Pin Diode LD: Laser Driver
TIA: Trans Impedence Amplifier

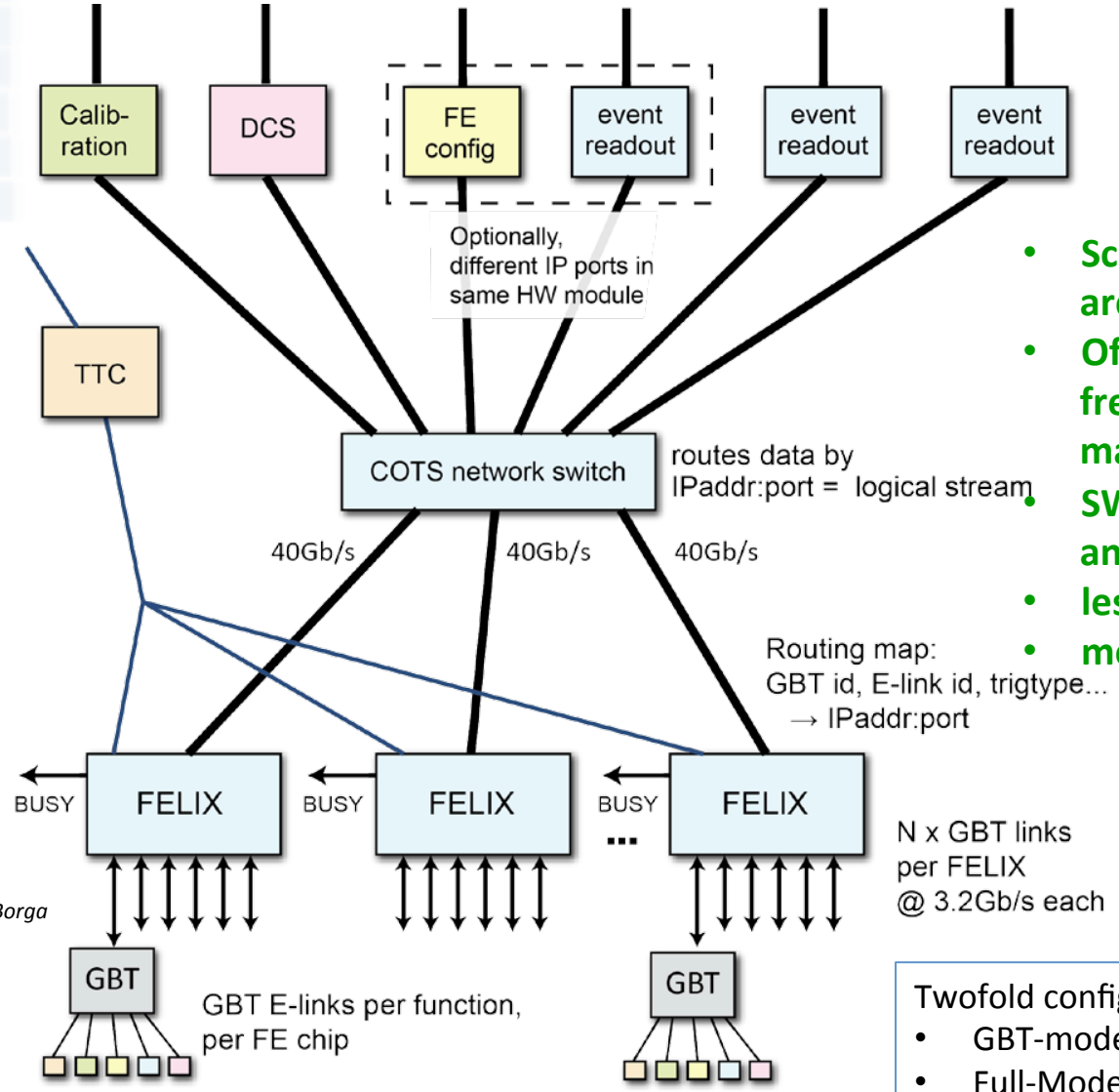
The GBT Project



The GBTx ASIC is part of the GBT chipset composed of the following **4 chips**:

- a **Trans-Impedance Amplifier** for the optical receiver (**GBTIA**)
- a **Laser Driver** (**GBLD**) [2]
- a **Slow Control Adapter** ASIC (**GBT-SCA**)
- and the **GBTx** link ASIC that implements all the needed functions of the data and timing transceiver.

The FrontEnd LInk eXchange (FELIX) topology



Courtesy of A. Borga

- **Scalable bidirectional architecture**
- **Off-detector end-points set free from point-to-point mapping of FE GBTs**
- **SW based data processors and handlers**
- **less custom electronics**
- **more COTS components**

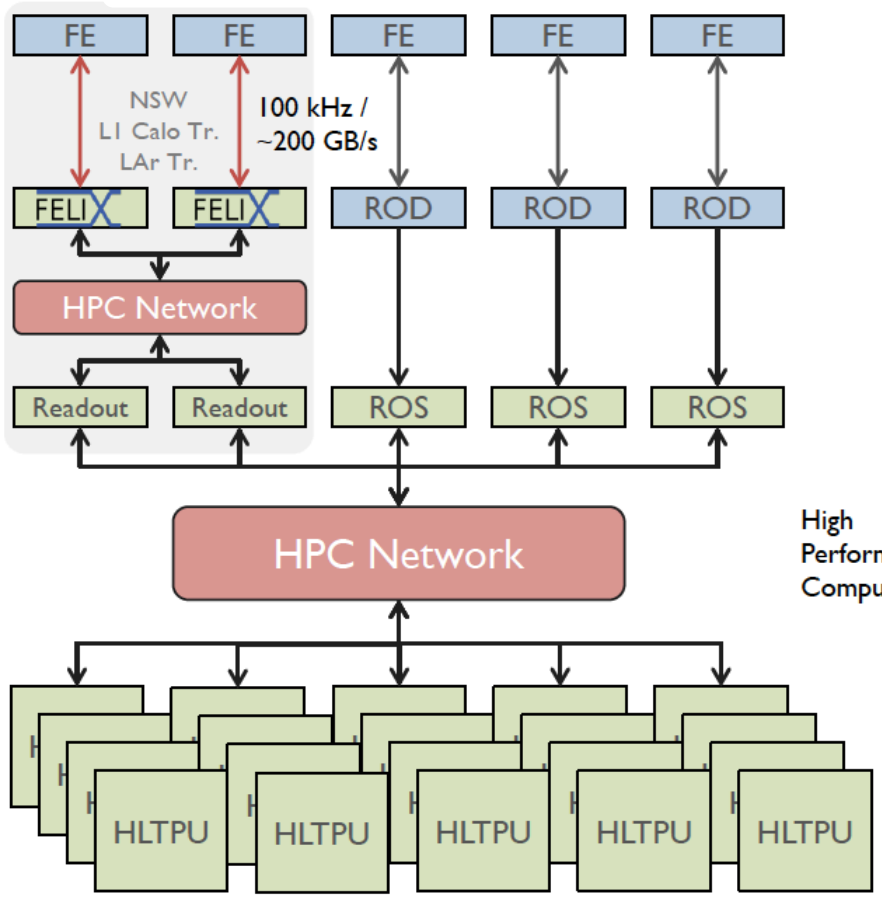
Twofold configuration for the FELIX
- GBT-mode FELIX
- Full-Mode FELIX

The FrontEnd LInk eXchange (FELIX) topology

Optical links / GBT protocol (FPGA – FPGA links in service cavern: S-link like protocol for data transfers to FELIX)

PCs

Multi Gb Ethernet



Courtesy of A. Borga

First Phase-I Upgrade using the FELIX (FLX-711) ← (GBT-mode FELIX configuration)

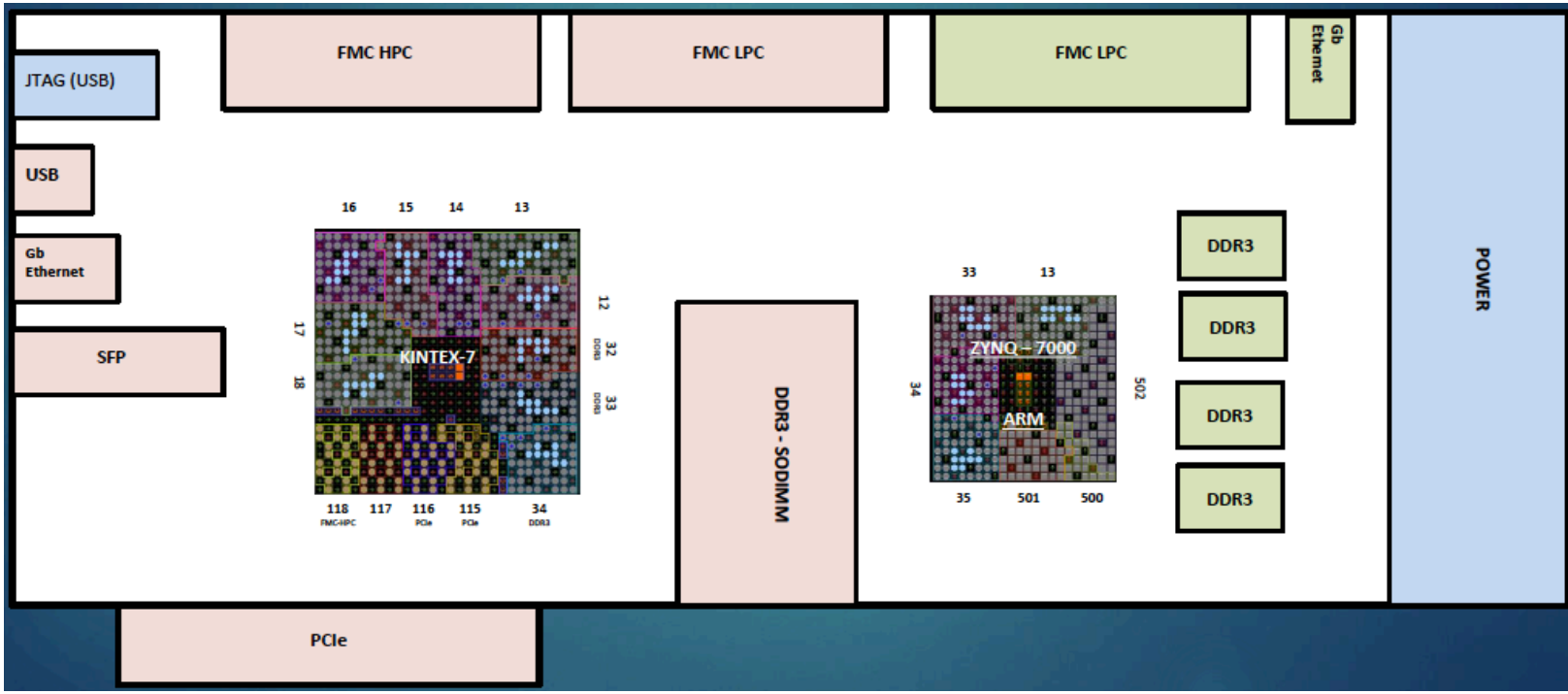
- **New Small Wheel muon end-cap chambers** ← (GBT-mode FELIX configuration)
- **Liquid Argon Calorimeters L1 calo trigger** ← (Full-Mode FELIX configuration)

Bologna challenge towards Phase-2

- In summary FELIX is a PC based DAQ system designed for bridging custom links (GBT) to a COTS computer network
- *Bologna is interested in joining the FELIX project to:*
  - *Profit from the experience and what learned from the IBL project*
  - *Profit from the HW, SW and FW tools developed in the recent years*
  - *Invest beyond Phase-0 and Phase-1 upgrade, towards Phase-2*

Bologna: Pixel_ROD design parameters

Device	Expected Performance
GBT	9,6 Gbps
PCIe	Minimum 2 Gbps per lane
Gb Ethernet	125 MHz
FMC	165 MHz

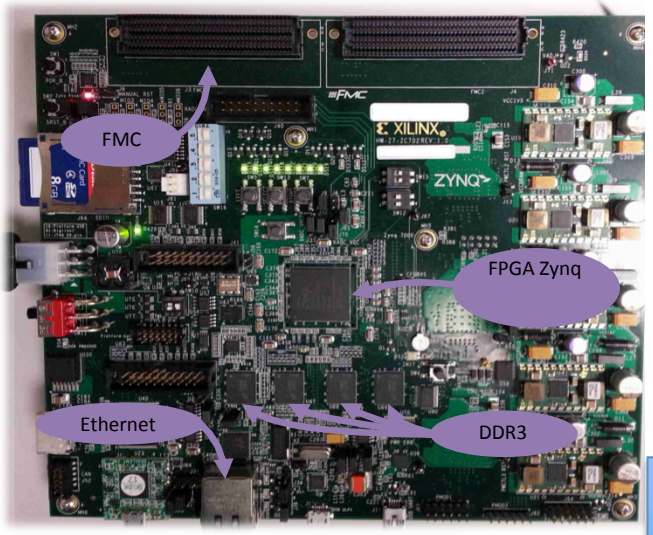


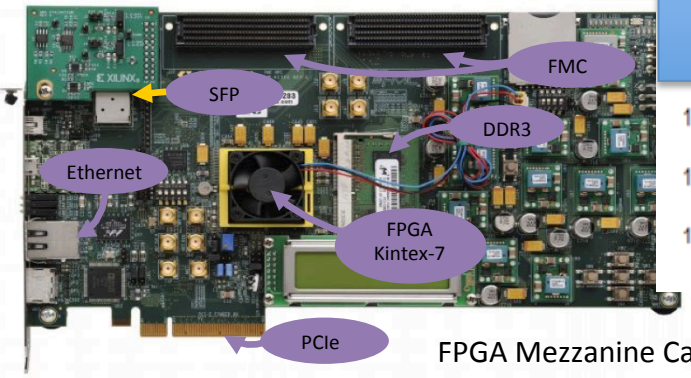
Low Pin Count (LPC)
High Pin Count (HPC)

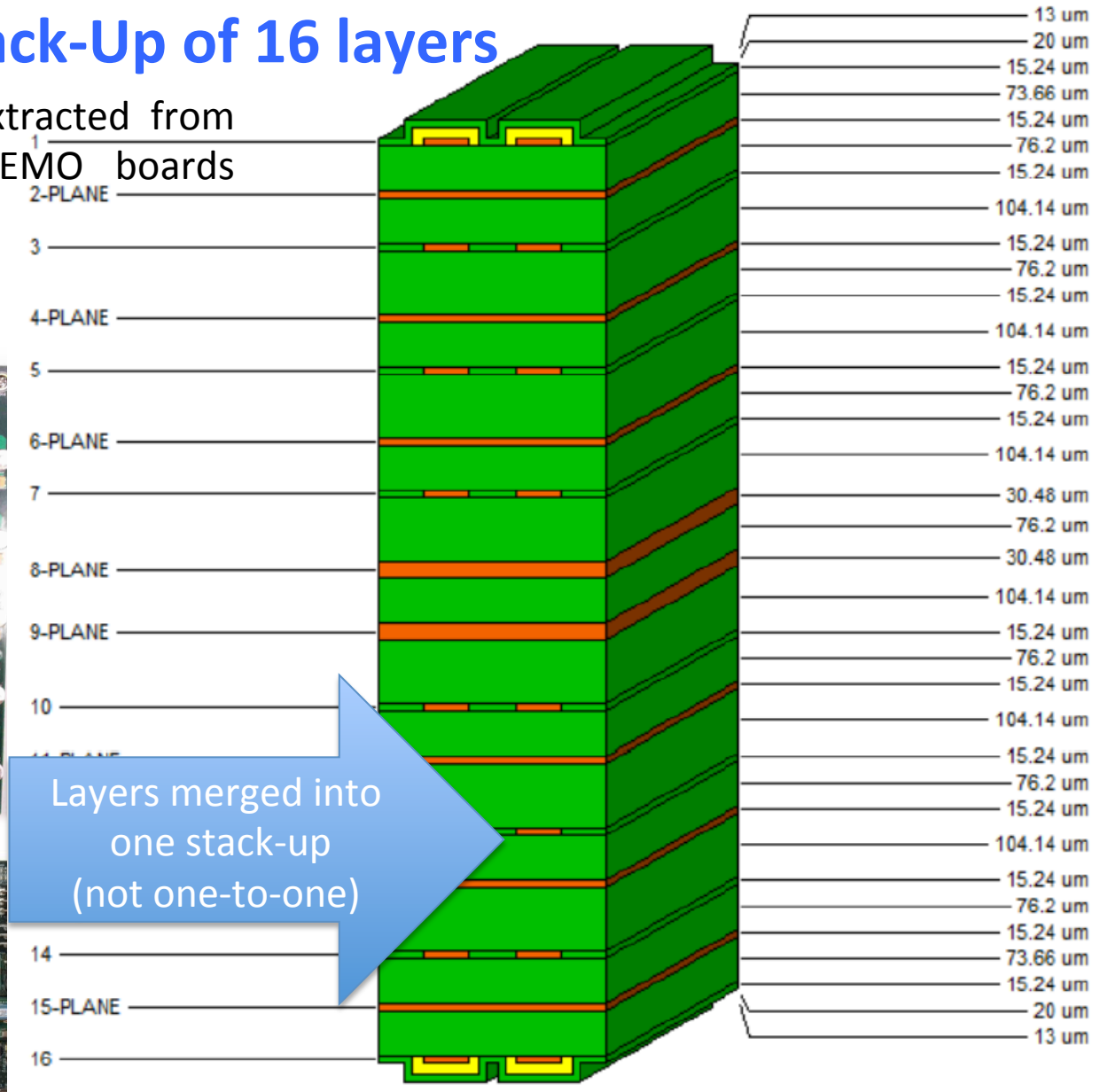
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)

PCB Stack-Up of 16 layers

Constraints extracted from two Xilinx DEMO boards KC705-ZC702



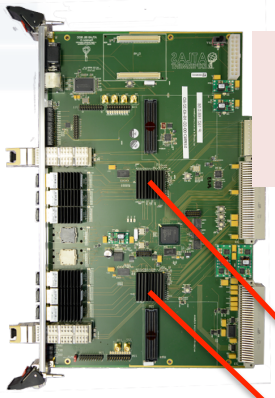




Layers merged into one stack-up (not one-to-one)

FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)

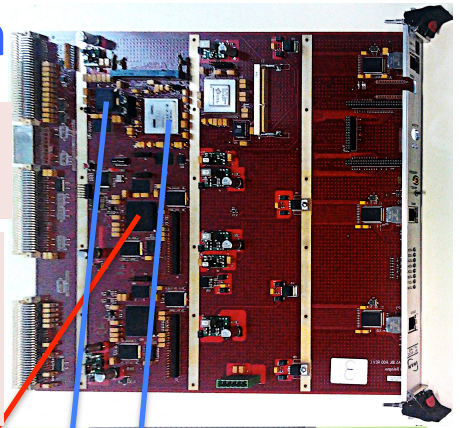
Pixel_ROD Design
(new board w.r.t. current IBL DAQ chain

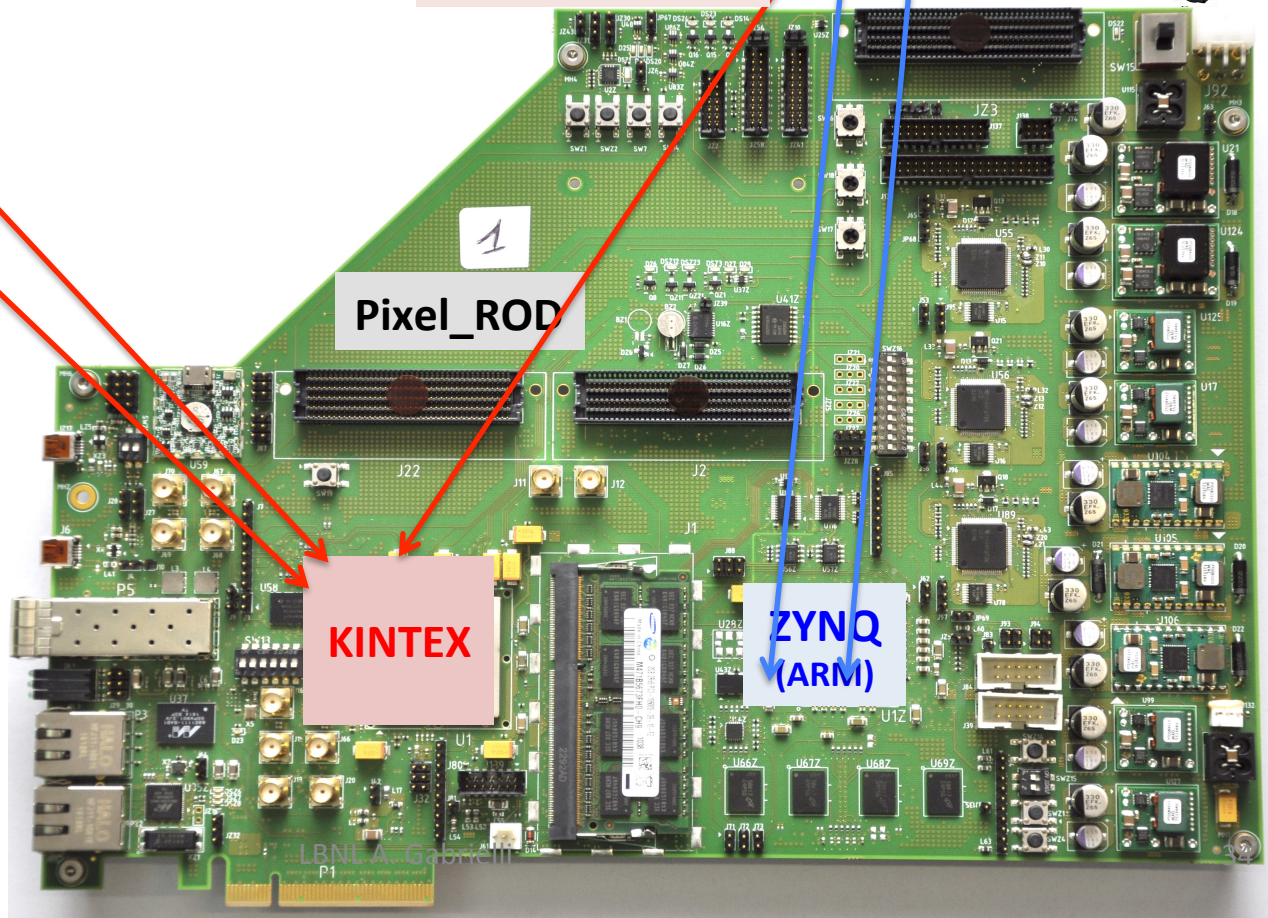


Current IBL BOC
1 x BMF out of 2
1 x BCF

Current IBL ROD
1 x SLAVE out of 2

IBL ROD
1 x MASTER
PPC → ARM
1 x PRM



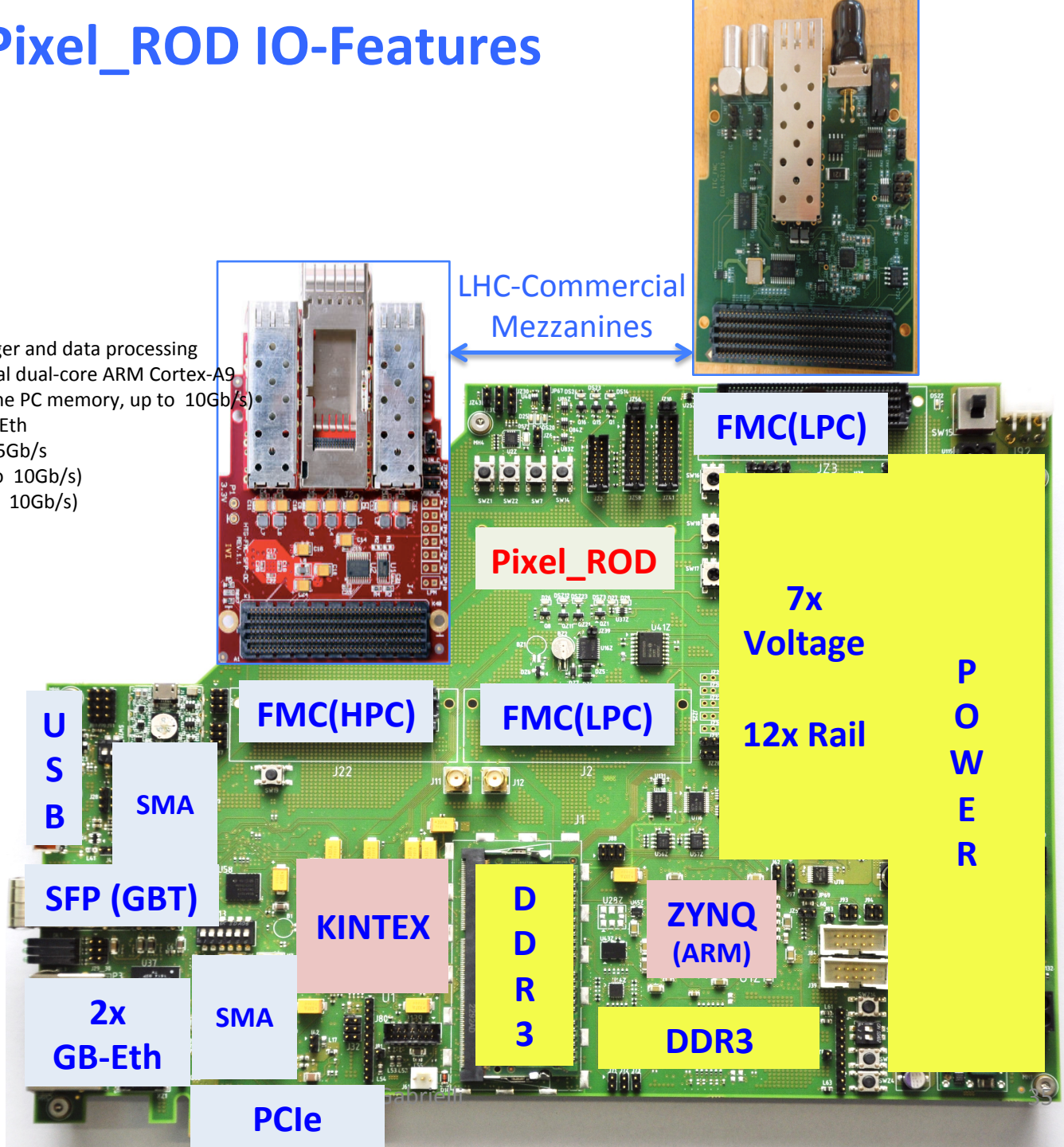


1 Pixel_ROD can interface up to 16 equivalent FEI4 channels as half of the 32 channels of the BOC-ROD pair

Pixel_ROD IO-Features

- 7-series Xilinx® FPGAs
  - ✓ Kintex7 XC7K325T-2FFG900C;for trigger and data processing
  - ✓ Zynq XC7Z020-1CLG484C with physical dual-core ARM Cortex-A9
- 1 x PCIe Express Gen2 8x-lane (2Gb/s min to the PC memory, up to 10Gb/s)
- 16 x GTX@ 12.5Gb/s on PCIe, SFP, SMA, FMC, Eth
  - ✓ 1 x SFP 10-Gb/s link (GBTx) tested at 5Gb/s
  - ✓ 1 x HPC (400-pin) HS diff lines (4 up to 10Gb/s)
  - ✓ 2 x LPC (160-pin) HS diff lines (1 up to 10Gb/s)
  - ✓ DDR3 2GB x 667 MHz (kintex)
  - ✓ DDR3 1GB x 667 MHz (Zynq)
  - ✓ 2 x GB/Eth (1 up to 10Gb/s)
  - ✓ 2 x USB JTAG
  - ✓ 2 x SMA (1 up to 10Gb/s)

- **2 Boards Fabricated**

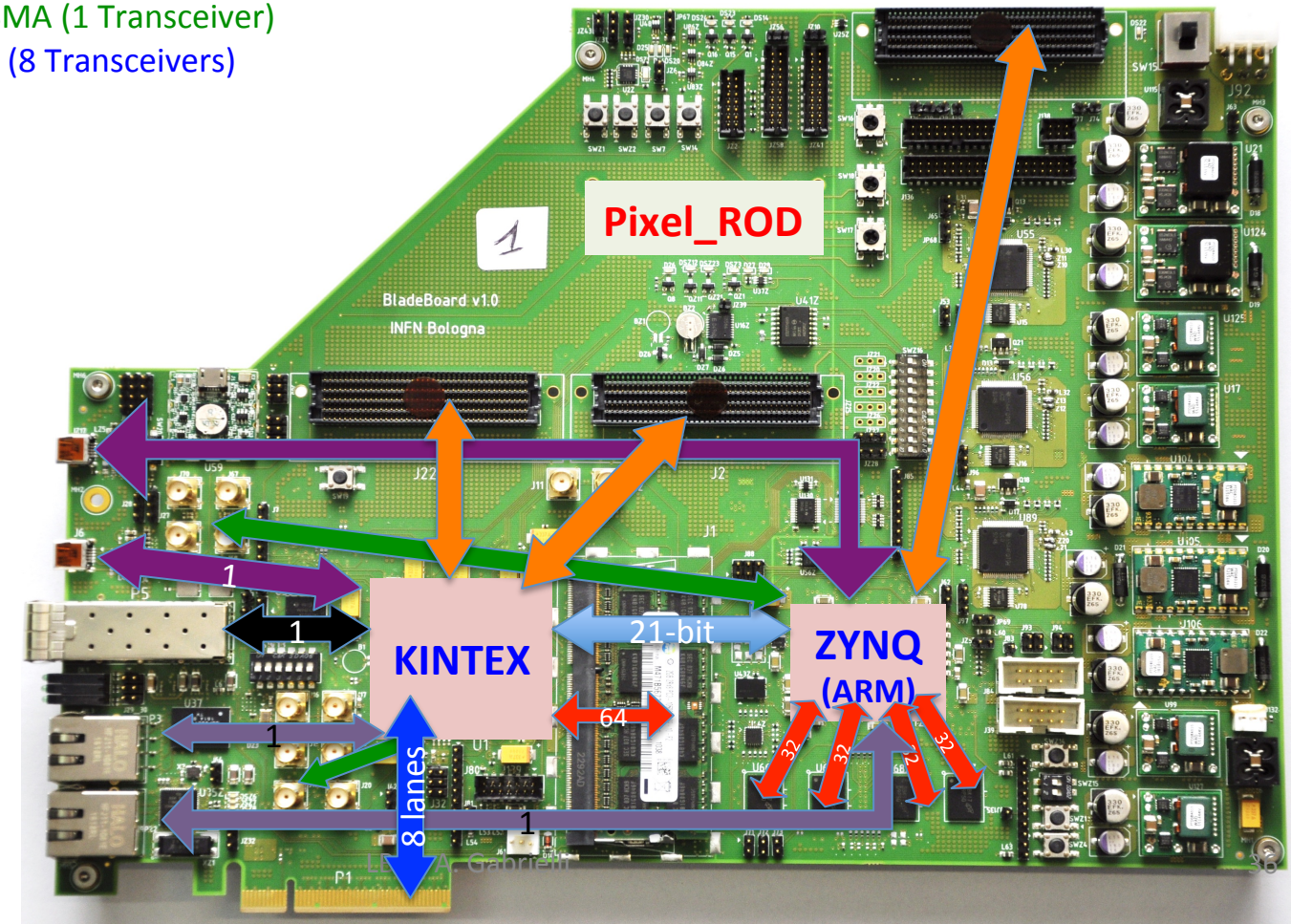


Low Pin Count (LPC)
High Pin Count (HPC)
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)
SubMiniature version A (SMA)

Pixel_ROD Buses

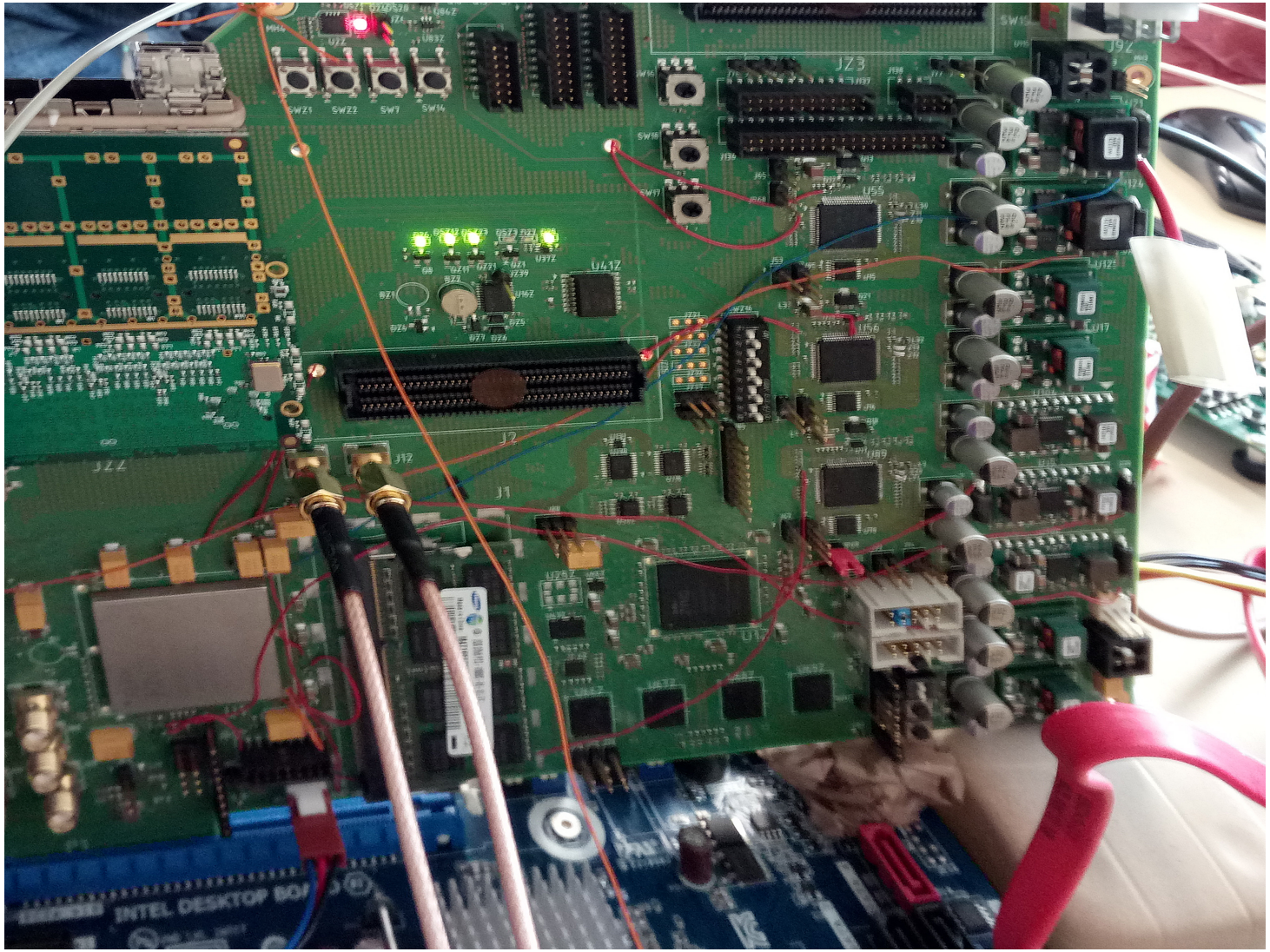
7-series Xilinx FPGAs

- ✓ Kintex7 to Zynq bus 21-bit differential bus
- ✓ 32-bit / 64-bit DDR3 differential buses
- ✓ SFP diff bus (1 Transceiver)
- ✓ 2x ETH diff buses (1 Transceiver)
- ✓ FMC (HPC) diff buses (4 Transceivers)
- ✓ FMC (LPC) diff bus (1 Transceiver)
- ✓ 2 x UART buses
- ✓ 2 x SMA (1 Transceiver)
- ✓ PCIe (8 Transceivers)

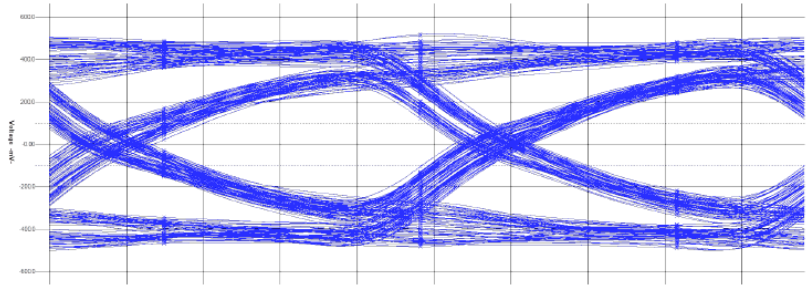


Low Pin Count (LPC)
High Pin Count (HPC)
FPGA Mezzanine Card (FMC)
small form-factor pluggable (SFP)
SubMiniature version A (SMA)

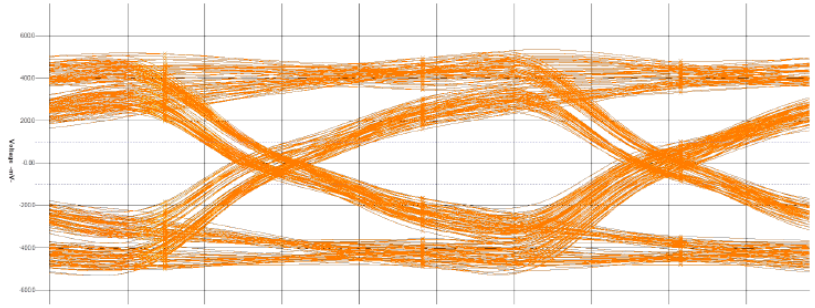
"Patched" boards under test



Test GBT (1)



(a) TX



(b) RX

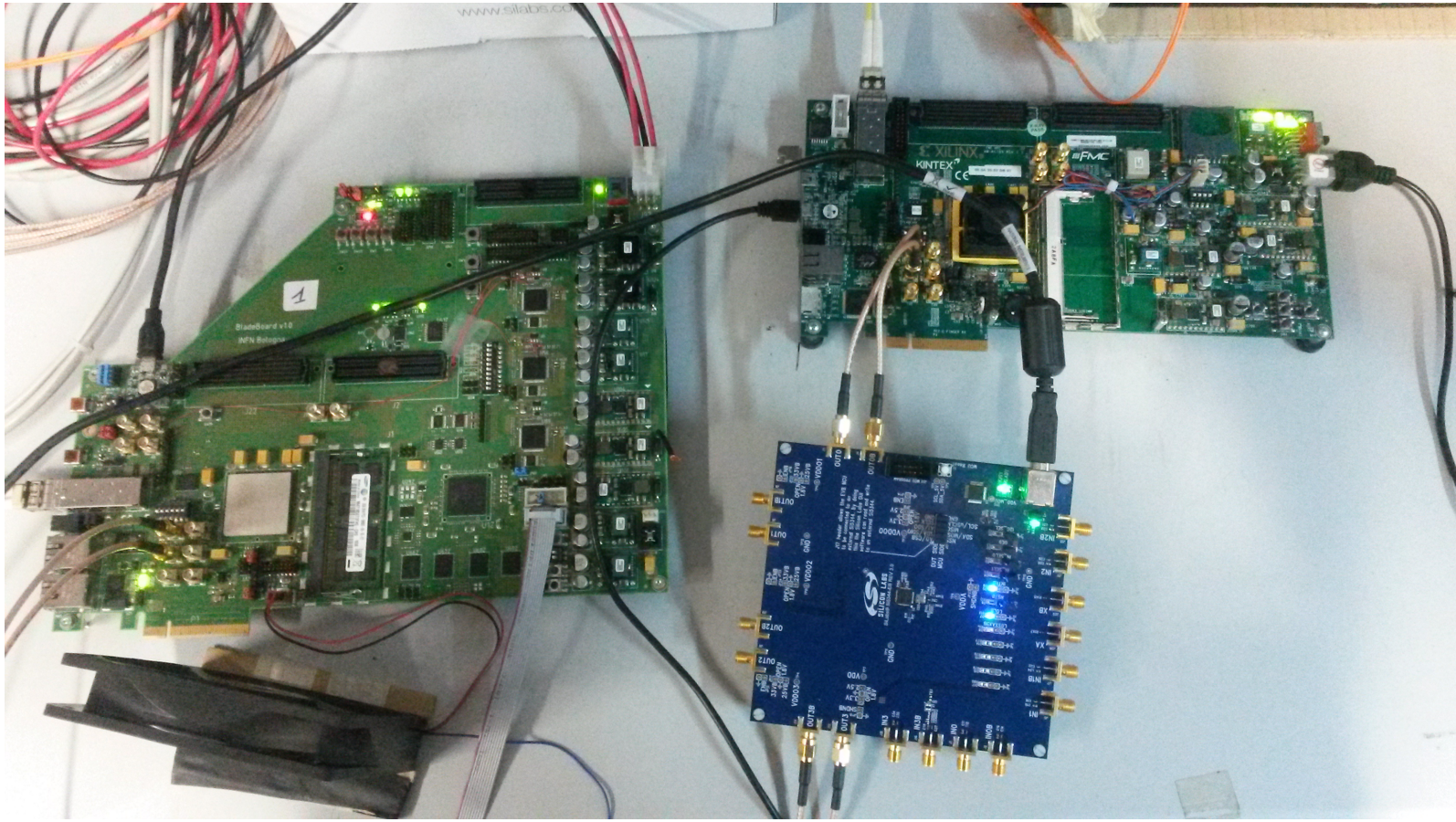
- GBTx 10 Gb/s simulation

- **Actual Link** between
  - Pixel-ROD
  - Xilinx demo-board KC705 using **firmware GBT-FPGA (CERN)**
- The two boards communicate at **4.8 Gb/s**.

- Test performed on both Pixel_ROD boards

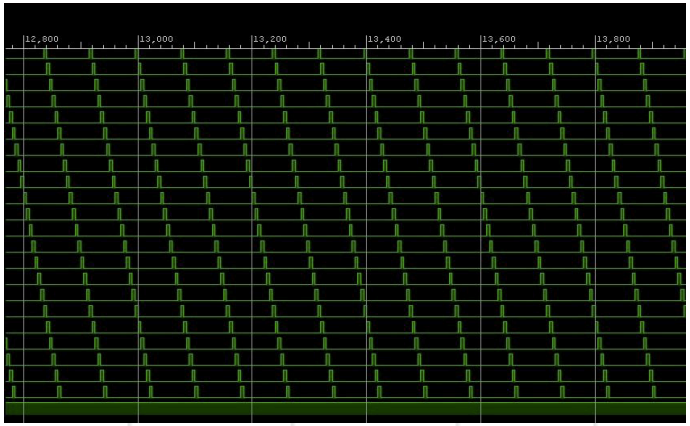
Test GBT (2)

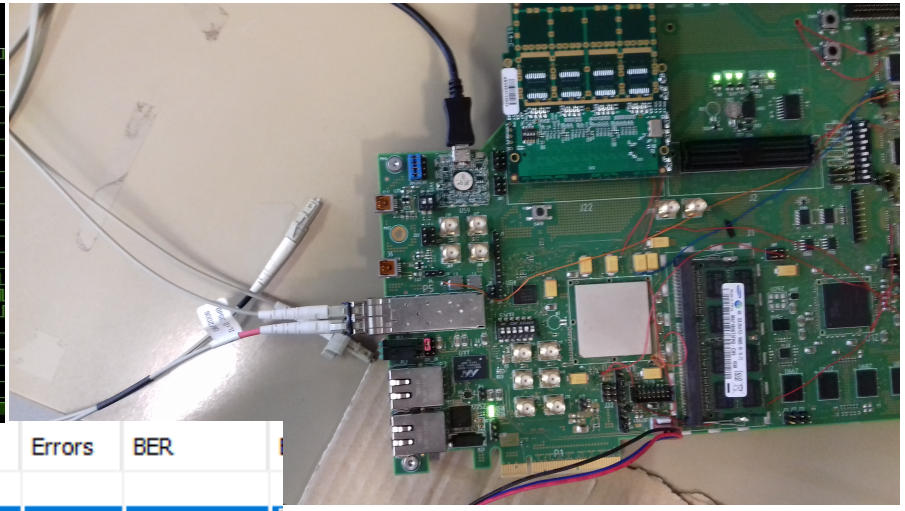
Actual link at 4.8 Gb/s with the GBTx ASIC on an ALICE TOF board



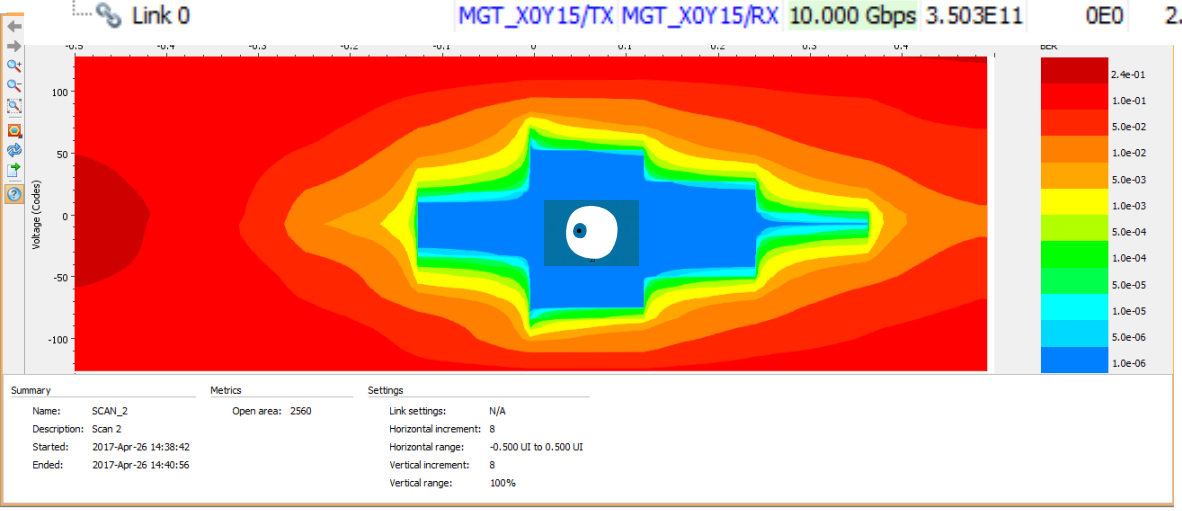
Transceiver Tests

Walking 1s test in loopback on **SFP** connector at 4.8 Gb/s with **BER ≈ 10^{-12}**





Name	TX	RX	Status	Bits	Errors	BER
Ungrouped Links (0)						
FMS14 Loopback Pixel Rod (1)						
Link 0	MGT_X0Y15/TX	MGT_X0Y15/RX	10.000 Gbps	3.503E11	0E0	2.855E-12



Eye diagram in loopback test on (HDC) **FMC** connector at:

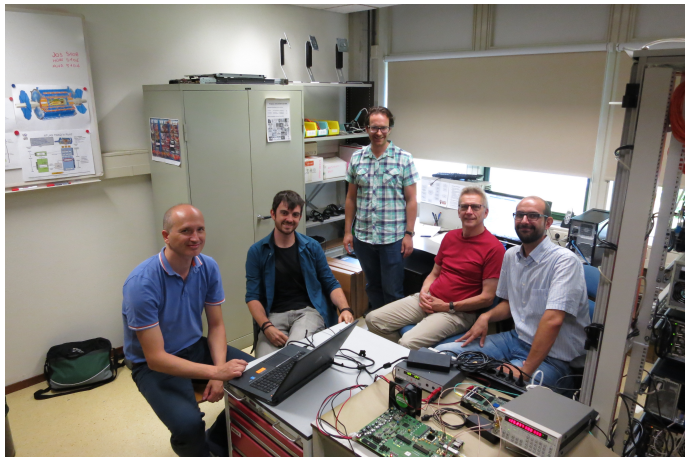
- **10 Gb/s, BER ≈ 10^{-11}**

Pixel_ROD integration test with Mini-Felix

Presentation of the current status within one of the next FELIX developers meetings

- **Current status (NIKHEF July 2017)**
  - Bologna is able to run the:
    - **Aurora** (64b/66b) protocol in **Duplex** mode: (4 lanes at 1.28 Gbps) in loopback only
    - **Aurora** (64b/66b) protocol in **Simplex** and **Duplex** mode: (1 lane at 5.12 Gbps)
    - Communication to FELIX in **GBT** mode: (4.8 Gbps)
    - Communication to FELIX in **Duplex mode** (custom protocol): (9.6 Gbps): ≈ 100 Gbyte of data transmitted in 100 s at NIKHEF on July 2017
- **Next steps**
  - 5 new Pixel_RODs are under construction: estimated delivery by Oct/Nov 2017
  - Presentation of the current status within one of the next meetings
    - (tentative schedule Sep. 18-23 2017)
  - We present a Poster at TWEPP-11 in Santa Cruz to introduce the Pixel_ROD board and the status of the art and the international community

Pixel_ROD integration test with Mini-Felix

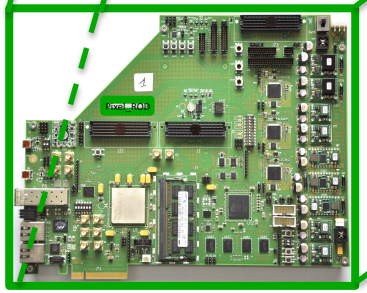


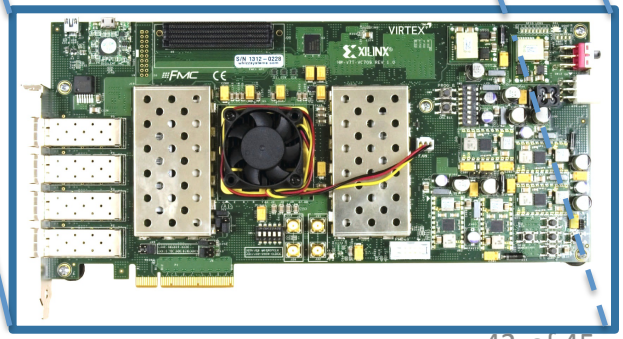
Stand-Alone Pixel_ROD running:
- GBT-FPGA protocol
- FELIX FULL-mode

Full Mode @ 9.6 Gbps
GBT Mode @ 4.8 Gbps

Mini-FELIX
Xilinx VC-709 kit

FELIX PC





Future workplan and tests in Bologna

SOME FUTURE PLANS

DAQ demo readout chain by designing :

- ✓ a Pixel_ROD FM version compatible to what currently used in the ATLAS Pixel detector, for any layer
- ✓ an emulated data-taking using the high-speed lines of the PCIe and FMC connectors, being compatible with RD53A and FEI4 data formats
- ✓ a fully compatible FW to cope with Aurora and GBT protocols

and within the DAQ community we are working to make available:

- ✓ ***A 4 x 1.28Gb/s Aurora protocol RD53 emulated data, concatenated to 1 x 5.12 GB/s again to be interfaced to the Felix card***
- ✓ ***A complete behavioural emulator of the next RD53A chip under submission***

By Summer-Fall 2017 the tests will be completed with a new batch of (patched) 5 boards

Thank you !!

Backup slides