The RD53A Pixel Readout Chip

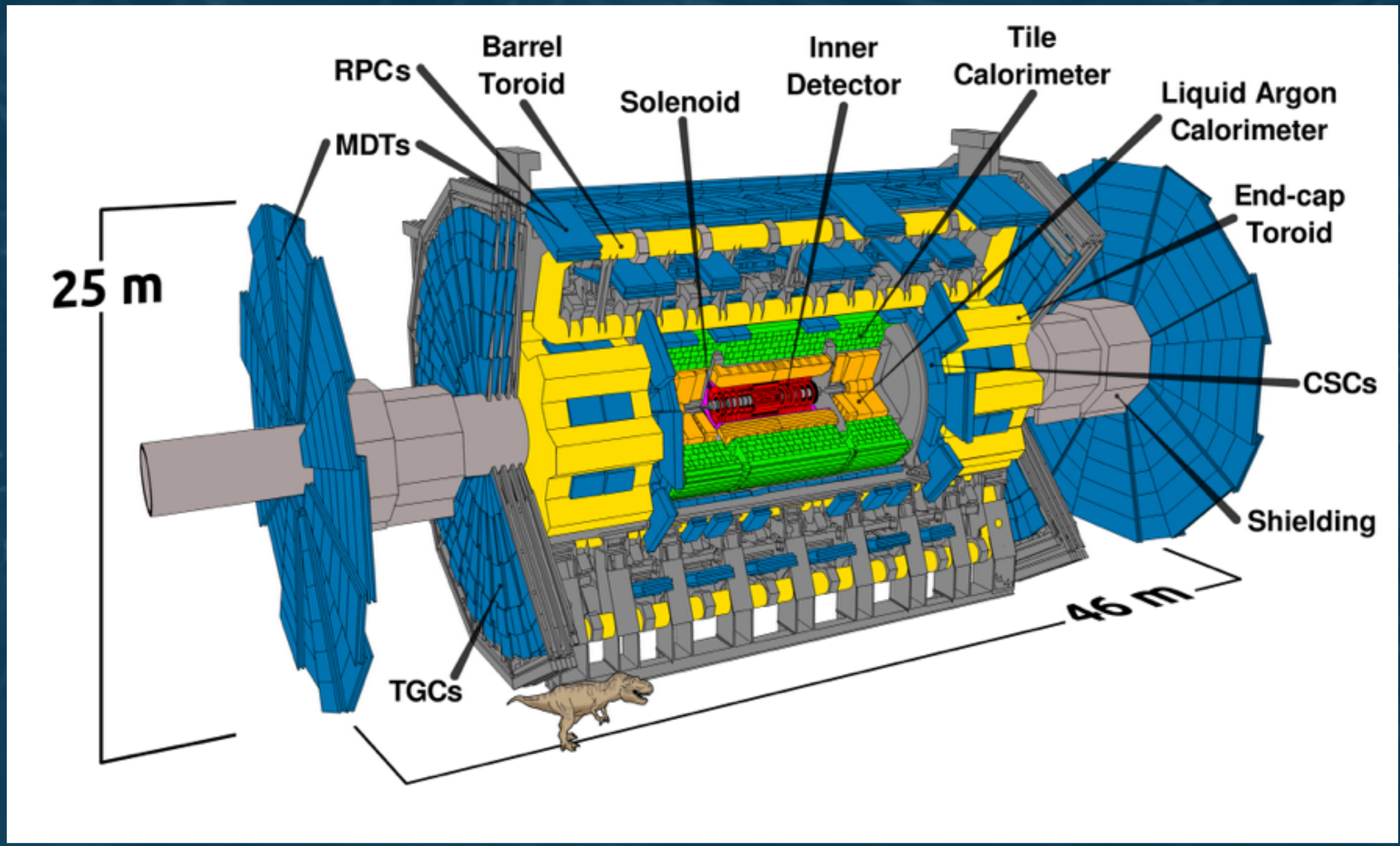
Instrumentation Brownbag
08/16/17

Timon Heim - LBNL

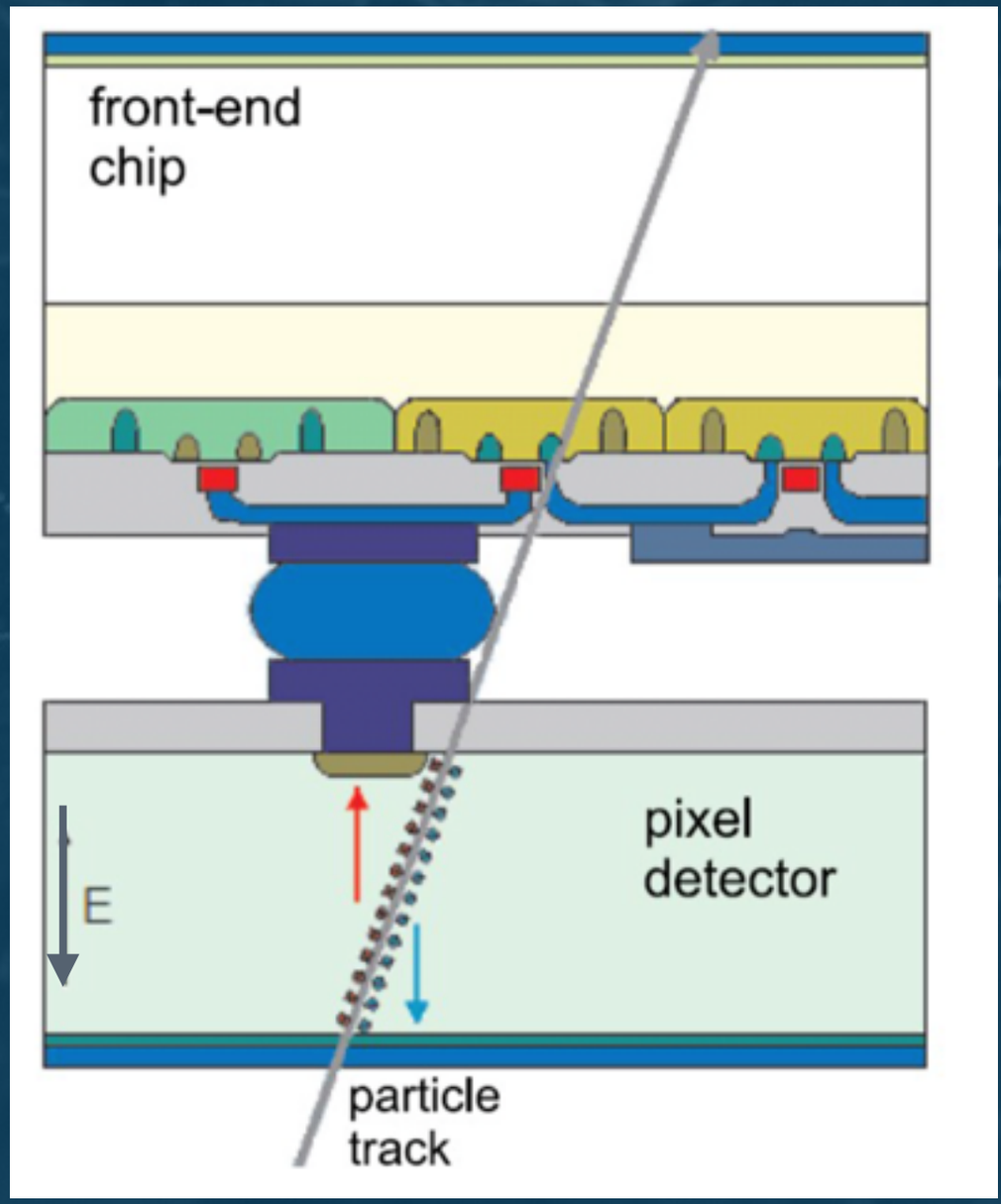
Outline

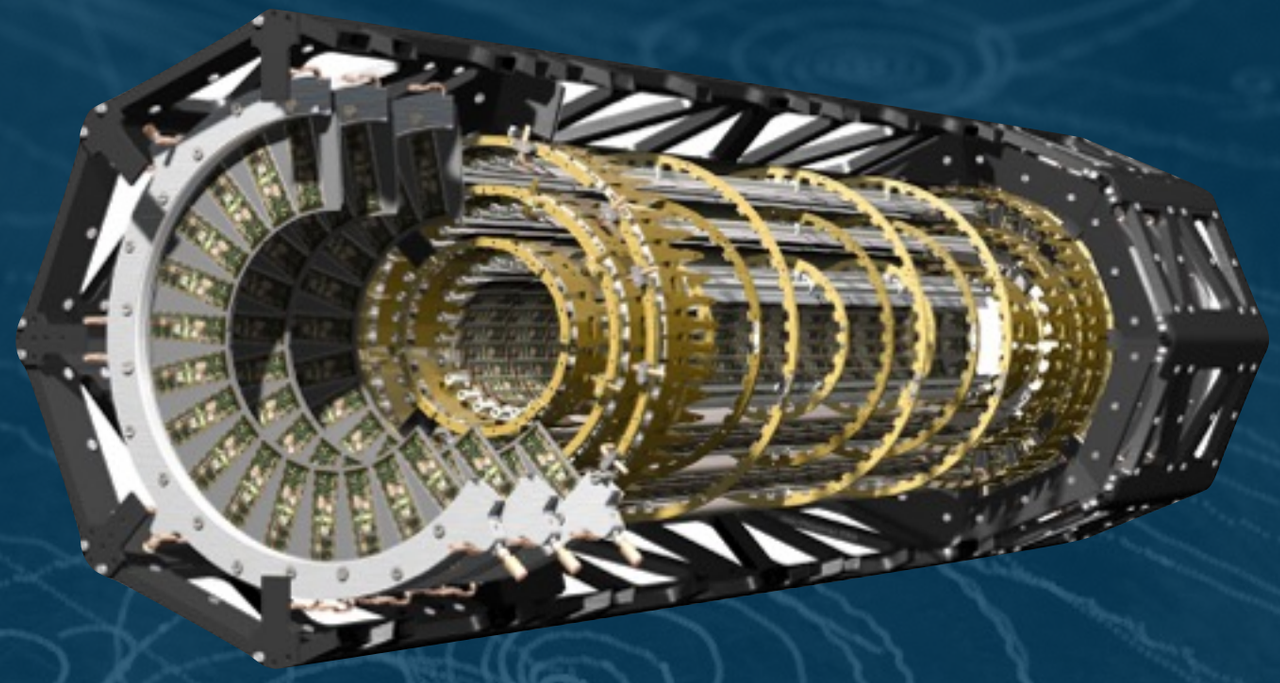
- ATLAS experiment and its Phase-2 upgrade in a nutshell
- RD53 collaboration and LBNL contribution
- Radiation tolerance of 65nm technology
- The RD53A demonstrator
  - Overview
  - Analog front-ends and results from test chips
  - Digital architecture
  - *New* features
- Preparations for testing
- Conclusion and Outlook

ATLAS Experiment



ATLAS Pixel Detector





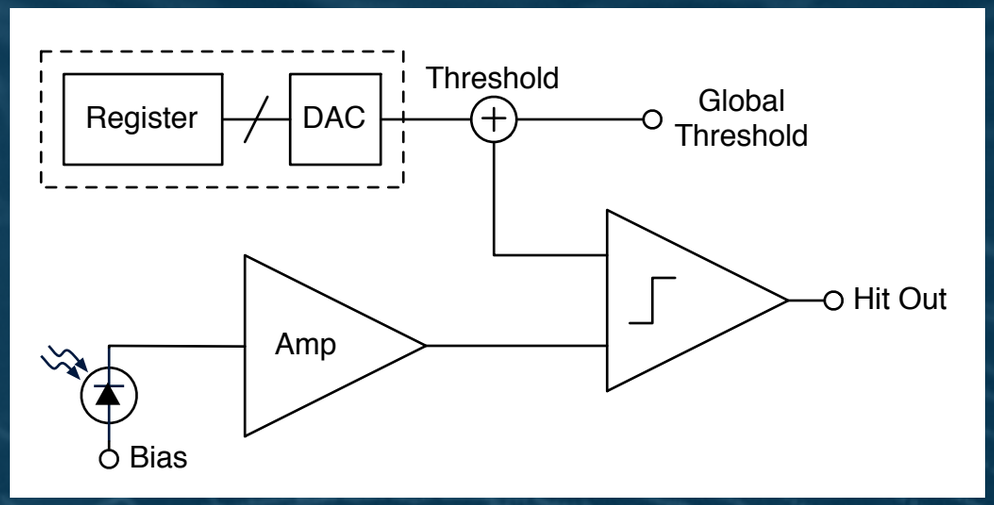
Hybrid Technology:

- Dedicated sensor and readout chip, connected via bump bond
- Mixed signal readout chip with per pixel amplifier and discriminator
- Two main sensor technologies:
  - Planar
  - 3D

Pixel Readout Chip at the LHC

Requirements:

- Collisions occur every 25ns
- Convert charge to digital value, typically Time-over-Threshold in 25ns units
- Store charge and time of each hit locally for a some µs (trigger latency)
- Read out hits which have been triggered, bandwidth > trigger frequency * number of hits

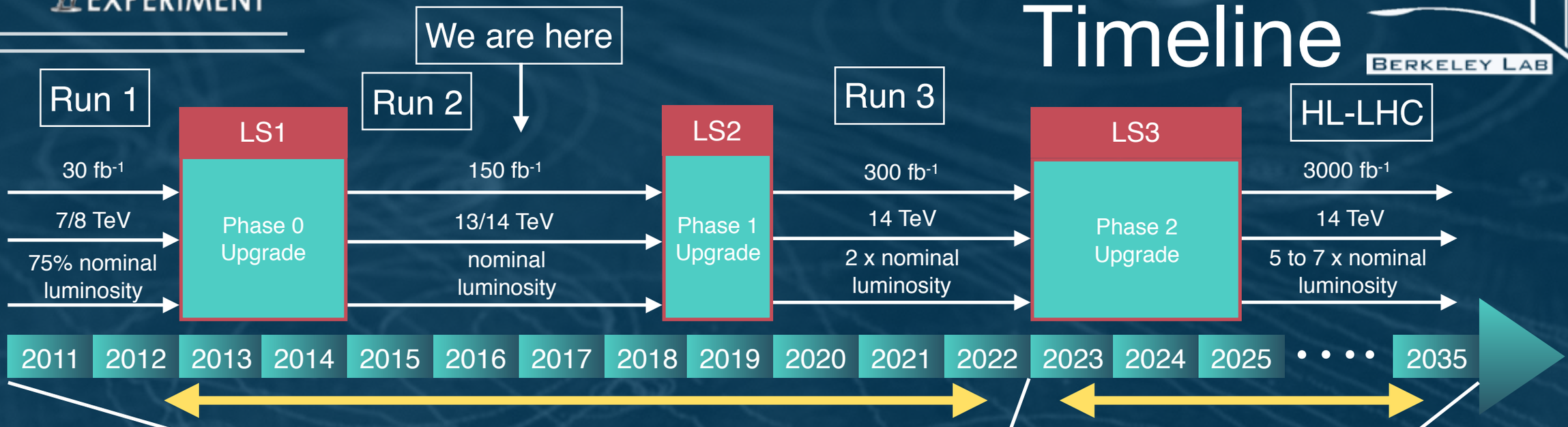


LHC → Summer Rain

HL-LHC → Pouring Storm

- Store full time sequence of drops until trigger (not collect in a bucket) → more memory
- High resolution to distinguish between drops → smaller pixels
- Drops damage sensor and readout chip → higher radiation tolerance

Timeline



	Current Tracker	ITk
Chip Size	2x2cm^2	2x2 cm^2
Pixel Size	50x250 µm^2	50x50 µm^2
Pixel Hit Rate	400 MHz/cm^2	3 GHz/cm^2
Trigger rate	200 kHz	1 MHz
Trigger Latency	6.4 µs	12.8 µs
Current consumption	20 µA/pixel	<8 µA/pixel
Radiation Tolerance	300 Mrad	0.5-1 Grad
Min. stable Threshold	1500 e	600 e

ATLAS Phase 2 Upgrade will replace Inner detector with new all-silicon tracker, the Inner Tracker (ITk)

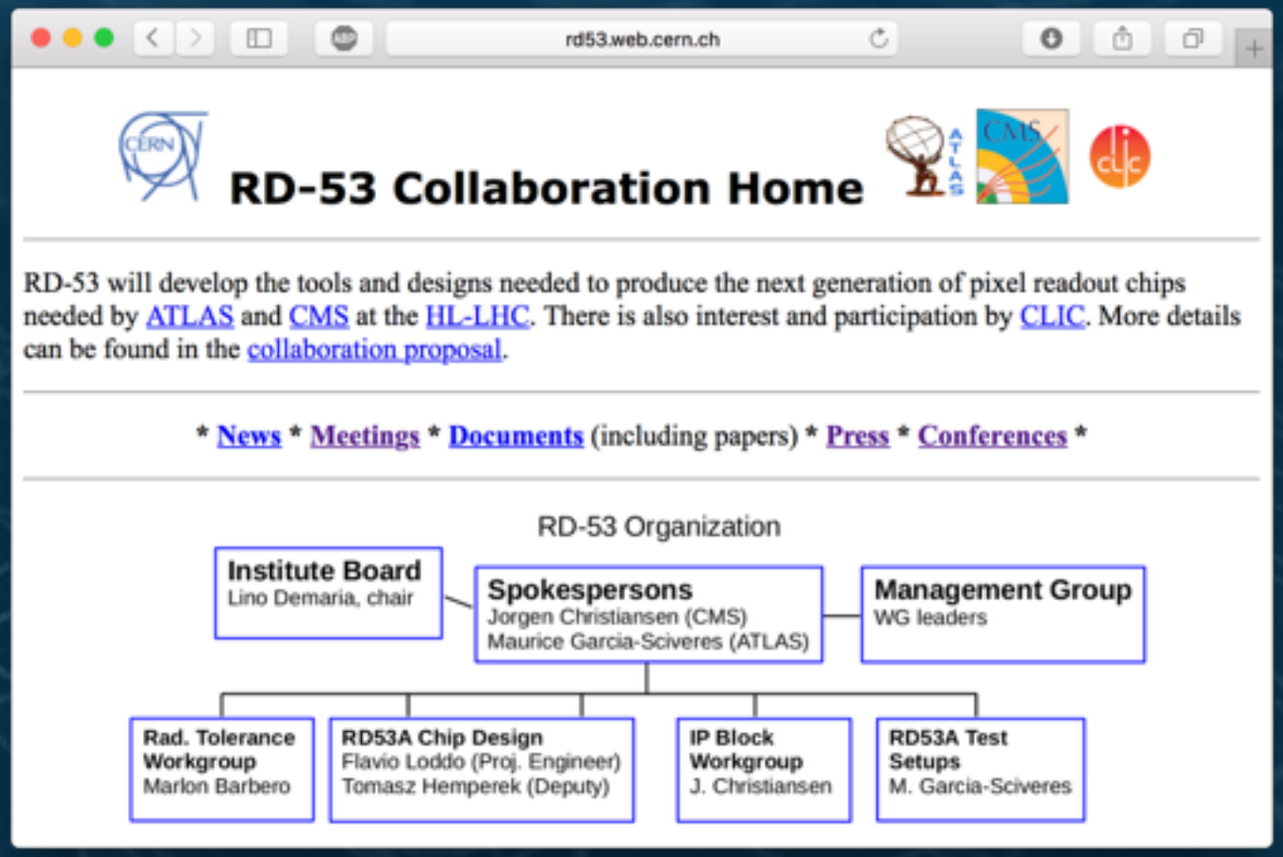
RD53 Collaboration

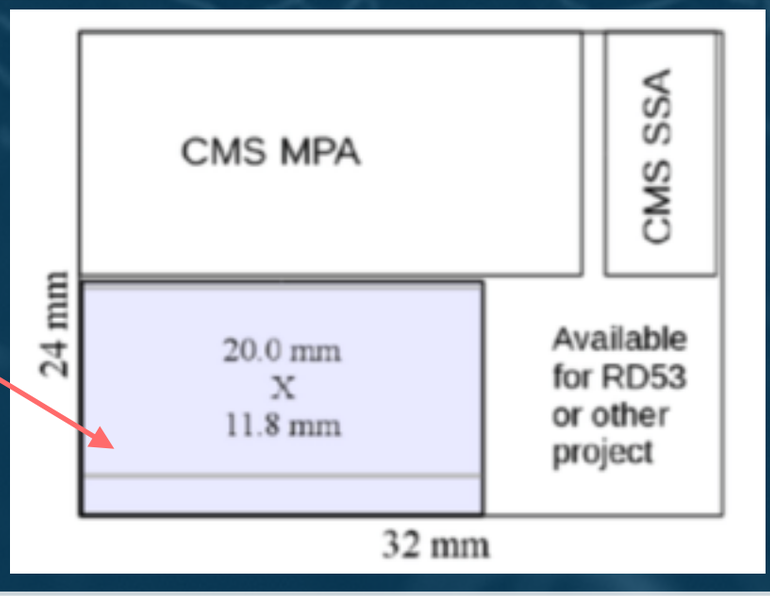
Overview:

- R&D program aiming to develop pixel readout chips in 65nm technology
- Consisting of ATLAS and CMS groups

Goals:

- Study of radiation effects in 65nm
- Develop design flow to efficiently design large pixel readout chips
- Design of shared rad-hard IPs
- Design and test a large scale 65nm pixel readout chip → RD53A





LBNL Contributions

Great internal collaboration with IC design group and external collaboration with Universities!

LBNL IC design group:

- Abder: Initial analog front-end design, FE65P2
- Dario: analog front-end design, FE65P2, DRAD, RD53A
- Amanda: RD53A analog front-end design

Visitors:

- FE65P2:
  - Testing: Lashkar
- RD53A:
  - DAQ: Nikola, Lev
  - Wafer probing: Xiangyang

LBNL ATLAS Group:

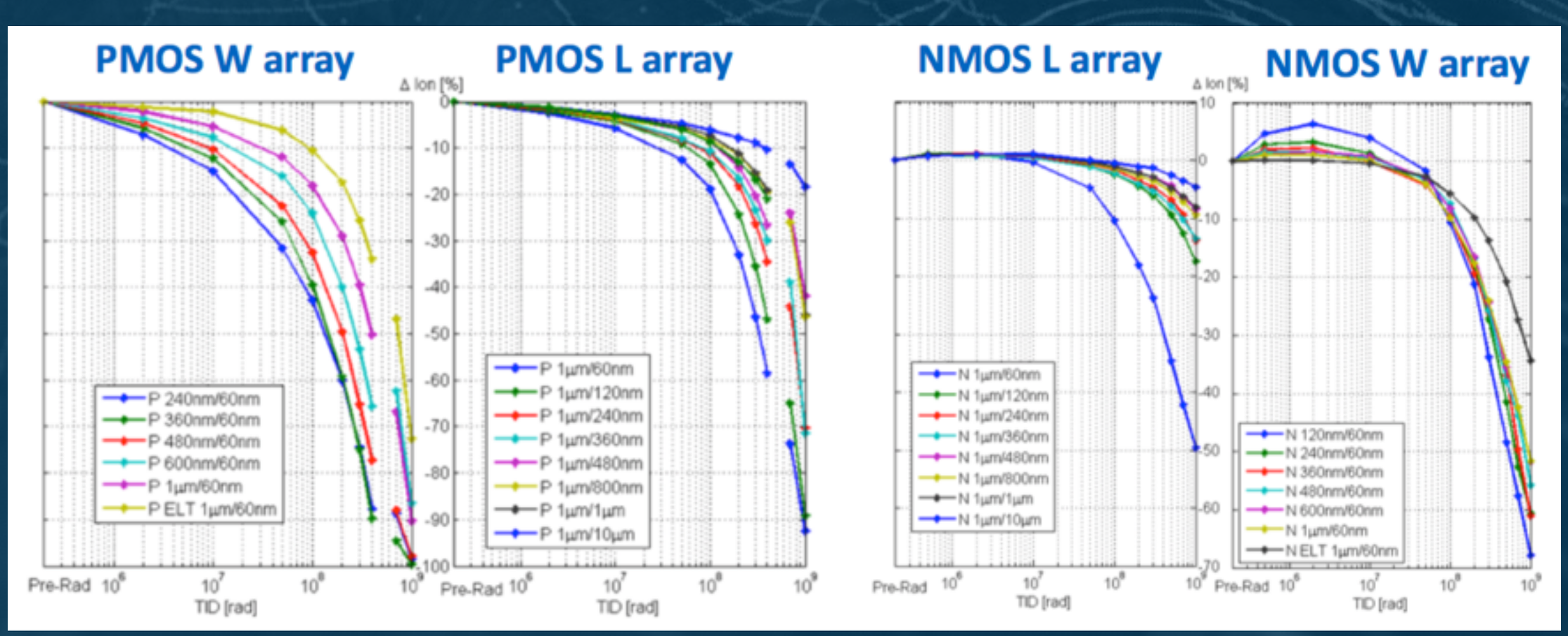
- FE65P2:
  - Verification: Rebecca
  - Testing: Ben, Katie, Rebecca, Maurice, Timon, Veronica
  - DAQ: Timon
- RD53A:
  - Verification: Cesar
  - Preparation for testing: Aleksandra, Katie, Adrien, Maurice, Timon
  - DAQ: Arnaud, Timon
  - Cable testing: Veronica

Radiation Hardness

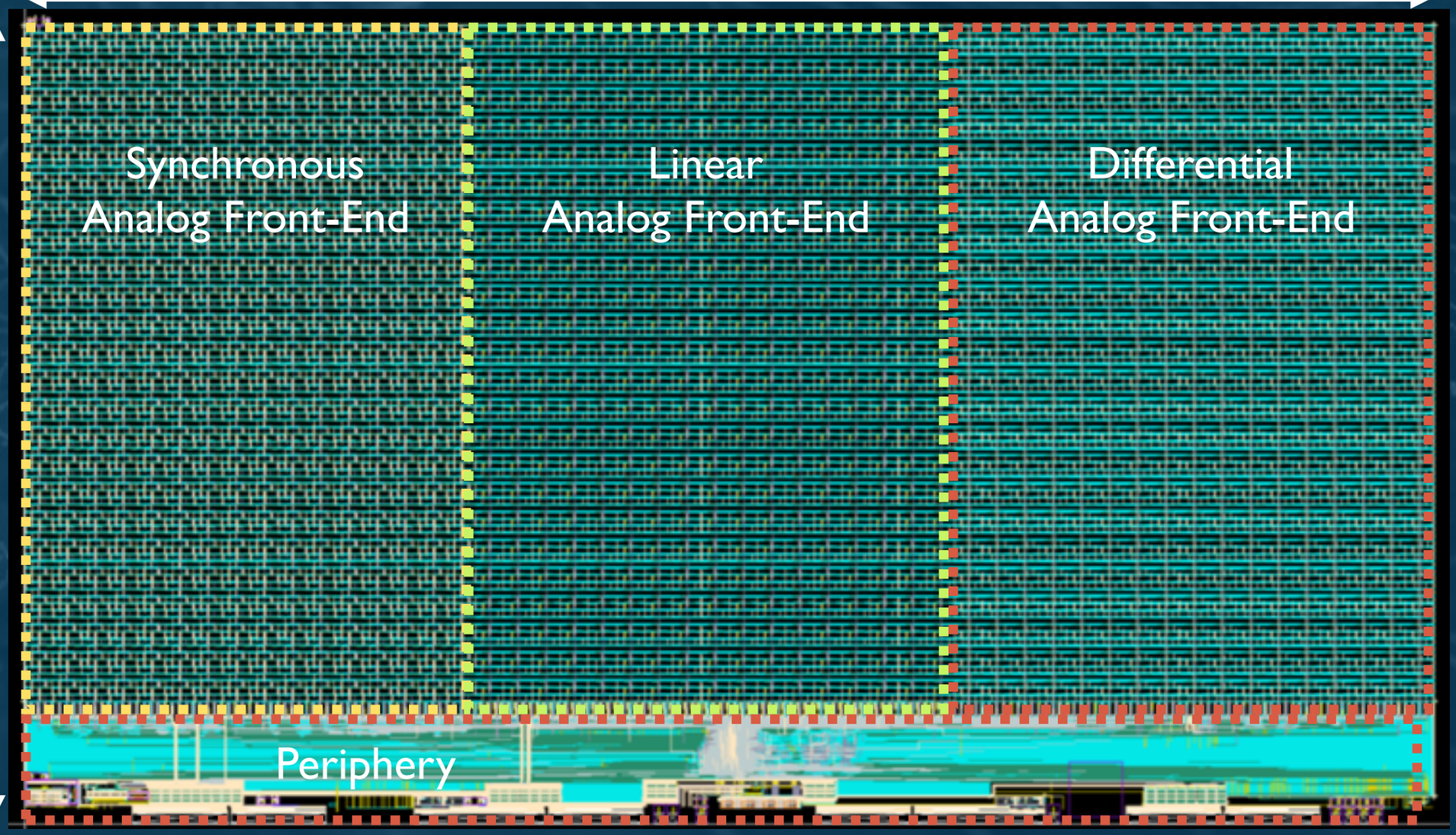
More details in Instrumentation Colloquium:
"Radiation Effects in CMOS Technologies for LHC Detector Upgrades"
by Federico Faccio

Take-away points:

- Total Ionising Dose (TID) effects can damage CMOS transistors
- 65nm is intrinsically very radiation hard
- Analog: avoid narrow & short transistors
- Digital: qualified 9T std library in dedicated test chip



RD53A Overview



76,800 x 50x50µm2 pixels

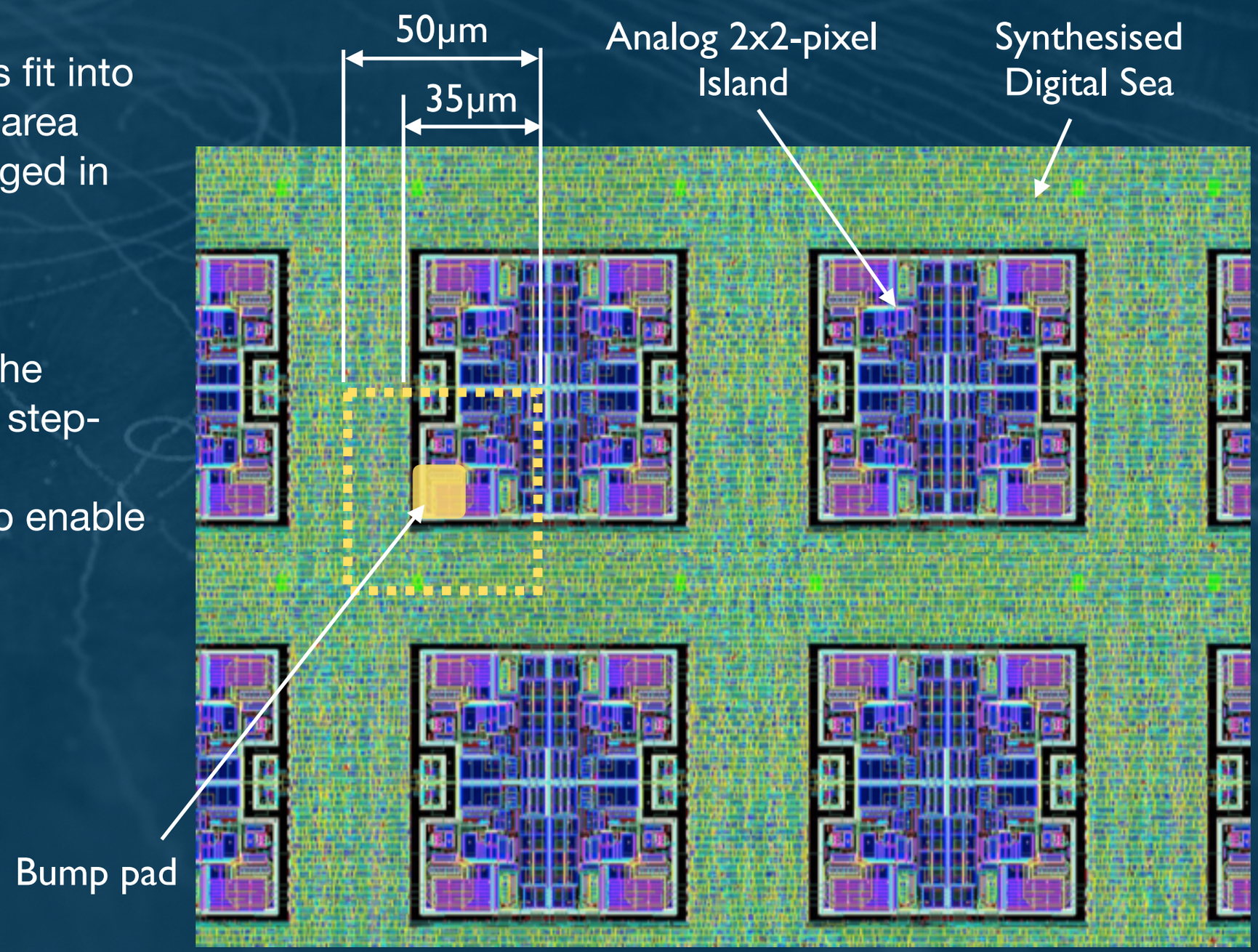
RD53A Specs

Specification	Value	Comment or Test Conditions
Input polarity	Negative	
Interior pixel capacitance	<100 fF	this applies to most pixels
Edge pixel capacitance	<200 fF	see subsection on edge pixels
Interior pixel leakage current	<10 nA	
Edge* pixel leakage current	<20 nA	*see Sec. 5.2 for details
Min. stable threshold setting	600 e^-	With 50 fF load, 4μA/pixel analog. For free running discriminated pixel. See Sec. 3.1
Min. charge above threshold resulting in <25 ns time walk	600 e^-	With 50 fF load, 4μA/pixel analog. For free running discriminated pixel. See Sec. 3.1
Min. in-time threshold with free-running front end	1200 e^-	With 50 fF load, 4μA/pixel analog. Simply the sum of the two above lines
Min. in-time threshold if using synchronous reset	750 e^-	With 50 fF load, 4μA/pixel analog. See Sec. 3.1
Hit loss from in-pixel pileup	$\leq$1%	at 75 kHz avg. hit rate. See Sec. 3.2
Recovery from saturation	<1 μs	See Sec. 3.2 for discussion
Trigger rate	1 MHz	
Trigger latency	12.5 μs	
Noise occupancy per pixel	$< 10^{-6}$	50 fF load; in a 25 ns interval
Single pixel noise (ENC)	design-dependent	See Sec. 3.1
Radiation dose	500 Mrad	delivered at -15 C. Room T annealing only
Temperature range	-40C to +40C	
Current consumption, analog	4 μA/pixel	periphery consumption not included
Current consumption, digital	<4 μA/pixel	periphery consumption not included
Current consumption, Total	<500 mA/cm^2	Note this is 1 W/cm^2 at 2 V input
SEU's affecting full chip	<0.05/hr/chip	in 1.5 GHz/cm^2 particle flux
SEU's affecting single pixel	<100/hr/chip	in 1.5 GHz/cm^2 particle flux
Charge scale shift	<2% / Mrad	change in mean with radiation
Threshold scale shift	<15 e^- / Mrad	change in mean with radiation
Threshold dispersion	<60 e^- / Mrad	added in quadrature
Charge meas. dispersion	<0.1 MIP/Mrad	added in quadrature

Analog Islands & Digital Sea

Design strategy:

- All analog FE flavours fit into the same 35x35µm2 area
- Analog FEs are arranged in 2x2 analog islands
- Digital on-top
- Digital logic can be synthesised around the analog islands → No step-and-repeat design
- Hierarchical design to enable fast verification

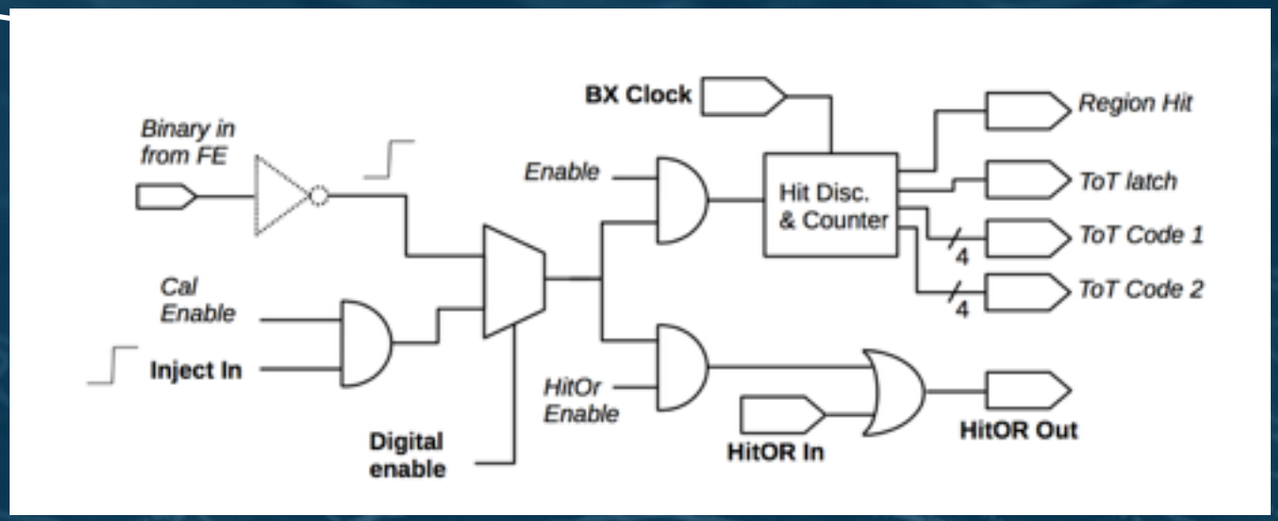


Digital Pixel Region

Distributed Buffer Architecture (CBA):

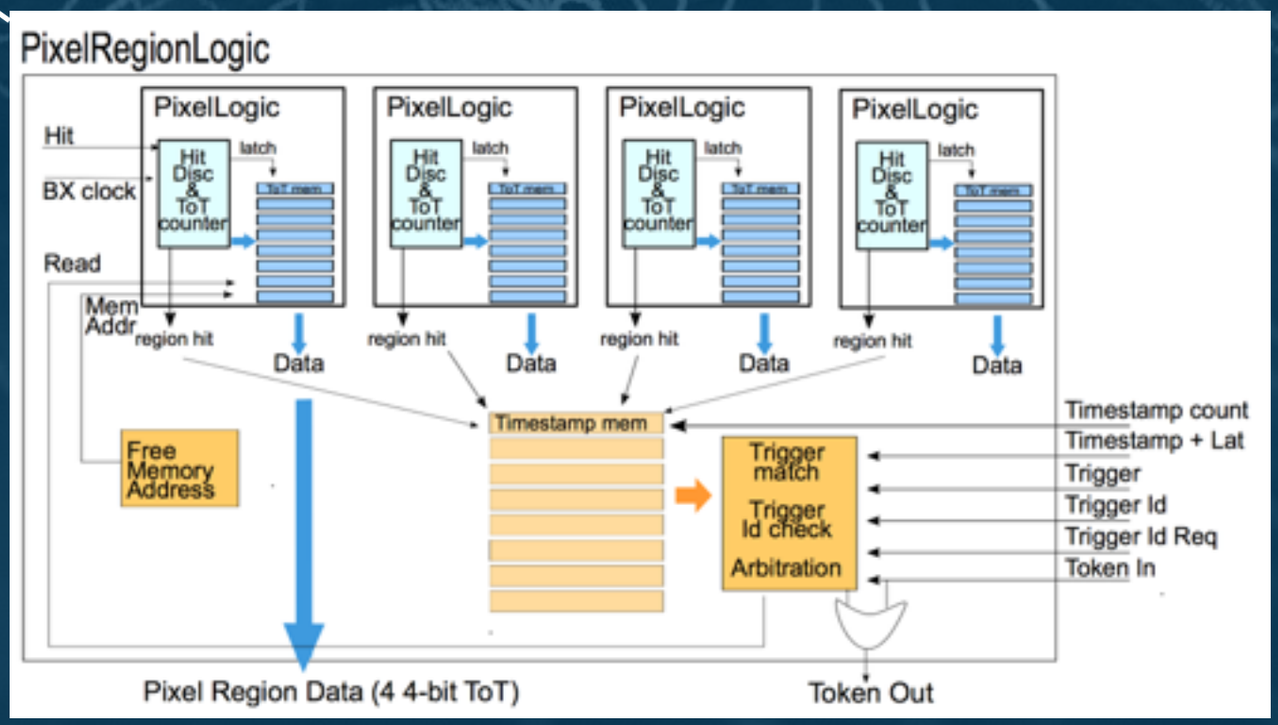
- 4x1 pixel per region
- Each pixel has 8 x 4-bit ToT memories
- Each region has 8 x 9-bit Latency timer memories
- P&R ~80-85% full

One Pixel:



Centralised Buffer Architecture (CBA):

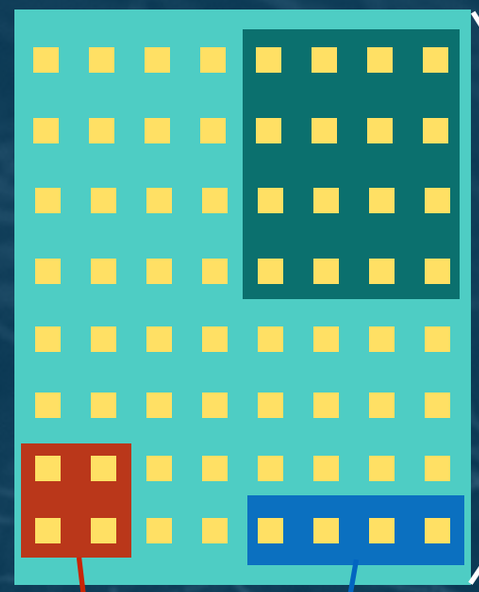
- 4x4 pixel per region
- Each region has 16 memories to store:
  - 9-bit timestamp
  - 16-bit hit map
  - 6 x 4-bit ToT values
- P&R ~90-95% full

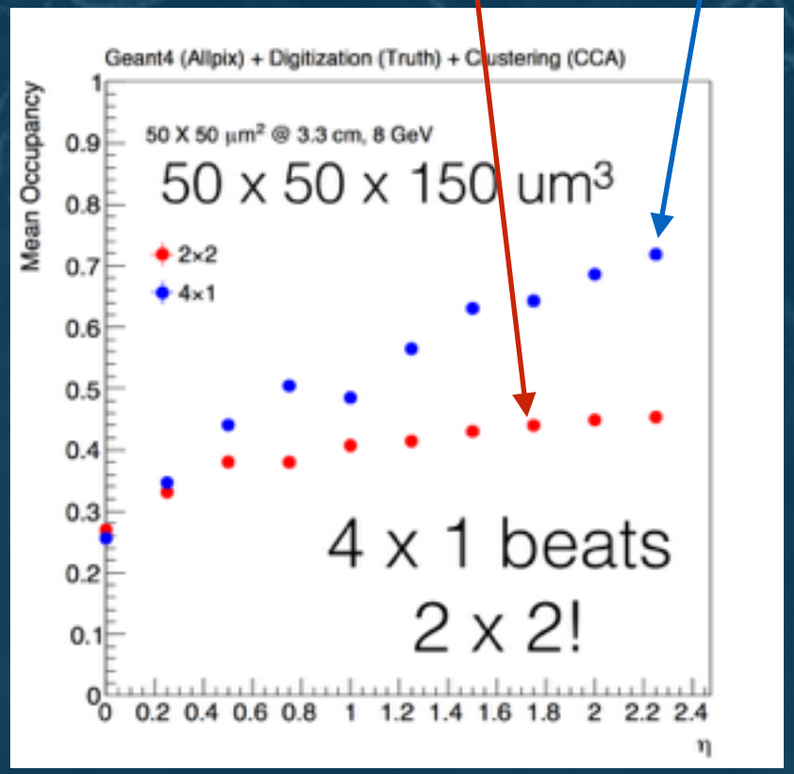


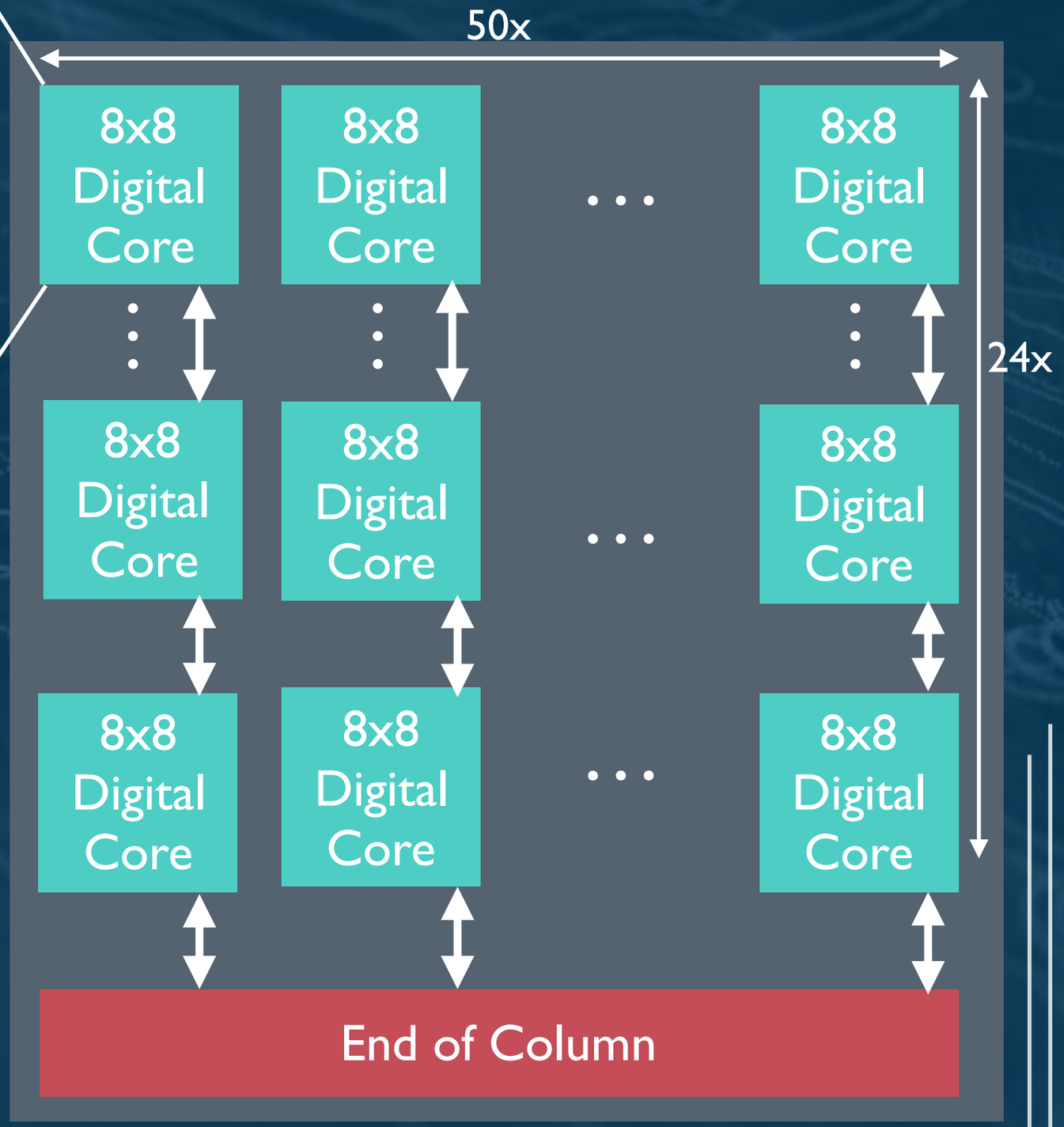
Digital Architecture

Digital Core:

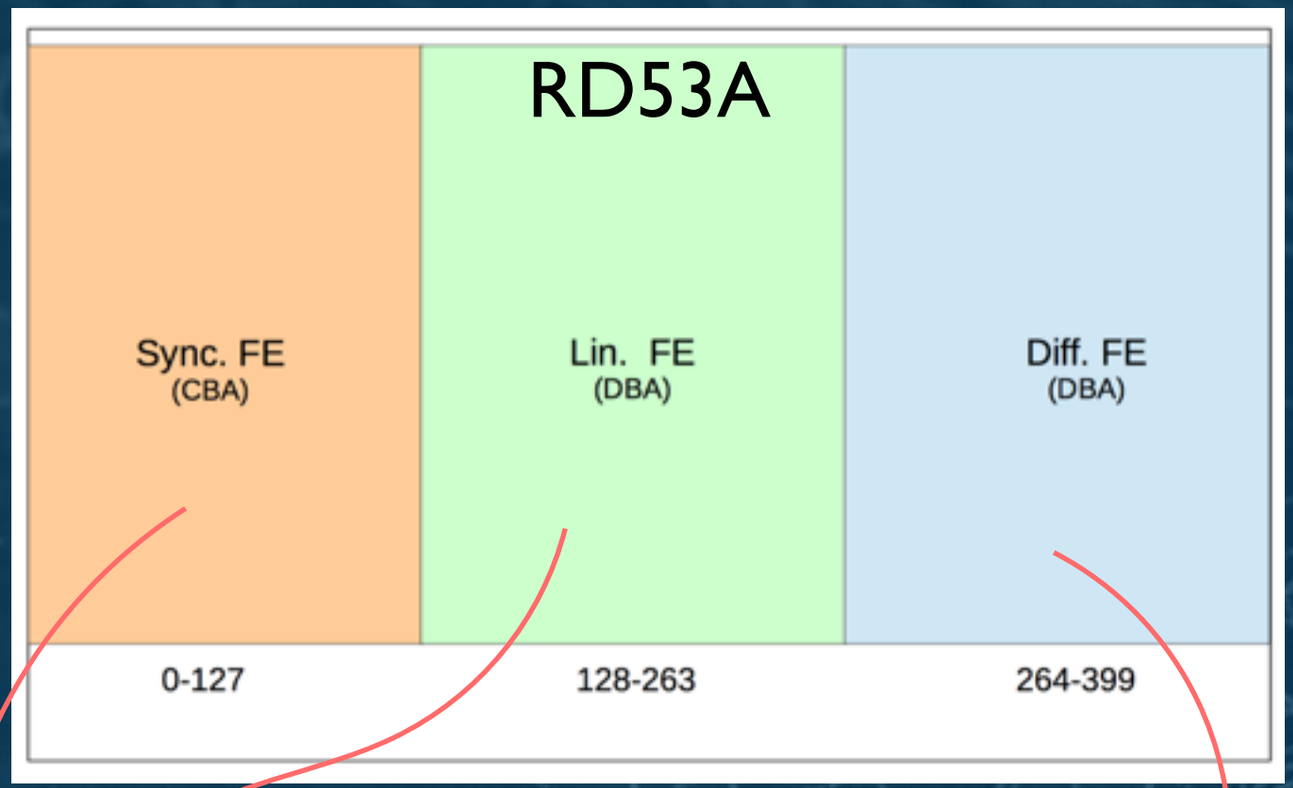
- Small enough for transistor level simulation
- Tiles of synthesised logic connected during place & route
- Two kinds of digital buffer architecture:
  - 4x4
  - 4x1







Analog Front-Ends

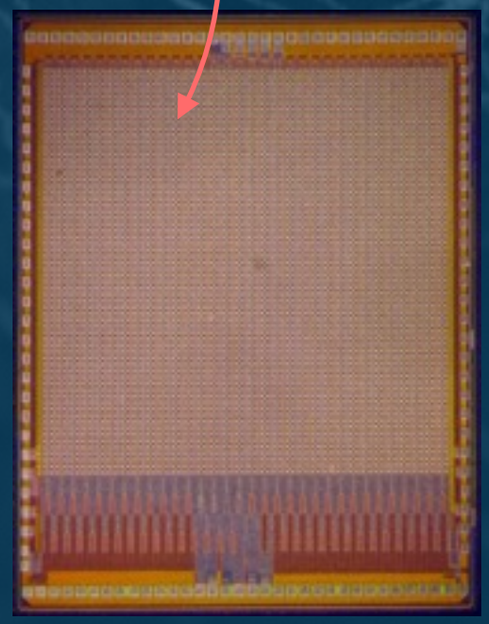


Towards RD53A:

- Two small scale prototypes:
  - Exercise “analog island in digital sea” design flow
  - Test analog front-end designs
  - Test vehicle for irradiations
  - 50x50µm2 sensor development

Chipix65:

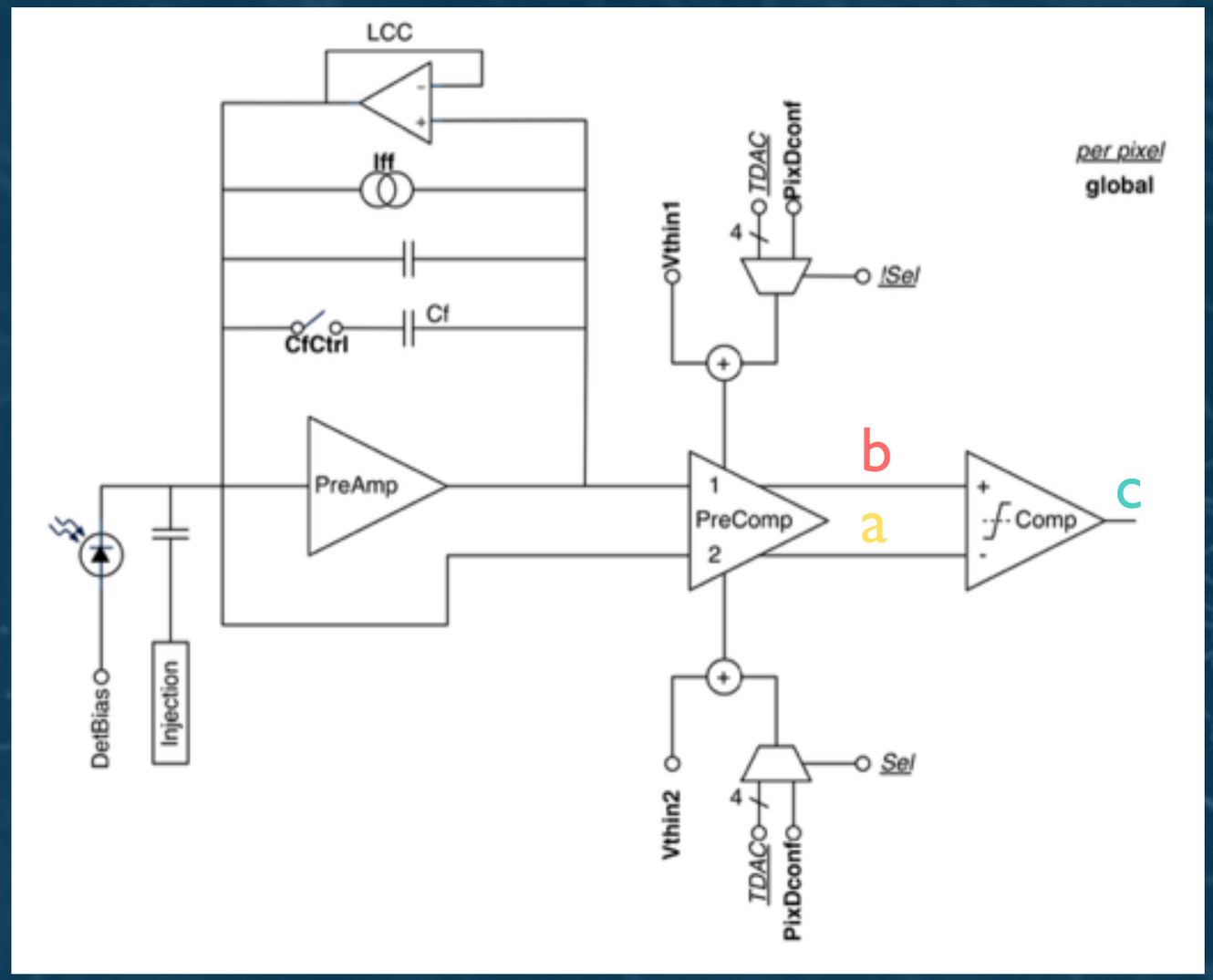
- 64x64 pixel
- Submitted summer 2016
- Synchronous and Linear front-end
- 4x4 Centralised buffer architecture
- 4x4 digital core
- DAC, ADC, bandgap, CERN I/O pads

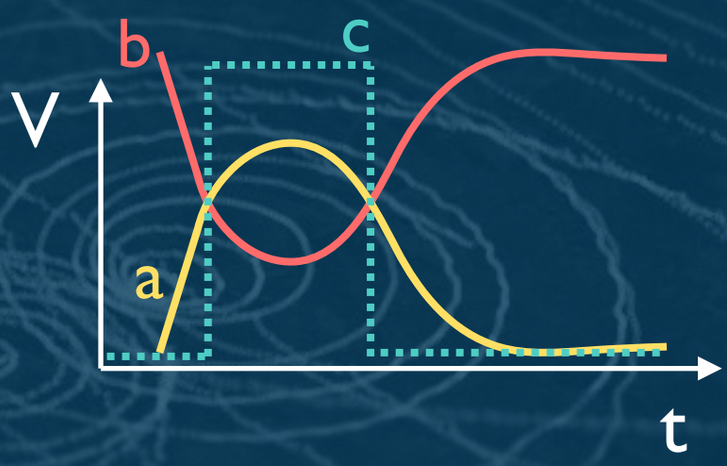


FE65P2:

- 64x64 pixel
- Submitted fall 2015
- Differential front-end
- 2x2 distributed buffer architecture
- 4x64 digital core
- Digital logic from FE-I4
- Barebone periphery

Differential Front-End





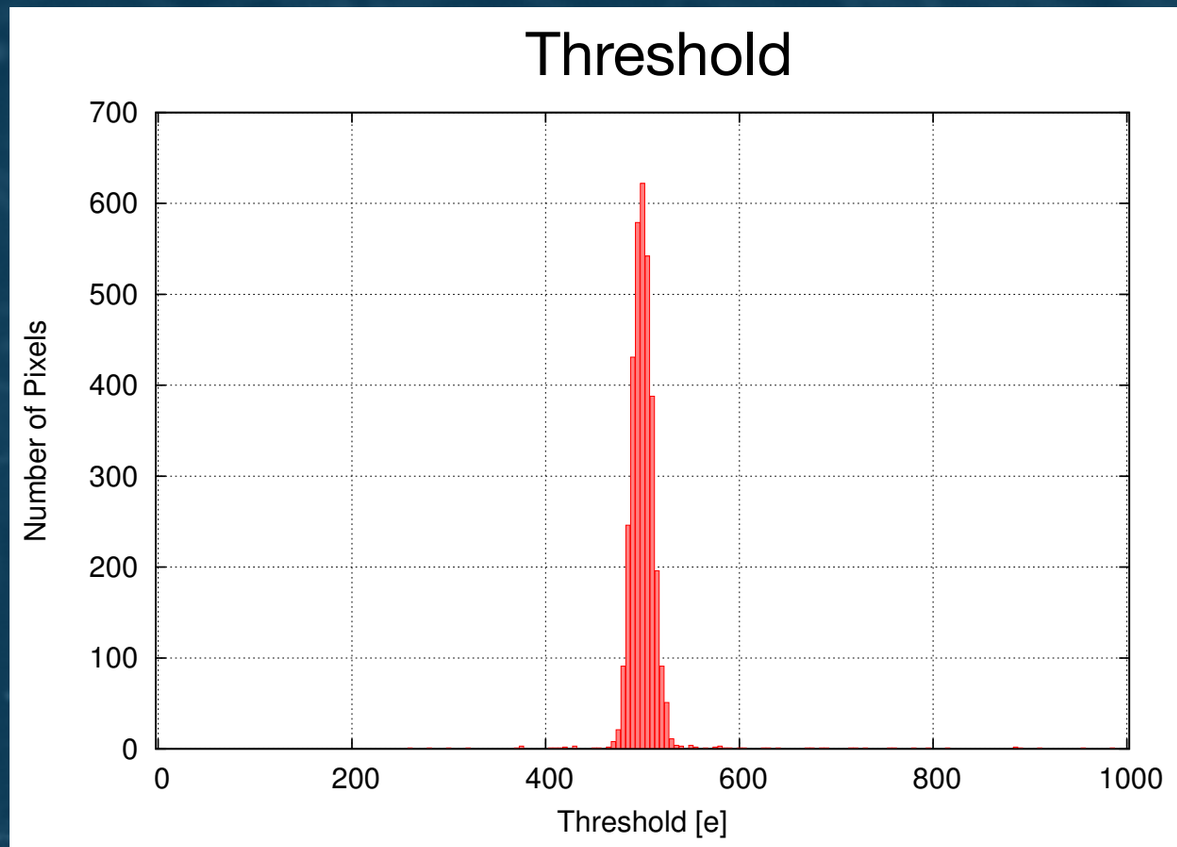
Charge Sensitive Amplifier:

- Straight cascode design
- Global settings for I_f (8bit DAC)
- No per pixel adjustment
- Selectable gain

Two Stage Comparator:

- Differential design
- Global 8bit threshold DAC
- Two per pixel 4bit threshold DACs
- Optimised for low threshold operation

Diff. Front-End II

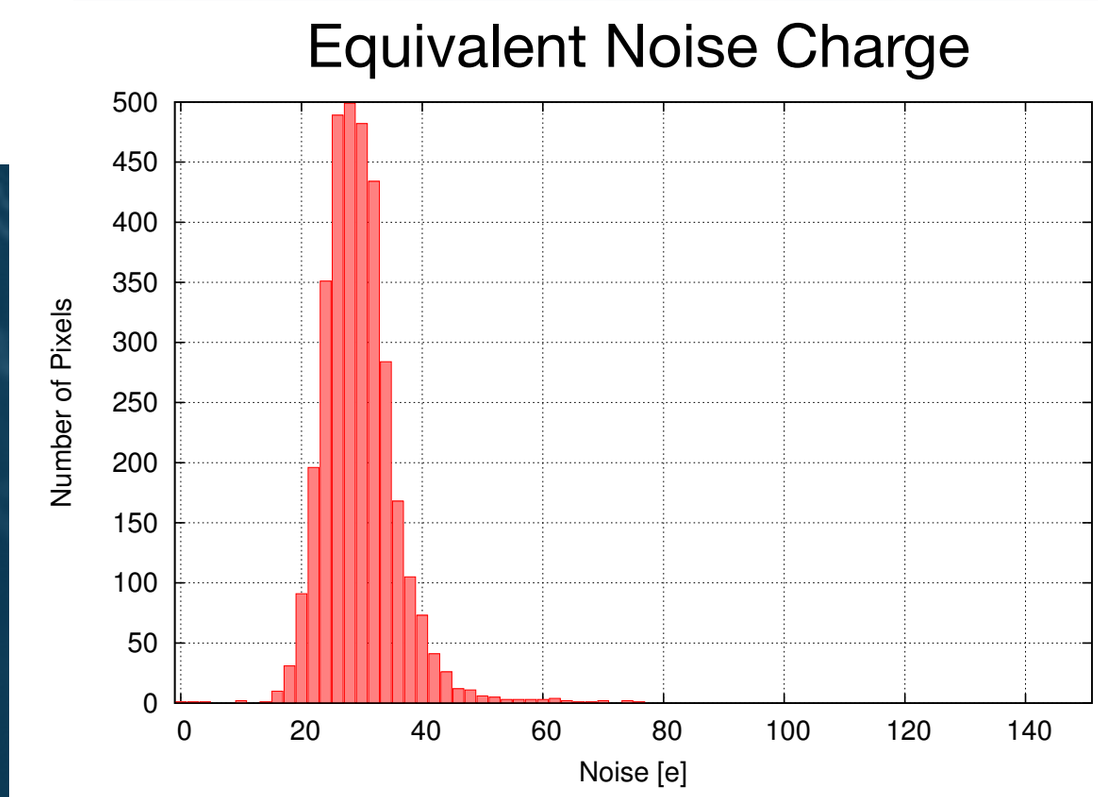


Threshold:

- 500e threshold with traditional tuning
- 30e threshold dispersion

Equivalent Noise Charge:

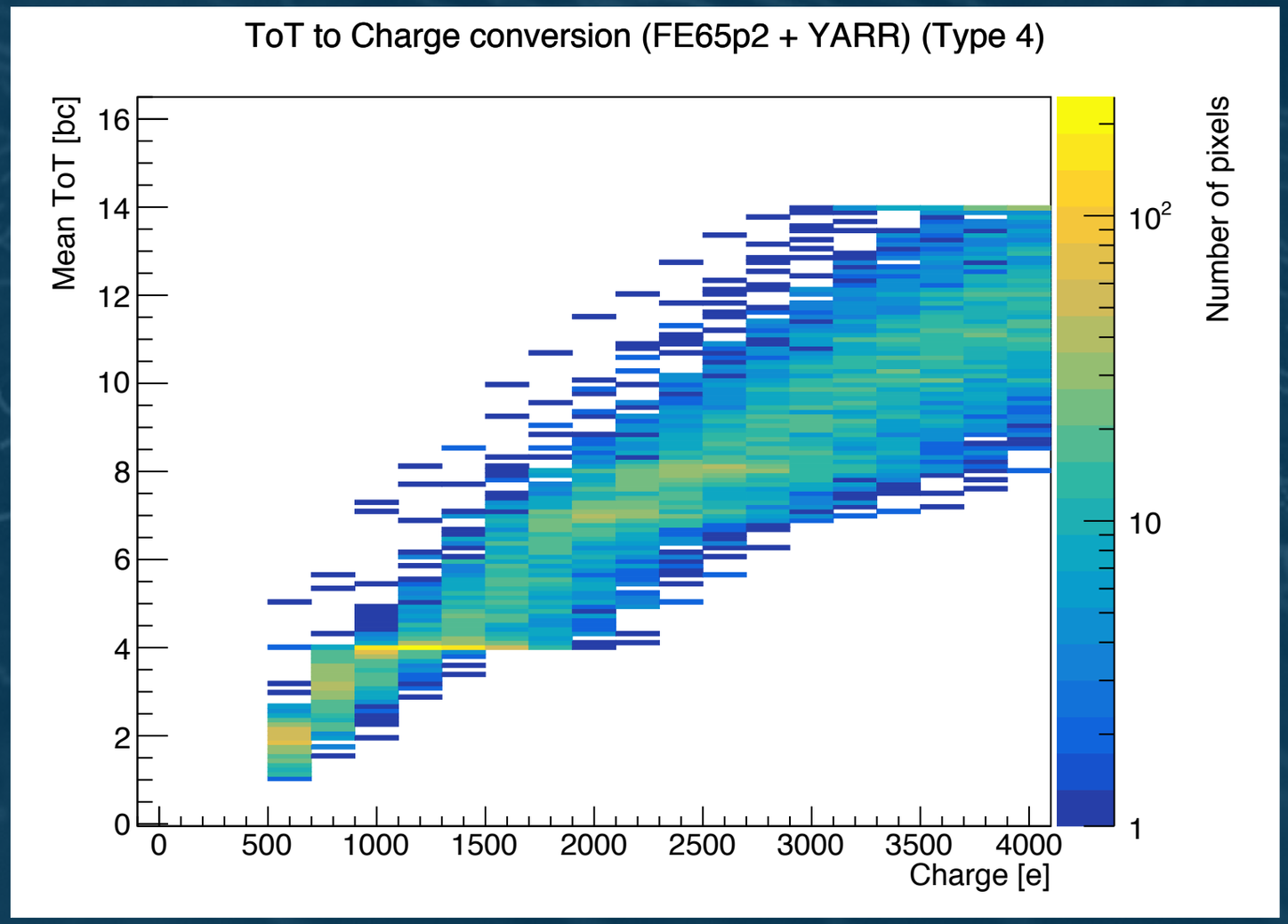
- Sigma of threshold s-curve
- Average of 35e noise w/o sensor



Charge Conversion

ToT:

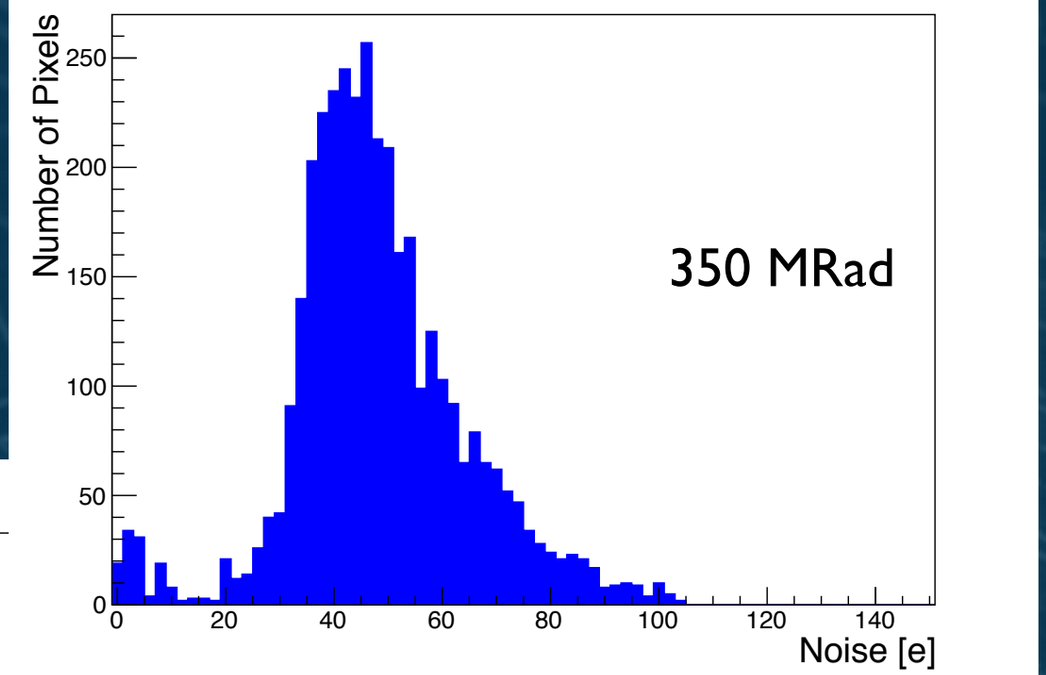
- No per-pixel adjustment
- Dispersion due to falling edge, primarily driven by mismatch in large PMOS
- Dispersion deemed to be acceptable (e.g. can be compensated via offline calibration)

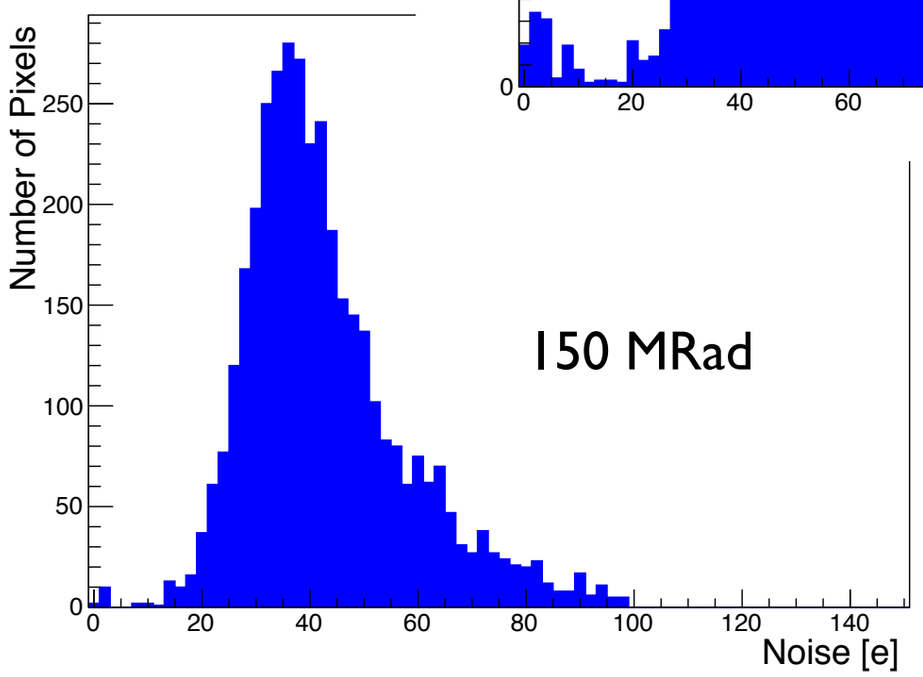


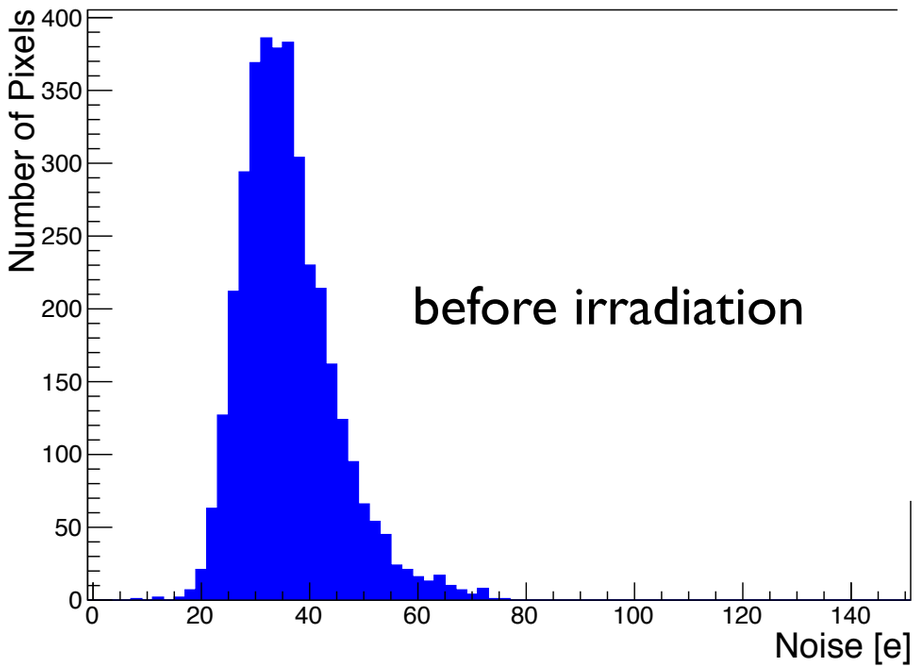
FE65P2 Irradiation

Proton irradiation:

- 800MeV protons at LANL
- Irradiated total of 6 modules
- Two chips for each TID: 150MRad, 350MRad, and 500MRad
- Unfortunately one 500MRad chip died of ESD before irrad., and the other was not centred in the beam



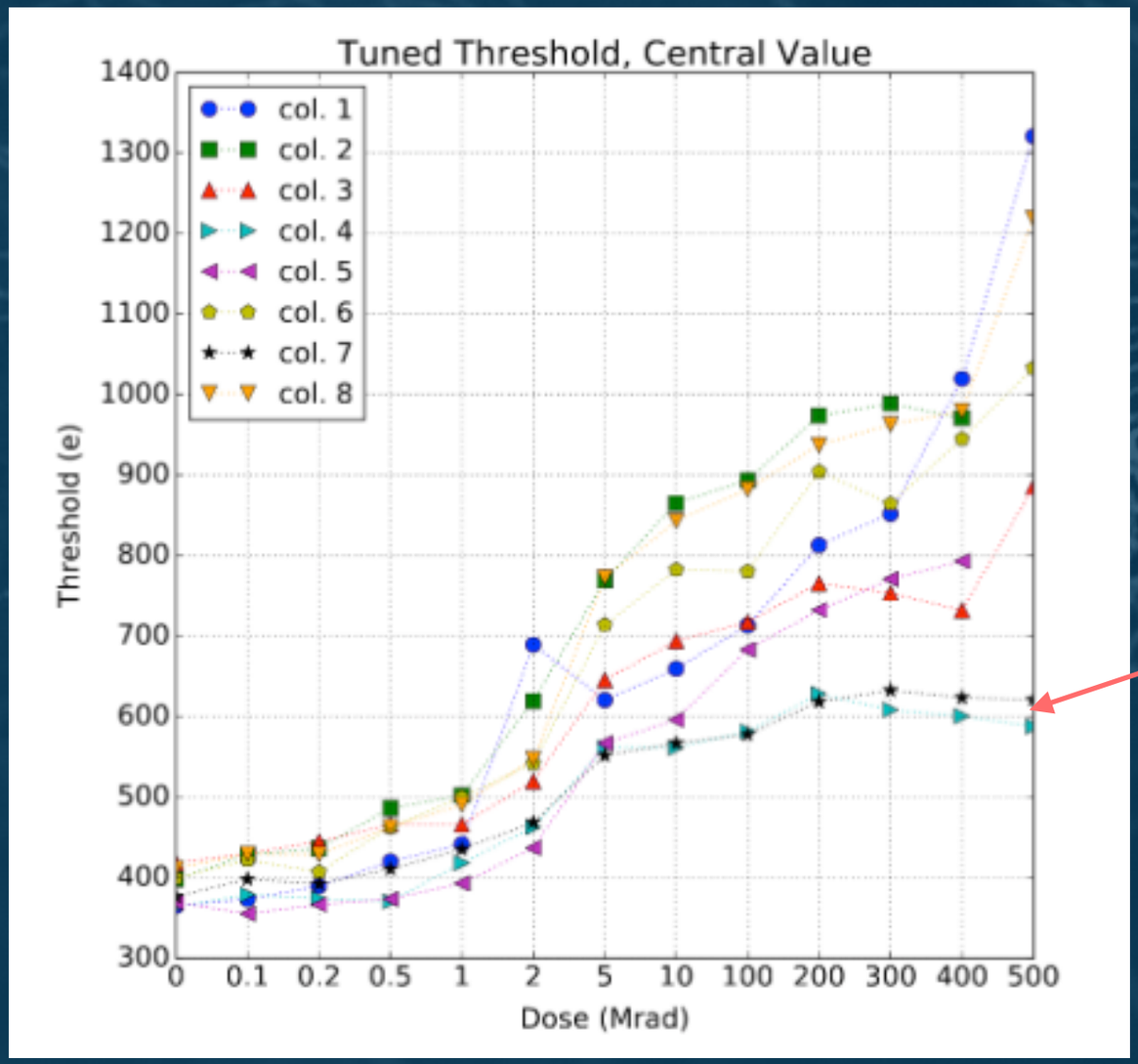




FE65P2 Irradiation II

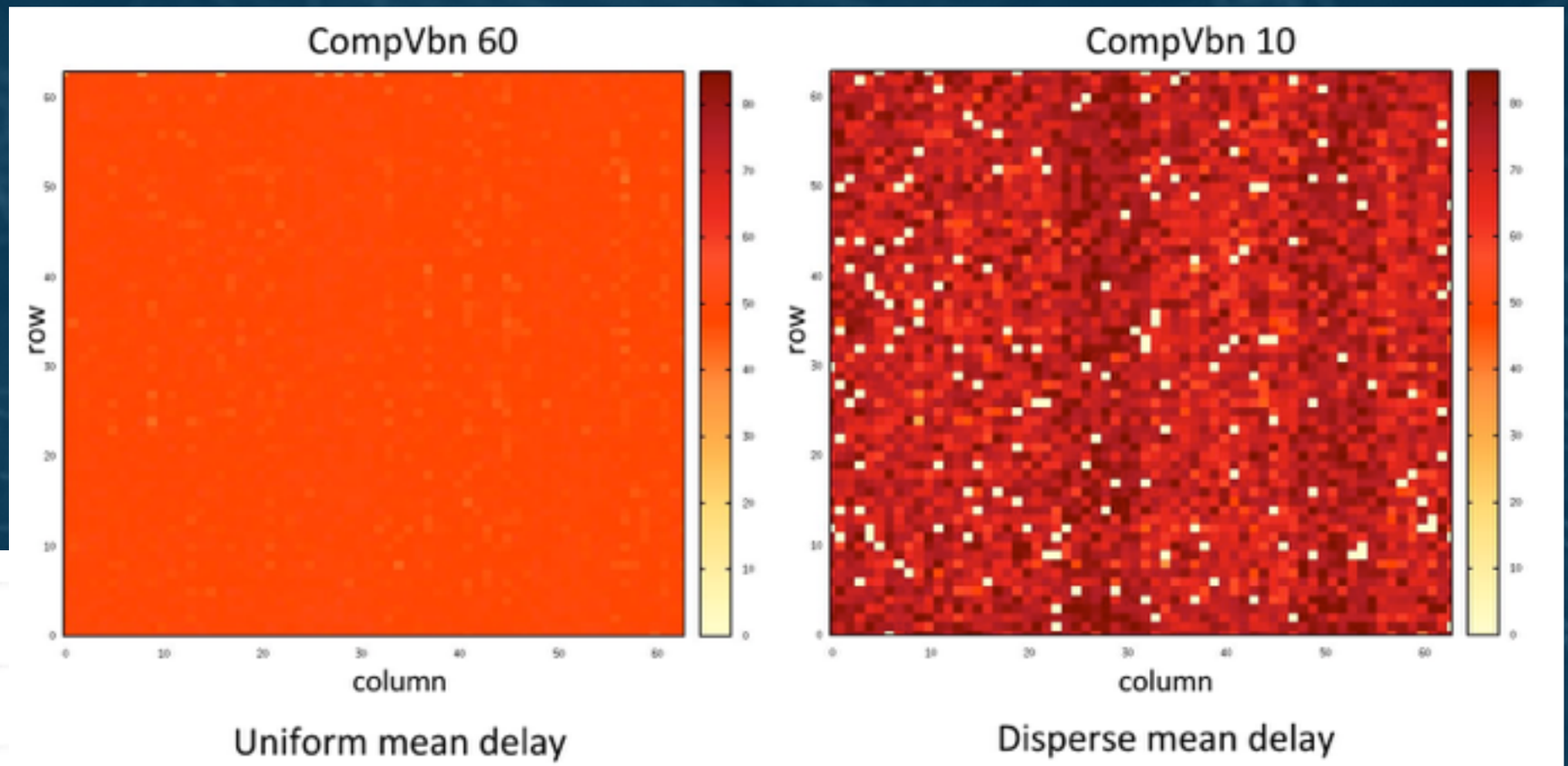
X-ray irradiation:

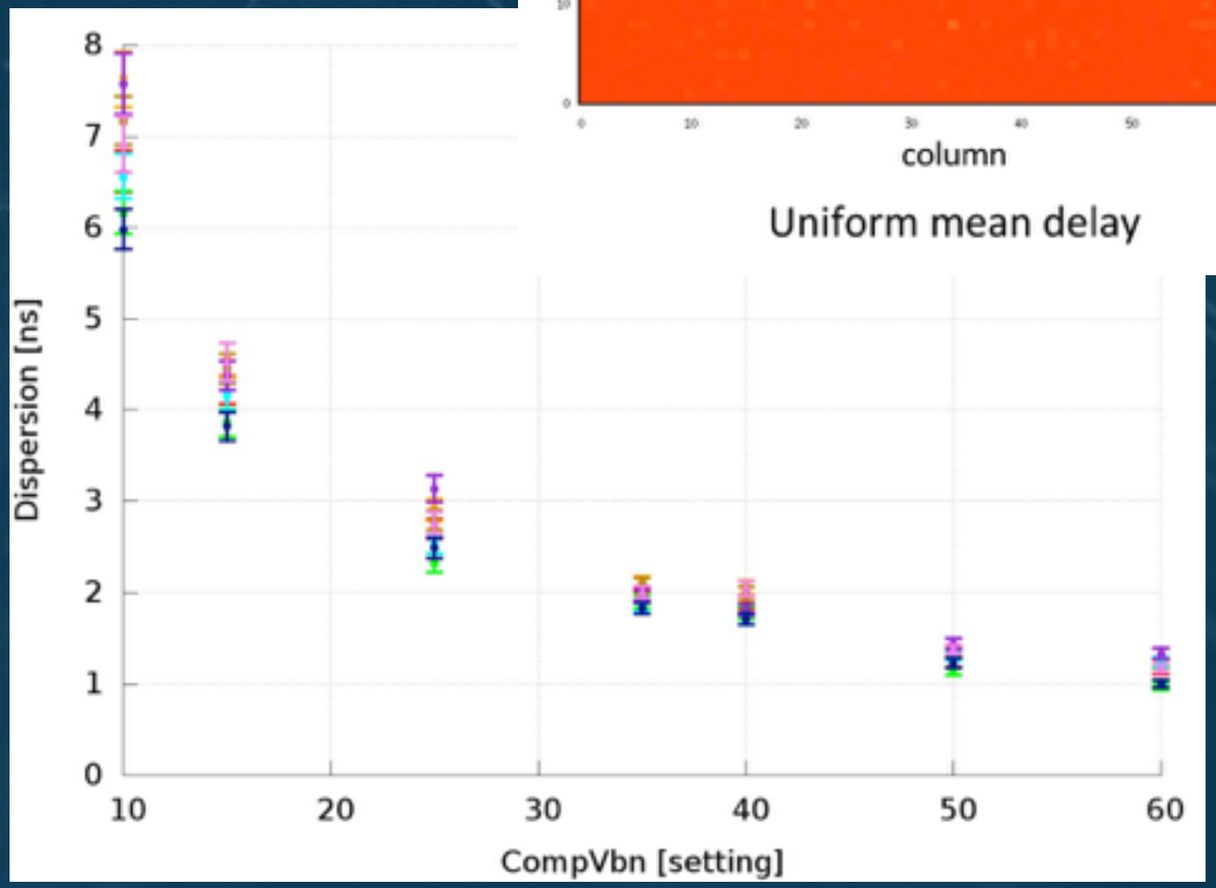
- Continuous monitoring during irradiation
- “Rad-hard” analog front-end behaves the best



used for RD53A

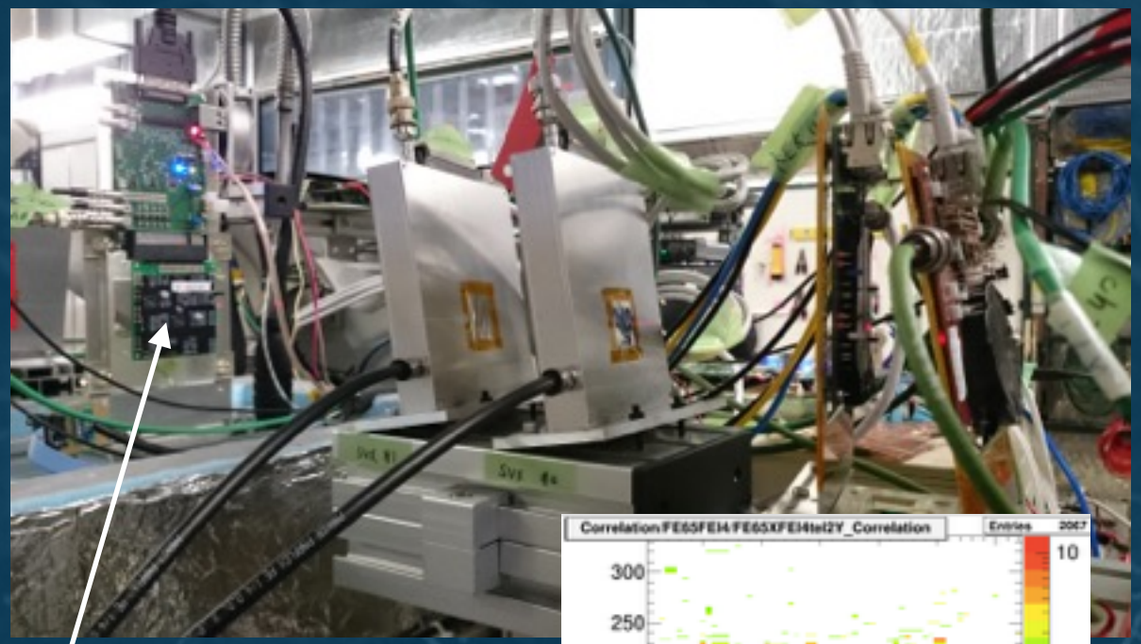
Discriminator Speed



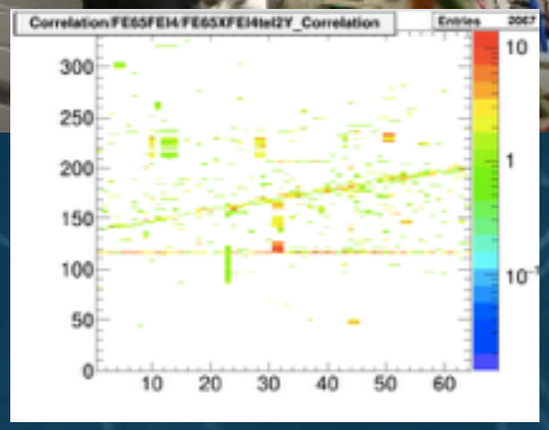


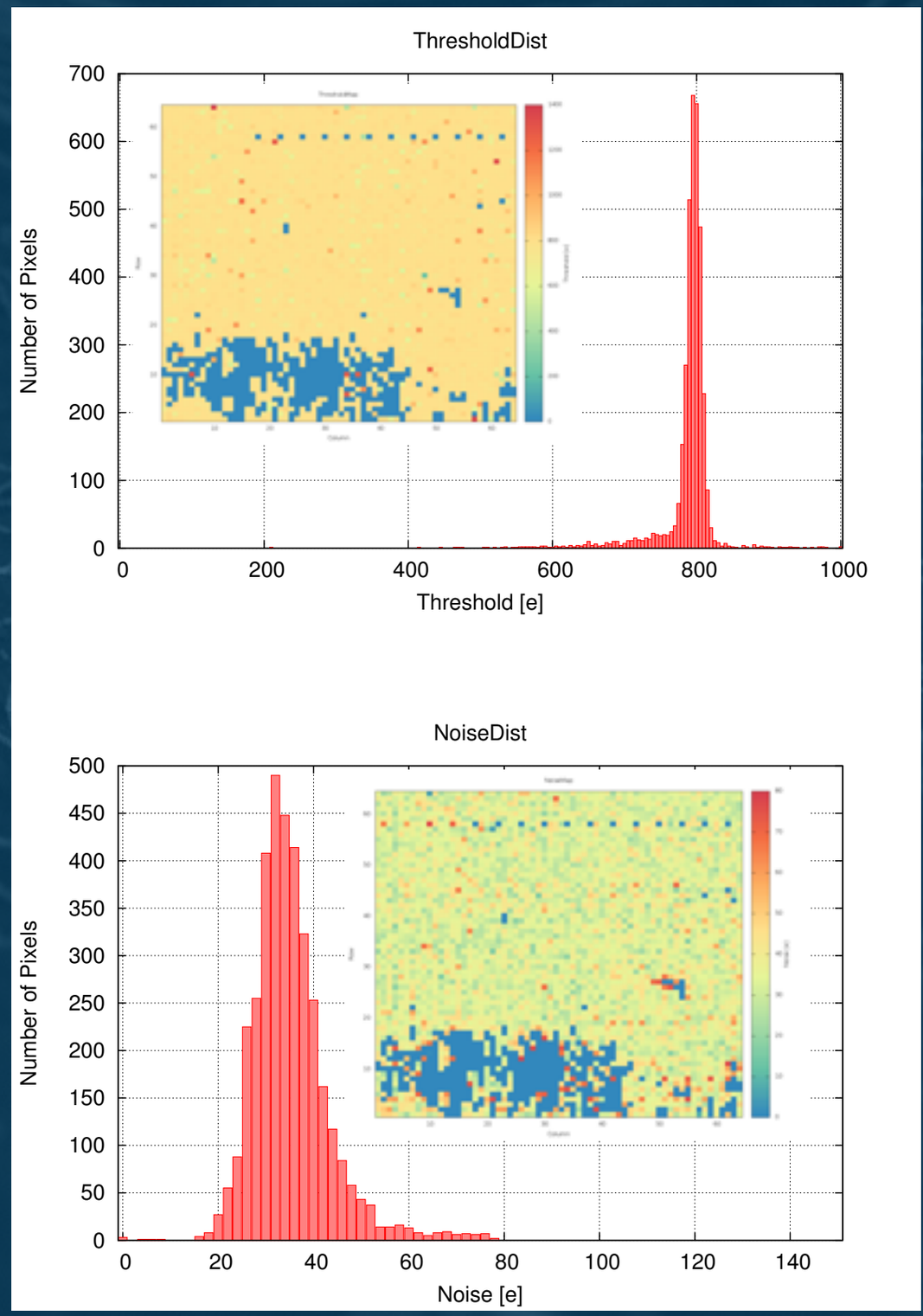
Trade-off:
higher CompVbn = less timing dispersion, but higher current consumption

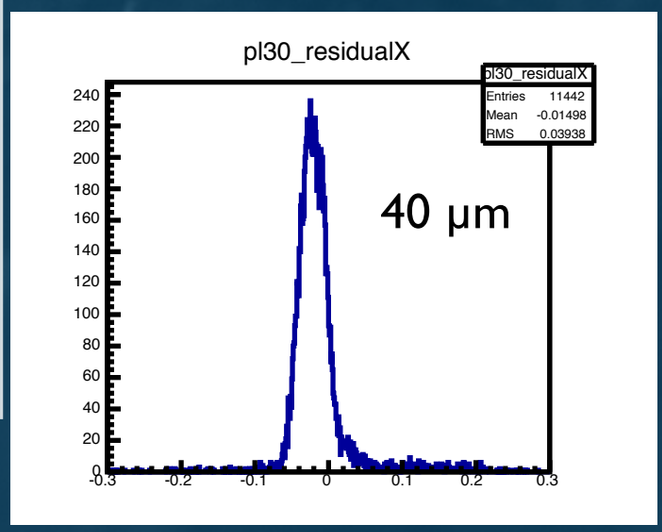
FE65P2 Sensor Module

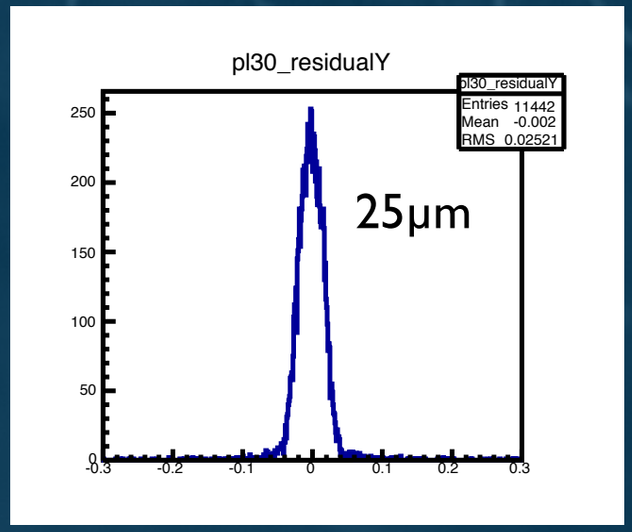


FE65P2

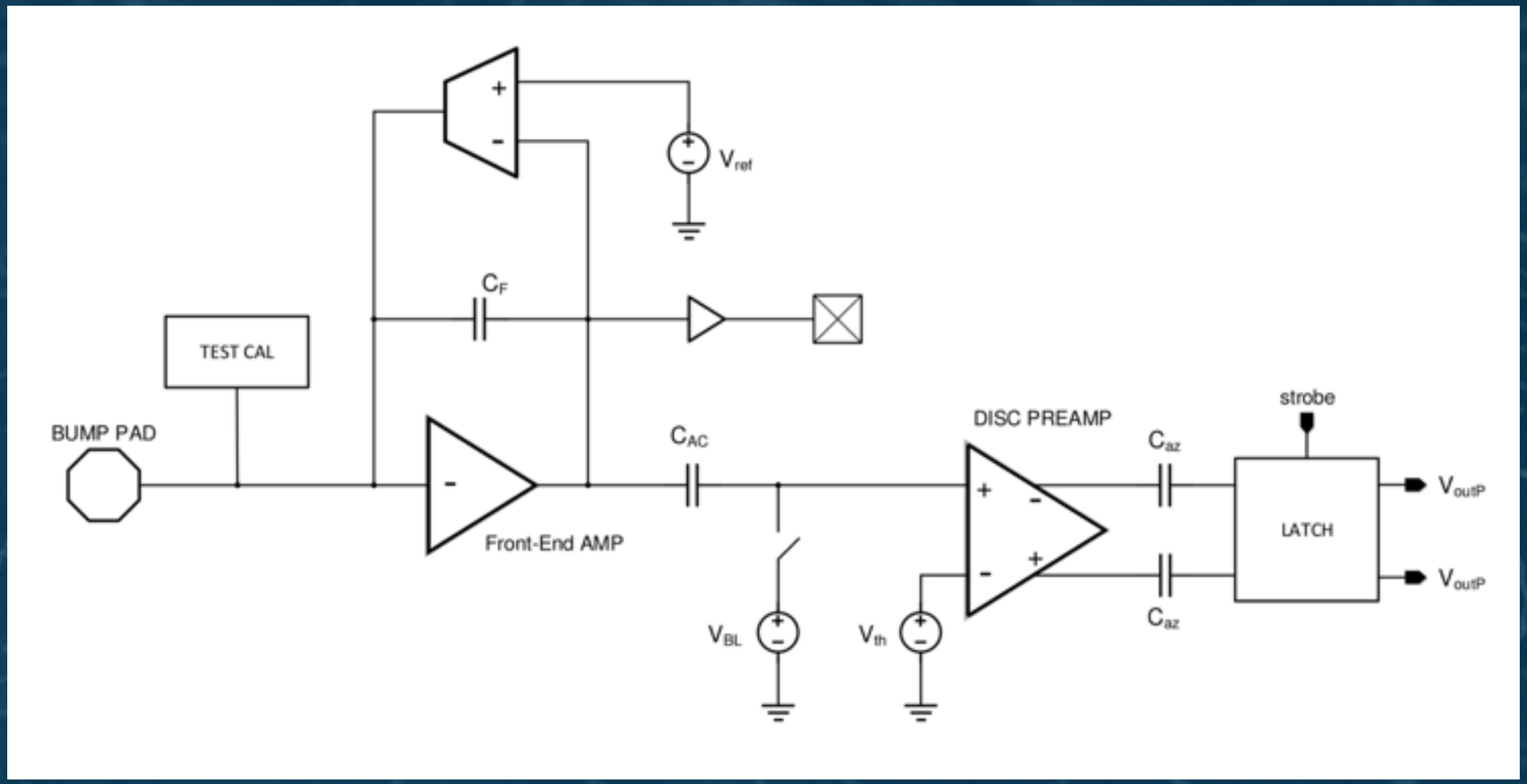








Synchronous Front-End



Charge Sensitive Amplifier:

- Telescopic cascade design
- Krummennacher feedback
- Selectable gain (4 settings)

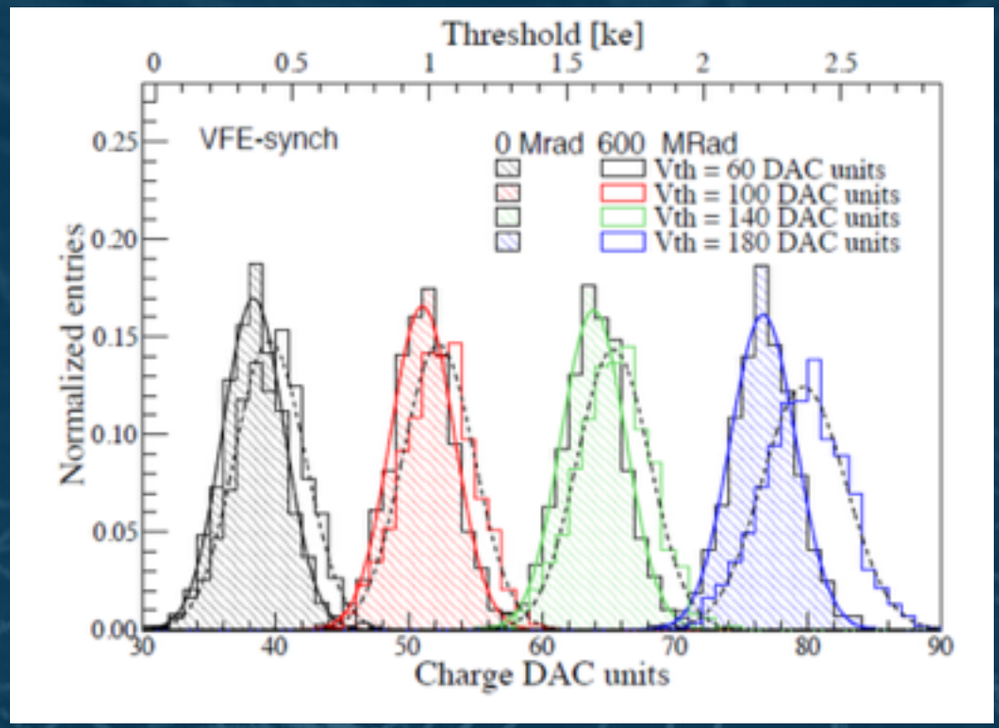
Discriminator:

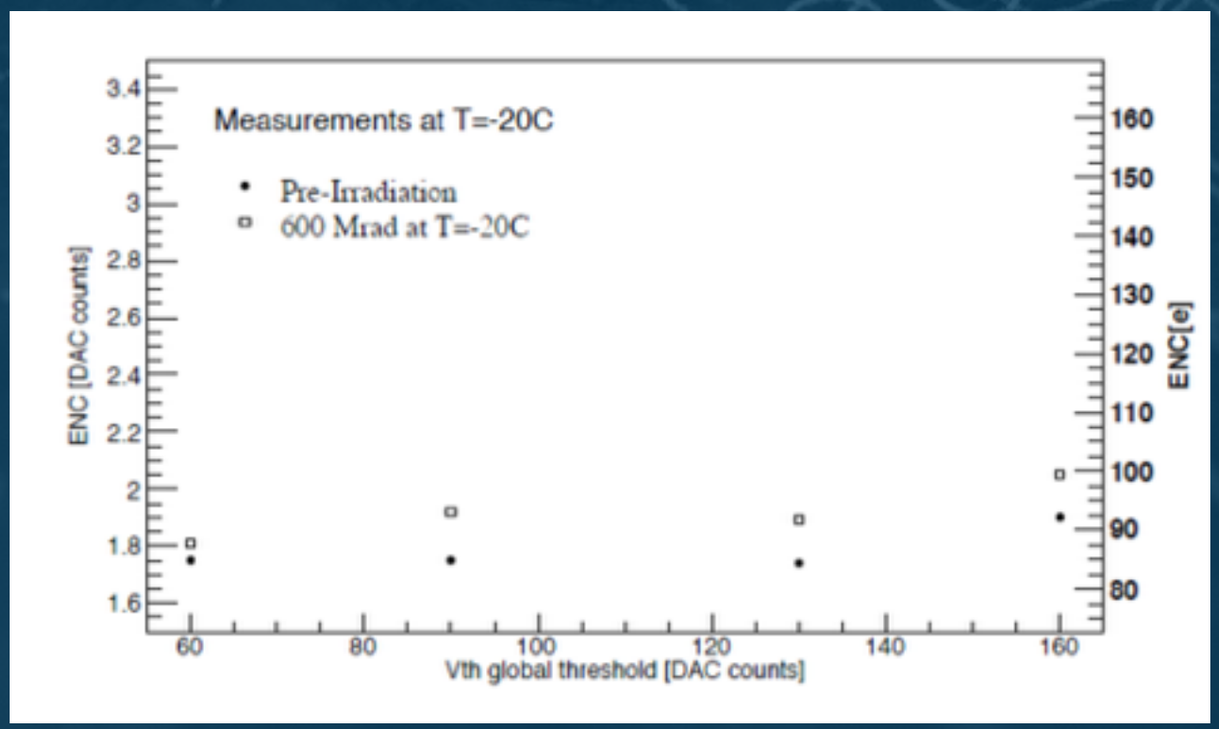
- “Auto-zeroing” mechanism to trim threshold
- Latch can be used as local Oscillator for fast ToT counting (up to 800MHz)

Sync. Front-End II

Threshold:

- Threshold DAC works linearly
- Dispersion only increases by ~10% after irradiation to 600MRad

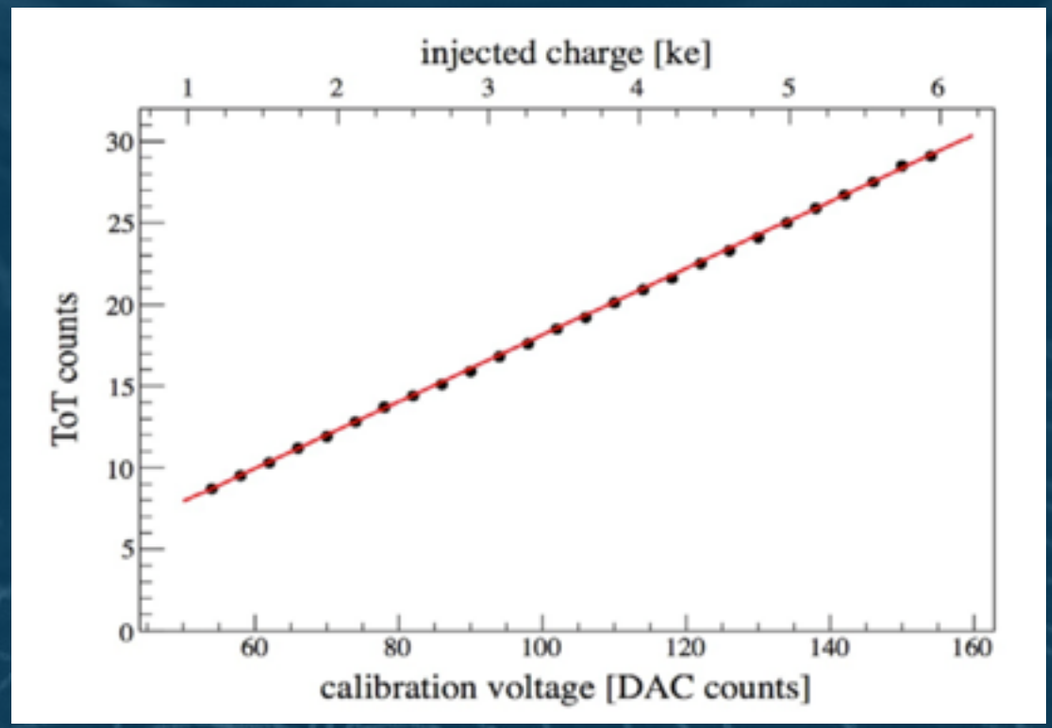




Equivalent Noise Charge:

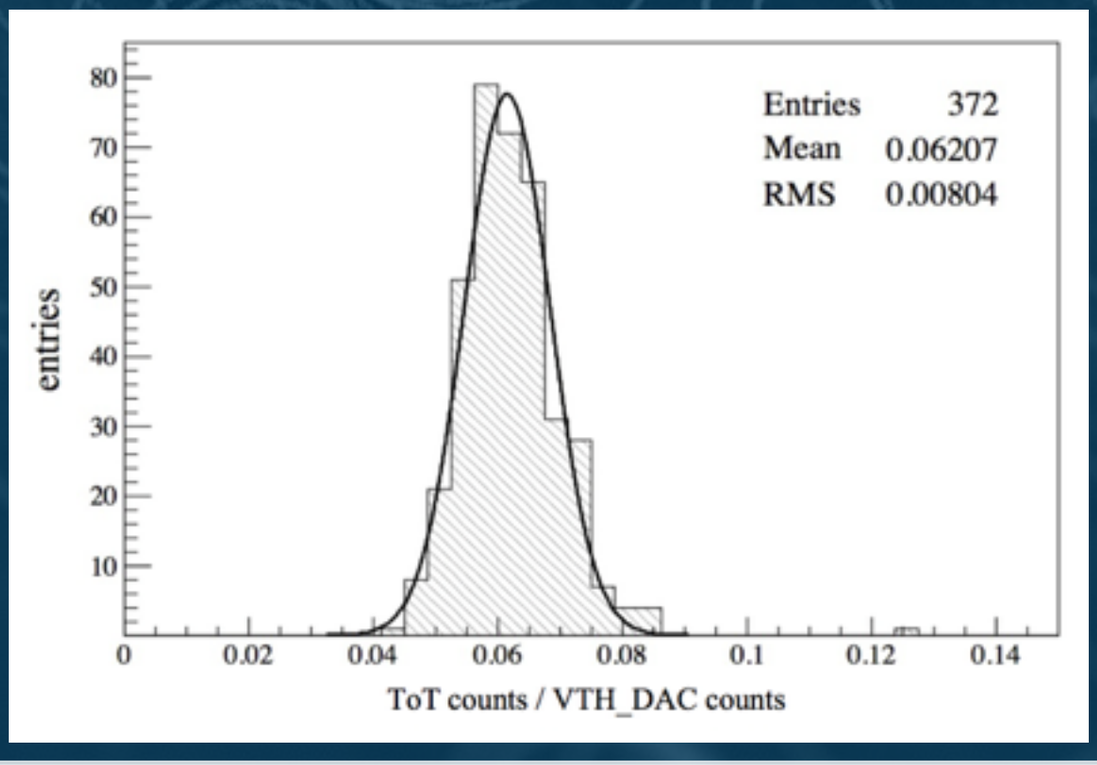
- ENC as predicted by simulation
- Only increases by 10% after irradiation to 600MRad

Sync. Front-End III

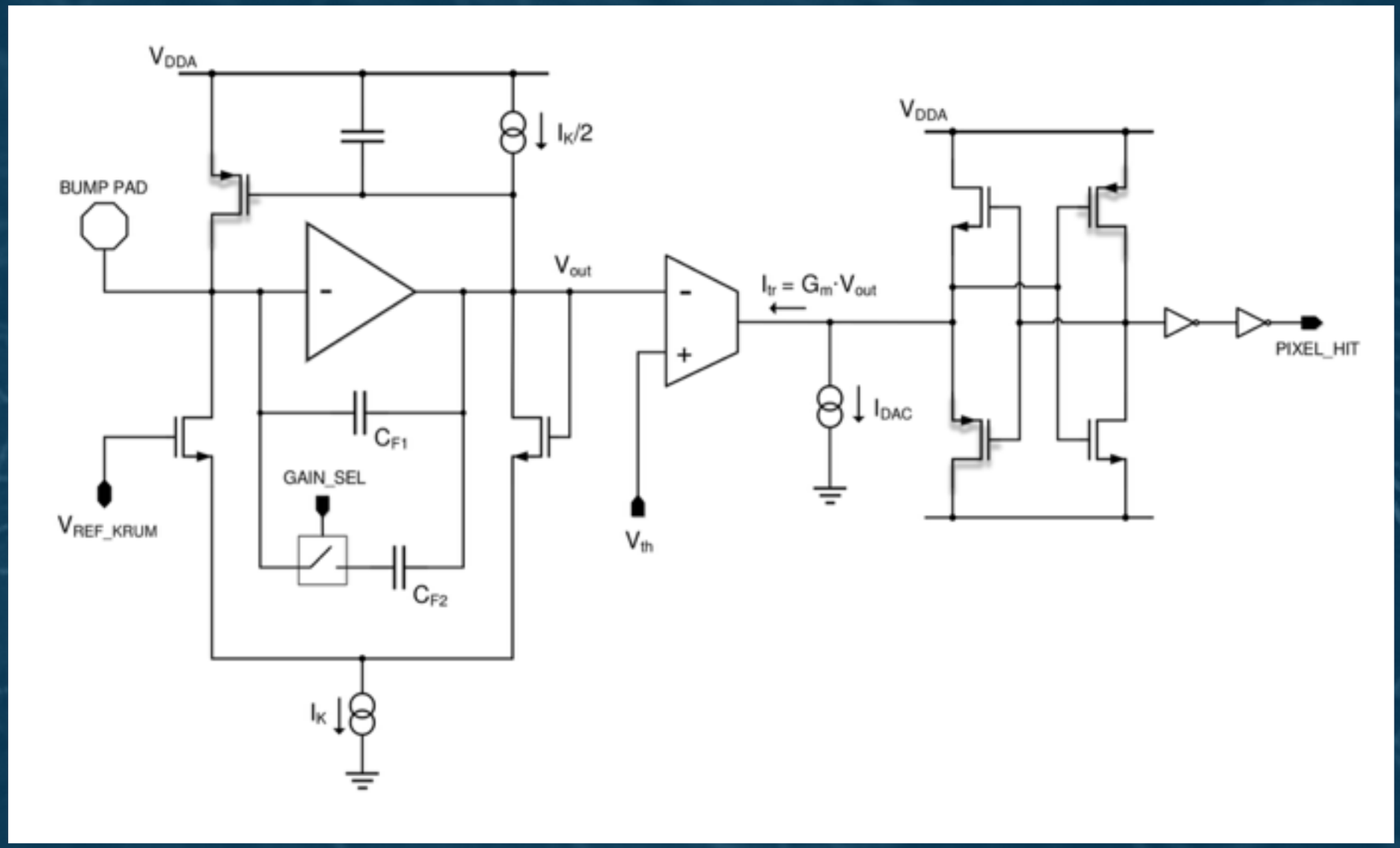


Charge Conversion:

- Used fast ToT counting with 320MHz
- Frequency will decrease due to radiation
- Mechanism tested after irradiation to 600MRad
- Good linearity for 5-bit ToT
- Acceptable dispersion of 10% due to transistor mismatch



Linear Front-End



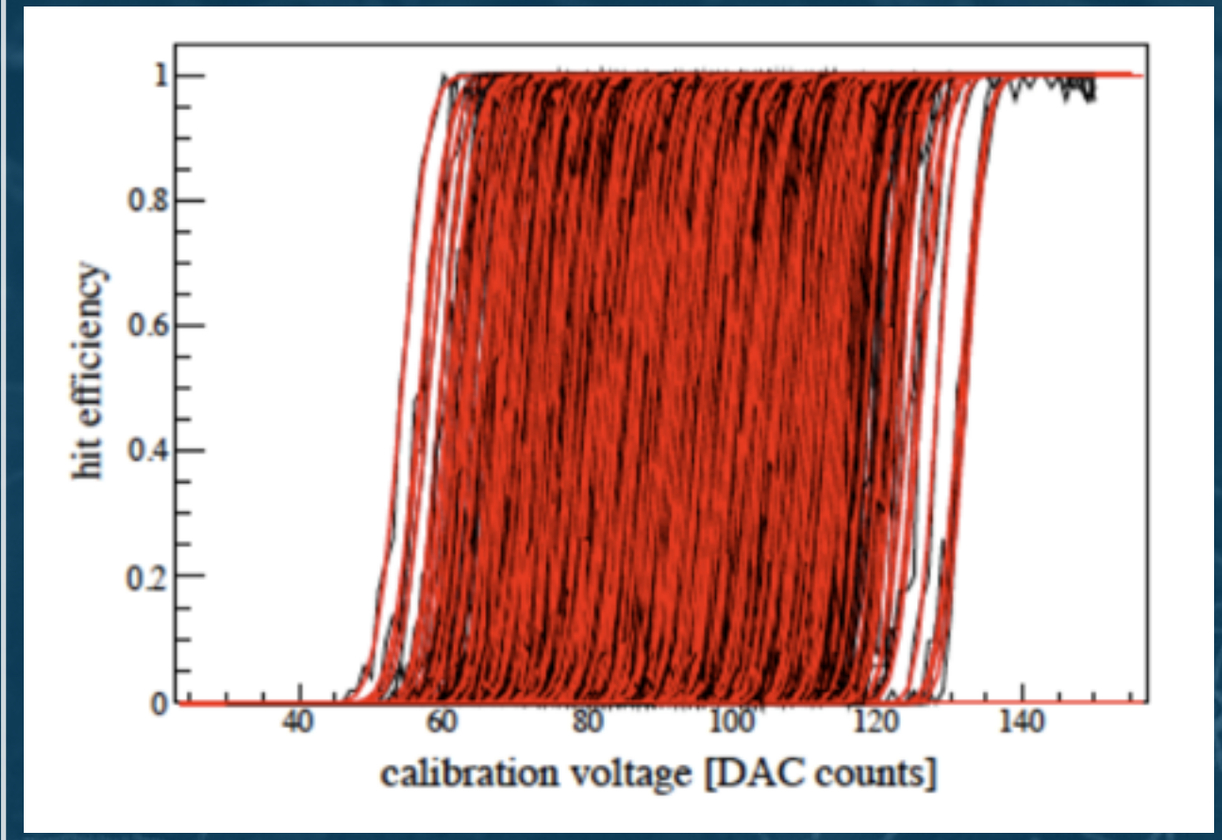
Charge Sensitive Amplifier:

- Folded cascode amplifier
- Selectable gain
- Krummenacher feedback
- Global setting for I_f (8-bit DAC)

Discriminator:

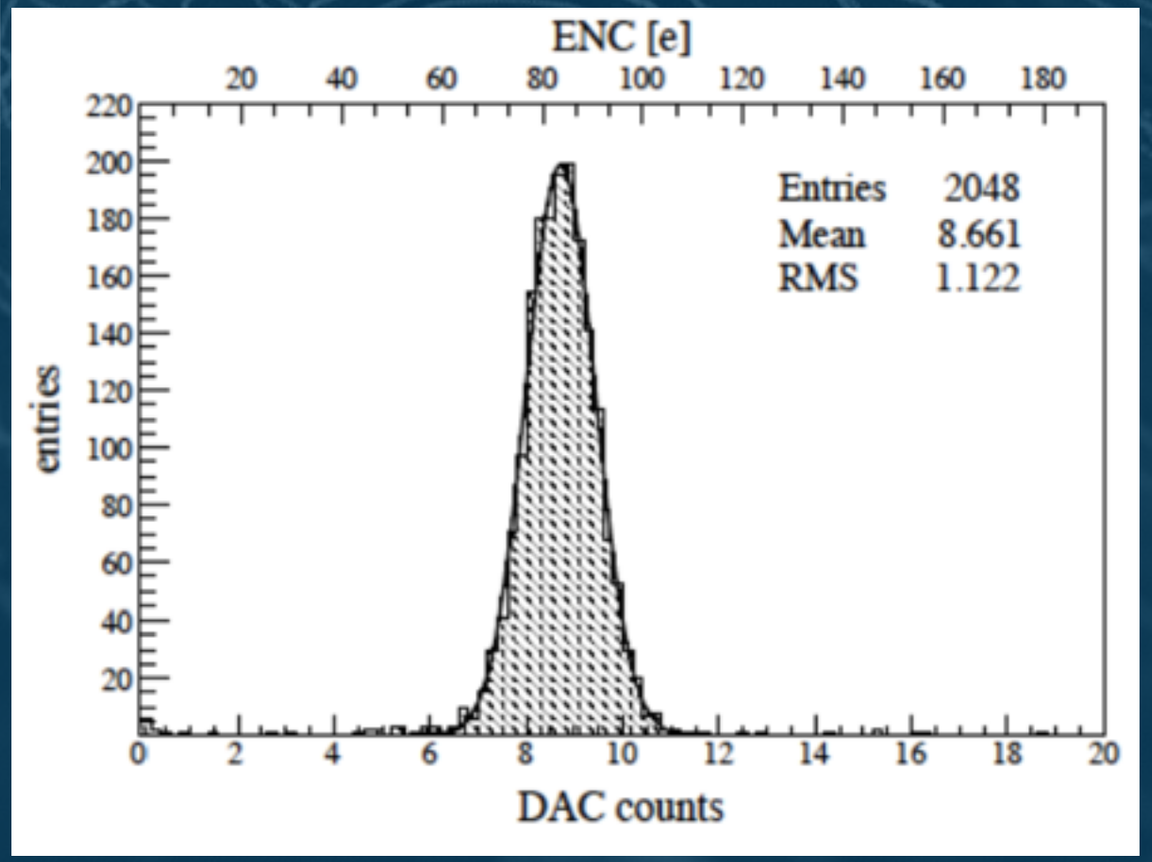
- Low power current comparator
- Per pixel 4-bit trim DAC

Linear Front-End II



Threshold:

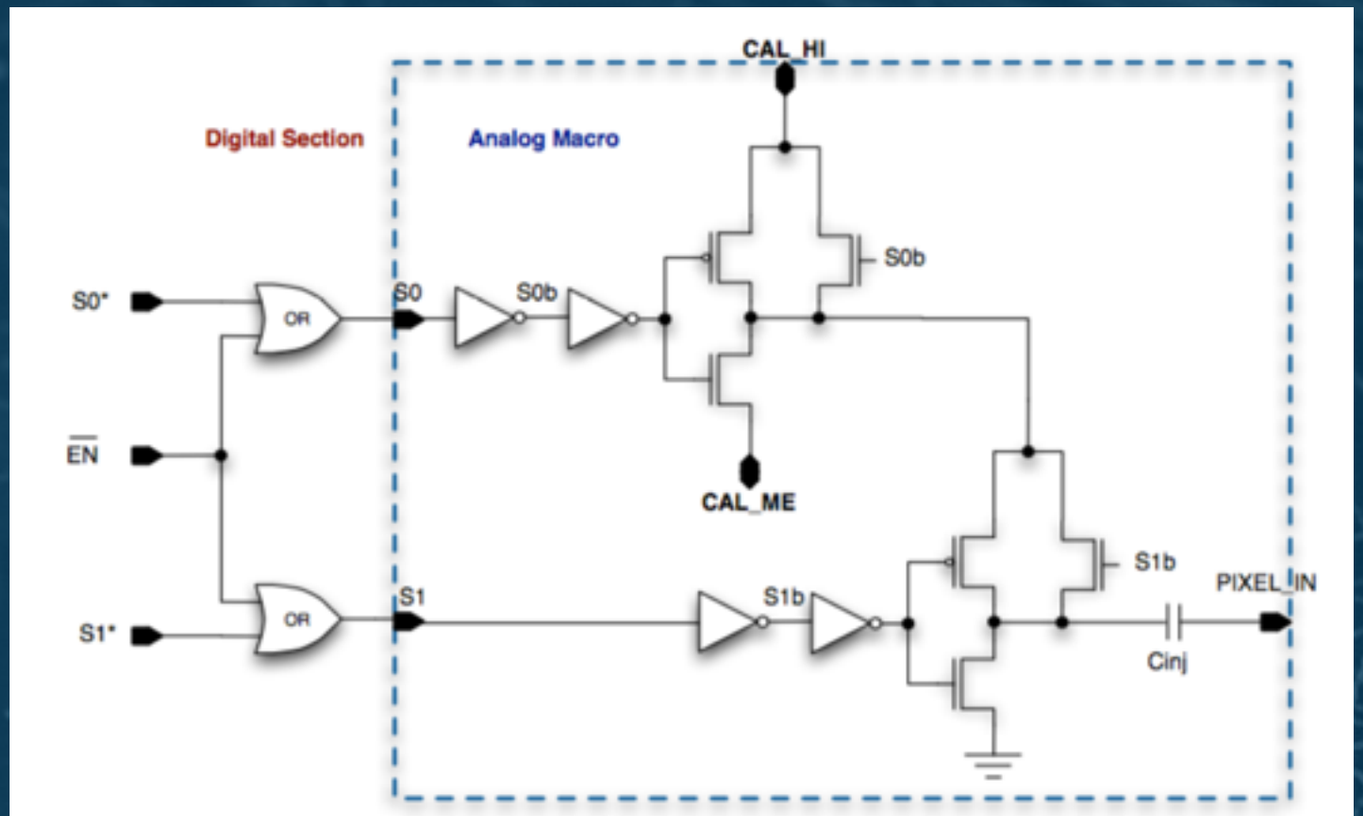
- 450e untrimmed calibration
- 125e after trimming, to be optimised by improving tuning procedure

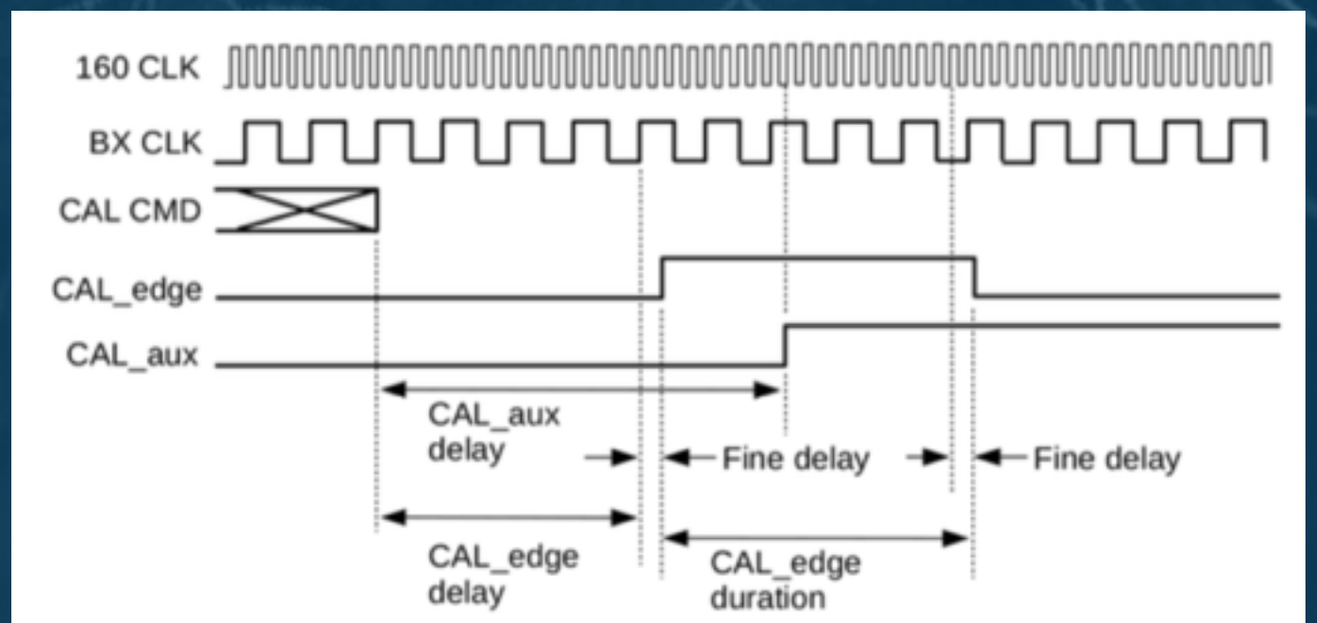


Equivalent Noise Charge:

- 85e noise w/o sensor

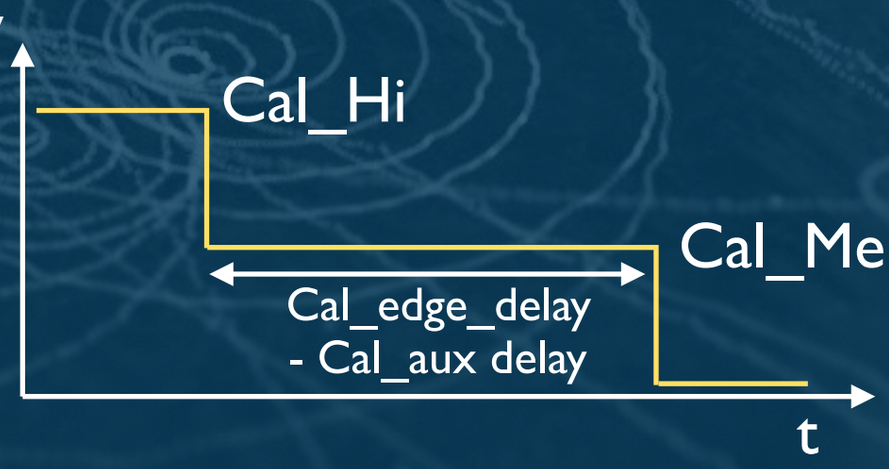
Calibration Circuit





Injection Pulse Generator:

- Can inject programmable charge into each pixel to calibrate response
- New: two step injection pulse enabling measurement of changes in pixel due to first injection



$$S0 = CAL\_edge \ \mathit{OR} \ CAL\_aux$$

$$S1 = \overline{CAL\_edge} \ \mathit{AND} \ CAL\_aux$$

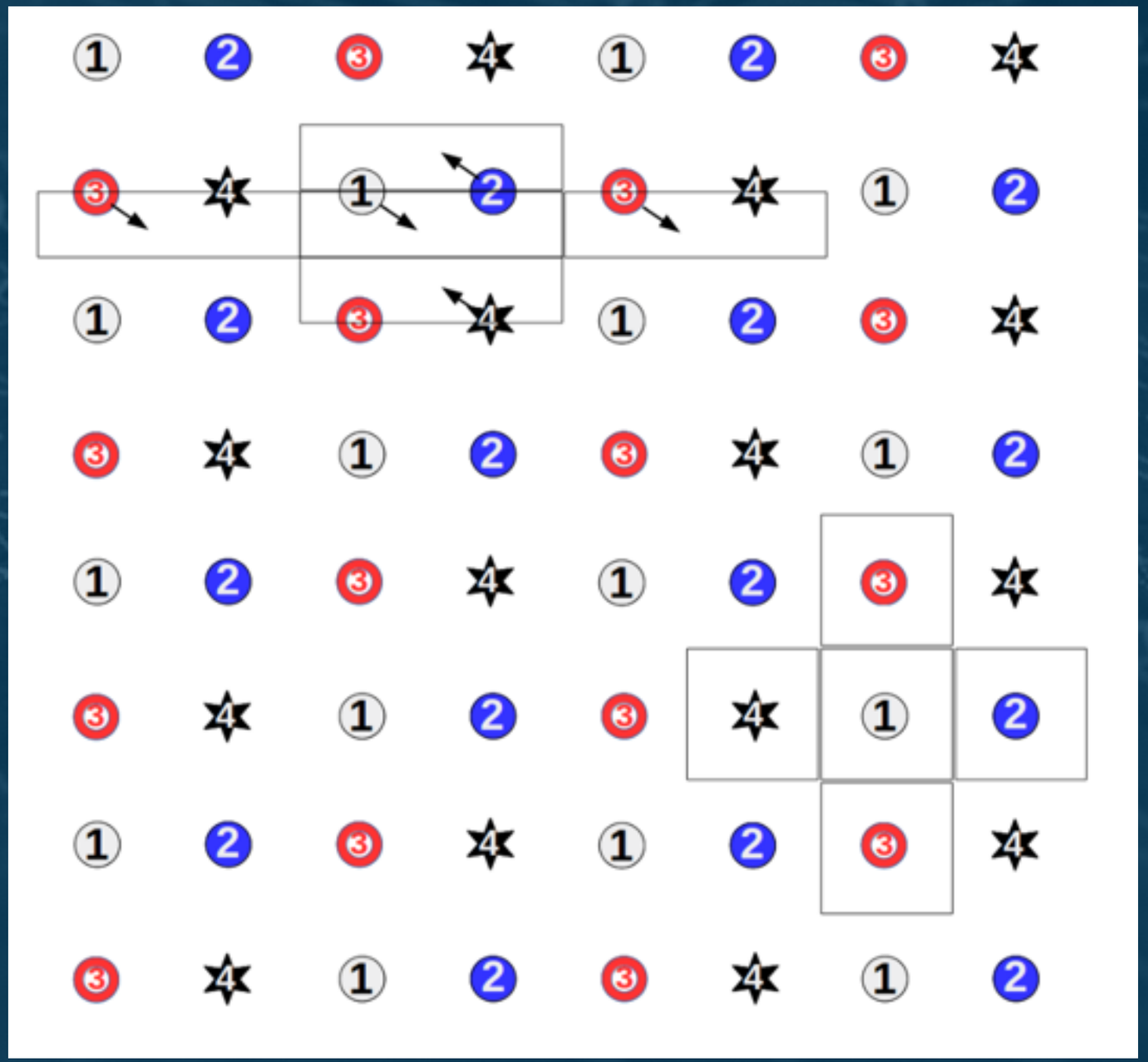
HitOr

HitOr Logic:

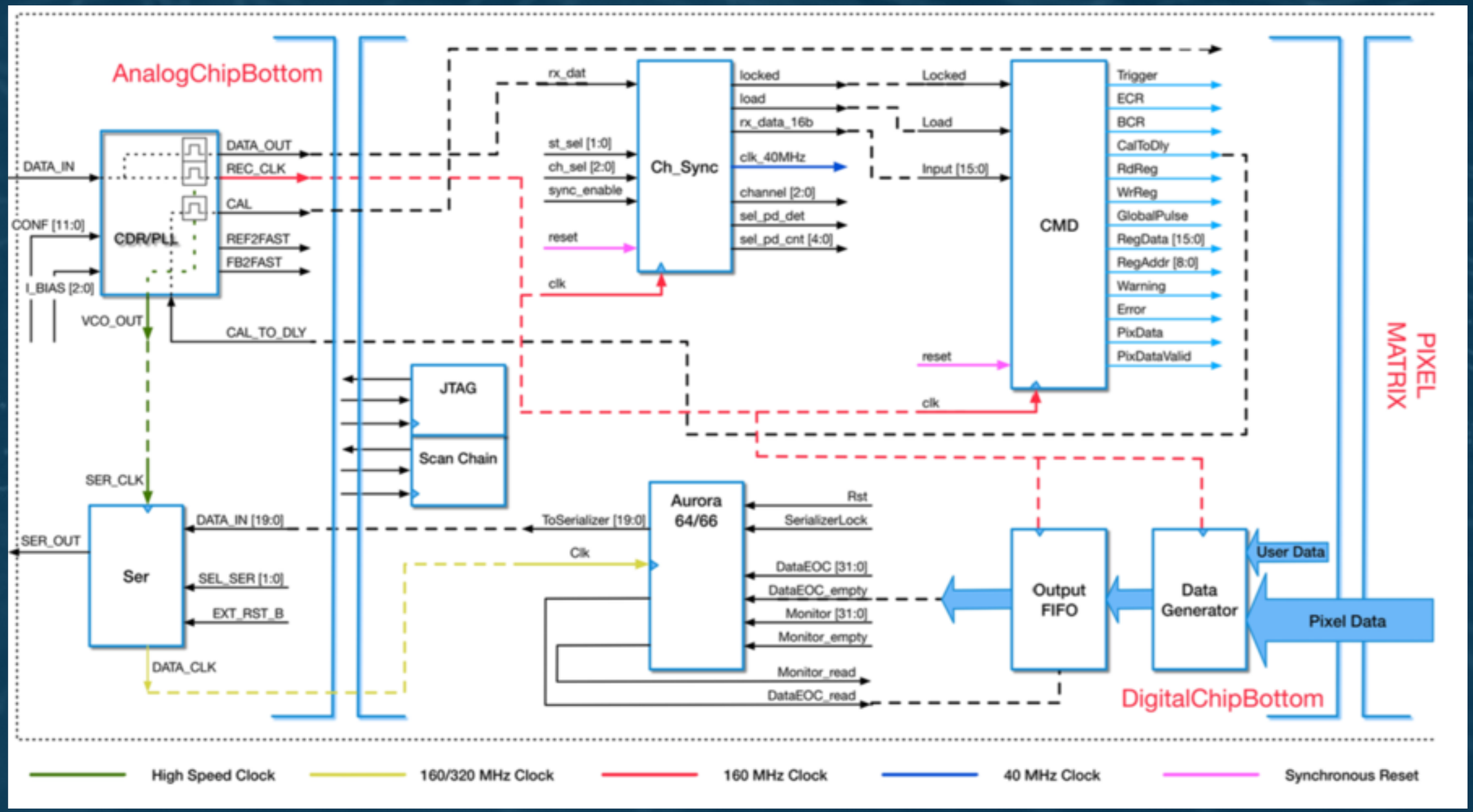
- Four different HitOr signals
- Signals organised in such a way to enable coincidence for specific cluster shapes (for both 50x50µm2 and 25x100µm2 sensors)

Selftrigger:

- Can use internal HitOr(s) to issue trigger
- Typically used for source scans
- New mechanism to trigger on cluster shapes could also be useful to use self trigger in other circumstances (test beam,



I/O


AnalogChipBottom
DATA_IN
CONF [11:0]
I_BIAS [2:0]
CDR/PLL
DATA_OUT
REC_CLK
CAL
REF2FAST
FB2FAST
VCO_OUT
CAL_TO_DLY
SER_CLK
SER_OUT
Ser
DATA_IN [19:0]
SEL_SER [1:0]
EXT_RST_B
DATA_CLK
JTAG
Scan Chain
rx_dat
st_sel [1:0]
ch_sel [2:0]
sync_enable
reset
clk
Ch_Sync
locked
load
rx_data_16b
clk_40MHz
channel [2:0]
sel_pd_det
sel_pd_cnt [4:0]
Locked
Load
Input [15:0]
reset
clk
CMD
Trigger
ECR
BCR
CalToDly
RdReg
WrReg
GlobalPulse
RegData [15:0]
RegAddr [8:0]
Warning
Error
PixData
PixDataValid
PIXEL MATRIX
ToSerializer [19:0]
Clk
Aurora 64/66
Rst
SerializerLock
DataEOC [31:0]
DataEOC_empty
Monitor [31:0]
Monitor_empty
Monitor_read
DataEOC_read
Output FIFO
Data Generator
User Data
Pixel Data
DigitalChipBottom
High Speed Clock
160/320 MHz Clock
160 MHz Clock
40 MHz Clock
Synchronous Reset

Command Input

CDR/PLL:

- 160Mbps command stream
- Custom encoding for DC balance
- Requiring frequent sync frames to ensure plenty of transitions

Command Encoding:

- 16-bit words
- Data encoded with custom 5-to-8-bit to ensure DC balance
- 15 x Trigger Cmds: 16-bit word sent with 160Mbps covers 4 bunch crossing, need to encode all possible trigger positions

Command	Encoding	ID/(A)ddress/(D)ata 5-bit Fields					
ECR	2× 0101_1010						
BCR	2× 0101_1001						
Glob. Pulse	2× 0101_1100	ID<3:0>,0	D<4:0>				
Cal	2× 0110_0011	ID<3:0>,D15	D<14:10>	D<9:5>	D<4:0>		
WrReg	2× 0110_0110	ID<3:0>,0	A<8:4>	A<3:0>,D<15>	D<14:10>	D<9:5>	D<4:0>
WrReg	2× 0110_0110	ID<3:0>,1	A<8:4>	A<3:0>,D<15>	D<14:10>	9×(D<9:5>	D<4:0>)
RdReg	2× 0110_0101	ID<3:0>,0	A<8:4>	A<3:0>,0	00000		
Noop	2× 0110_1001						
Sync	1000_0001_0111_1110						

Why not 8b10b? → Synchronous trigger

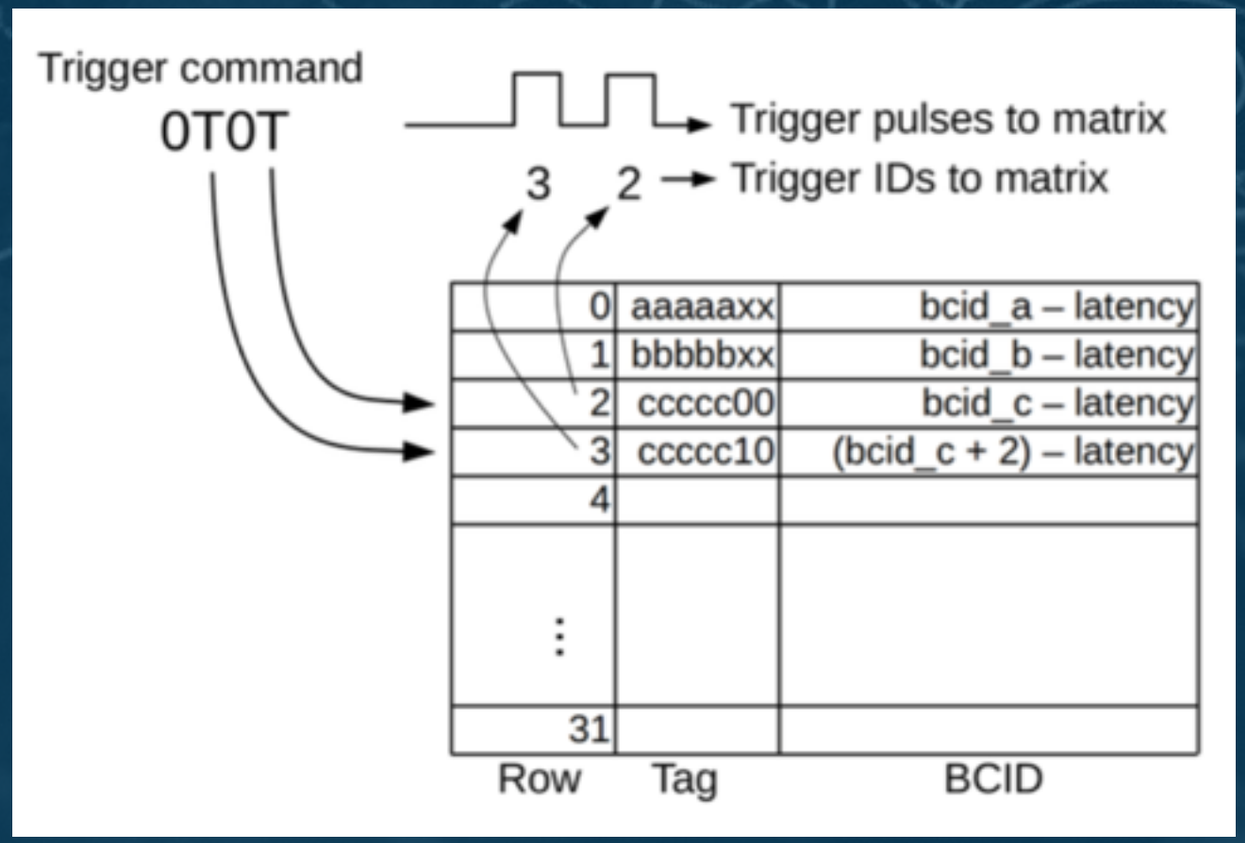
Trigger Tagging

W/o tagging:

- All readout chips had their own bunch crossing counter
- All chips had to be synchronised, if counter slipped all future hits being read out would be invalid as they could not be matched
- Mayor issue in the current detector to keep all chips synchronised for a long time

With tagging:

- DAQ sends 5-bit trigger tag to chip
- Chip creates table with which tag corresponds to which bunch crossing id
- On receiving data for a tag, DAQ adds correct bunch crossing id
- Chips do not needs to be synchronised anymore



Trickle Configuration

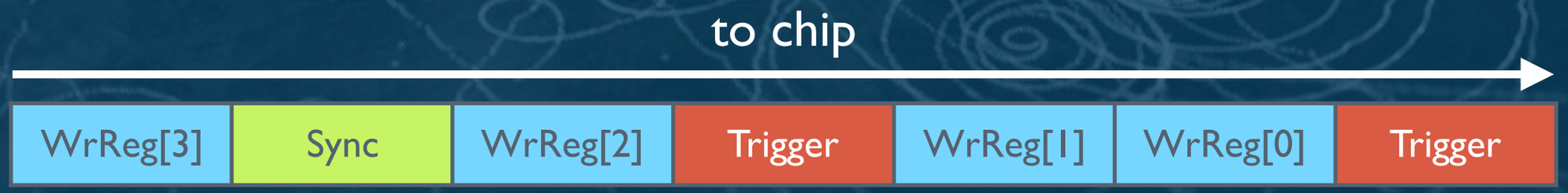
Single Event Upsets:

- Very high SEU rate at HL-LHC
- Not enough space in pixel array to make pixel registers SEU hard
- ~1% of bits corrupted by SEUs per second
- Need to avoid “de-configuration” in some other way

→ Continuously re-configure pixel (and global registers)

Command Stream:

- Need multiple 16-bit frames to write to any register
- Write/Read register commands do not need to be contiguous, can fill gaps in between trigger/sync frames
- Cmd Stream priority:
  - Trigger
  - Sync
  - Write/Read Register



Back of the envelope:

- 1MHz trigger stream max. bandwidth is 16Mbps
- 1 sync frame every 32 frames = 5Mbps
- ~130Mbps available to “trickle” configuration
- Full config data stream is ~350kB = 17.5ms

Data Output

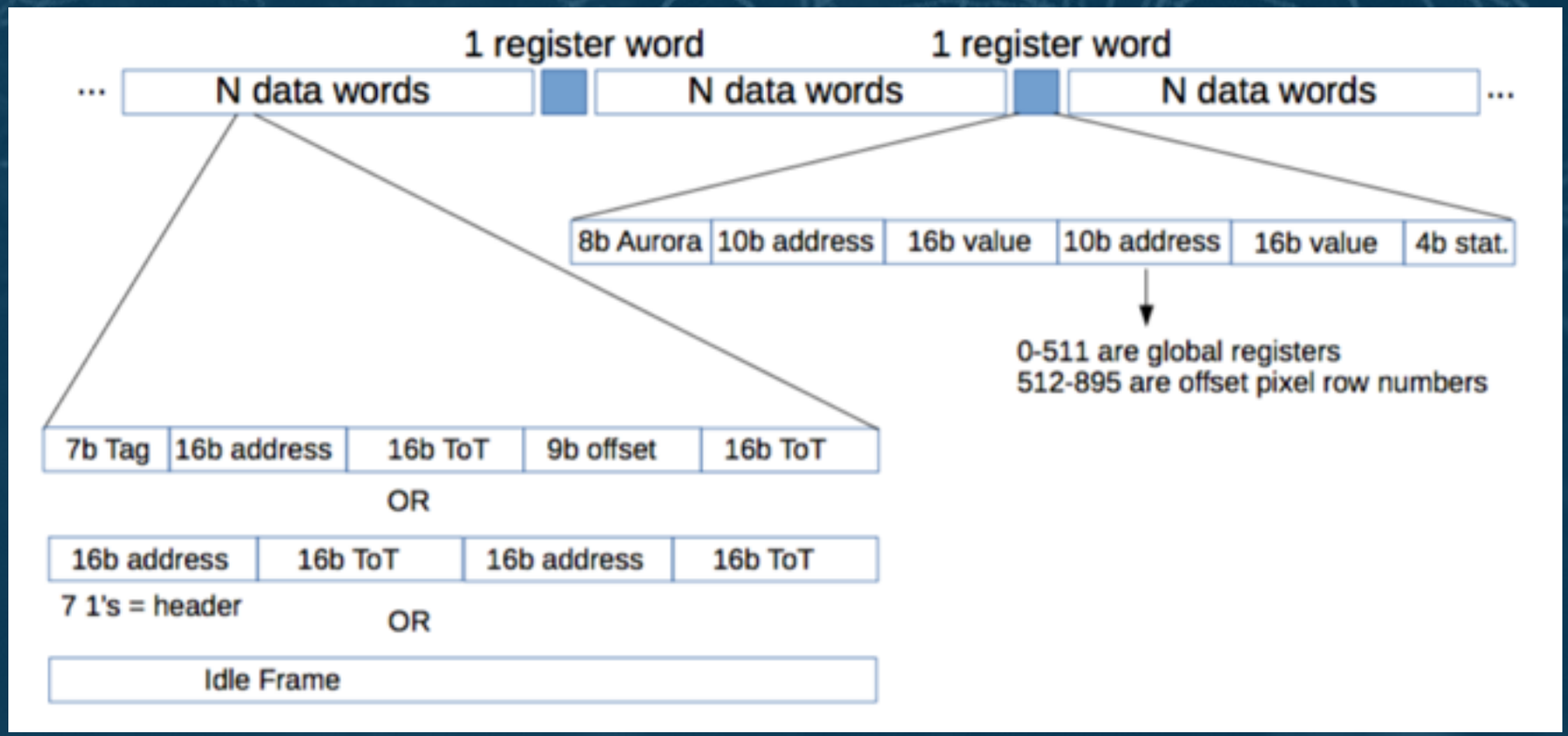
Aurora 64b/66b protocol:

- Trying to make life easier for DAQ
- established protocol available for Xilinx FPGA multi gigabit transceiver
- 64-bit frames, scrambled to ensure DC balance
- 2-bit sync header
- Register words every N data/idle words
- Inherent multi lane support

Bandwidth:

- Innermost layer has highest occupancy: 10-3 per pixel per bc
- 400x400 pixels per chip = 160 hits per bc
- Max one 64-bit frame for 2 hits
- Required bandwidth for 1MHz trigger rate → 5.128 Gbps

→ 4 x 1.28Gbps data output lanes



High Speed Serialiser

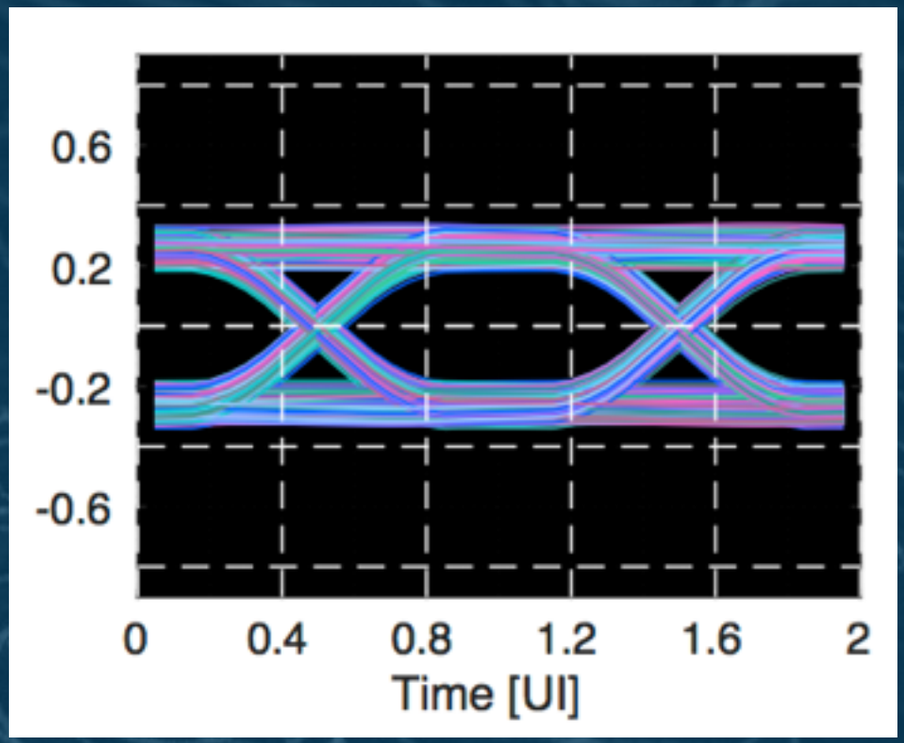
The Original Plan:

- Need to reduce mass of detector
- One 5Gbps cable has less mass than four 1.28Gbps (and less volume)
- Need to transmit electrically for about ~6-9m before we convert to optical
- Cable results look promising

Reality:

- Need very low jitter on 5Gbps output (<100ps)
- But we recover the clock from slow (160Mbps) command stream
- Multiplying clock and possible jitter up to 5GHz, currently too challenging
- Might even result in too much jitter for 1.28Gbps (will depend on CDR/PLL performance)

5,128Gbps, 64b66b, DFE, PreEmph.

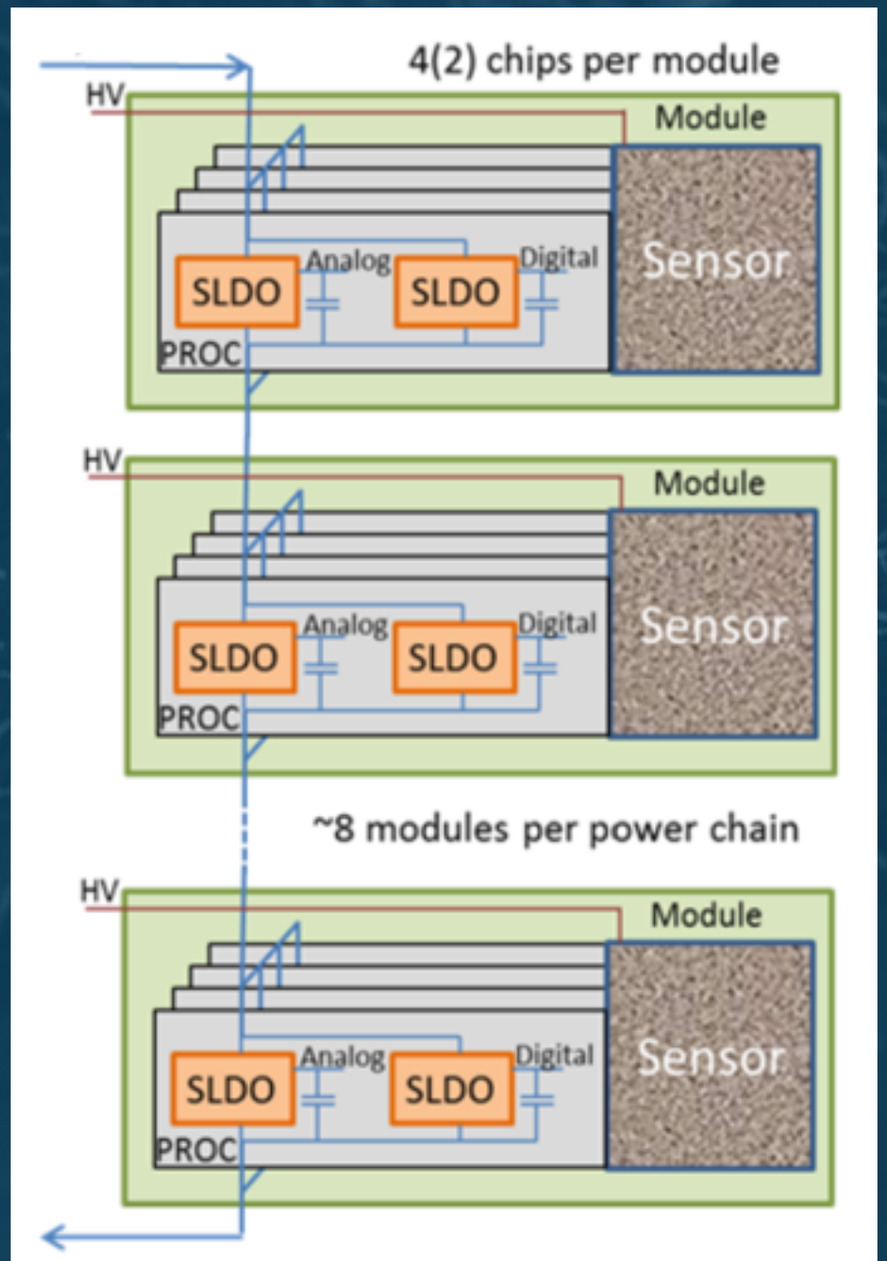


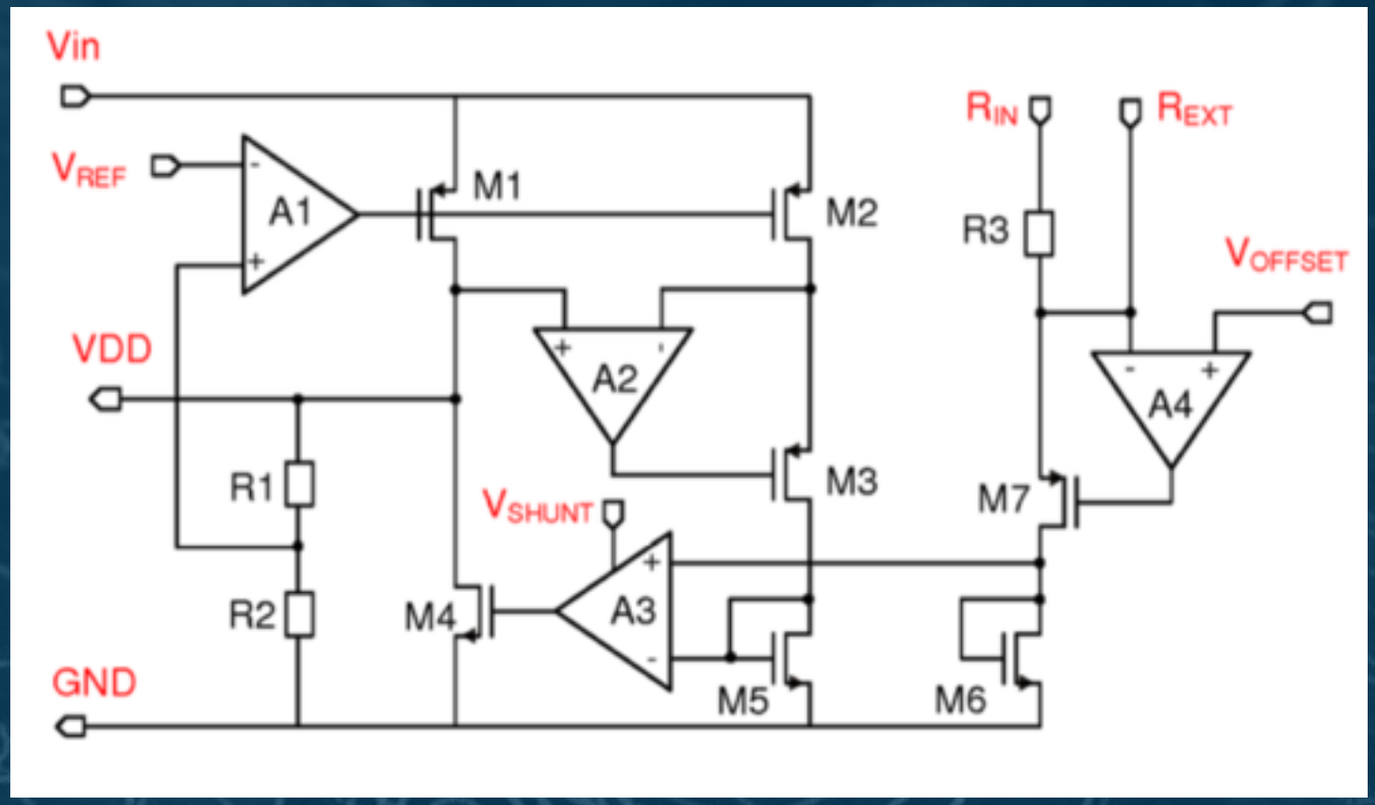
Possible solutions:

- Data output does not need to be synchronous to 40MHz LHC clock
- Can recover any clock in DAQ (to some degree)
- Clock serialiser from local clock generator (e.g. lpGBT LC circuit)

Serial Powering

Example of serial powering chain:





ShuLDO:

- Similar circuit to FE-I4 but adapted to 65nm and ~2x current
- Shunt burns excess current, looks like resistor to the outside
- Can daisy chain multiple modules and run power supply in constant current mode

→ Reduces amount of necessary power cables and therefore mass in the tracker

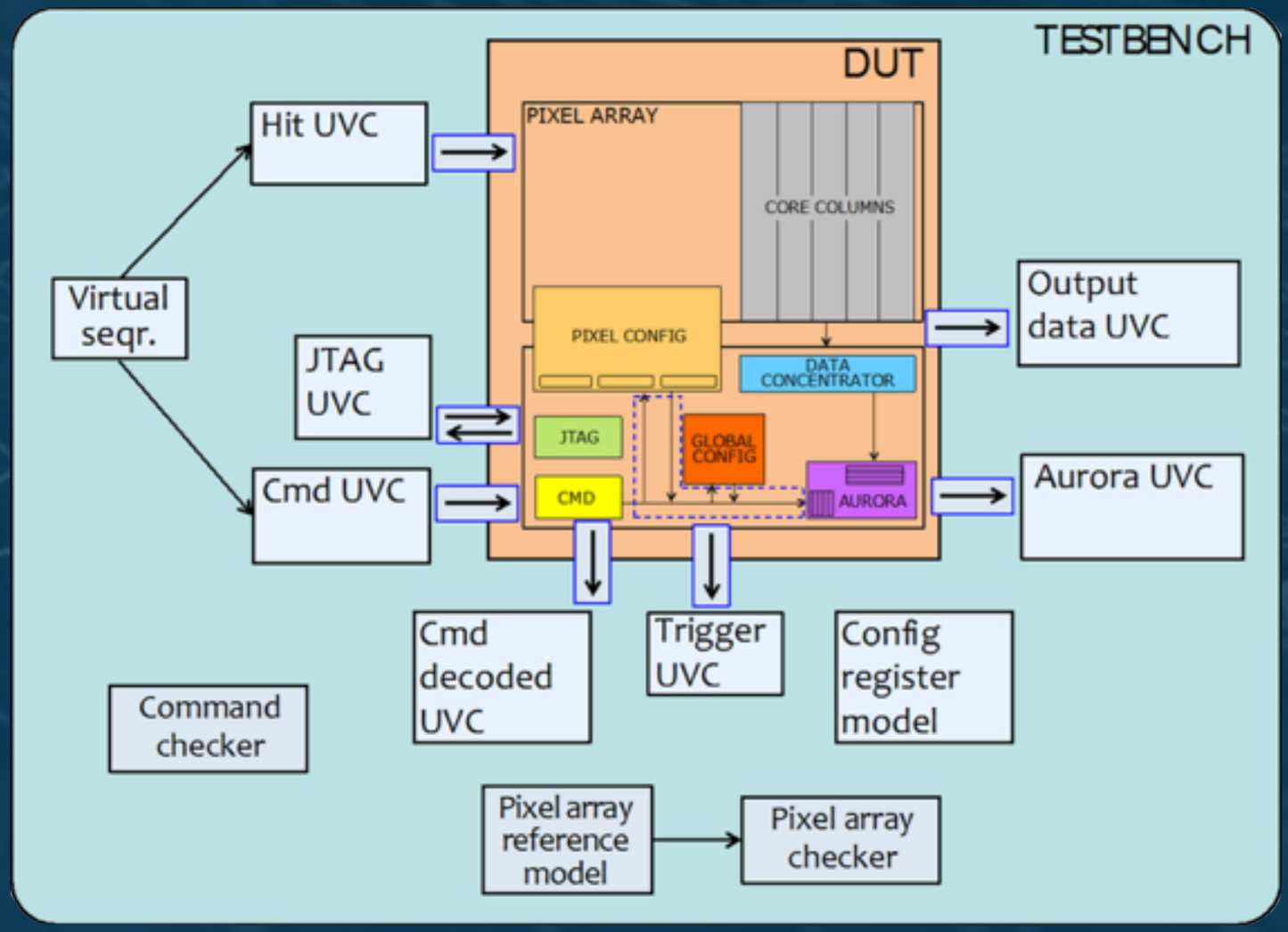
Verification

Testbench:

- UVM based verification model
- Main interfaces: Hit input, Command input, JTAG input, and Aurora output
- Automated verification components:
  - Pixel hit output prediction
  - Configuration register model

Verification types:

- Constrained random test (e.g. random hit input, or automated global register verification)
- Directed tests (custom command sequence)
- Stimuli for analog simulation



Preprations for Testing

DAQ:

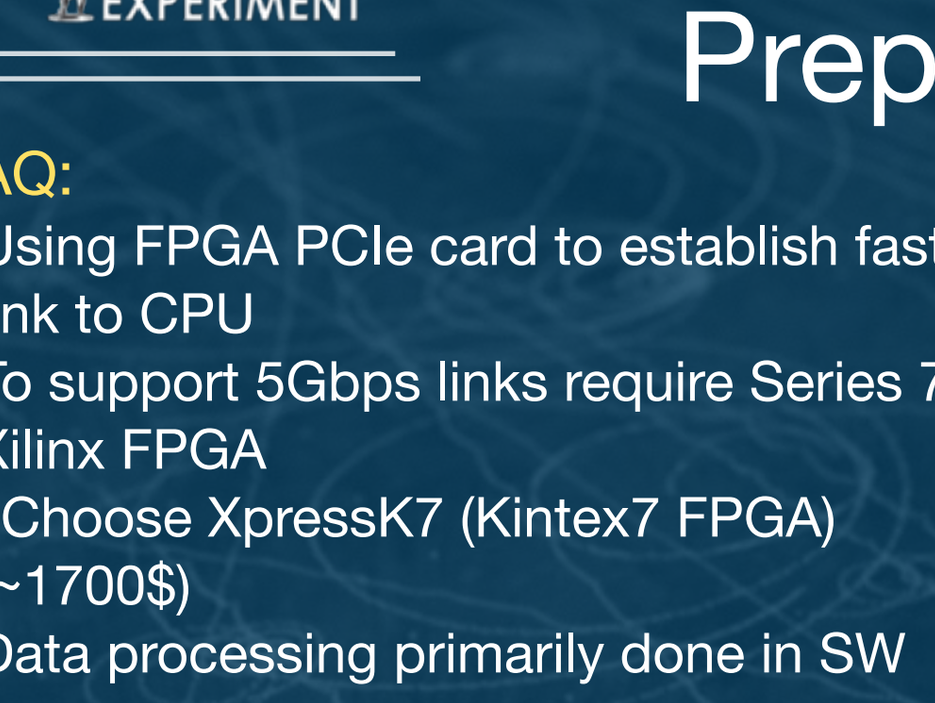
- Using FPGA PCIe card to establish fast link to CPU
- To support 5Gbps links require Series 7 Xilinx FPGA

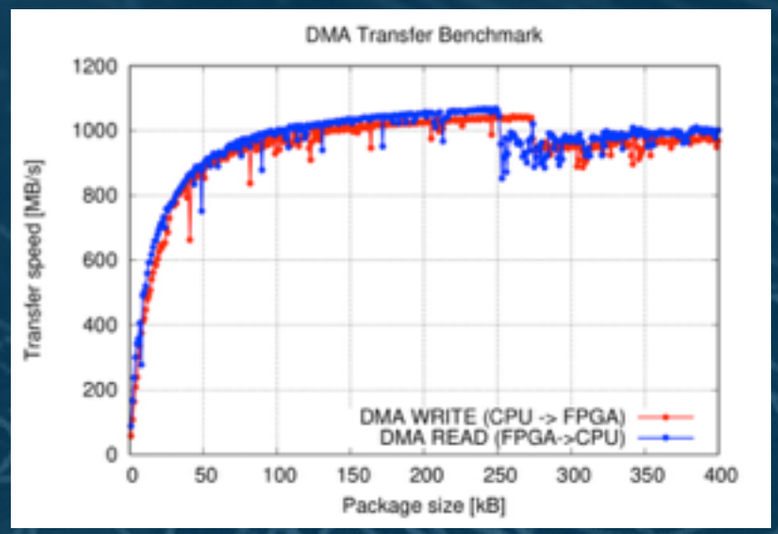
→ Choose XpressK7 (Kintex7 FPGA) (~1700$)

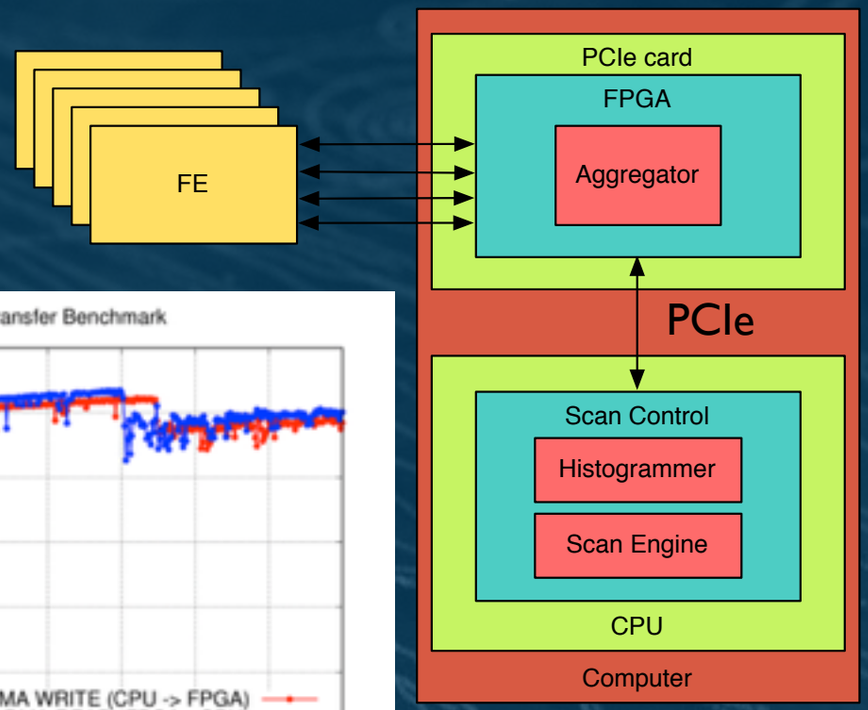
- Data processing primarily done in SW

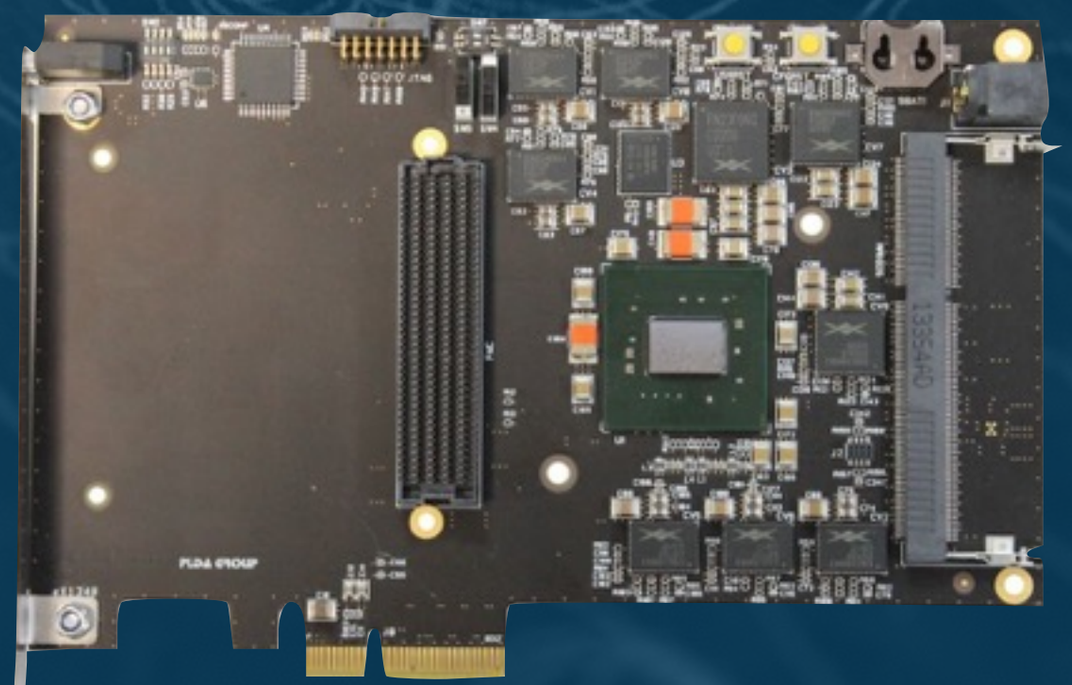
Wafer probing:

- Will perform 12-inch wafer probing
- Preparations going on in IC group lab









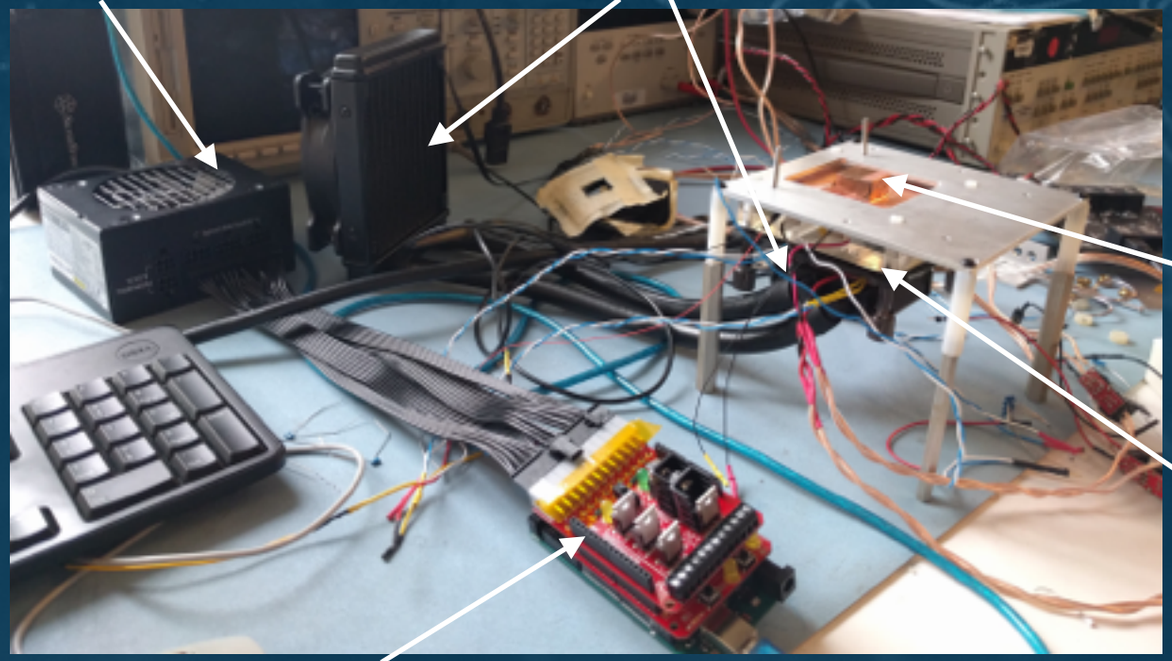
Preparations for Testing II

Cooling:

- In serial powering mode a single RD53A chip will dissipate up to 4W
- Quad chip modules will dissipate 16W

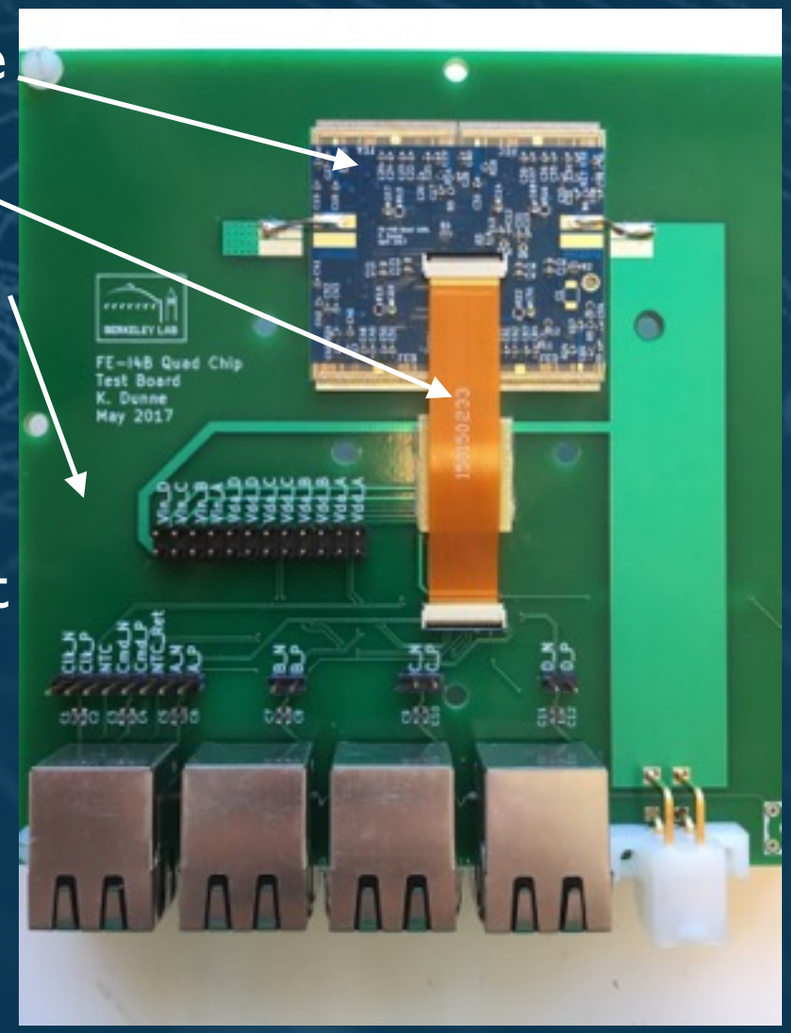
→ Need cooling solutions which can be used to easily support many testing setups

→ Developing Peltier based cooling setup, reducing the price per cooling unit by reusing commercial components



Module Protoyping:

- RD53A flex module serial powering chains
- Test interconnect schemes
- Preparations ongoing with FE-I4

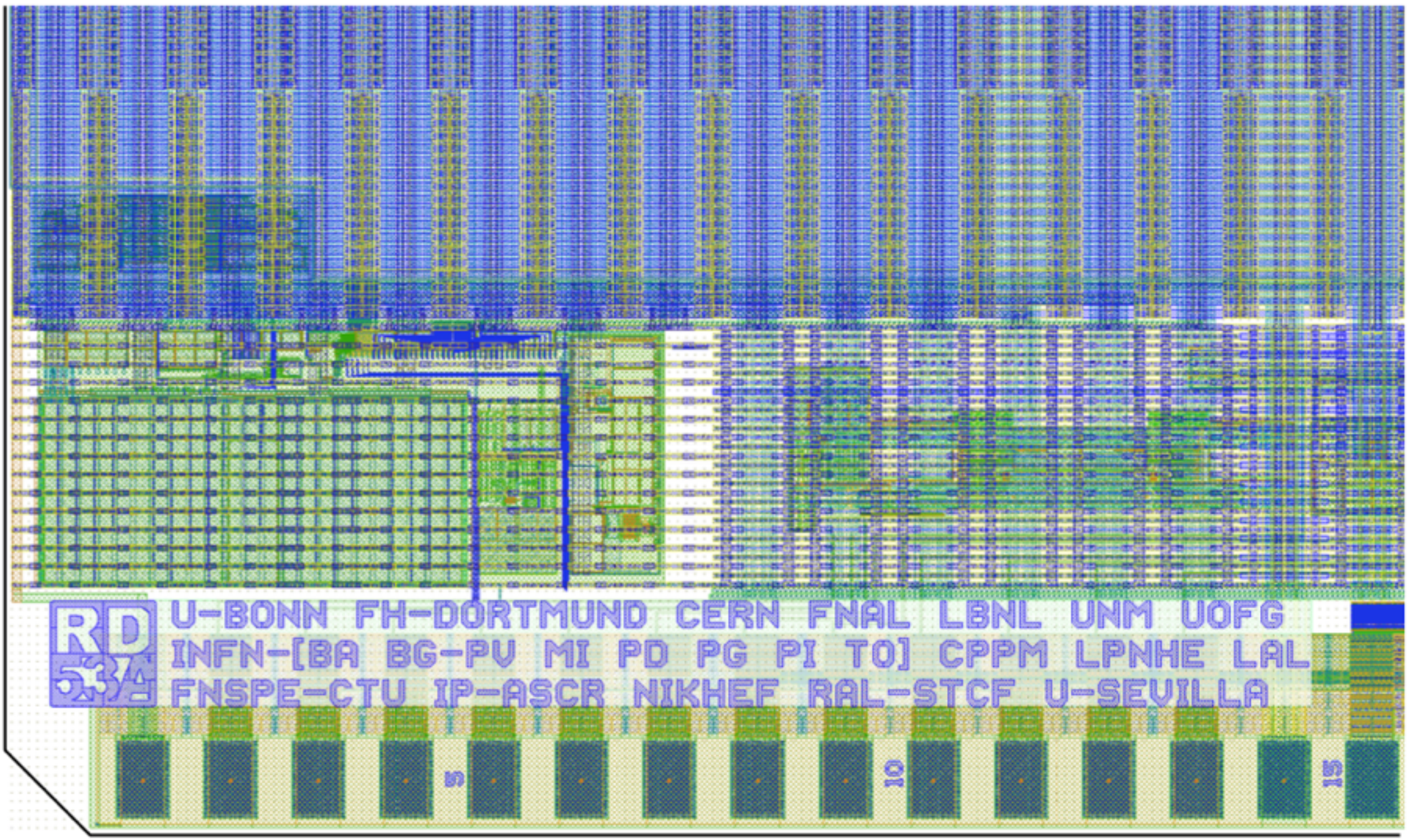


Summary and Conclusion

- RD53A is the first large scale 65nm pixel readout demonstrator chip developed by the RD53 collaboration
  - 76,800 x 50x50μm2 pixels
  - Three analog front-end types
  - All bells and whistles required for a real pixel readout chip
  - 4x1.28Gbps high speed data outputs
- Too be submitted very very soon!

Outlook for the next chip

- Many features did not make it into RD53A, but will be implemented into the ATLAS specific chip:
  - 5Gbps serialiser and driver
  - Non-linear ToT: increase ToT resolution in low/high ToT region
  - Auto-tune mechanism: automatically tune thresholds by measuring noise occupancy
  - Data compression: Use bandwidth more effectively
  - 80MHz ToT counting: use both edges to count ToT
  - 8-bit ToT count: combine two 4-bit memory to save one 8-bit ToT
  - Event truncation: cut-off events larger than a certain size


RD
53A
U-BONN FH-DORTMUND CERN FNAL LBNL UNM UOFG
INFN-[BA BG-PV MI PD PG PI TO] CPPM LPNHE LAL
FNSPE-CTU IP-ASCR NIKHEF RAL-STCF U-SEVILLA
5
10
15

Backup

RD53A Overview II

Powering:

- Separate internal analog and digital DCDC regulators
- Integrated shunt-mode for serial powering
- Estimated power consumption: 0.75A @ 1.5V (1.2V internally)

Analog Front-Ends:

- Contains three different types of analog front-end for testing:
  - Synchronous
  - Linear
  - Differential
- All front-ends were tested in two prototype chips with 64x64 pixel:
  - Chipix65: Synchr. & Linear
  - FE65P2: Differential

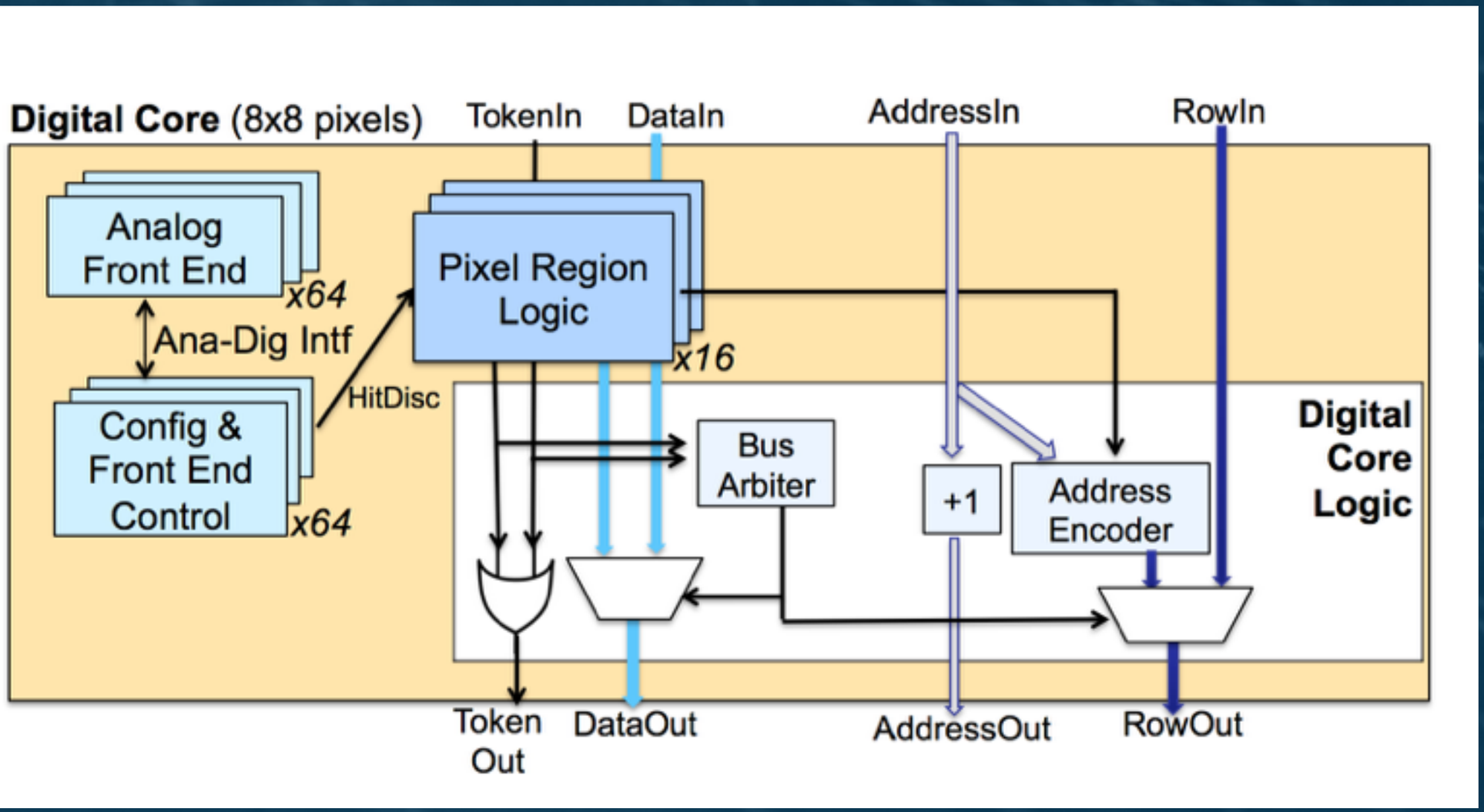
Periphery:

- Monitoring ADC
- Reference current
- Bias DACs
- 2-level Injection pulse generator
- Power-On-Reset
- PLL

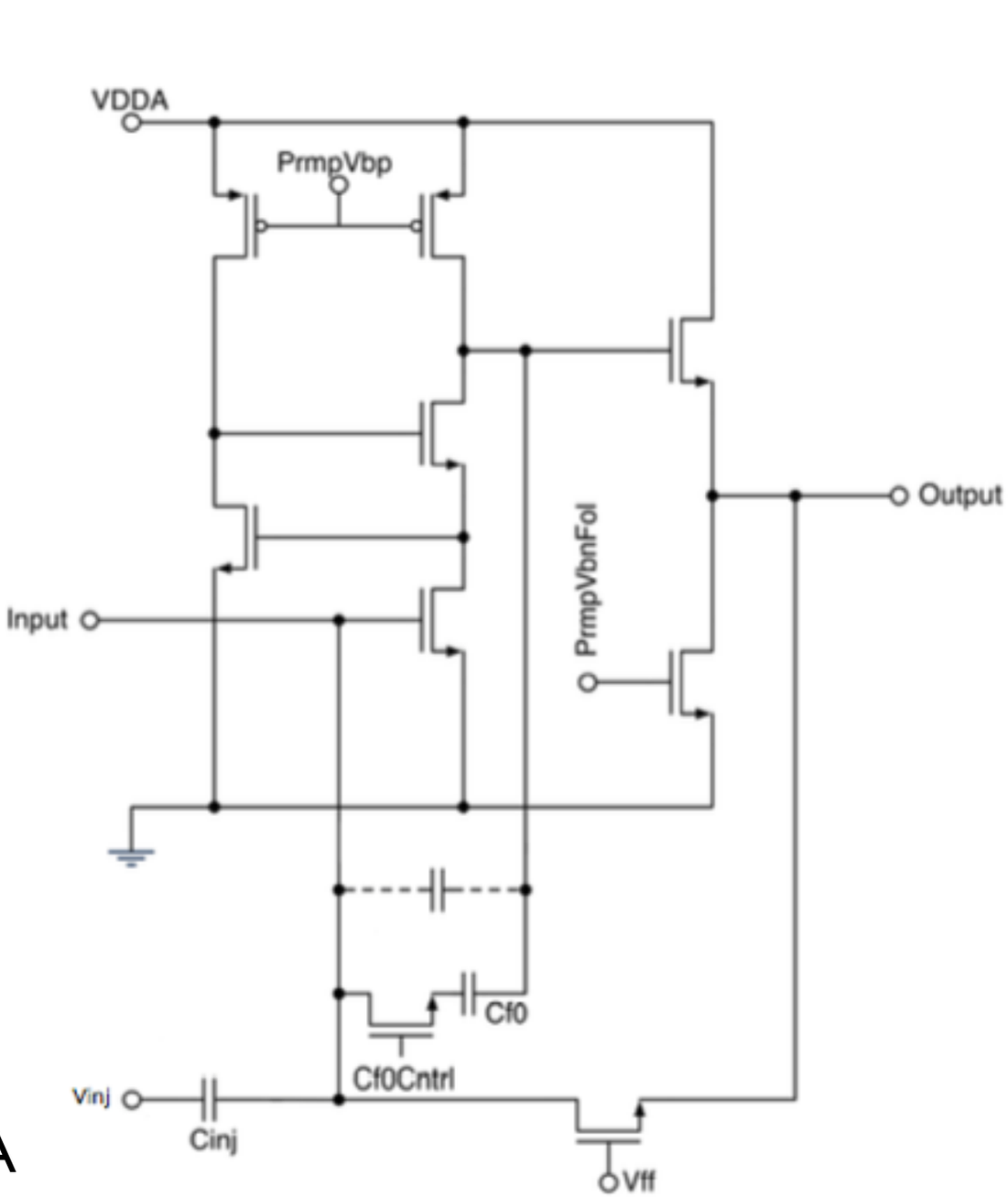
I/O:

- 160Mbps custom encoded DC balanced command input
- 160MHz Clock recovery from command stream
- Trigger tagging
- Four 1.28Gbps data output serialisers using Aurora protocol
- JTAG

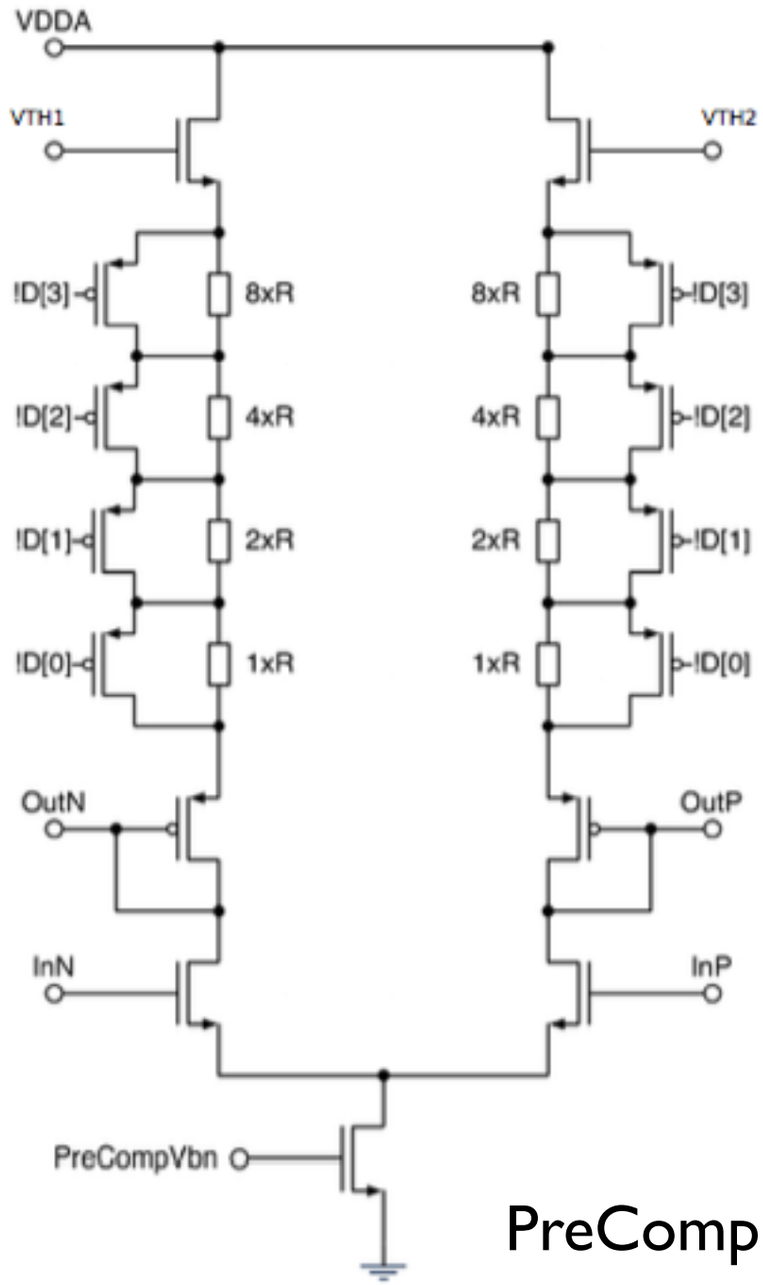
Digital Core



Diff. Front-End Schematic

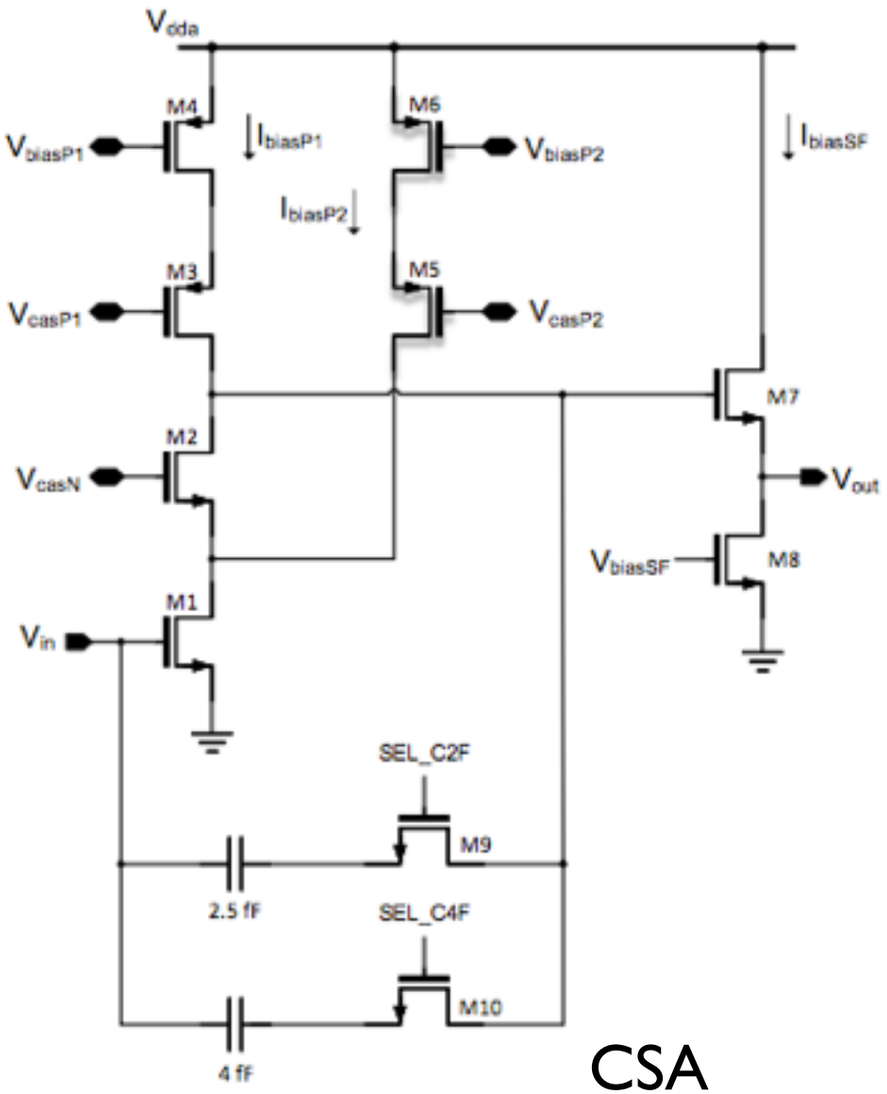


CSA

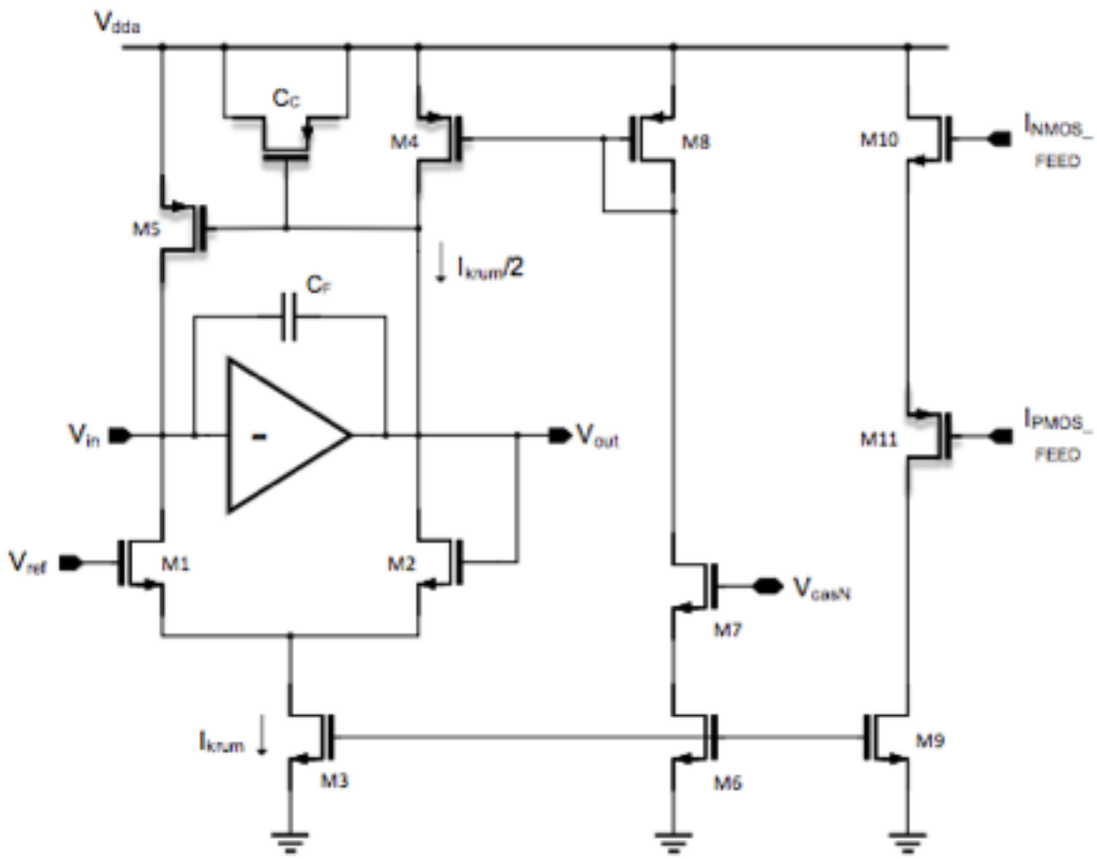


PreComp

Sync. Front-End Schematic

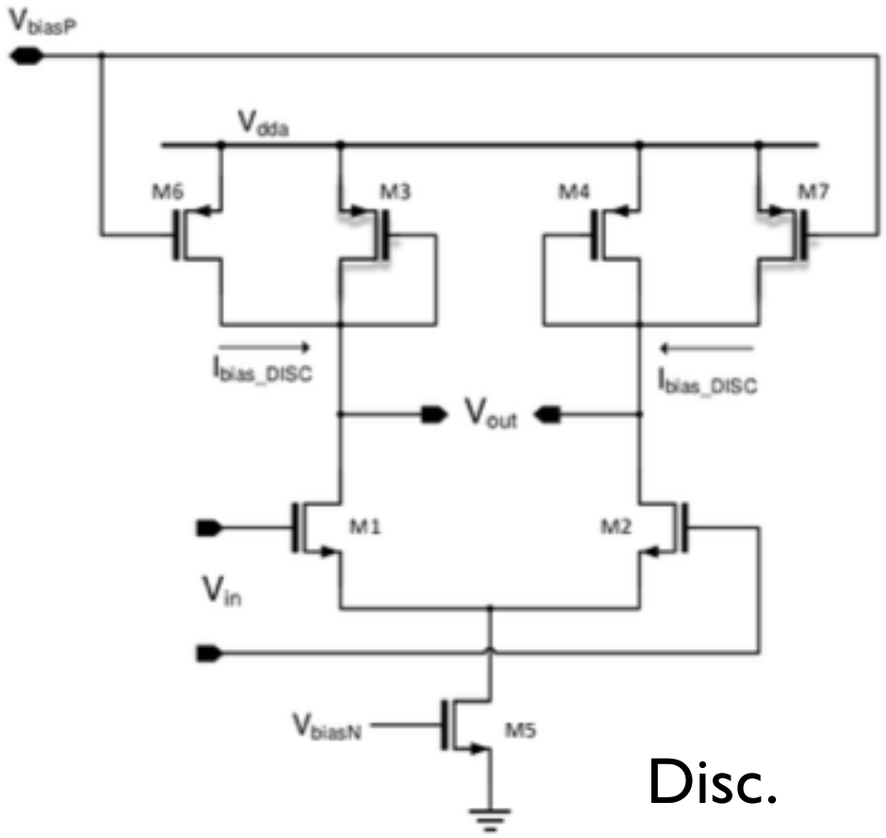


CSA

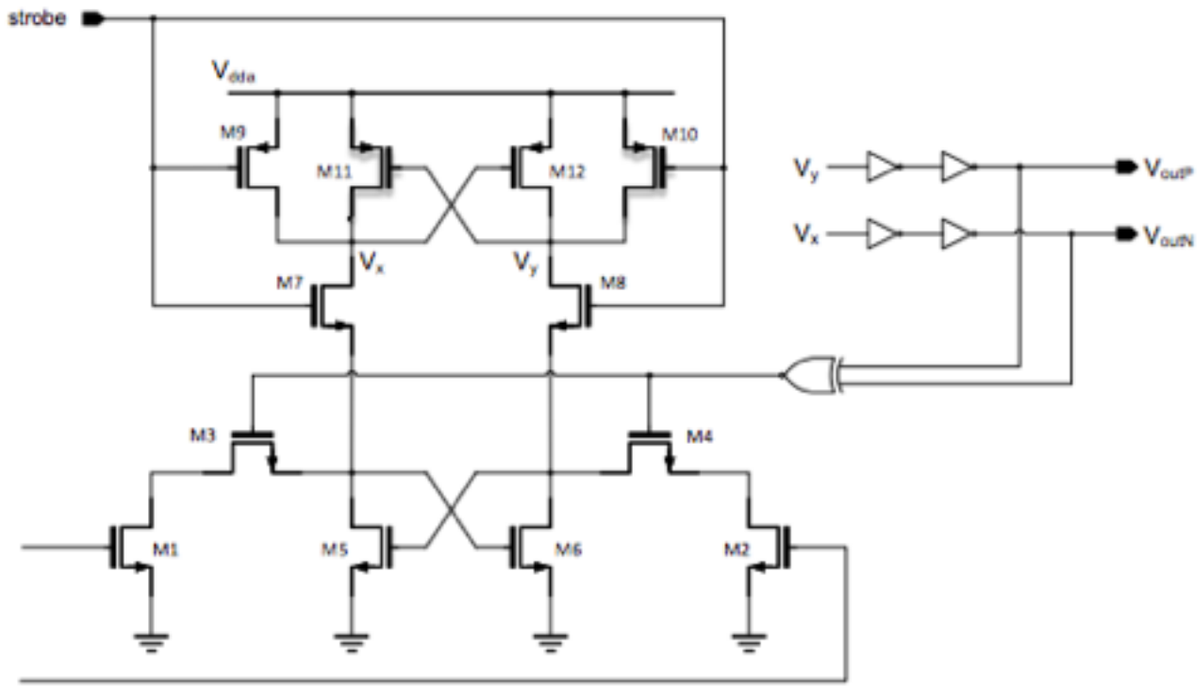


Krummenacher Feedback

Sync. Front-End Schematic II

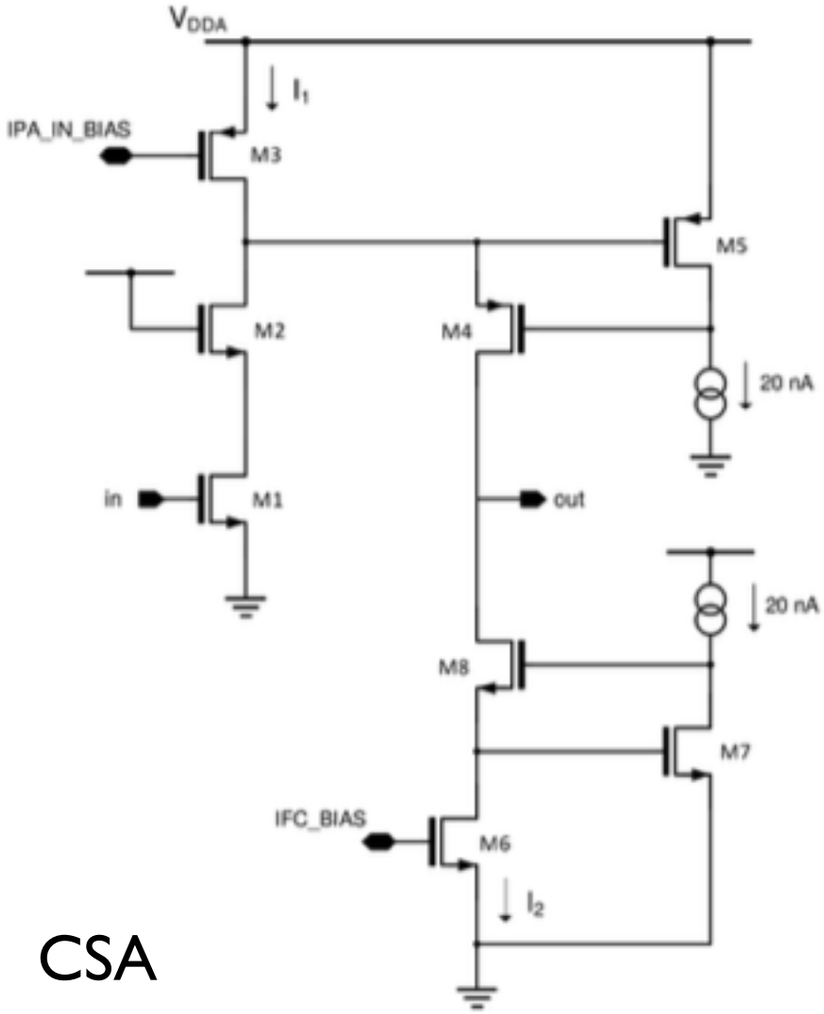


Disc.

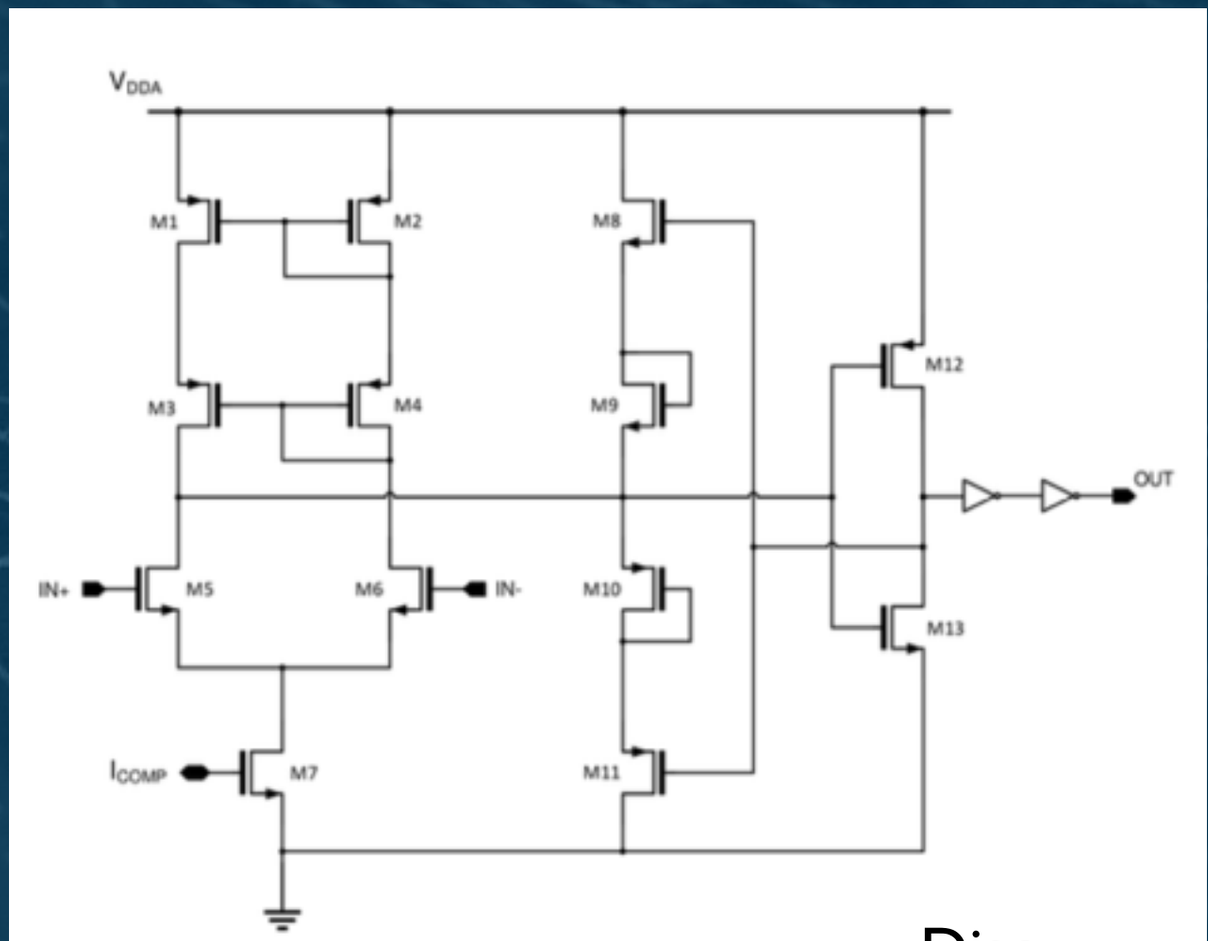


Latch

Lin. Front-End Schematic



CSA

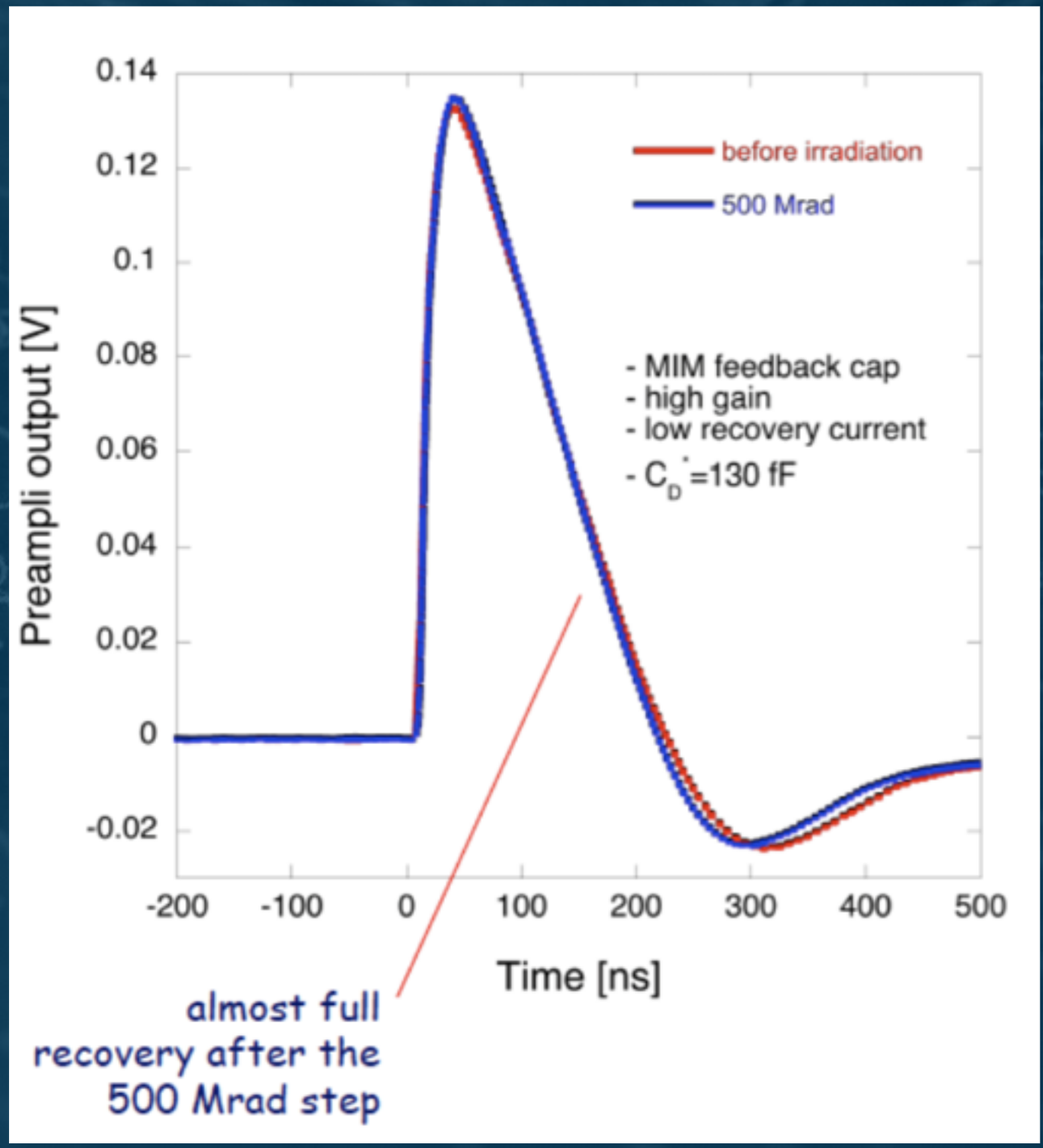


Disc.

Linear Front-End III

Irradiation:

- CSA working fine before and after irradiation to 500MRad



Analog Front-End Summary

FE65P2:

- 8 different flavours of analog front-ends
- Picked one for RD53A which showed best performance
- Fixed some issues observed with adjusting the feedback current

Chipix65:

- ??

Simulation Results for RD53A:

	Synch.	Linear	Diff	Spec
Charge Sensitivity [mv/ke]	43	25	103	
ENC rms [e]	67	83	53	<126
Threshold Dispersion rms [e]	93	32	20	<126
In-time overdrive [e]	<50	<100	0	<600
Current Consumption [μA]	3.3*	4.3	3.5	<4
ToT (6ke charge) [ns]	121	99	118	<133

*5.1 μA with latch