



# **Cold Electronics for Pixelated Readout of LAr-TPCs**

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# Overview

## **Developing front-end ASIC for scalable LAr-TPC pixel readout**

- True 2D readout: each pixel connected to an independent front-end channel
- Scalable: power use must be very low to avoid excess heat generation in LAr

## **Positive result from initial Design Study (Dec. 2016):**

- Circuit simulation satisfies requirements within allowed power budget.

## **First-generation prototype ASIC:**

- Detailed design currently in development
- Requirements focused on most critical components, not final functionality
- Aggressive Target: Receive chips at LBNL in late Summer

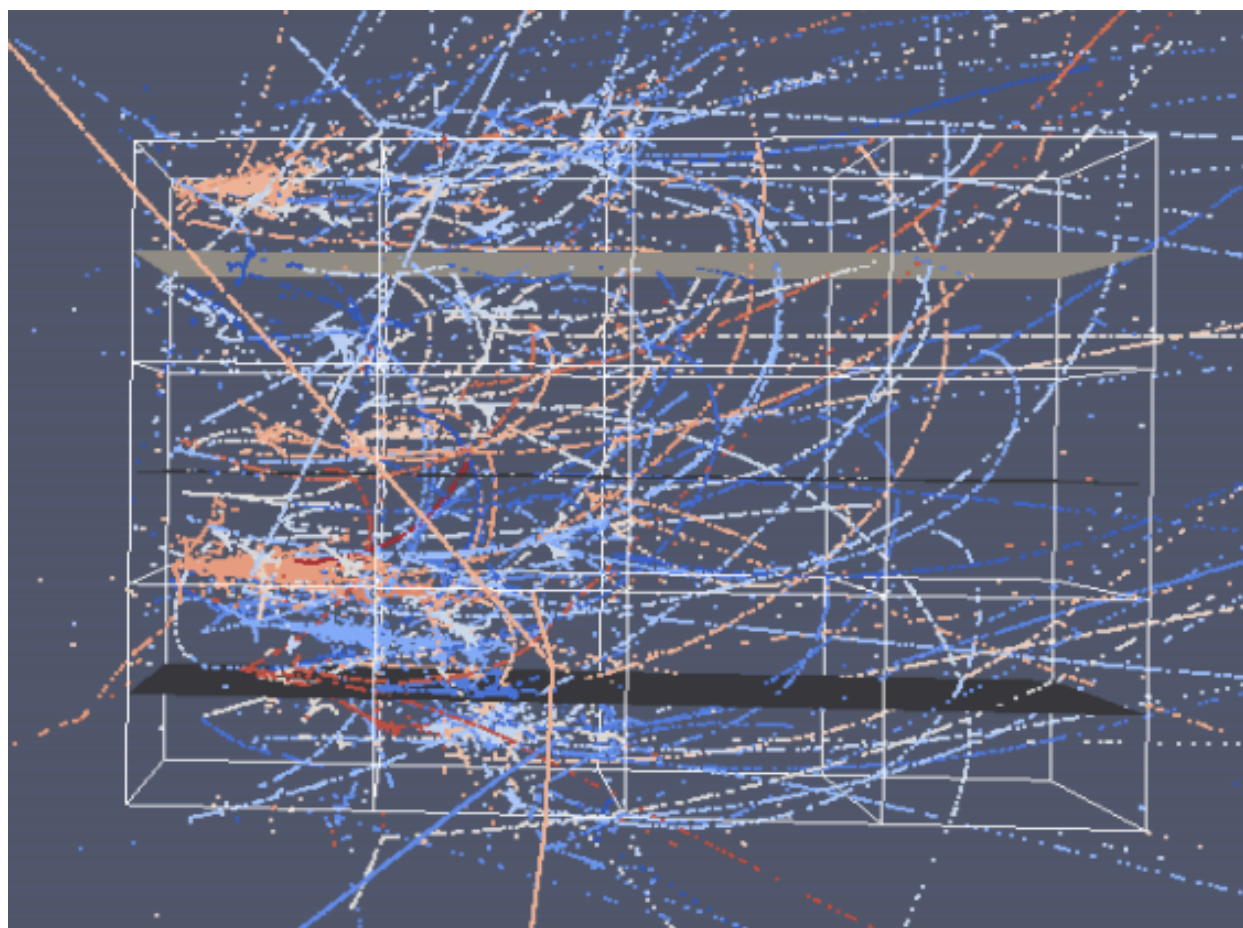
## **Testing program at LBNL:**

- Now formulating and preparing IC testing program

# Motivation: Fight Pile-up

## DUNE Near Detector:

**High-rate environment overwhelms wire readout technique.**



Example simulation of neutrino pile-up for a single neutrino beam pulse.

Each color represents a separate neutrino interaction.

Combination of neutrino interactions in LAr-TPC with external backgrounds.

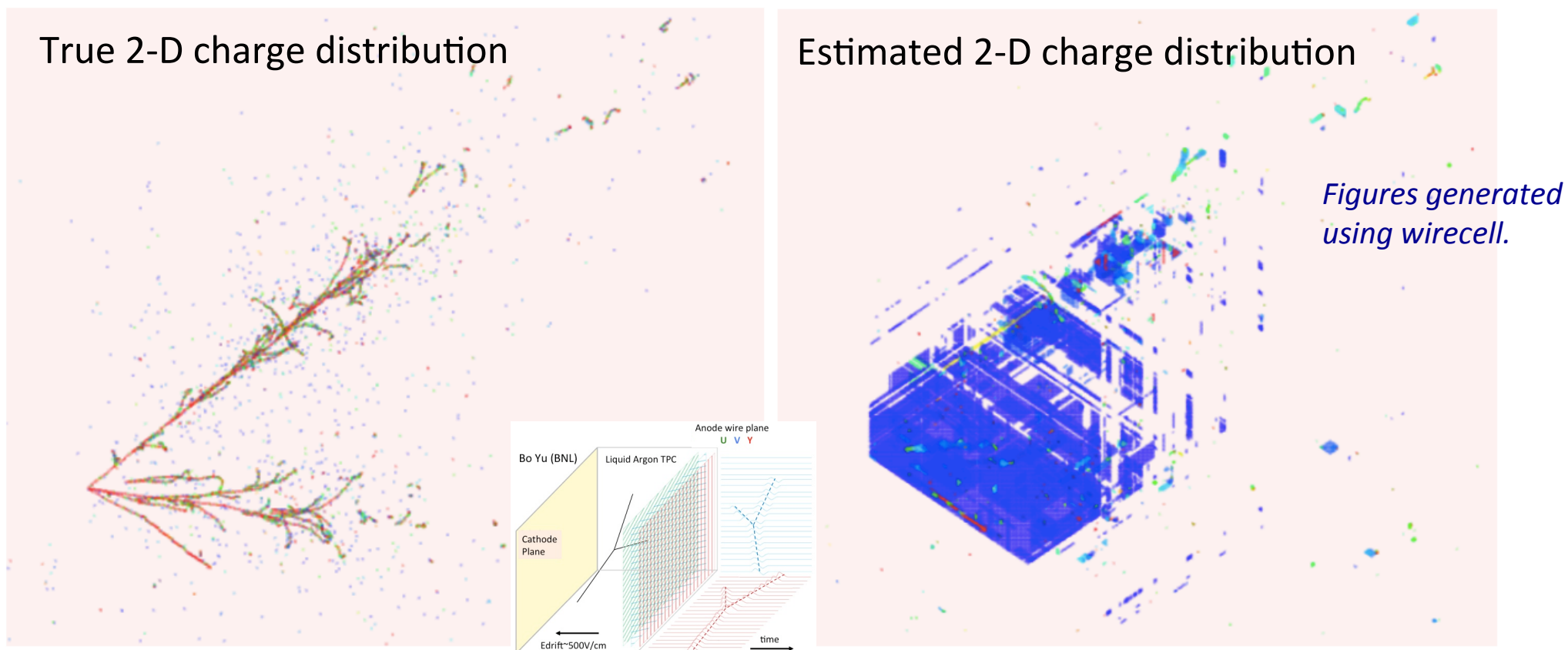
*From J. Sinclair*

**2-D pixel readout would overcome LAr near detector pile-up**

# Wire Signal Ambiguity

**2-D charge distribution (at fixed time) can be ambiguous**

**Example:** 3 GeV electron neutrino charged-current interaction in liquid argon.



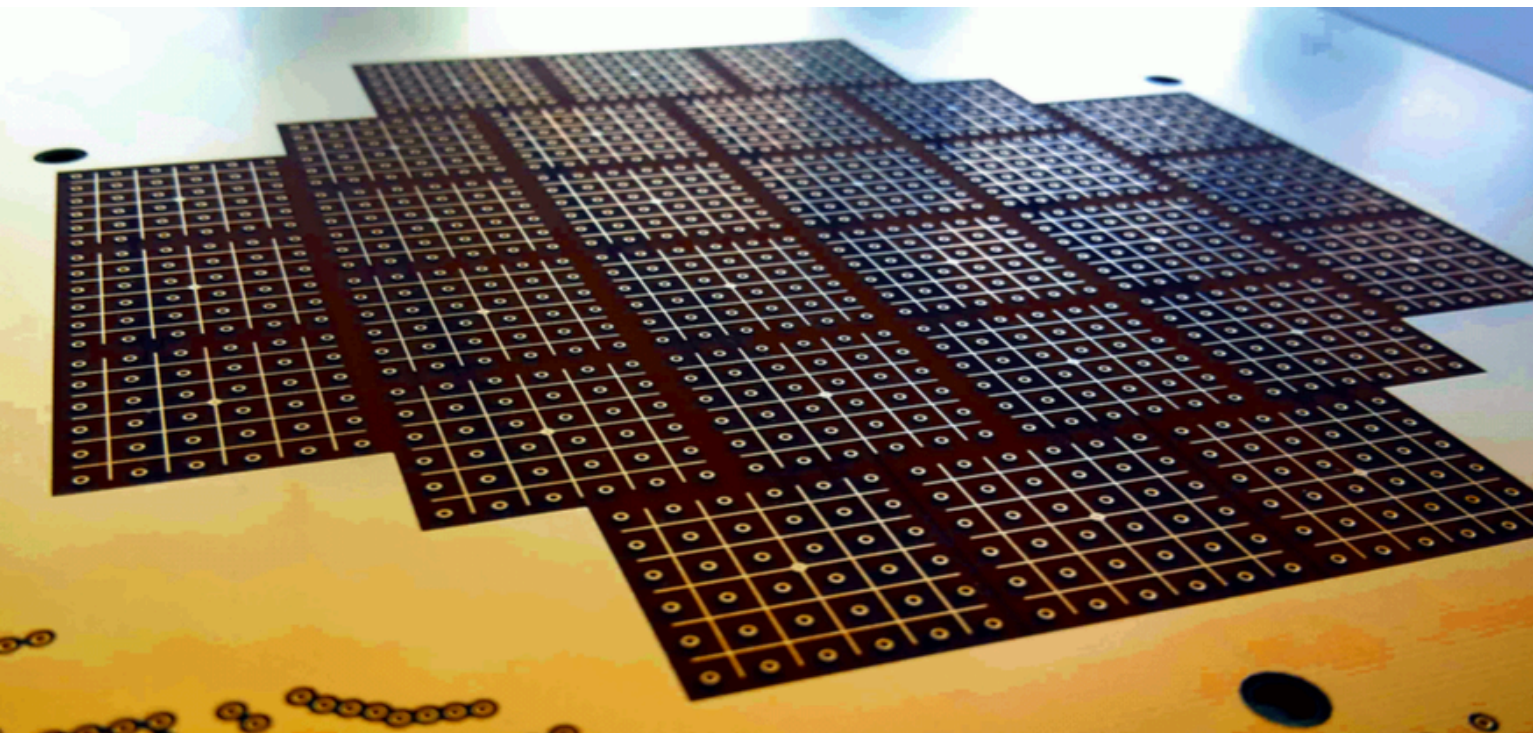
When tracks/showers parallel to anode plane, all wire signals are simultaneous.

*For impact on Far Detectors, see talk at Sep. 2016 DUNE Collab Meeting by C. Zhang.*

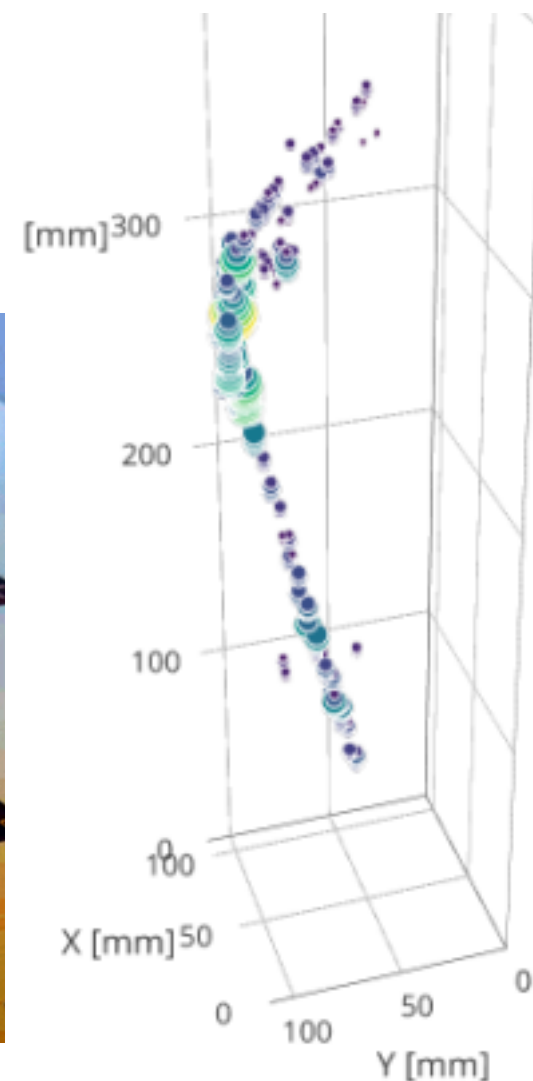
# Pixel Sensor Development

## LHEP group at Univ. of Bern / ArgonCUBE:

- Demonstrated pixel sensor in LAr (Summer 2016)
- Need low-power electronics for large-scale feasibility



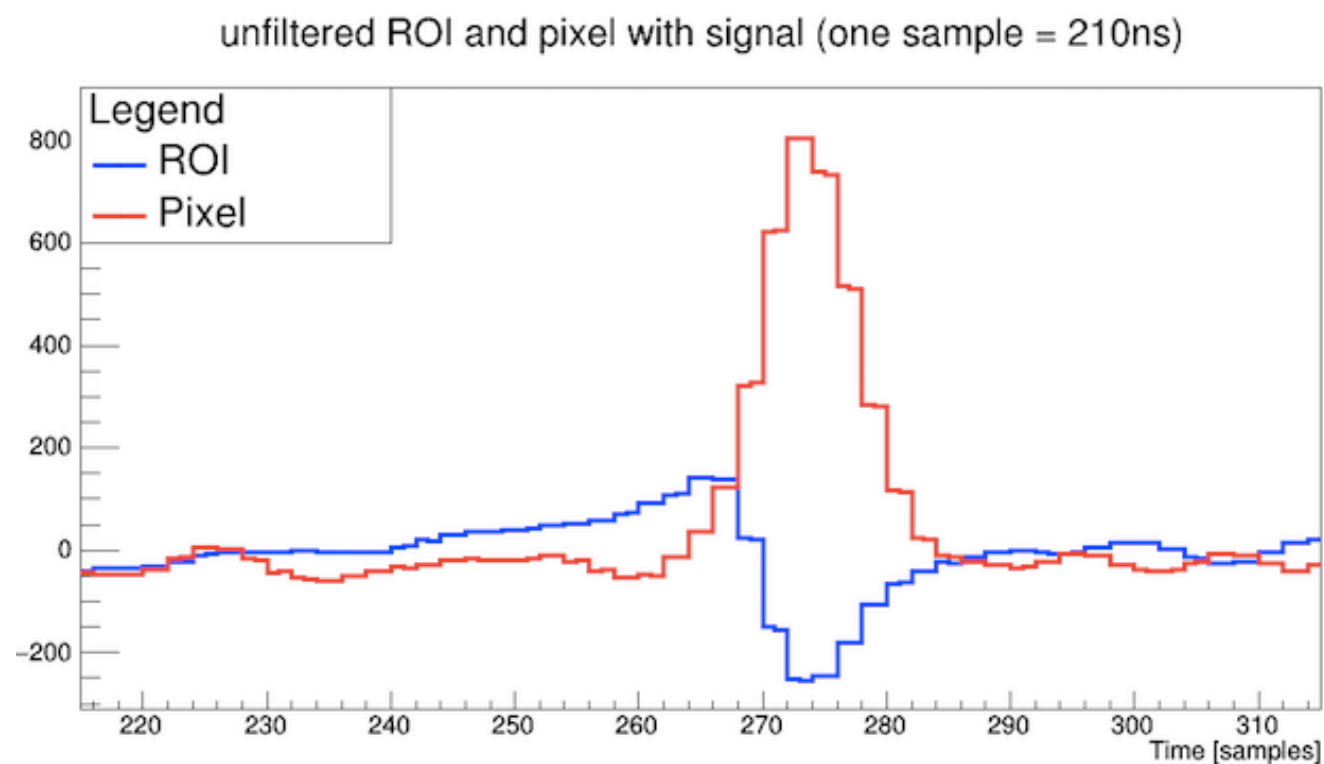
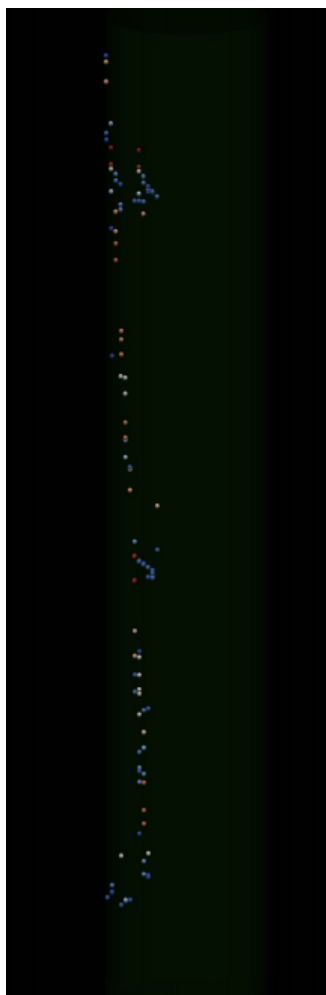
*Pixel spacing: 3mm*



# Pixel Sensor Development

## New results with 2<sup>nd</sup> generation sensor @ Bern (Mar. 2017):

- Reduced noise in test system
- Examining timing of ROI (focus grid) signal relative to pixel signal



*See yesterday's talk by J. Sinclair.*



# Prototype IC Requirements

## v1 prototype considerations:

- Limit requirements in order to advance schedule, increase chance of success
- Focus on two critical aspects:
  - 1) Demonstrate low-noise low-power cryogenic amplifier
  - 2) Demonstrate MIP-track detection capability in test TPC

### Goal 1: Amplifier

**Noise:**  $< 1600$  ENC

SNR of 9 to 1 for MIP signals

**Power:**  $< 50$   $\mu\text{W}/\text{channel}$

Total heat load:  $\sim$ few  $\text{W}/\text{m}^2$

**Channel Density:**  $\geq 16$  ch / chip

Minimize system complexity, cabling

### Goal 2: MIP-track detection

**Multiplexed:**  $\geq 100\text{s}$  of pixels per output

Achieve MIP detection with feasible # of feedthroughs.

**ADC LSB:**  $\text{LSB} < 1600$  ENC

Digitization noise  $<$  amplifier noise

**ADC Range:** 6-bit range

Span MIP signal range

**ADC Time-resolution:**  $\leq 2$   $\mu\text{s}$

Equal or better than spatial resolution (3 mm)

**Deadtimeless:** Buffer  $> 1500$  digitizations

Handle worst-case: track perpendicular to pixel



# Prototype IC Requirements

## Not included in v1 Prototype:

**ADC Range:** Will not yet target full dynamic range (~12-bit)

**Digital Power:** v1 multiplexing and readout may exceed power constraints

**Channel Calibration:** Built-in calibration capacitor may be low-precision

**Reliability:** Not aiming for long-term cold qualification.

Will not include signal rerouting around dead ICs

## **Postpone these features to next generation IC:**

- Advances schedule of design and delivery of v1 IC
- Substantially increases odds of v1 IC success





# LArPix v1: Design Concept

## Amplifier with Self-triggered Digitization and Readout

### A. Front-end amplifier:

Charge-collection only, noise requirements relaxed  
Tunable baseline for adaptation in cold  
Integrated calibration capacitor

### B. Self-triggering Discriminator:

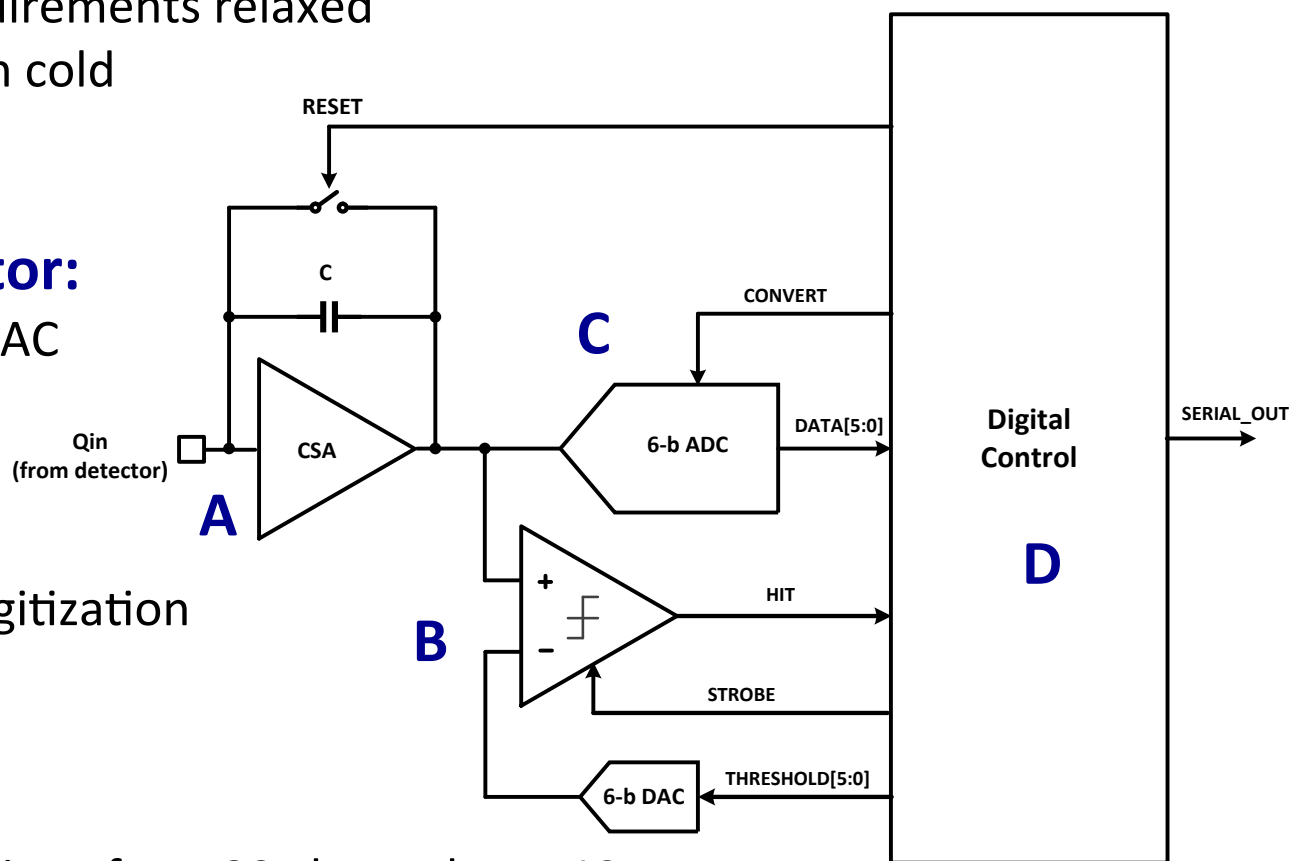
Configurable threshold via 6-bit DAC  
Latching design for low power

### C. Standard SAR Digitizer:

6-bit successive approximation digitization  
Driven by trigger

### D. Digital Control

Multiplexes I/O via UART (2 wire) interface, 32 channels per IC  
FIFO memory buffer facilitates low power readout  
Up to 256 ICs daisy-chained on a single pair of UART digital I/O lines





# LArPix v1: Progress and Schedule

## Preliminary Design Study completed (Dec. 2016)

Initial IC designed and simulated, in 180nm TSMC process

Design met requirements, based on simulation:

Noise: 795 ENC (amplifier only), 820 ENC (amp + digitizer)

Power: 25  $\mu$ W (amplifier), 0.002  $\mu$ W (discriminator), 0.54  $\mu$ W (digitizer)

## V1 Prototype IC:

### Feb-Mar. 2017:

System-level design completed.

Digital core synthesized.

Data I/O format established.

### Apr. 2017:

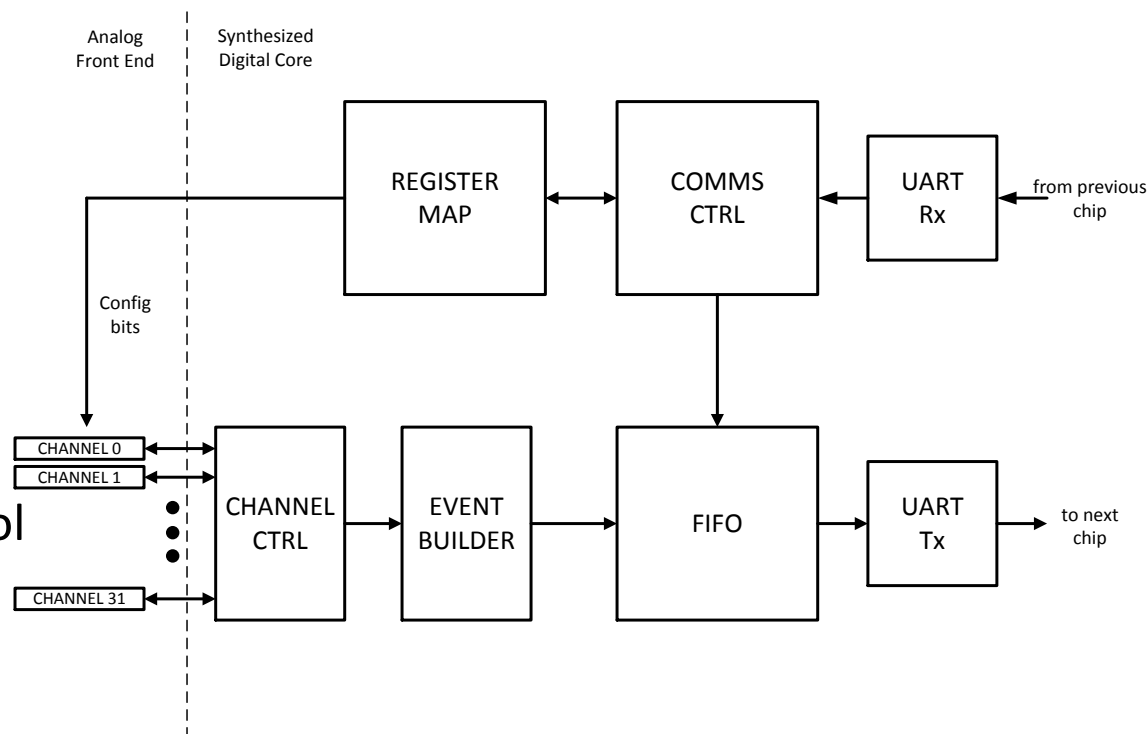
Finalize analog front-end, calib. & control

Floor-planning, routing, and verification

### May 2017: Contingency

### May-Jun 2017: Send out for production

### Jul-Aug 2017: Receive prototype ICs at LBNL





# LArPix v1: Data I/O Format

## UART Data I/O Format:

Allows bi-directional digital communication over 2 wires:

- No chip select, dedicated clock, or synchronization pins required

For simplicity, all I/O words (data, configuration, test) a common length: 54-bits

Includes test patterns to simplify synchronization with master FPGA.



## Data Word:

[1:0]	Packet type
[9:2]	Chip ID
[16:10]	Channel ID
[40:17]	Timestamp
[52:41]	Data word (e.g. ADC)
[53]	Parity bit

## Configuration Word:

[1:0]	Packet type
[9:2]	Chip ID
[17:10]	Register map address
[25:18]	Register map data
[52:26]	(empty)
[53]	Parity bit



# LArPix v1: IC Simulation

The screenshot displays a Verilog simulation environment with a waveform viewer and a transcript window. The waveform shows digital signals for UART data and FIFO status. Annotations with arrows point to specific events: 'UART in' (data arrival), 'FIFO write' (data being pushed into the FIFO), and 'FIFO overflow' (data being lost due to a full FIFO). The transcript window shows test results for FIFO operations, including a panic test that passes.

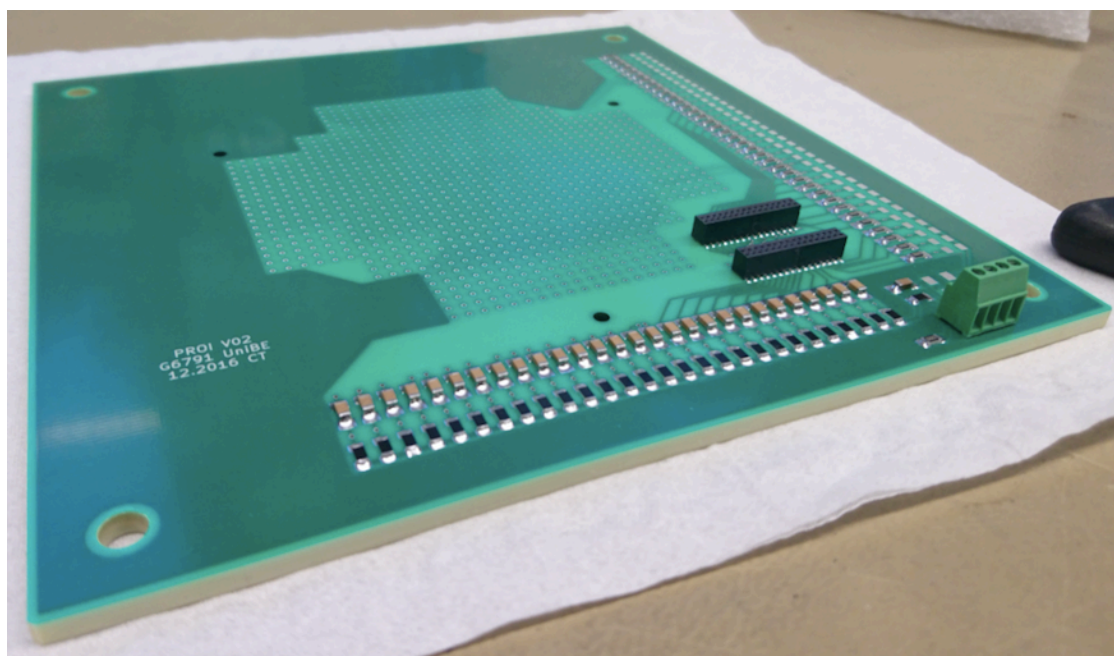
FIFO operation tests

FIFO overflow test (make sure LArPix doesn't hang)

# LArPix PCB Design

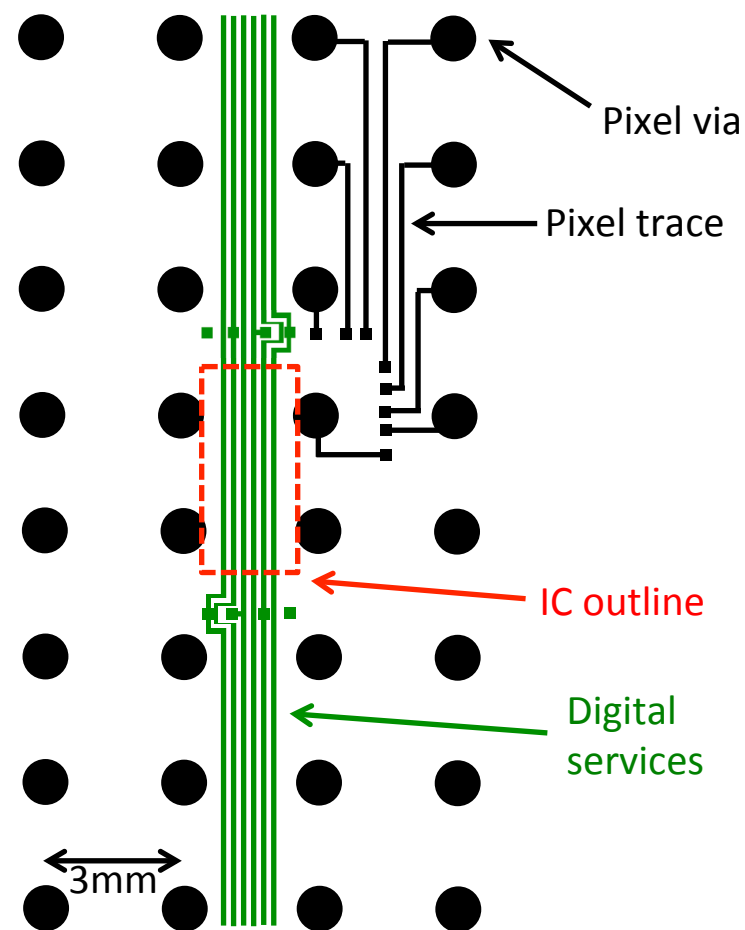
## v1 prototype requires modified pixel PCB:

- James provided details of existing LHEP PCB design
- Altering layout to support independent readout of each pixel



## Example: 32-channel PCB block

- Tile large plane by repeating basic block
- Simple two-layer PCB may be sufficient
- ICs daisy-chained along service lines
- Prototype IC: will epoxy & wirebond to PCB





# LArPix v1: Testing

## Step 1: IC characterization with test board

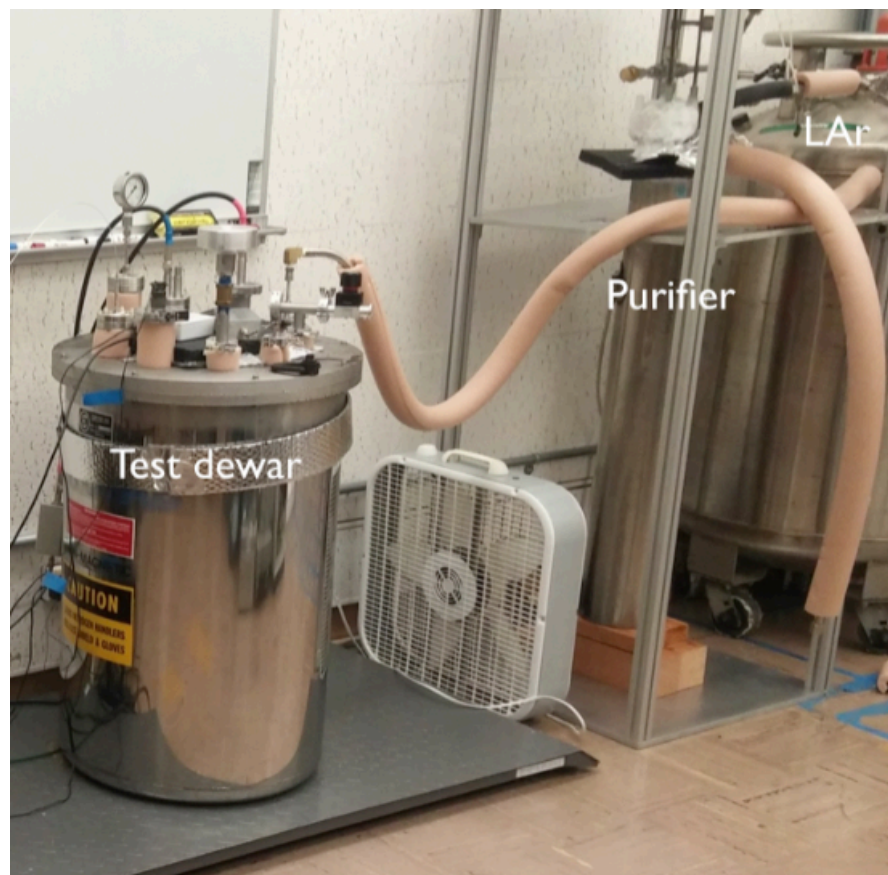
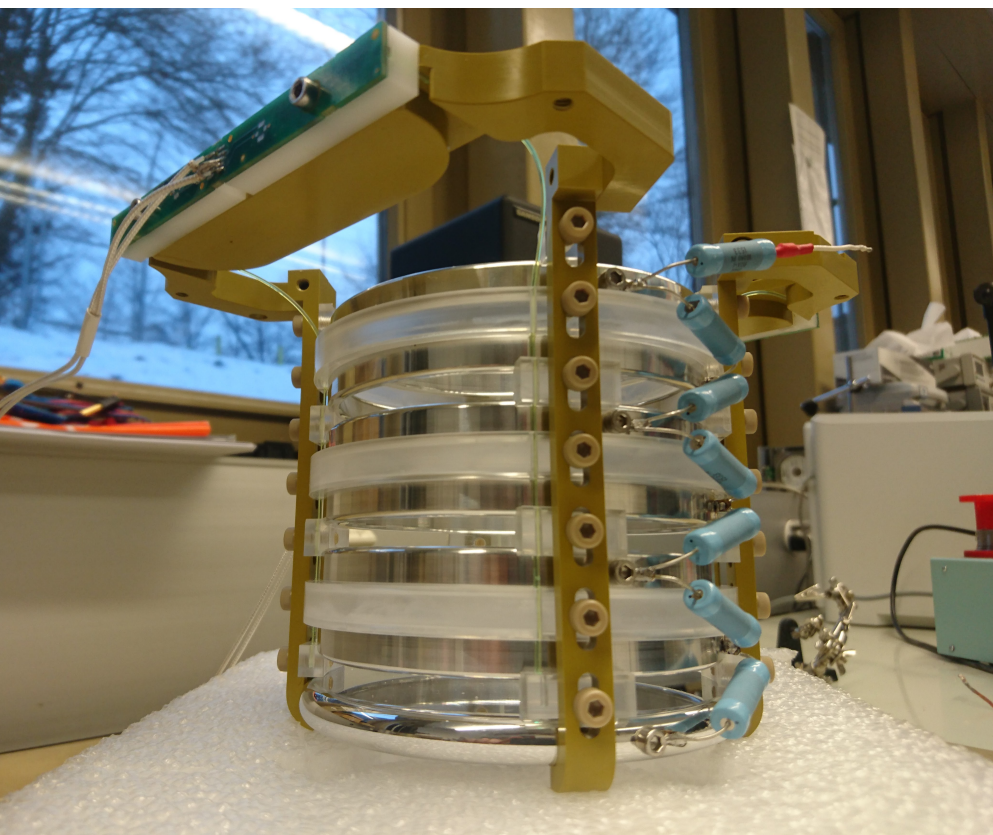
Able to reuse test boards from previous LBNL IC project.

## Step 2: Testing in LArTPC

Test in 'mini' ArgonCUBE Pixel Demonstrator TPC provided by LHEP group

## Existing LUX/LZ test system available:

- Single-pass LAr purification and cryostat
- Purity seems sufficient for our tests (electron lifetime: >few hundred  $\mu$ s)





# Summary

## **LAr-TPC Near Detector Module:**

Hindered by signal pile-up from LBNF beam intensity.

ArgonCUBE prototype: demonstrated feasibility of 2D charge readout

Large-scale deployment requires low-power readout electronics

## **LArPix v1 IC:**

Dedicated IC for low-power 2D charge readout.

Design study: suggested IC feasibility, no obvious show-stoppers

Prototype design progressing quickly; most of layout now established

Targeting start of production in ~2 months, in 180nm TSMC process

Aiming for demonstration of noise & power performance in late 2017



# Backup





# Triggering Methods

**Consider three methods of triggering and readout:**

## **1) Channel (self) triggering:**

- All channels always on
- Digitize and readout whenever channel above threshold
- Issue: Unoccupied channel power use must be very low.

*Potential fallbacks if power use is too high:*

## **2) Global triggering:**

- Receive external trigger from beam or light-detection system
- Enable all channels in detector
- Collect hits and readout for  $\sim 10$  ms

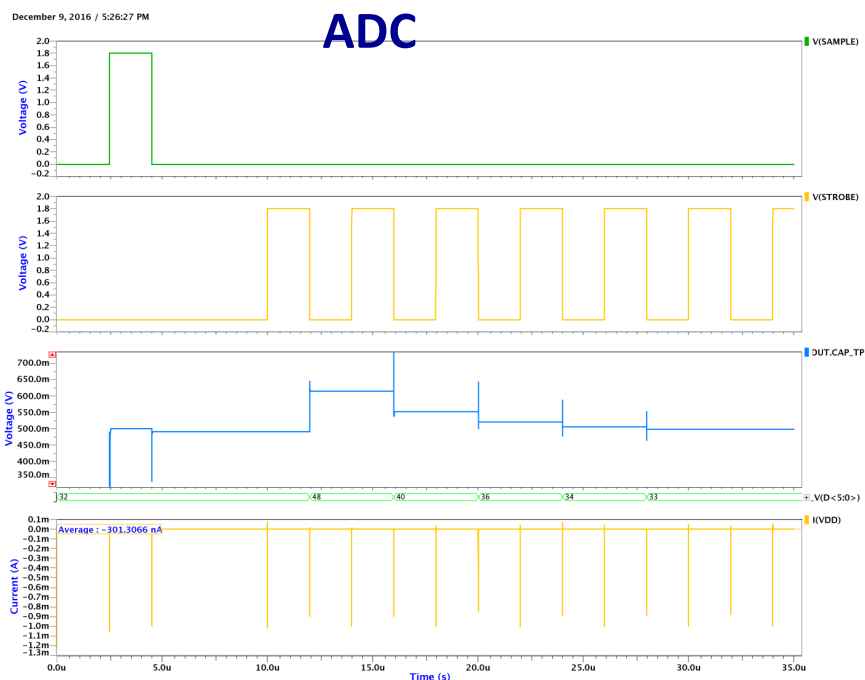
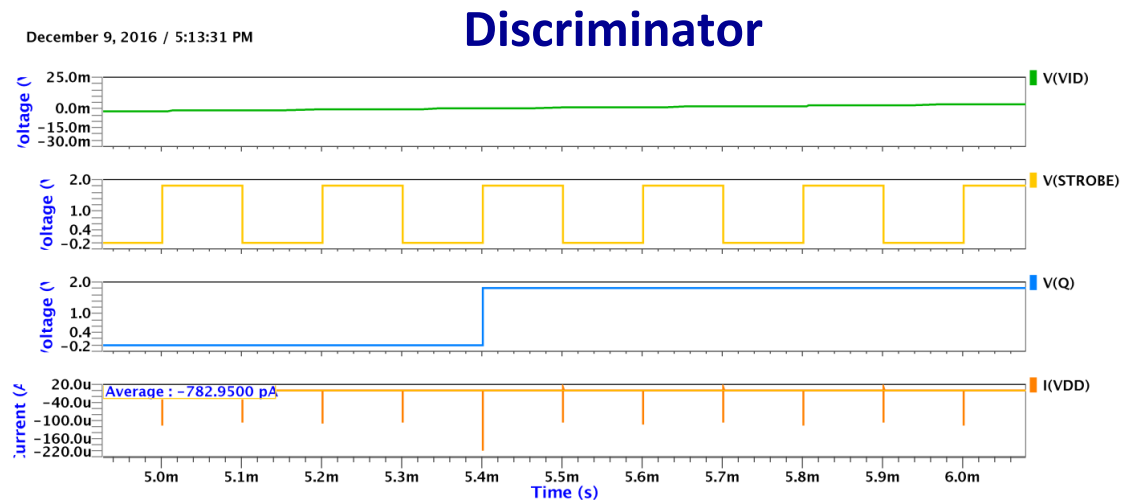
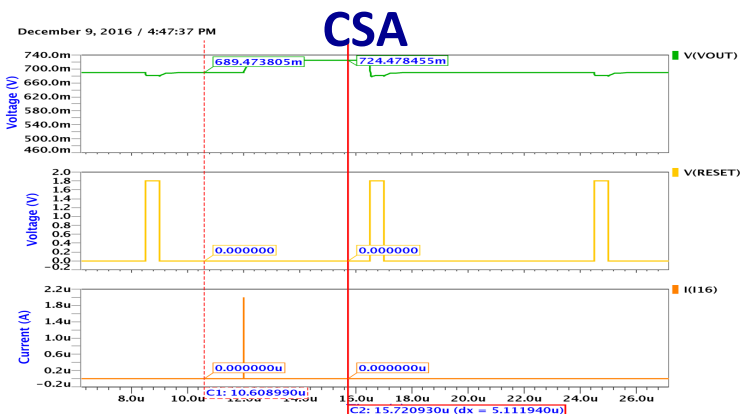
## **3) Region triggering:**

- Use inductive signal to detect incoming charge
- Enable pixel channels  $O(100)$  in single inductive region
- Collect hits and readout for  $\sim 10$   $\mu$ s
- Issue: Inductive signal provides very little lead-time ( $\sim 2$   $\mu$ s), difficult to 'wake-up' pixel this quickly.



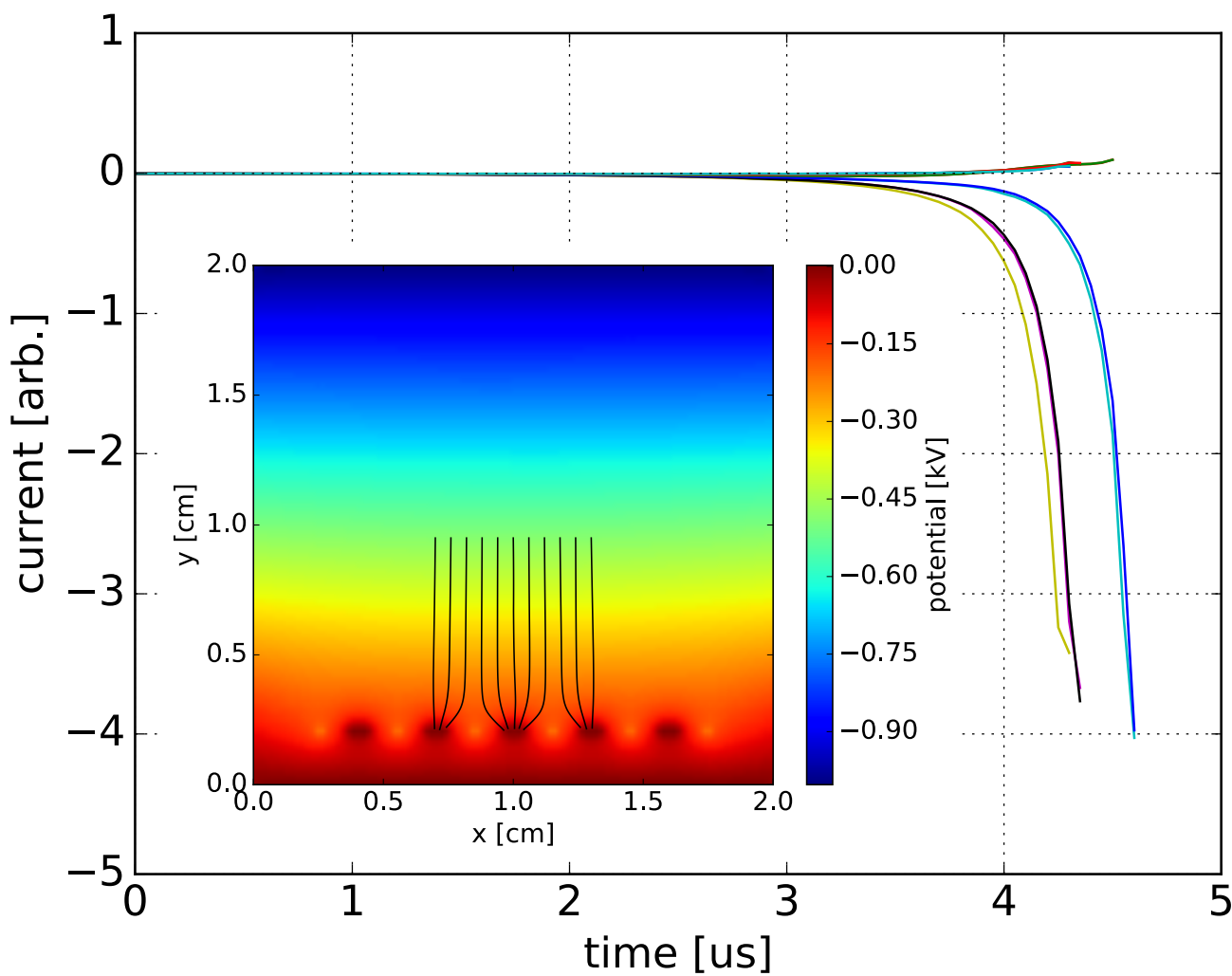
# Simulation

## Noise and power performance of CSA, discriminator, ADC



# Pixel Signal Modeling

Implemented 3-D field and charge drift for pixel signal modeling.



## Electron Paths:

Start in middle of 2-cm box, along  $z=1\text{cm}$  'slice', from  $x=0.7\text{cm}$  to  $1.3\text{cm}$

Propagate in e-field until electron strikes surface.

## Configuration:

- Drift Field: 500 V/cm
- Focus grid potential: -200 V
- Pixel pitch: 3mm

## Observations:

- 200V focusing sufficient
- Signal time scale:  $\sim 1\mu\text{s}$
- $\sim 0.3\mu\text{s}$  variation in e- arrival
- $\sim 3\%$  signal induced on neighbor