



Stony Brook University
Electrical and Computer Engineering

Microelectronics for Radiation Detectors

Gianluigi De Geronimo

gianluigi.degeronimo@stonybrook.edu, degeronimo@ieee.org

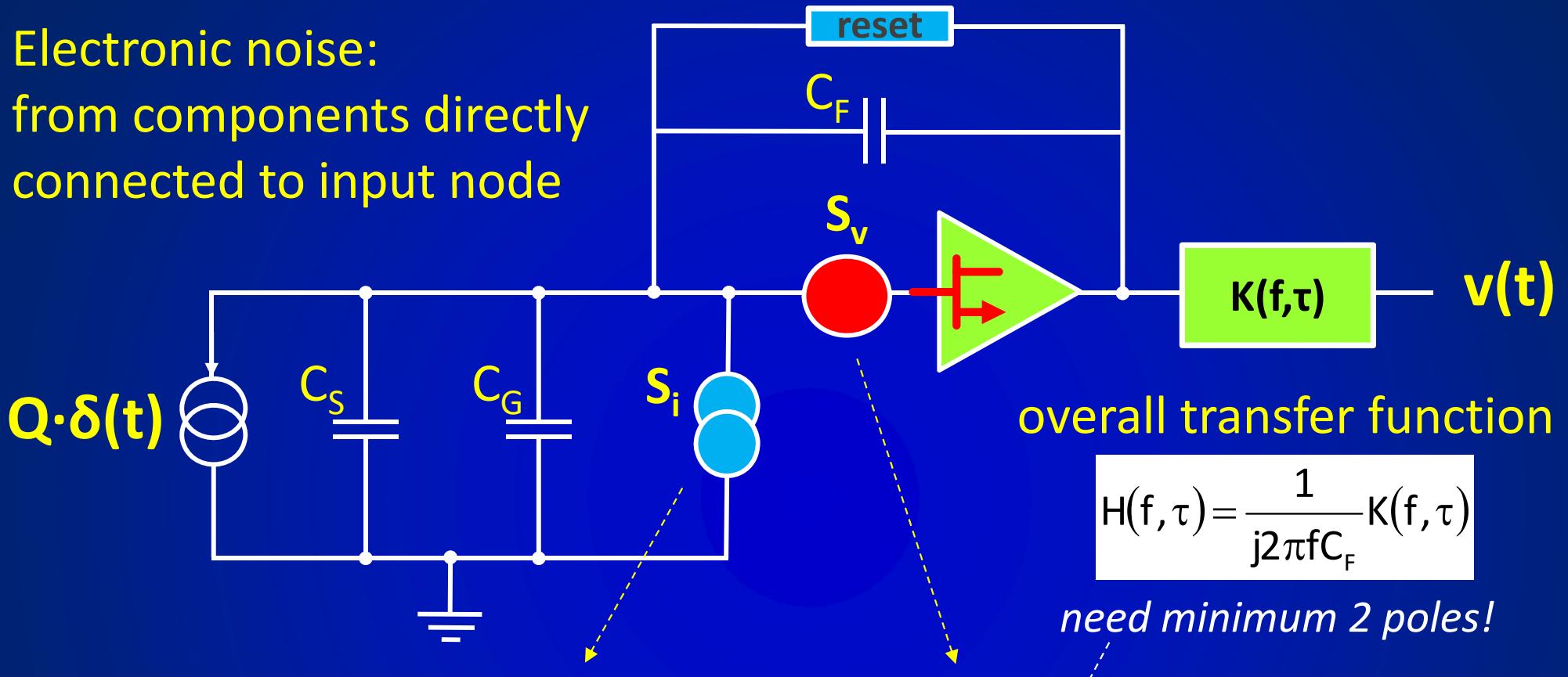
Lawrence Berkeley National Laboratory
December 20th, 2016

Outline

- Introduction
- Charge Amplification in CMOS
- Evolution of FE ASICs
- Conclusions

Sources of Electronic Noise

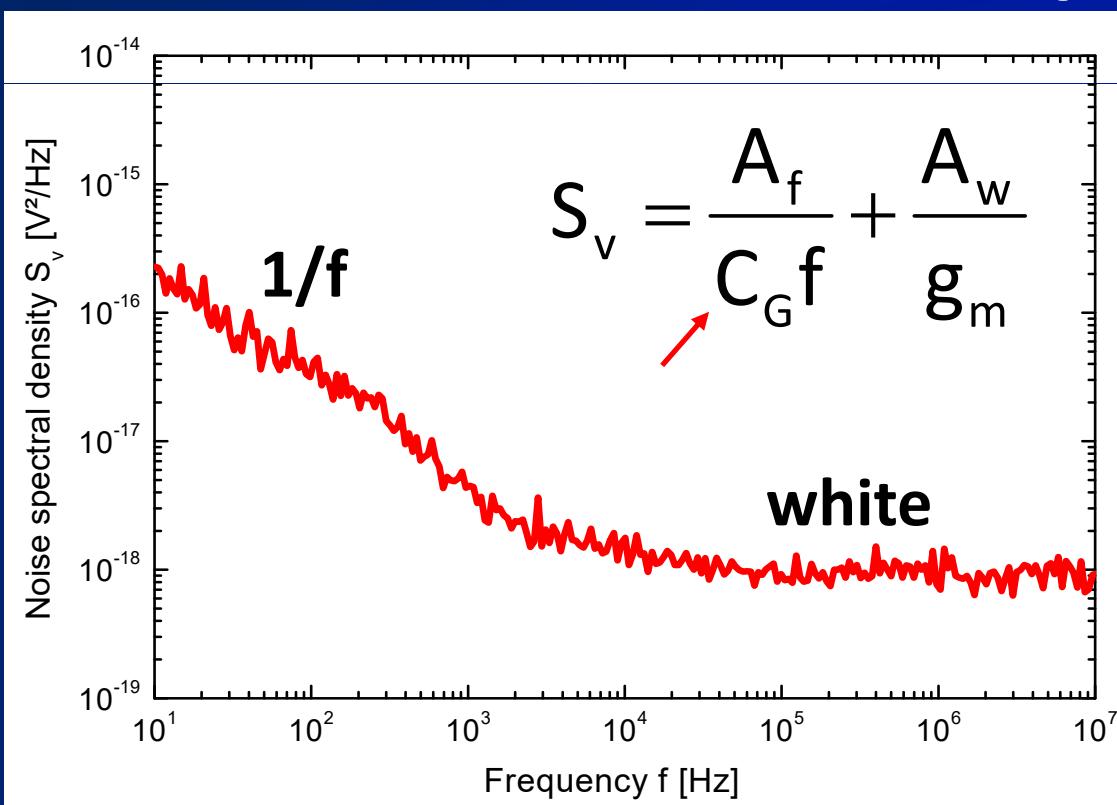
Electronic noise:
from components directly
connected to input node



$$ENC^2 \cong \frac{\int_0^\infty S_i |H(f, \tau)|^2 df + \int_0^\infty S_v \omega^2 (C_S + C_G)^2 |H(f)|^2 df}{h(t)_{\max}^2}$$

Time-variant \rightarrow time-domain analysis (noise weighting function)

Noise from Input Transistor



C_G intrinsic gate capacitance
proportional to the gate size

$C_G = C_S$ (capacitive matching)

From input
transistor:

$$\text{ENC}_v^2 = a_f A_f \frac{(C_s + C_G)^2}{C_G} + \frac{a_w}{\tau} \frac{A_w}{g_m / C_G} \frac{(C_s + C_G)^2}{C_G}$$

$f_{T\max T}$ $f_{(\max \text{ current})}$

ASIC: power constraints

Input Transistor in CMOS

From transistor's white noise:

$$\text{ENC}_{\text{vw}}^2 \approx \frac{a_w}{\tau} \frac{A_w}{g_m(I_D)/C_G} \frac{(C_s + C_g)^2}{C_g}$$

Fix power = fix drain current I_D
 → size (W,L) ?

$V_{GS} \gg V_{th}$ (strong inversion)

$$g_m(I_D) \approx \sqrt{\frac{2\mu c_{\text{ox}}}{n} \frac{W}{L} I_D} \propto \sqrt{\frac{C_g I_D}{L^2}}$$



$$\text{ENC}_{\text{vw}}^2 \propto \frac{L}{\sqrt{I_D}} \frac{(C_s + C_g)^2}{\sqrt{C_g}}$$



$V_{GS} \ll V_{th}$ (weak inversion)

$$g_m(I_D) \approx \frac{I_D}{nV_T} \propto I_D$$

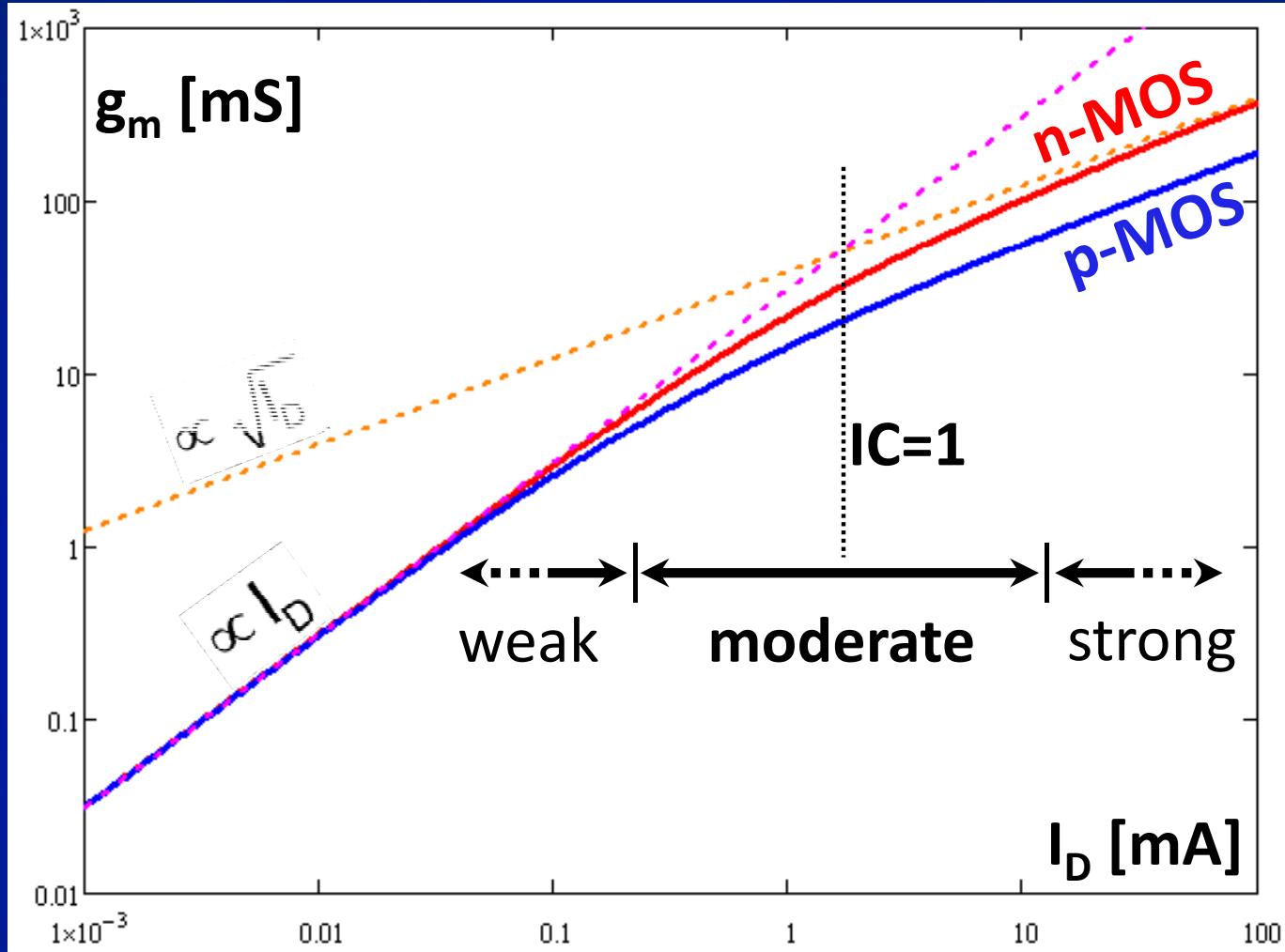


$$\text{ENC}_{\text{vw}}^2 \propto \frac{(C_s + C_g)^2}{I_D}$$

- minimum L
- $C_g = C_s/3$
- independent of L
- $C_g = 0$ pushes back towards strong inversion

→ $V_{GS} \approx V_{th}$ (moderate inversion): model?

Moderate Inversion



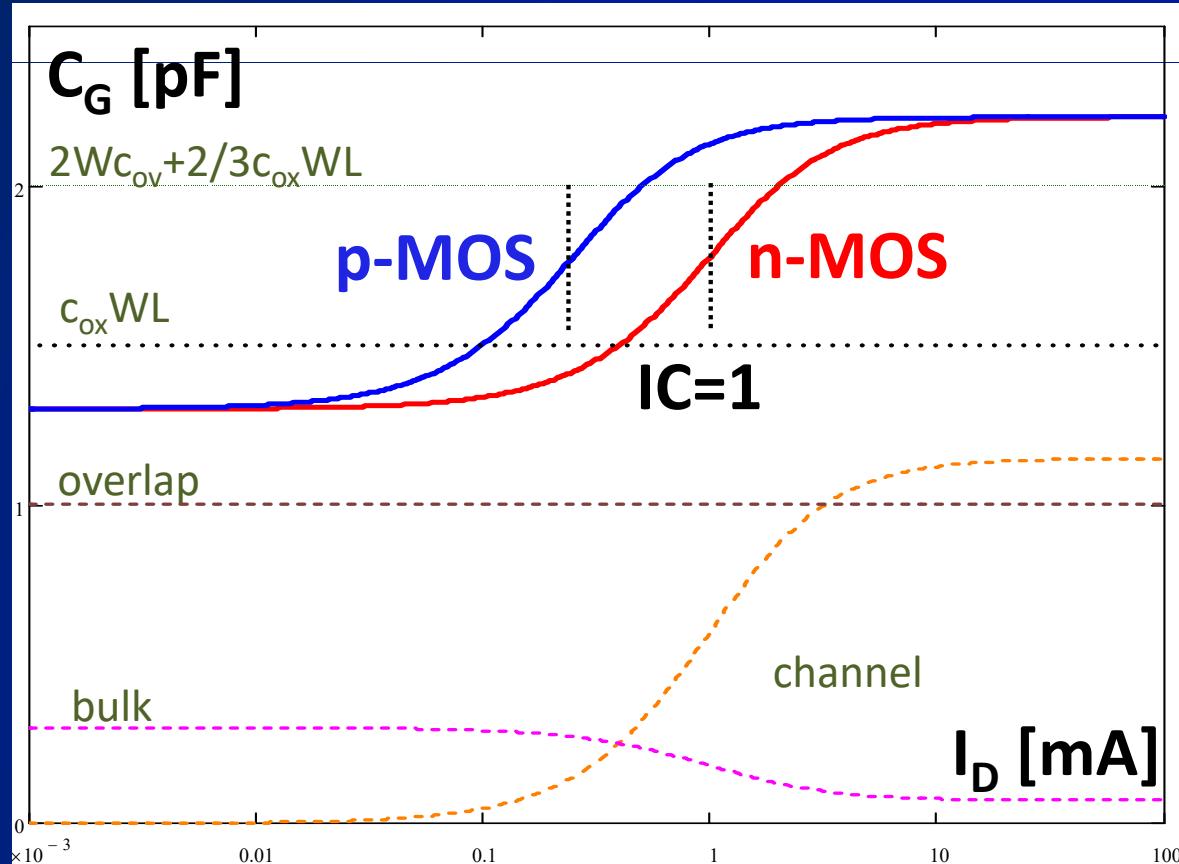
From EKV model

$$g_m(I_D) \approx \frac{I_D}{nV_T} \frac{\sqrt{1 + 4 \cdot IC} - 1}{2 \cdot IC}$$

$$IC = \frac{L}{W} \frac{I_D}{2nV_T^2 \mu c_{ox}}$$

inversion coefficient

Gate Capacitance



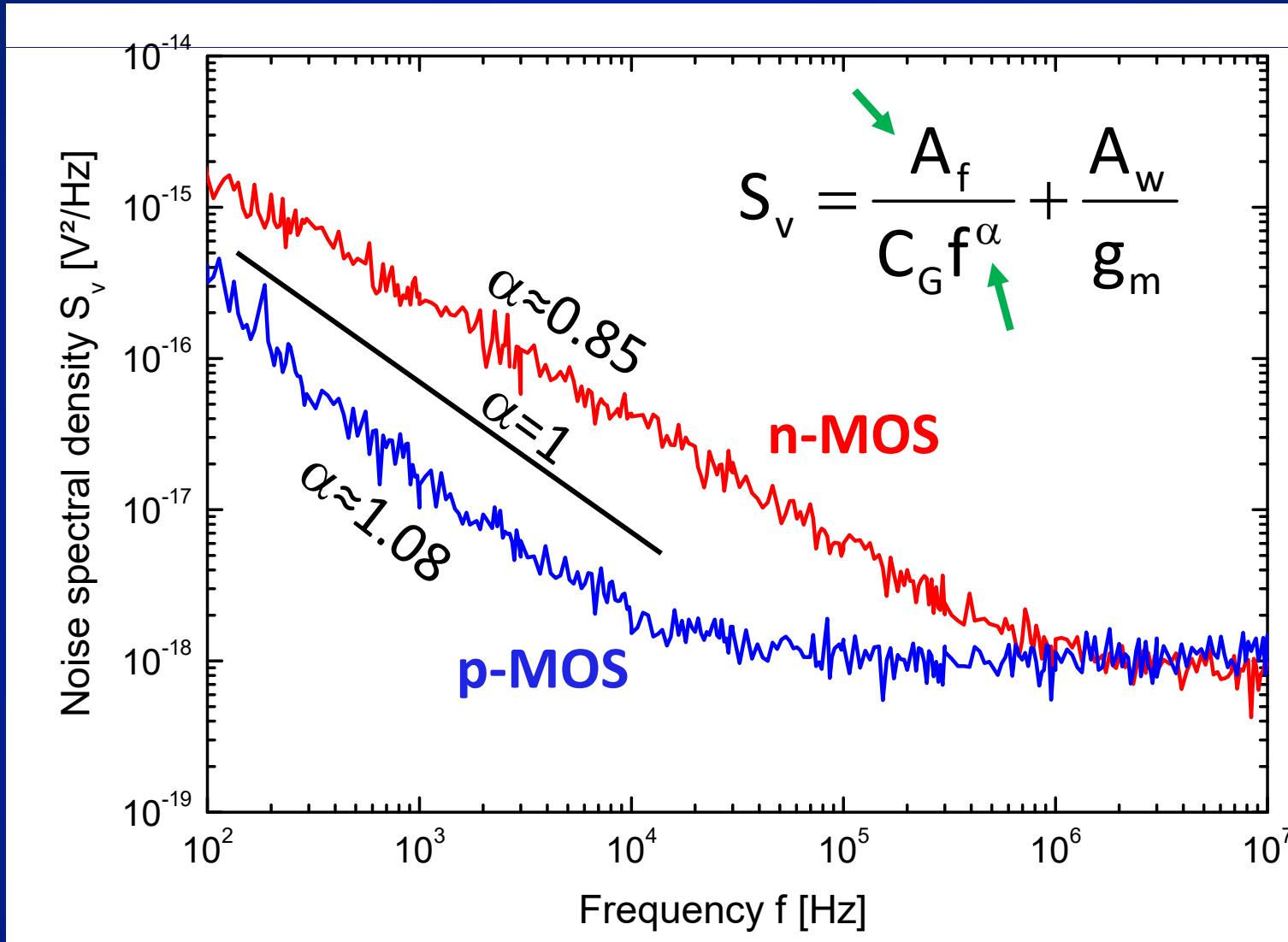
~~$\propto C_{ox}WL$~~

$$C_G(I_D) \approx 2c_{ov}W + C_{ox}WL \left(\gamma_c(IC) + \frac{n-1}{n} [1 - \gamma_c(IC)] \right)$$

$$\gamma_c(IC) \approx \left(\frac{3}{2} + \frac{1}{3} \frac{\sqrt{1+4 \cdot IC} + 1}{IC^2} \right)^{-2/3}$$

Both g_m and C_G push towards using n-channel and $L = L_{\min}$

Low-Frequency Noise

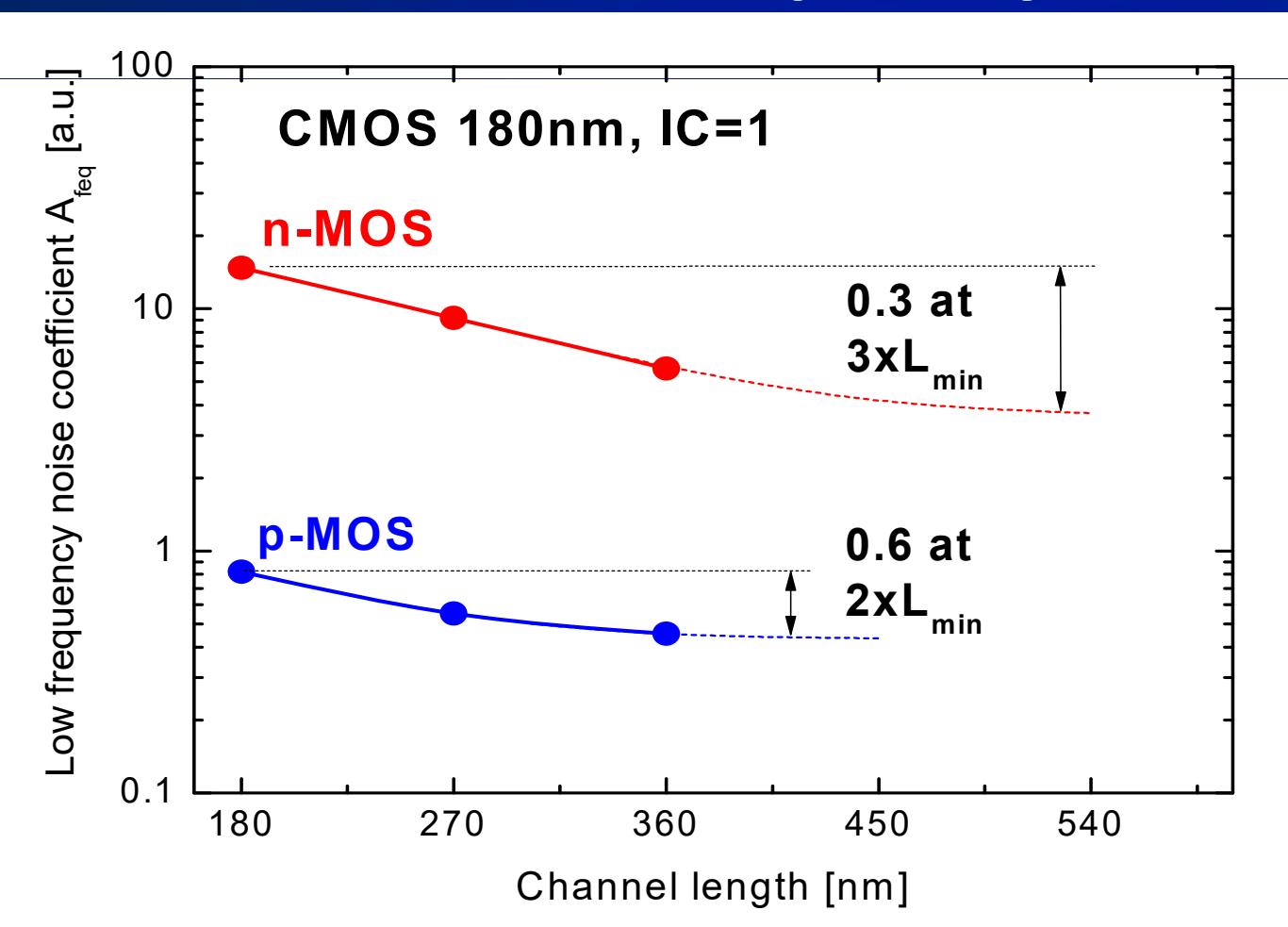


From transistor's
low-freq. noise:

$$\text{ENC}_{\text{vf}}^2 = a_f(\alpha) \frac{A_f}{\tau^{1-\alpha}} \frac{(C_s + C_G)^2}{C_G}$$

depends
on τ

Low-Frequency Noise vs L



$$S_v = \frac{A_f(L)}{C_G f^\alpha} + \frac{A_w}{g_m}$$

↓

1/f equivalent, IEEE TNS 58, 2011

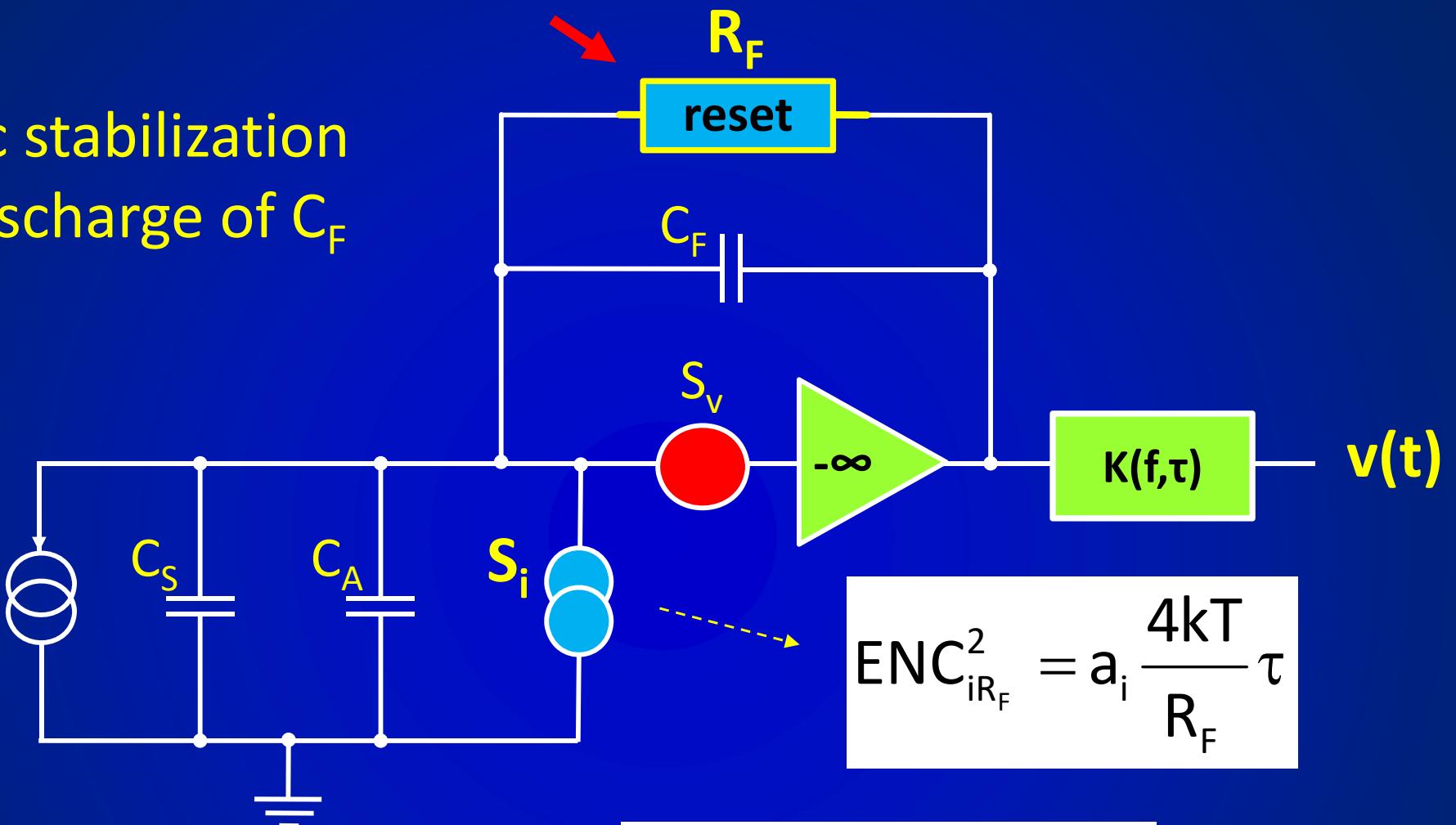
From transistor's
low-freq. noise:

$$\text{ENC}_{\text{vf}}^2 = a_f(\alpha) \frac{A_f(L)}{\tau^{1-\alpha}} \frac{(C_s + C_G)^2}{C_G}$$

LF noise pushes towards p-channel & $L > L_{\min}$

Discharge Network (Reset)

- dc stabilization
- discharge of C_F



$$\frac{4kT}{R_F} \ll 2qI_S$$



$$R_F I_S \gg \frac{4kT}{2q} (\sim 50\text{mV}) \quad \text{"50mV rule"}$$

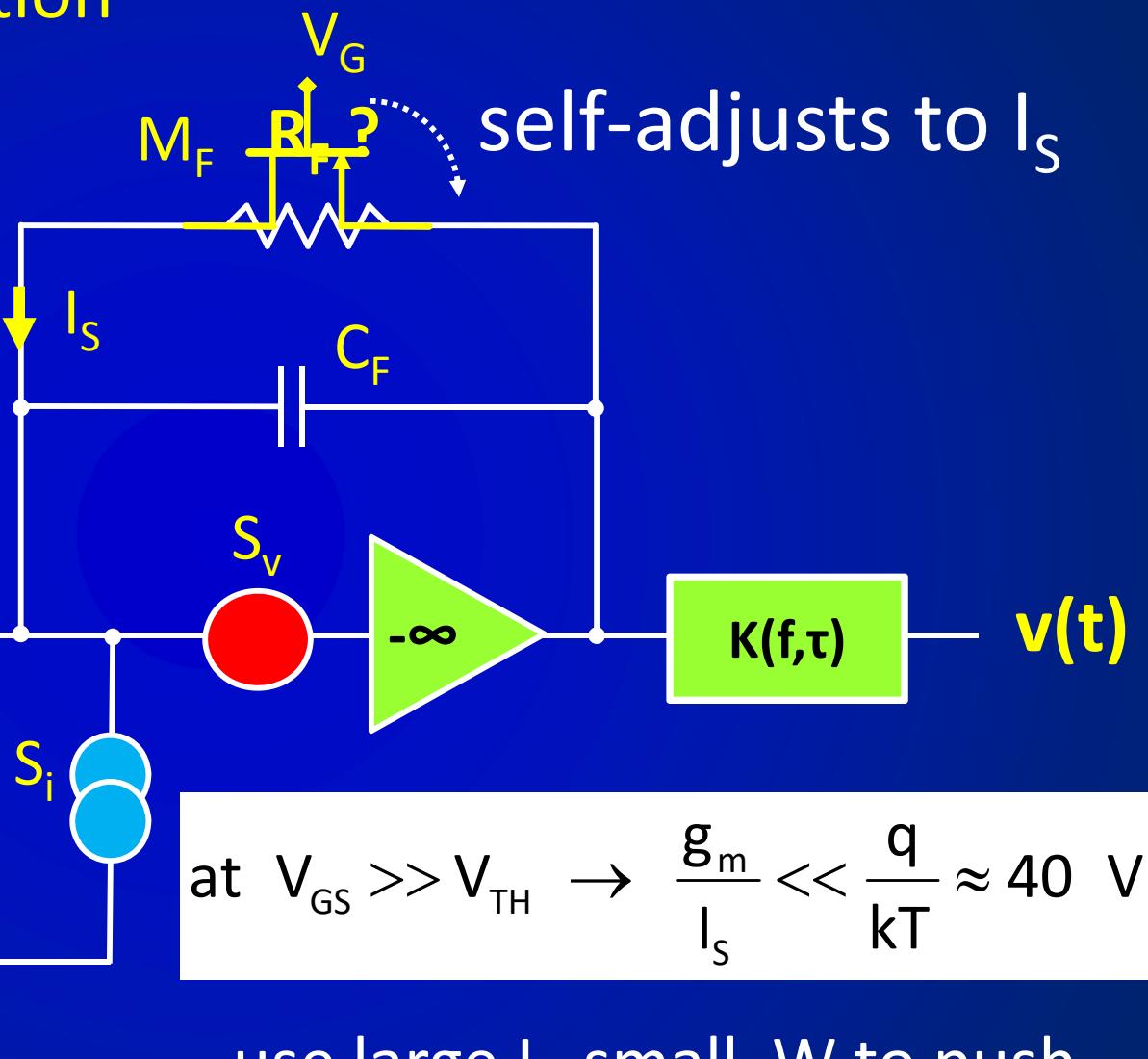
sensor shot noise
from leakage current I_S

examples [$CZT: I_S = 1\text{nA} \rightarrow R_F \gg 50\text{ M}\Omega$
 $Si: I_S = 1\text{pA} \rightarrow R_F \gg 50\text{ G}\Omega$]

Reset in CMOS

- linear region saturation
- noise

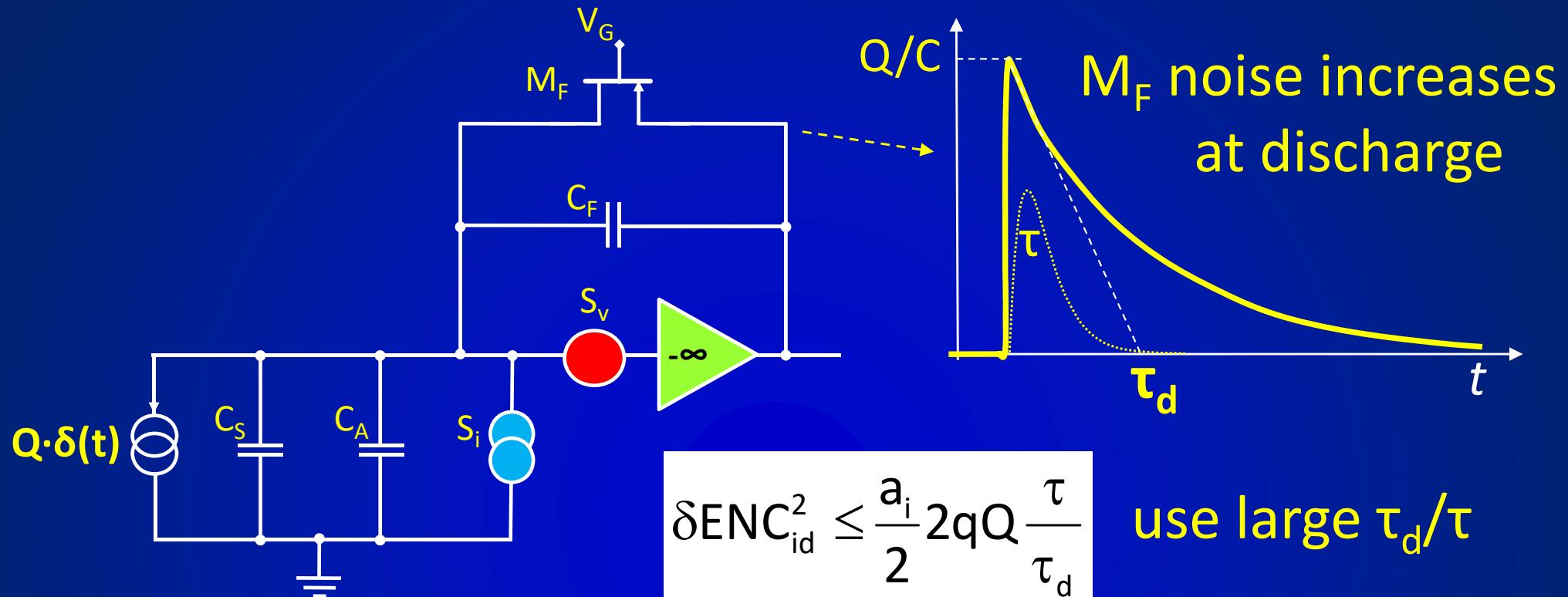
$$S_{iM_F} = \begin{cases} 4kTg_m & V_{GS} \gg V_{TH} \\ 2qI_s & V_{GS} \ll V_{TH} \end{cases}$$



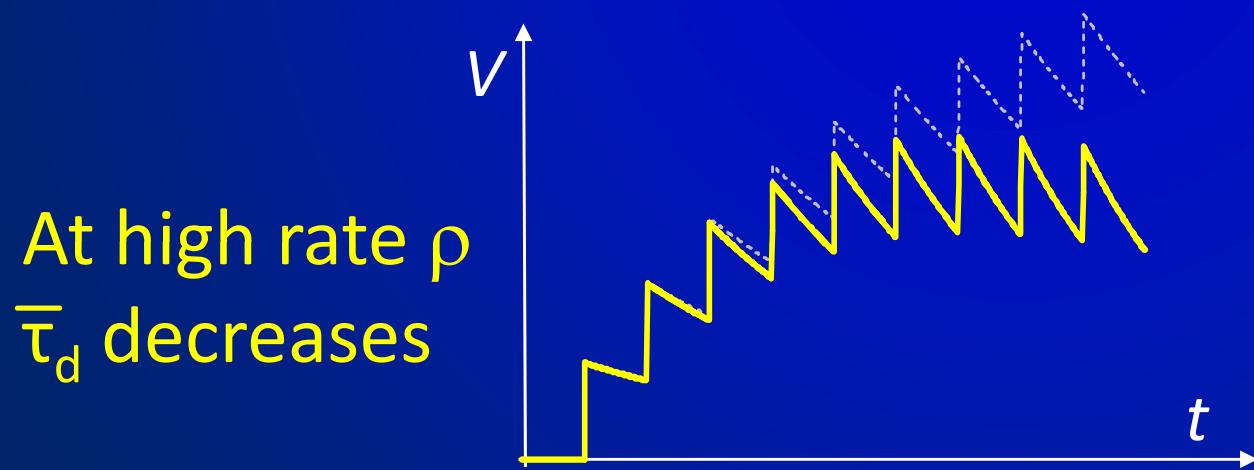
Noise at discharge ?

use large L, small W to push M_F towards strong inversion

Reset in CMOS - Discharge Noise



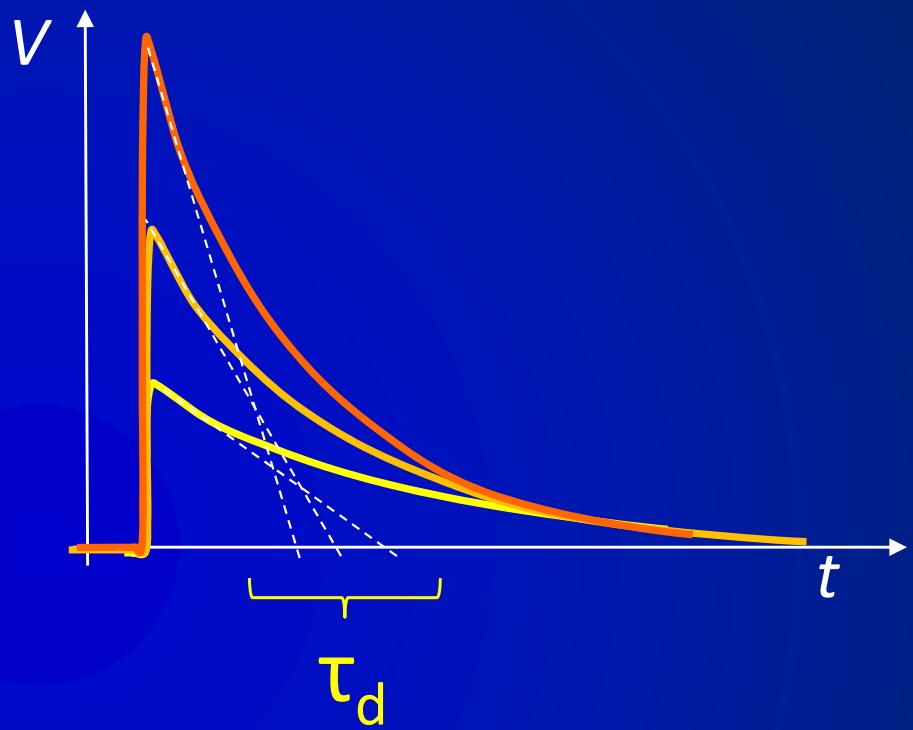
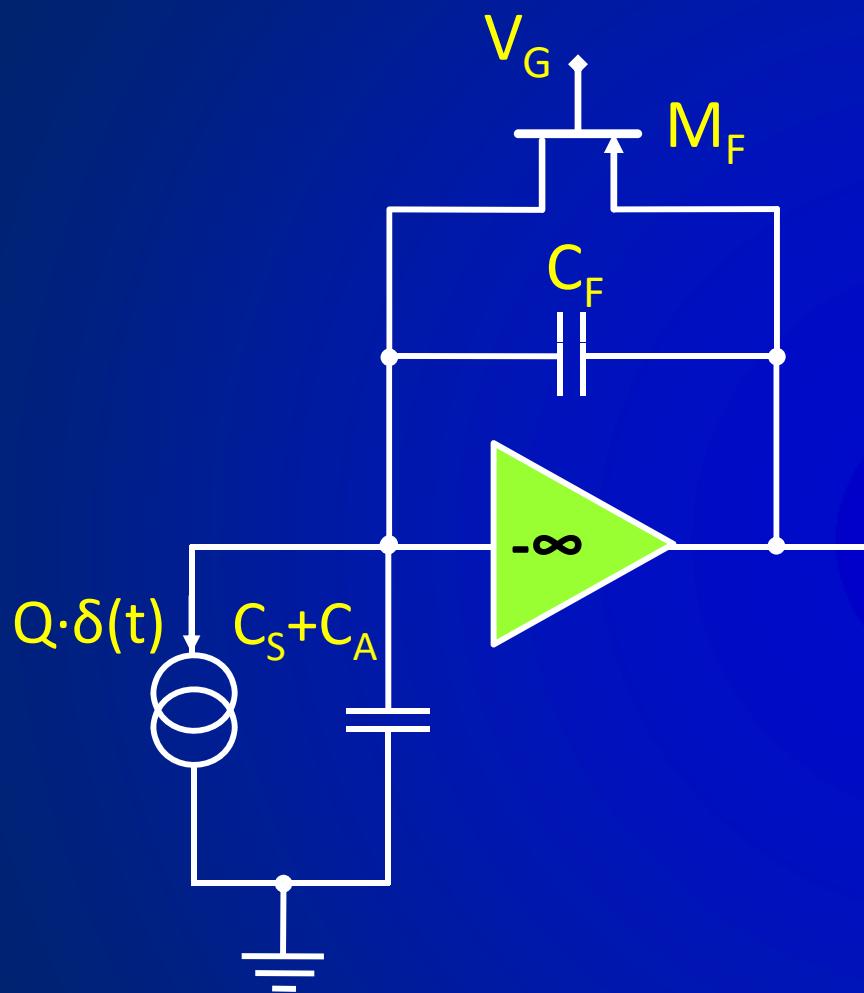
De Geronimo, NIM A 421, 1999



$$\delta\text{ENC}_{\text{idr}}^2 \leq \frac{a_i}{2} 2qQ\rho\tau$$

alternative: use M_F as switch or adopt time-variant discharge

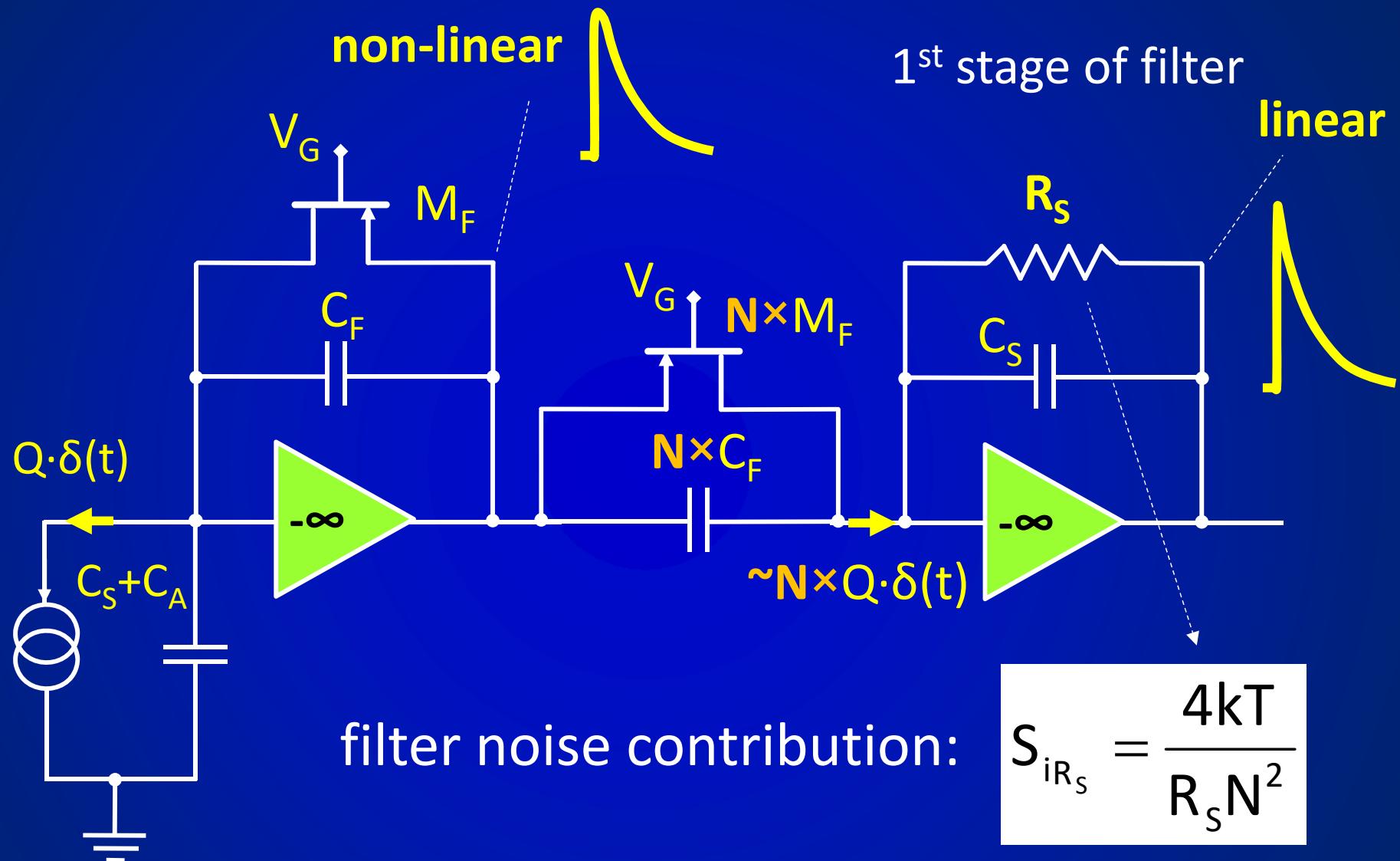
Reset in CMOS - Pole Linearity



τ_d depends on amplitude
and may affect baseline

How to realize a linear pole-zero cancellation ?

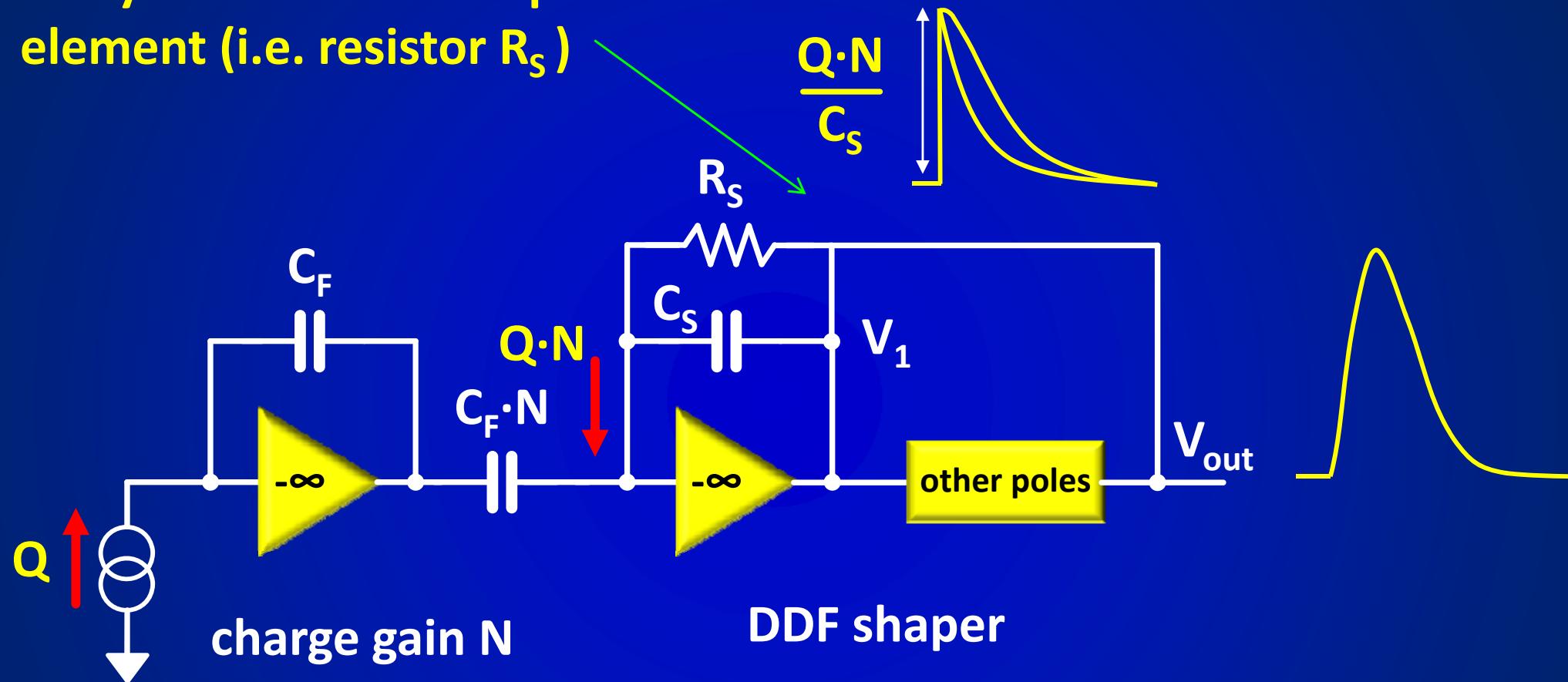
Reset in CMOS - Pole-Zero Cancellation



Effective linear "charge amplification" by N

Delayed Dissipative Feedback (DDF)

delay feedback of dissipative element (i.e. resistor R_s)

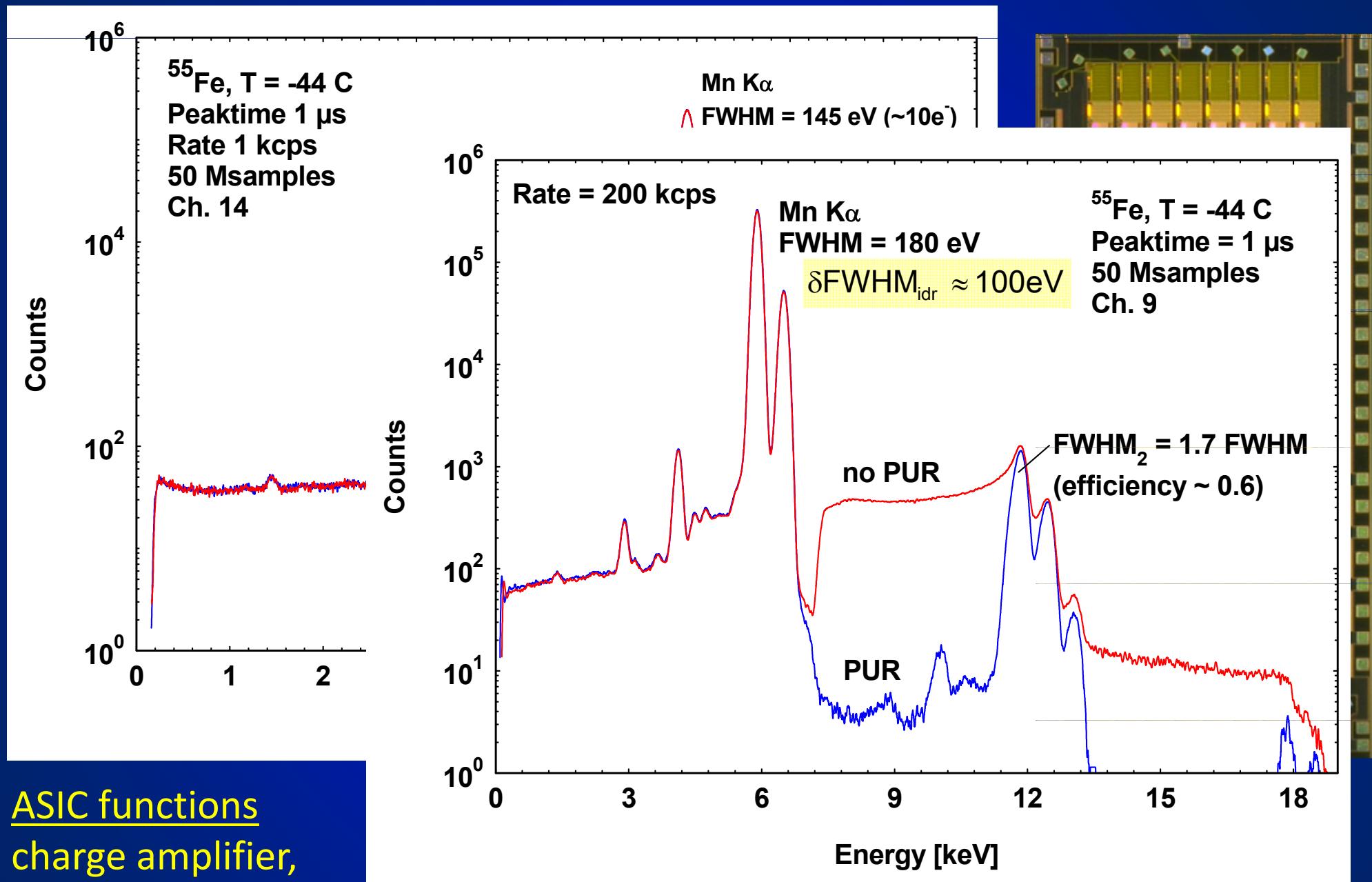


high analog dynamic range

De Geronimo, IEEE TNS 58, 2011

$$DR_a \approx \frac{Q_{\max}}{ENC_{ca} + ENC_{sh}}$$

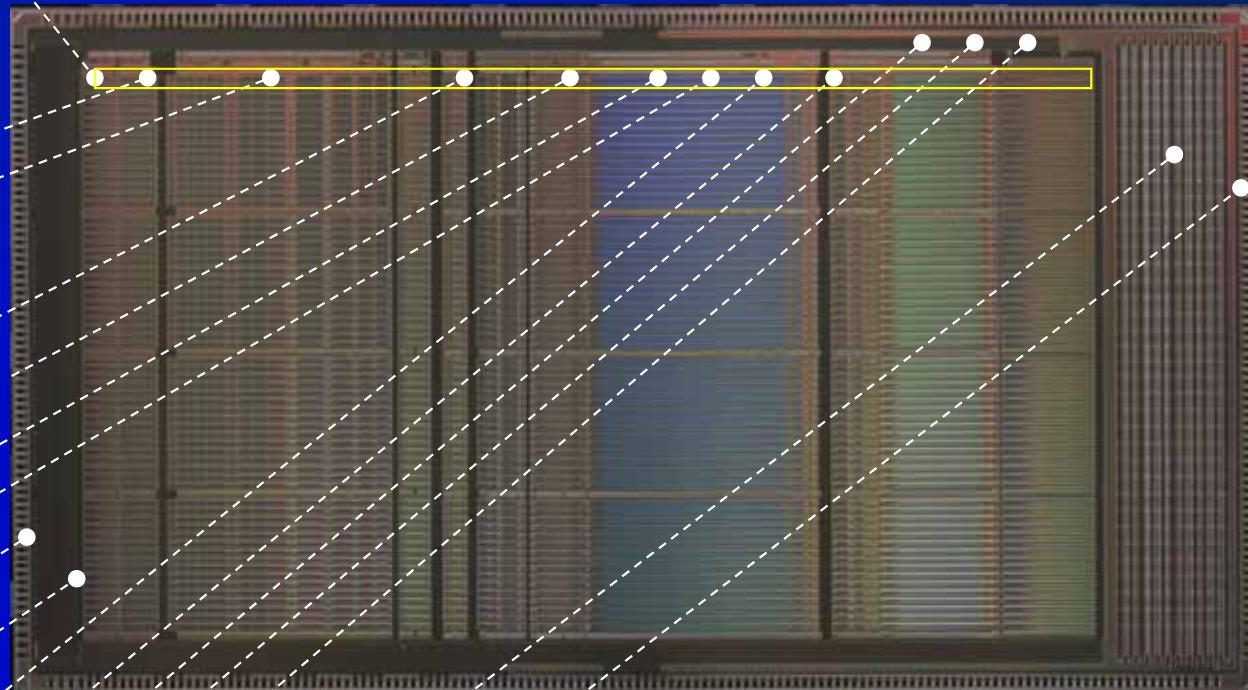
Front-End ASIC for X-Ray Spectrometers



Collaboration with NASA
De Geronimo, IEEE TNS 57, 2010

Circuits in a Front-End ASIC

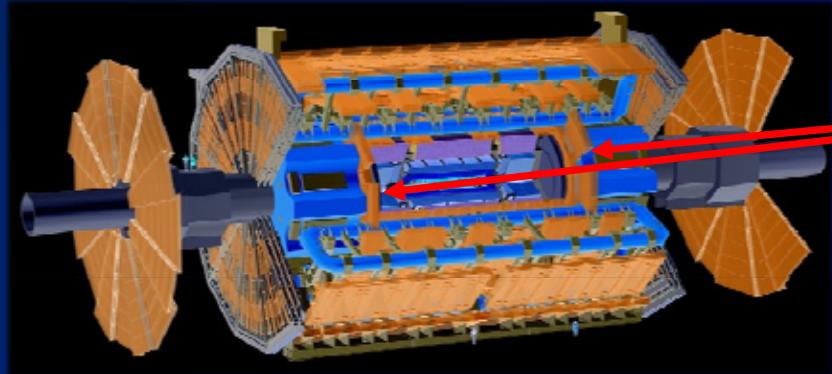
- Low-noise, low-power **charge amplifiers**
 - gas, liquid, solid state detectors
 - capacitances from $\sim fF$ to $\sim nF$
- Switched and continuous adaptive **reset**
- **High-order filters**, stabilizers, drivers
 - peak time / gain adjustment
- Single- and multi-level **discriminators**
- Peak and time detectors, derandomizers
- Analog **memories** and multiplexers
- Digital memories and **counters**
- Configuration **registers**
- ESD protections
- Calibration **pulse generators**
- Analog-to-digital converters
- Digital-to-analog converters
- Precision **band-gap references**
- Temperature sensors
- Readout control logic
- Digital signal processing (DSP)
- Low-voltage differential signaling (LVSD, SLVS)



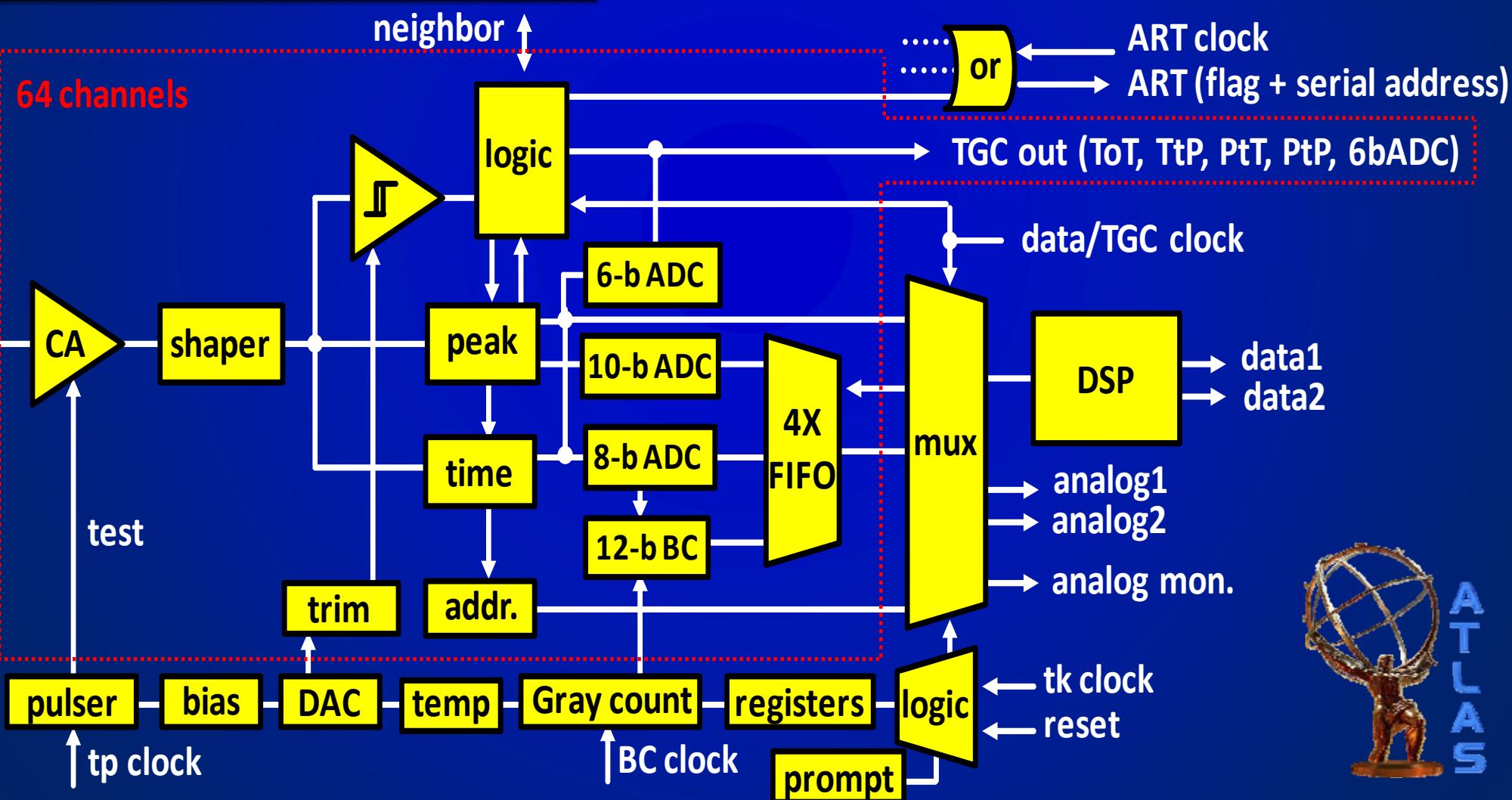
64-ch. VMM ASIC
ATLAS Muon Upgrade
 $14 \times 8.5 \text{ mm}^2$, $\sim 0.4 \text{ W/cm}^2$
 $> 6\text{M MOSFETs} (> 90\text{k/ch.}), 2016$

Pace of FE ASIC Evolution?

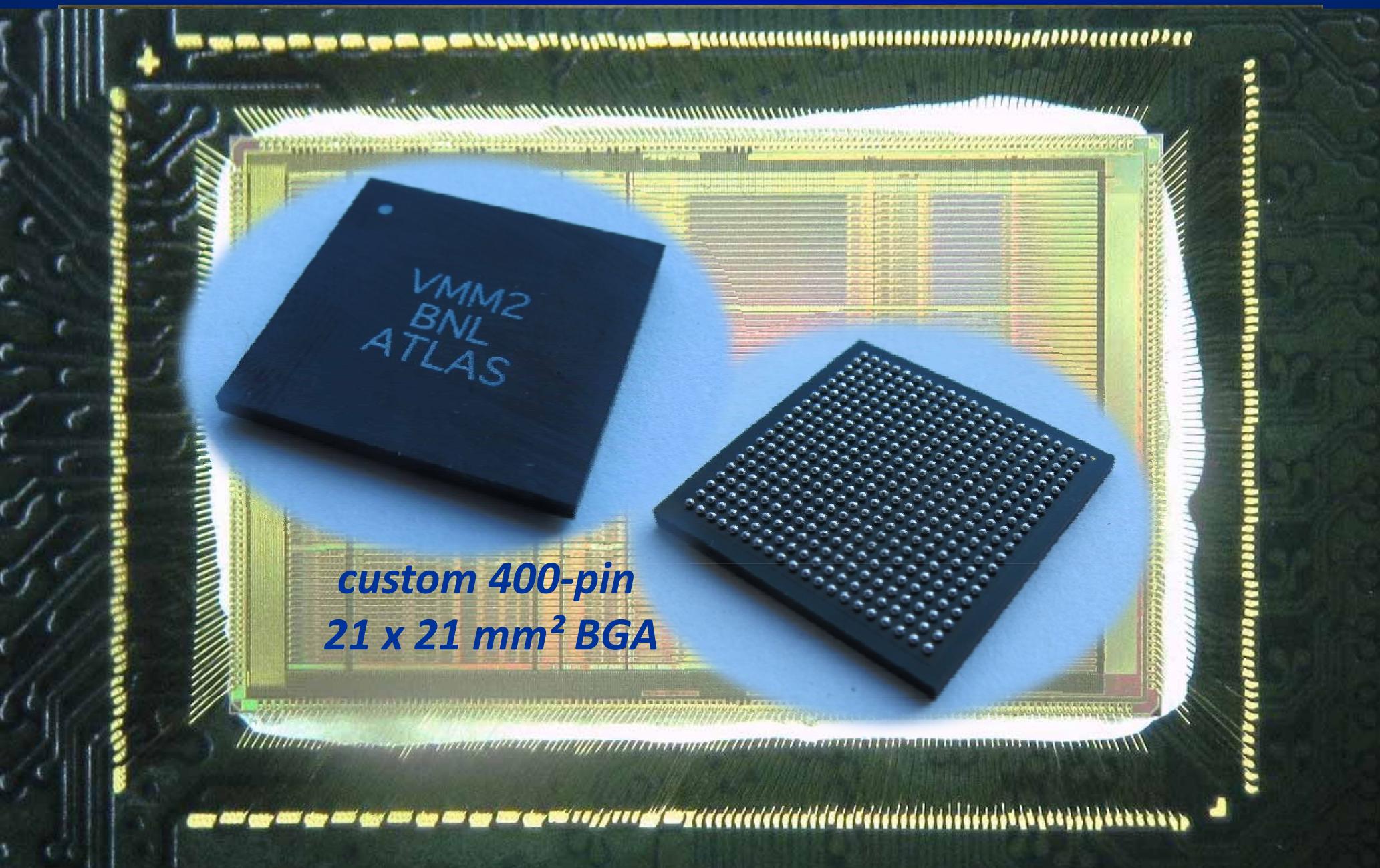
VMM (2012-16) for P1 Muon Upgrade



ATLAS Muon New Small Wheels
- sTGC and MicroMegas technologies
- 2.3M channels, 50 to 2000 pF



Physical Layout

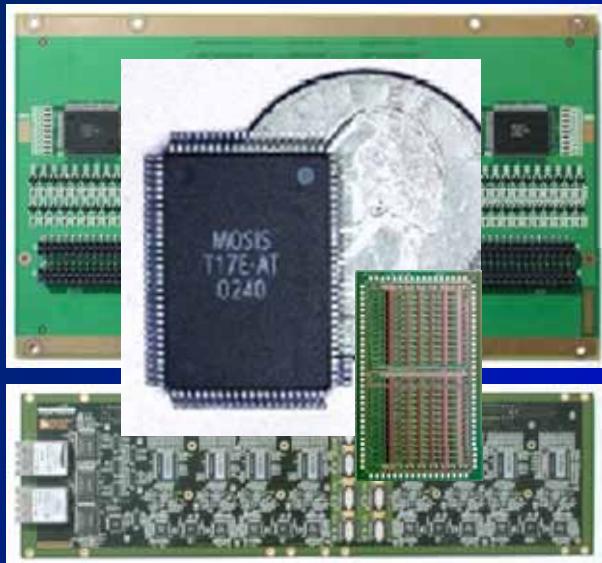


*custom 400-pin
21 x 21 mm² BGA*

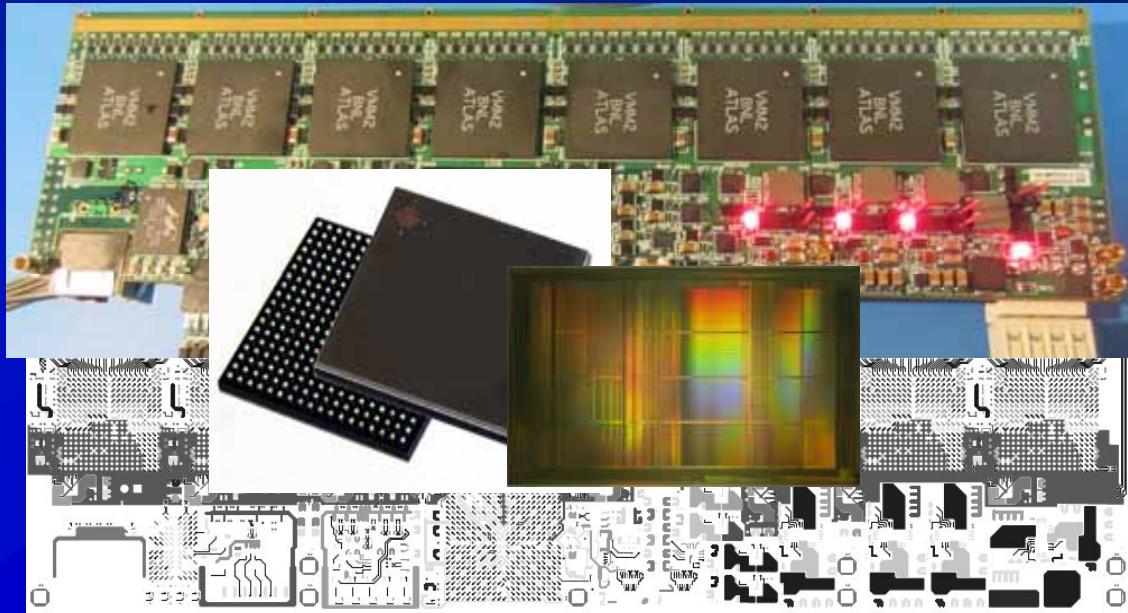
~ 400 bonding pads

130 nm
fabrication at compatible pricing
Sdropste

Impact on Radiation Detector



2005 - ASM



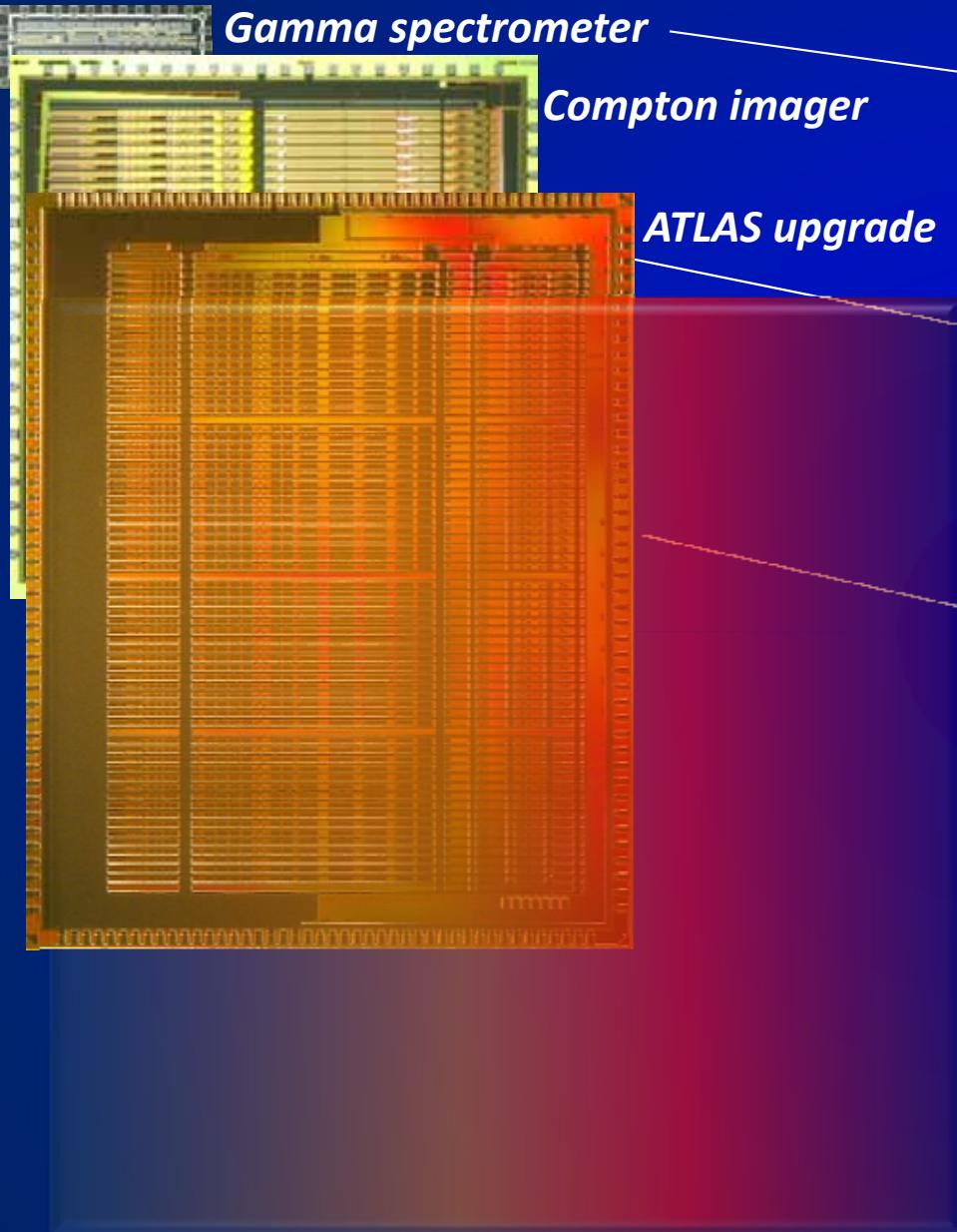
2015 - VMM

- 60x sensing elements, 10x element density, 3x power dissipation
- data-driven, trigger primitives, peak, timing, ADCs, DSP, ...

Advances in radiation detectors are tightly coupled to advances in front-end ASICs

Front-end ASICs are rapidly becoming very high functionality systems-on-chip (SOC)

Evolution of Front-End ASICs



~ year 2001
CMOS 500nm, 3.3V, ~2mm²
~ 10k transistors (~100/ch)
preamplifier/filter

~ 2006
250nm, 2.5V, 25mm²
~ 100k transistors (1k/ch)
+ discrim/peakdet/count/mux

~ 2011
130nm, 1.2V, 50mm²
~ 1M transistors (~ 10k/ch)
+ timedet/multifunc/trigprim

~ 2016 to 2020
< 90nm, < 1.2V, >100mm²
> 10M transistors (>100k/ch)
+ ADCs+DSP VMM is 90k!
SOC = System on Chip
EOC = Experiment on Chip

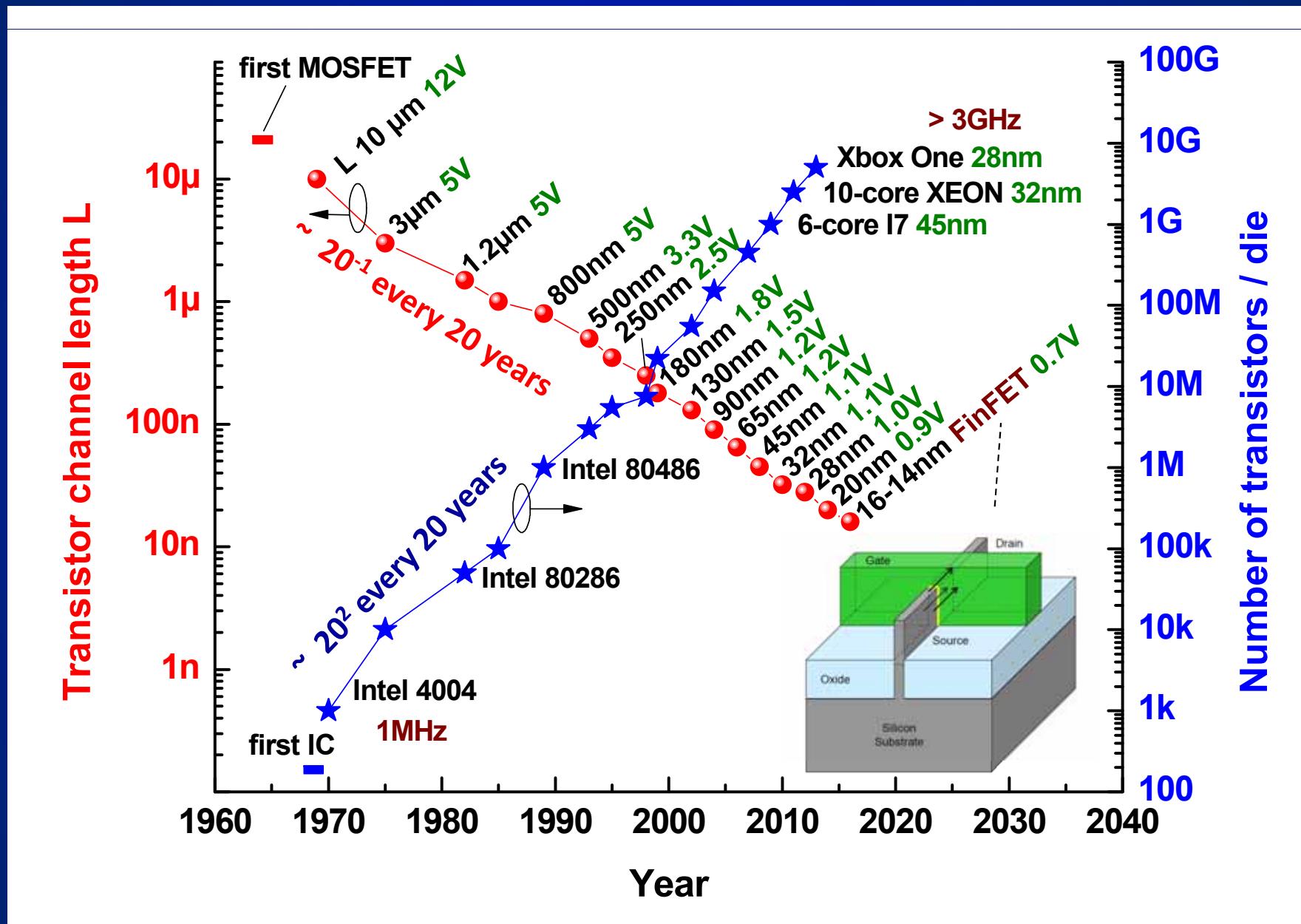
Designers	1 - 2
Years	1 - 2
Revisions	1 - 2
Simul. time	1m/ch

2 - 4
2 - 4
2 - 4
1h/ch

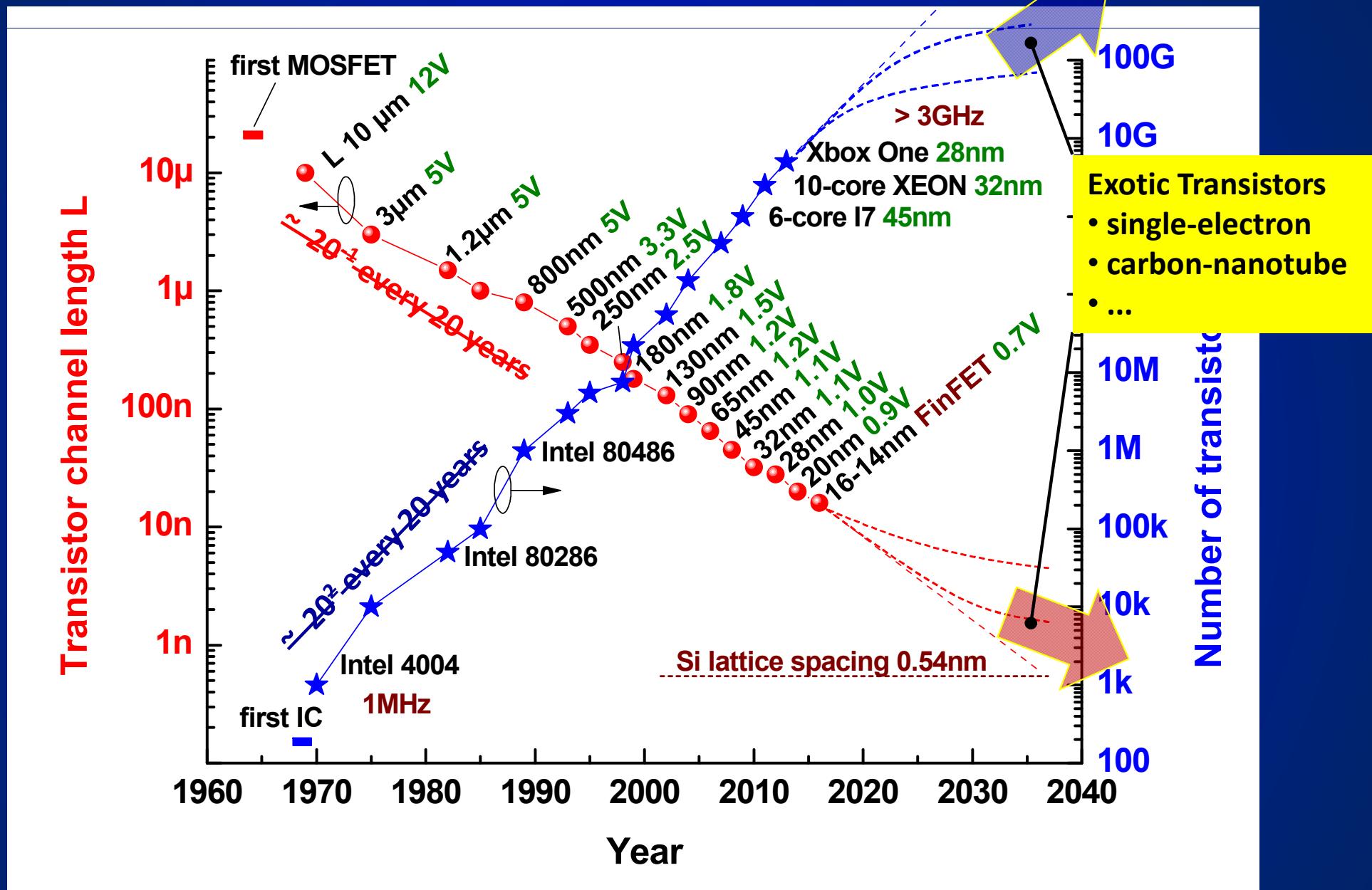
> 5
3 - 5
3 - 5
>1d/ch

Complexity and functionality are rapidly increasing

The Rapid Evolution of Microelectronics

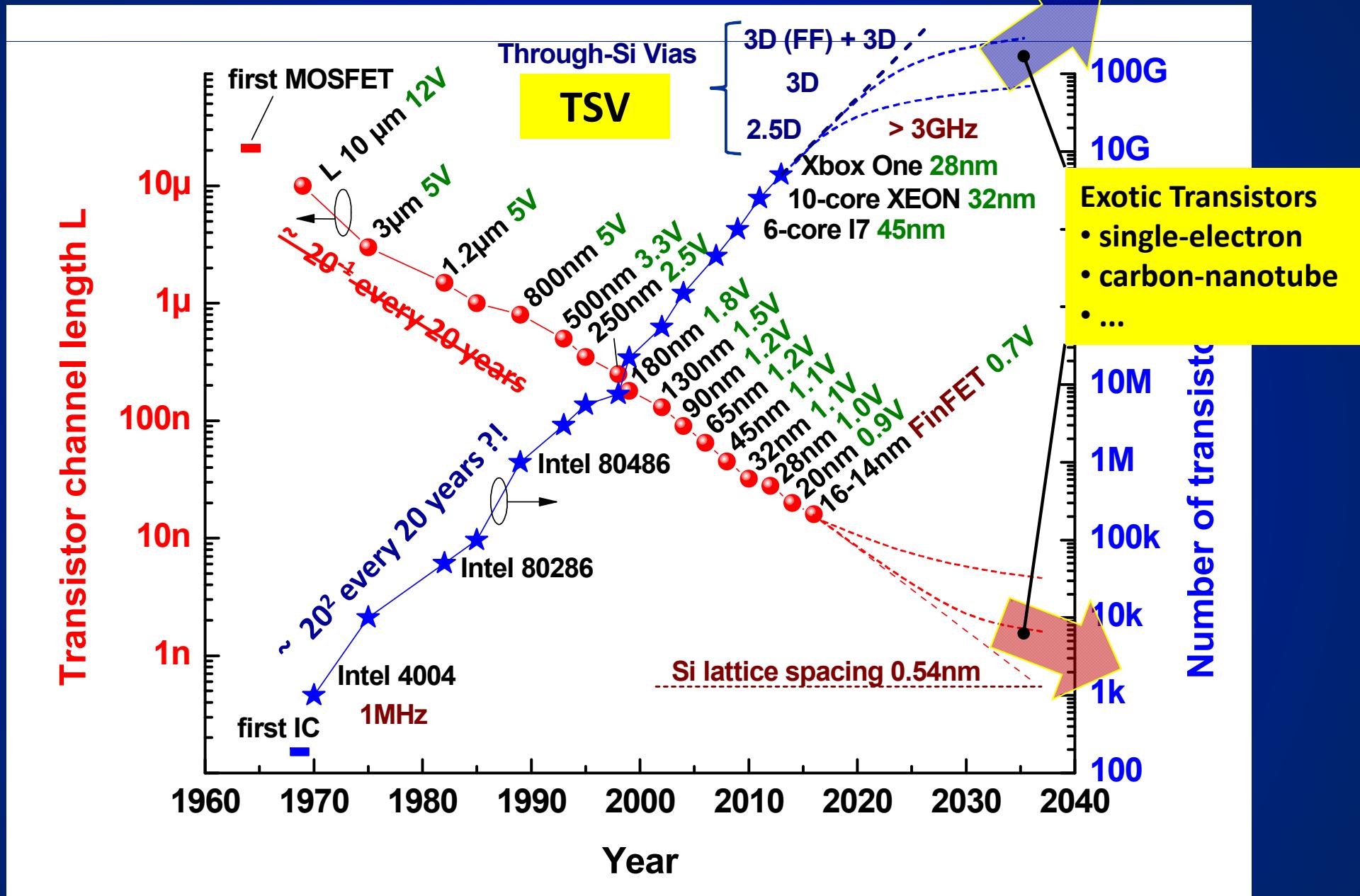


The Rapid Evolution of Microelectronics



Introduced in the '90s, exotic transistors made considerable progress, but are still far from achieving reproducibility and reliability required for microelectronics

The Rapid Evolution of Microelectronics



Progress heavily driven by consumer electronics

AMPLEX (1988) - First Large Scale

Particle physics ASIC

16 channels, ~800 MOSFETs (~50/ch)

3 μ m CMOS, 5V, 1.1 mW/ch, 16 mm²
amplifier/filter/track & hold/mux

for Silicon micro-strips at UA2

Nuclear Instruments and Methods in Physics Research A288 (1990) 157–167
North-Holland

157

AMPLEX, A LOW-NOISE, LOW-POWER ANALOG CMOS SIGNAL PROCESSOR FOR MULTI-ELEMENT SILICON PARTICLE DETECTORS

Eric BEUVILLE ^{3)*}, Kurt BORER ¹⁾, Enrico CHESI ³⁾, Erik H.M. HEIJNE ³⁾, Pierre JARRON ³⁾, Bohdan LISOWSKI ^{3)**} and Simon SINGH ²⁾

¹⁾ Laboratorium für Hochenergiephysik, Universität Bern, Switzerland

²⁾ Cavendish Laboratory, University of Cambridge, UK

³⁾ CERN, EF Division, 1211 Geneva 23, Switzerland

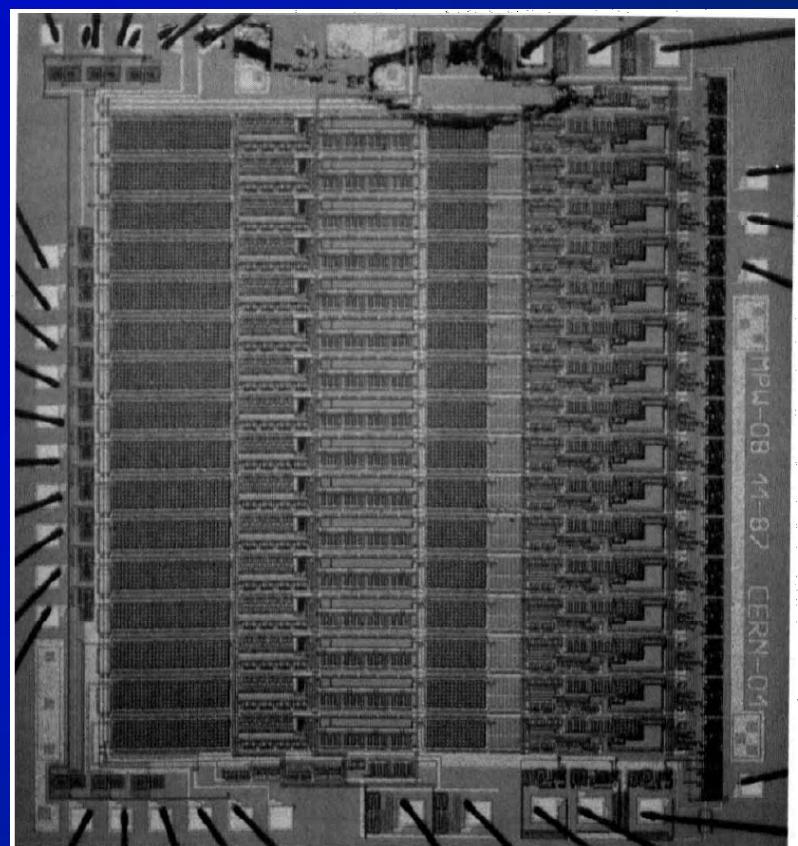


Fig. 7. Picture of the 16-channel AMPLEX chip. The size is 4.1 × 4 mm².

FE-I5 (2016-17)

Particle physics ASIC

260k pixels, 1G MOSFETs ($\sim 4,000/\text{px}$)

65nm, 1.2V, 0.5-1 W/cm 2 , $>400\text{mm}^2$

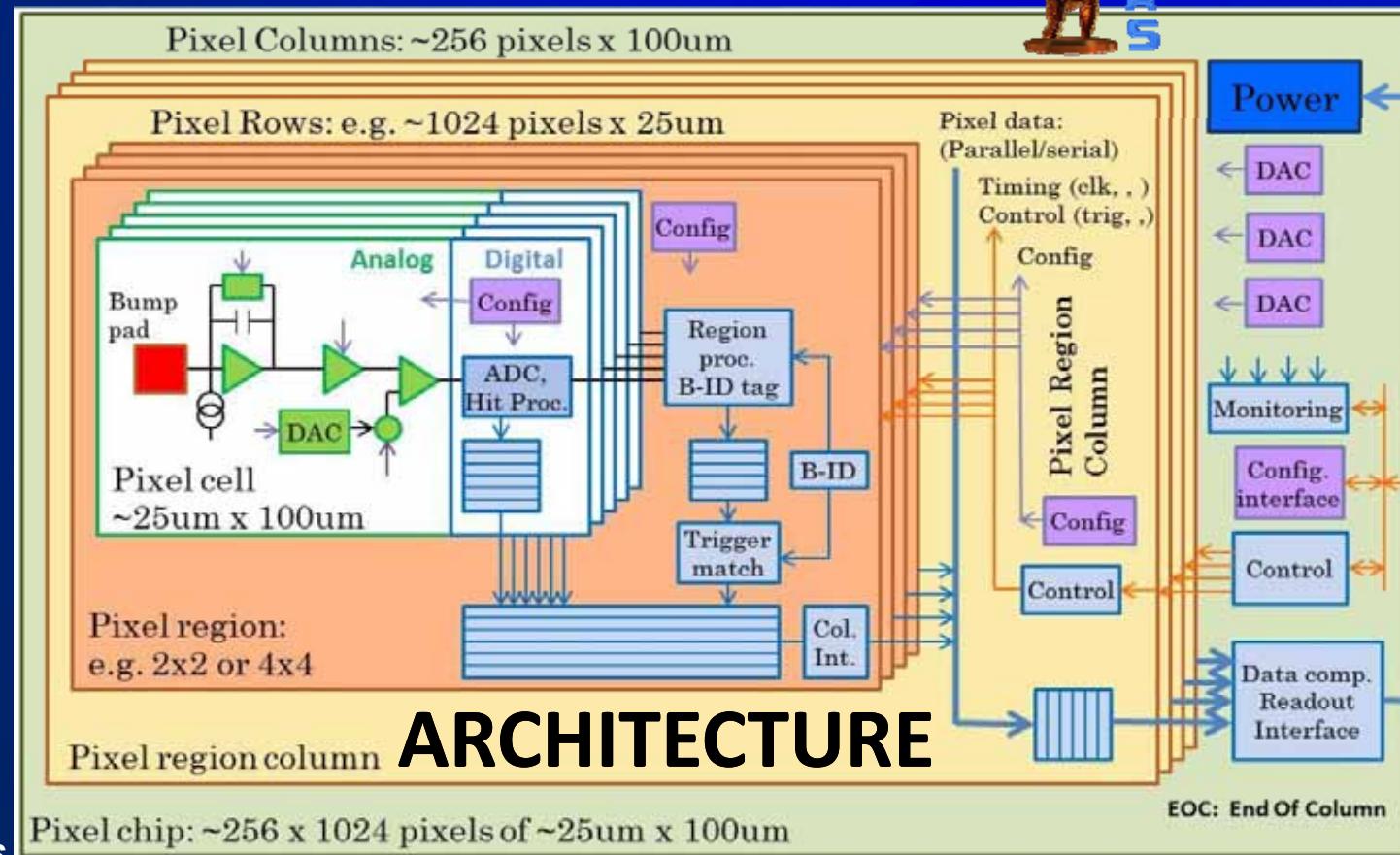
high complexity/functionality, DSP

for ATLAS vertex hybrid pixels



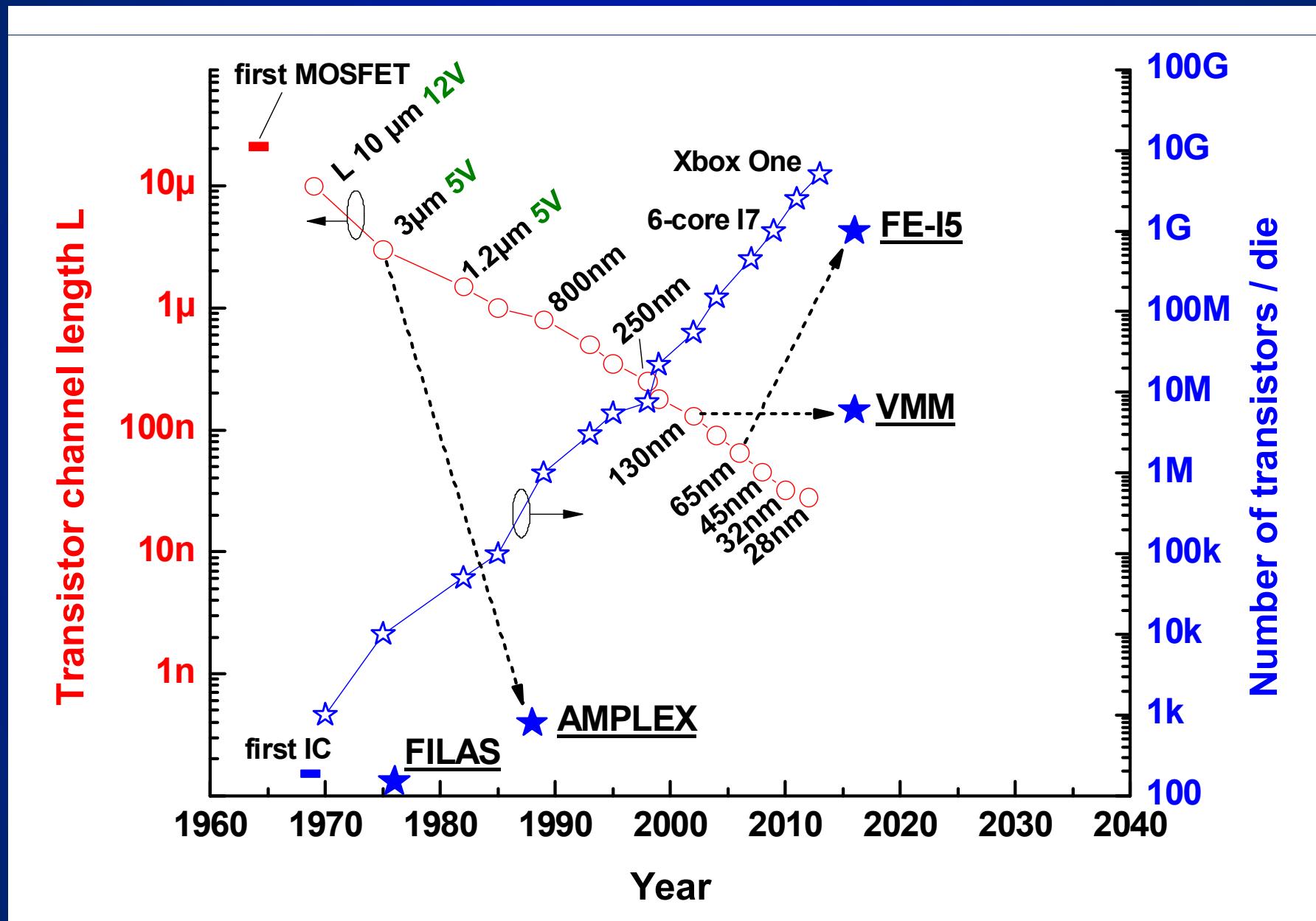
Institute	WG1 Radiation	WG2 Top level	WG3 Sim./Ver	WG4 I/O	WG5 Analog	WG6 IPs
Bari	C		A			A
Bergamo-Pavia	A			C	A	B
Bonn	C	A	A	R	R	A
CERN						
CPPM						
Fermilab						
LBNL						
LPNHE Par						
NIKHEF						
New Mexico						
Padova						
Perugia						
Pisa		B	A	A		A
PSI	B	A		C	A	A
RAL		B	B		A	C
Torino	C	B	C	B	A	A
UCSC	C	B	C			A

19 institutions
specialized working groups
100 collaborators
(~50 ASIC designers)



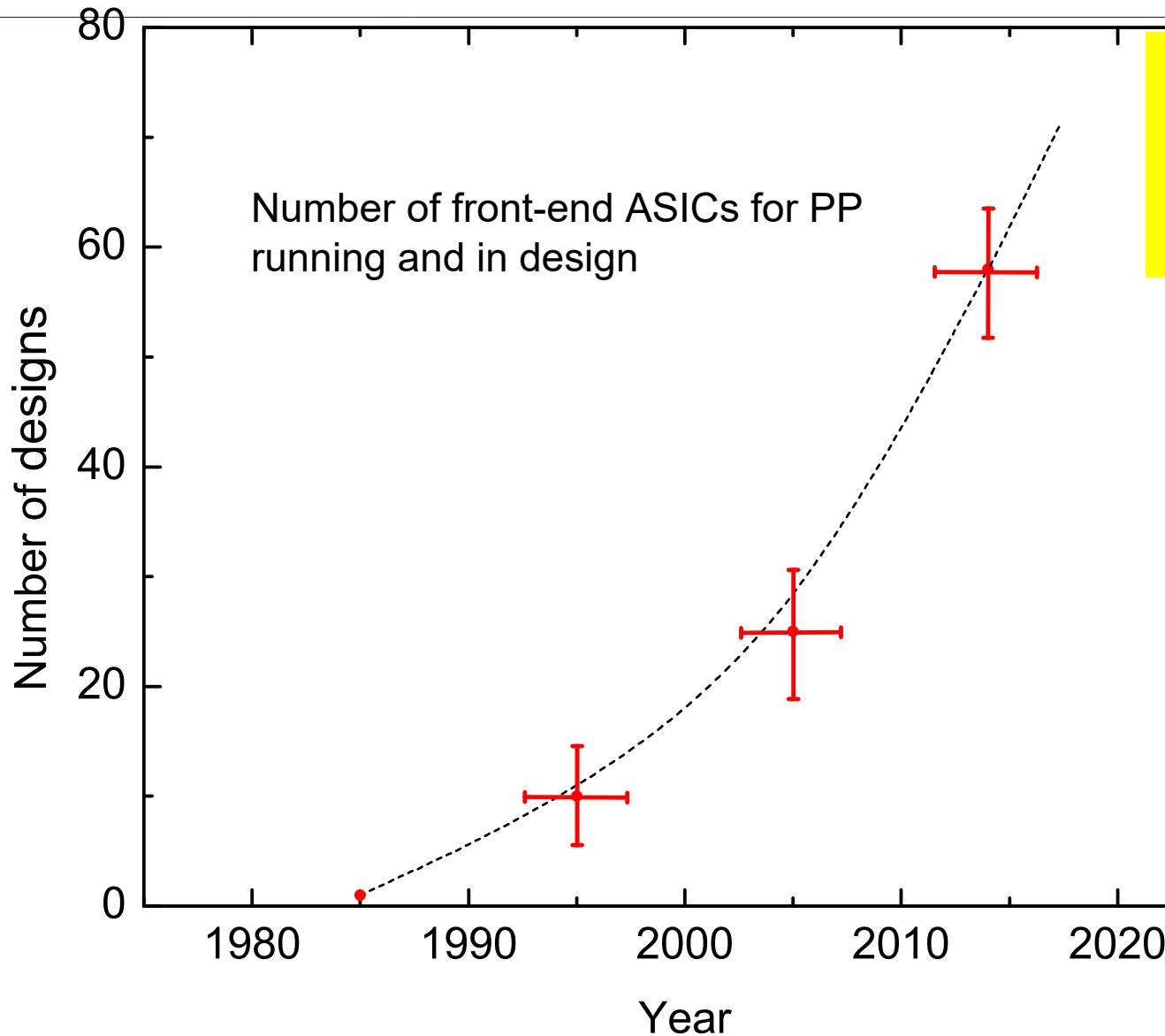
2X2 pixel unit

Compare to Evolution of Microelectronics



Front-end ASICs keep pace, but with ~decade delay

Front-end ASICs / Year (Particle Physics)



2013

~ 60 FE (out of ~140)

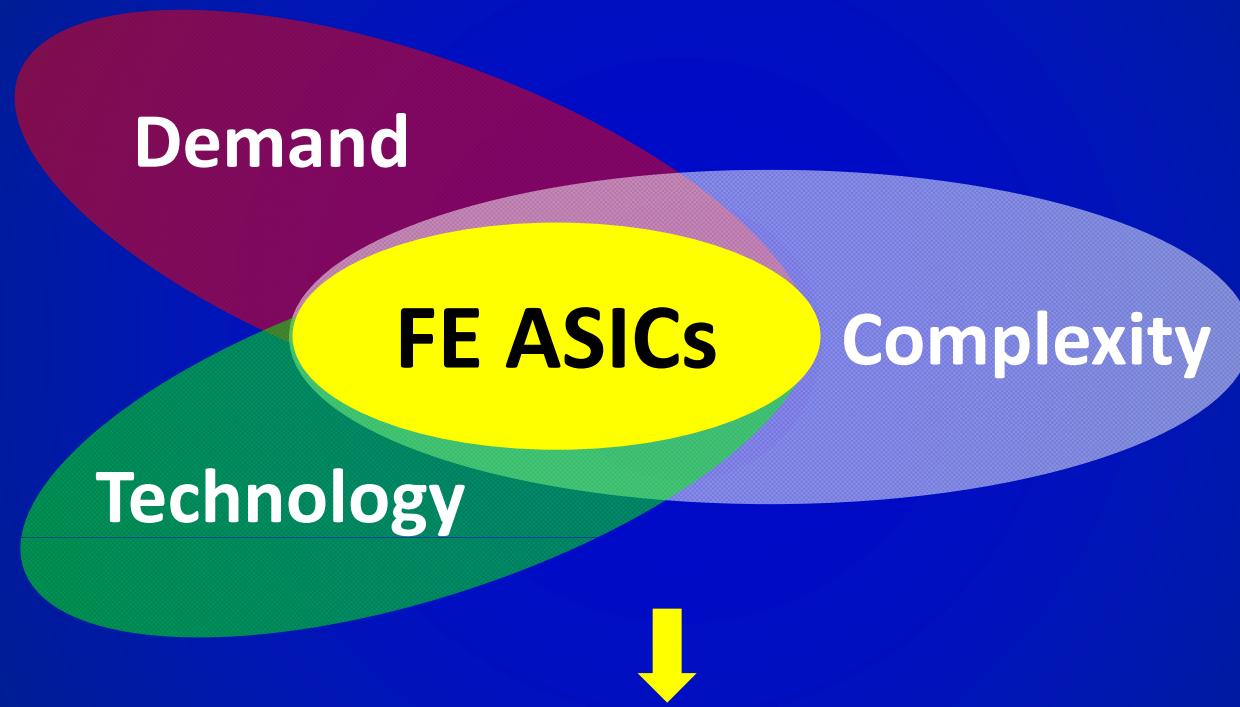
~ 35 FE in design

arXiv:1307.3241

Exponential increase in demand for FE ASICs

Paradigm

Advances in radiation detectors are tightly coupled to advances in front-end ASICs



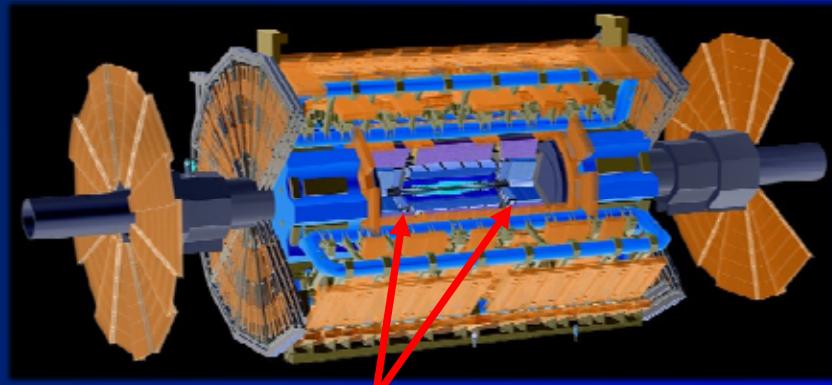
- Design resources must be increased
- Collaborations must be promoted

Impact of R&D on Front-End ASICs at BNL

Year	Novel Circuit	Collaborator	Patent	Publications	Impact areas
1998	adaptive reset	eV Products	*♦	*	RHIC, ATLAS, NSLS, Nonproliferation, Security, Medical
1998	high order complex shaper	eV Products		*	ATLAS, LBNE, LEGS, SANS, NSLS, Nonproliferation, Security, Medical
1999	band-gap references	R&D			ATLAS, LBNE, LEGS, SANS, NSLS, Nonproliferation, Security, Medical
2001	multi-phase peak detector	R&D	*♦	*	ATLAS upgrades, LEGS, SANS, NSLS, Nonproliferation, Security, Medical
2003	low time-walk time detector	LEGS TPC		*	ATLAS upgrades, LEGS, NSLS, Nonproliferation, Security, Medical
2003	neighboring logic	LEGS TPC		*	ATLAS upgrades, LEGS
2004	peak-detector derandomizer	eV Products	*♦	*	NSLS, Nonproliferation
2004	low voltage adaptive reset	LEGS TPC	*♦	*	ATLAS upgrades, LEGS, SANS, NSLS, Nonproliferation, Security, Medical
2005	coplanar grid time correction	LANL	*	*	Nonproliferation
2006	coplanar grid ampl. correction	R&D	*	*	Nonproliferation
2006	multi-window photon counting	eV Products	*♦	*	NSLS, Medical
2006	current-mode ADC	He ³ SANS	*	*	SANS, ATLAS upgrades
2007	sub 10-electron front-end	NASA		*	NSLS
2008	bipolar cathode timing	DoD	*	*	Nonproliferation
2010	threshold-peak pile-up rejector	NASA	*	*	NSLS
2011	delayed dissipative feedback	ATLAS	*	*	ATLAS upgrades, NSLS, Nonproliferation
2011	multiphase current-mode ADC	LBNE	*	*	LBNE, ATLAS upgrades
2012	sub-hysteresis discrimination	ATLAS	*	*	ATLAS upgrades
2013	current-output peak detector	ATLAS	*	*	ATLAS upgrades
2016	low-noise termination	ATLAS	*		ATLAS upgrades
	R&D				
2011-	cryogenic circuits	R&D, Physics		*	LBNE, Neutrinoless, Dark matter, Nonproliferation, NSLS II
2011-	flip-chip interconnects	R&D			NSLSII, Nonproliferation, Neutrinoless
2013-	2D front-ends	R&D, NSLS		*	NSLSII, Nonproliferation, Physics
2013-	ADCs for front-ends	R&D, SBU, LDRD?			all areas
2014-	Integrated DSP & SOC	R&D, SBU			all areas

♦ commercialization

LAr Calorimeter P2 Upgrade

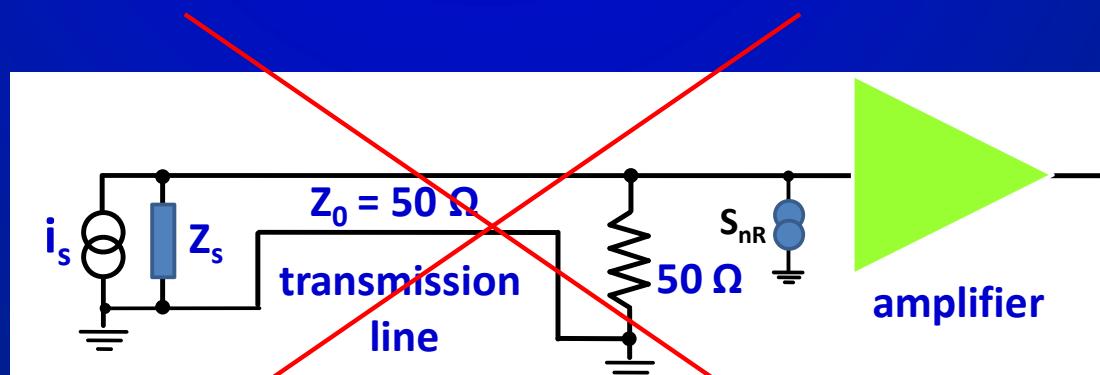


ATLAS LAr Calorimeter

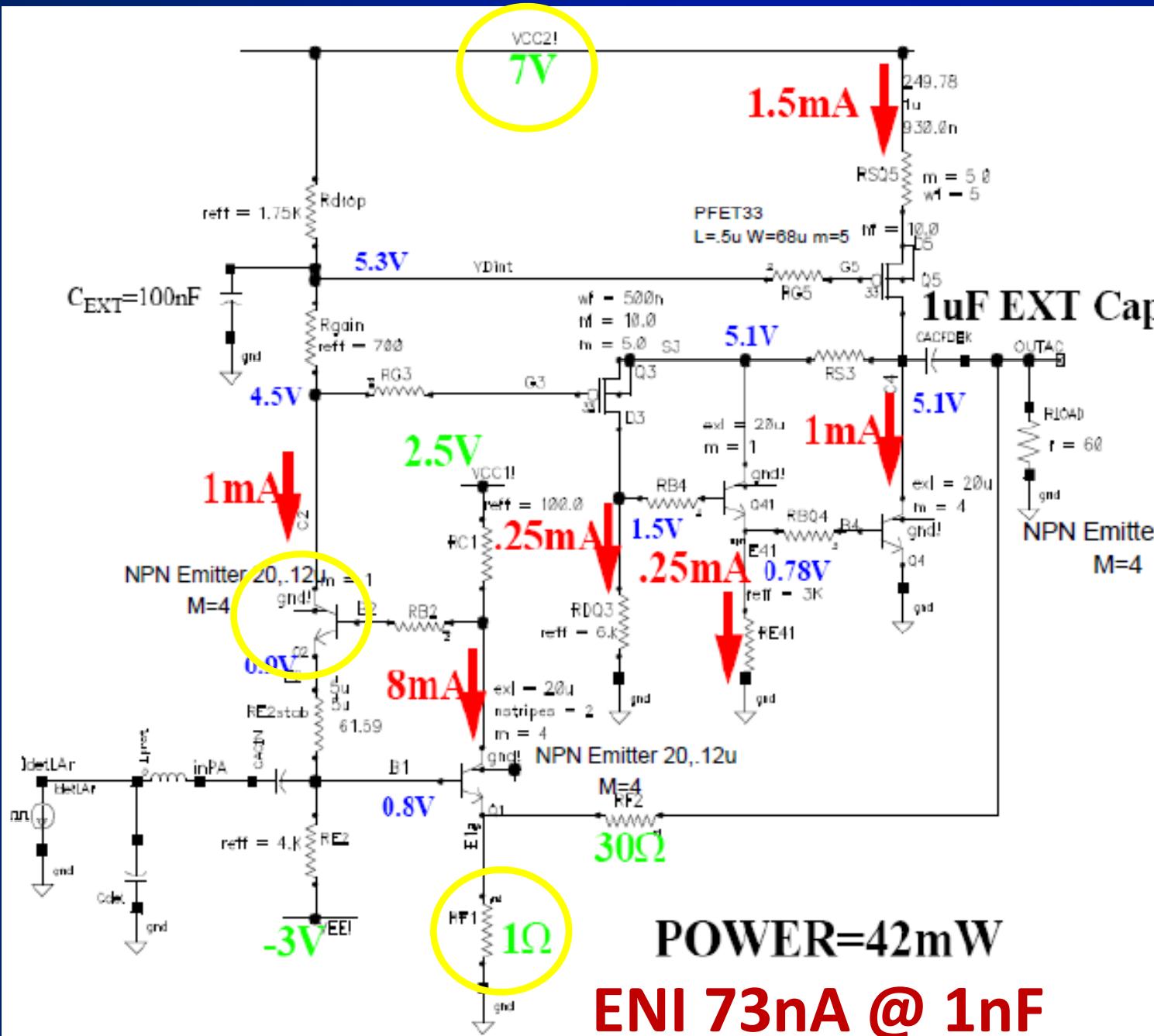
- Capacitance up to 2.5nF
- Termination $25/50\ \Omega$
- Current up to 10mA
- ENI 60nA rms
- Linearity 0.2%
- 180k channels

Can we use a termination resistor?

$$\text{ENI}_R \approx \frac{4kT}{R\tau_{P\delta}^{1/2}} \approx 110\text{nA @ 20ns}$$



LAr Calorimeter Reference Design



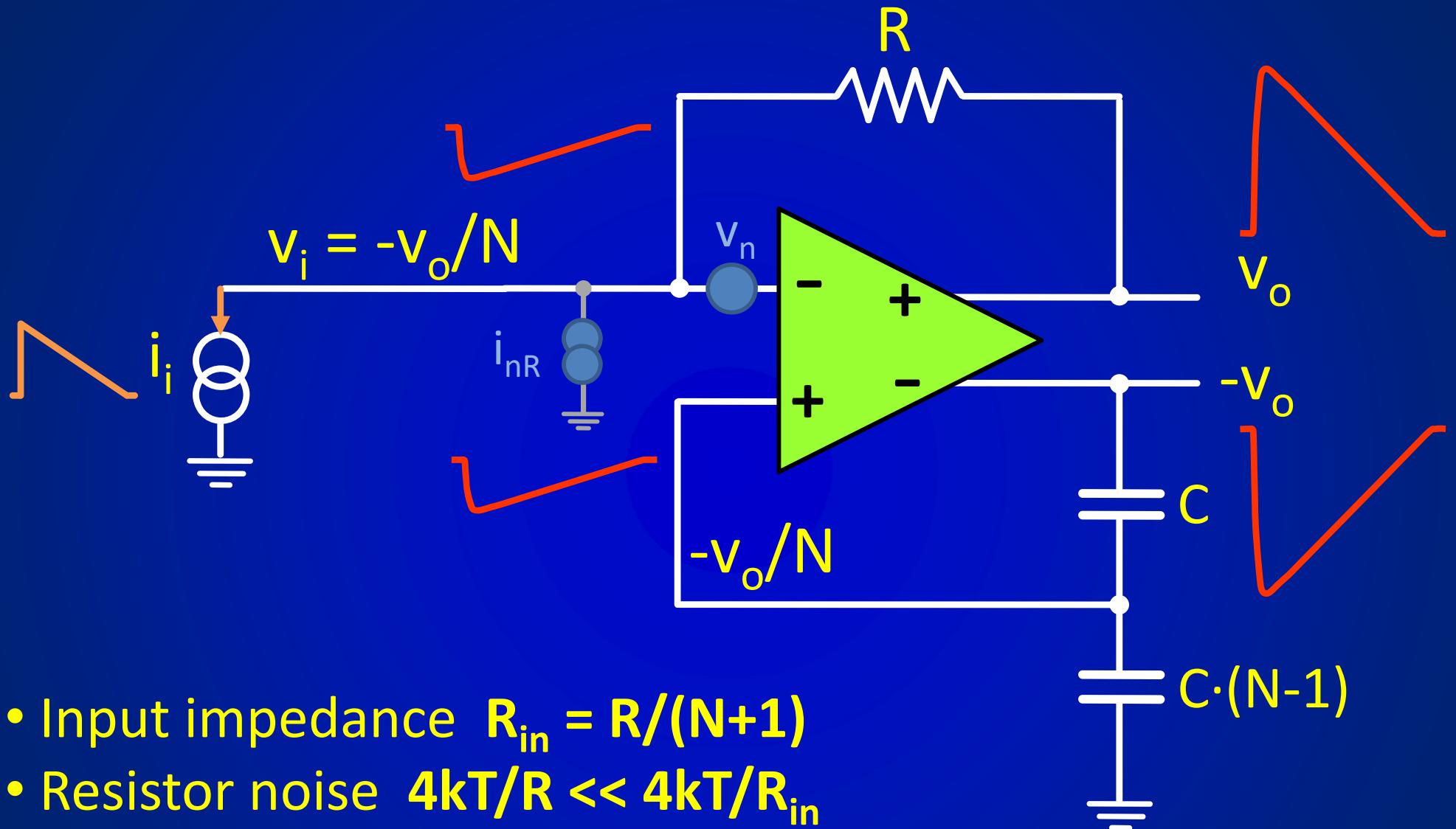
- Based on low noise line-terminating preamplifier circuit topology presently used in ATLAS LAr
- SiGe higher base doping \Rightarrow lower r_{bb} , for low noise
- “high breakdown” ($V_B=3.6$ V devices) allow for higher swing to accomodate full 16-bit dynamic range
- thick “analog” metal allows for low resistance connections to input, E_1
- BJTs are excellent drivers: output current ~ 170 mA at $I_{in}=5$ mA
- $e_{n, equiv} = 0.26$ nV/ \sqrt{Hz}
- $ENI = 73$ nA rms (incl. 2nd stage, $C_d = 1$ nF)
- $P_{tot} = 42$ mW

Newcomer-Rescia

• TWEPP 2009

<https://inspirehep.net/record/1196637/files/ATL-LARG-PROC-2009-017.pdf>

HLC - Fully-Differential FE with Passive Feedback



- Input impedance $R_{in} = R/(N+1)$
- Resistor noise $4kT/R \ll 4kT/R_{in}$
- Very stable termination (R, N indep. of signal current and active components)
- Fully-differential output
- High linearity, ENI<60nA

Conclusions

- Advances in radiation detectors are tightly coupled to advances in front-end ASICs
- Successful ASIC design needs close collaboration with lead scientists and detector experts
- Increase in demand, complexity and functionality (towards front-end systems-on-chip)
- Maintaining front-end ASIC design capability requires substantial increase in resources

Acknowledgment

Brookhaven National Laboratory and the ATLAS Collaboration
Kai Vetter (LBL)