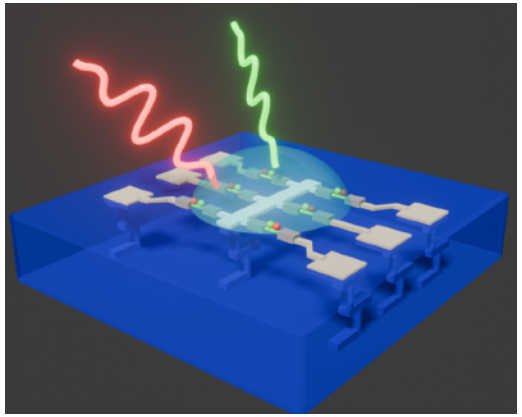
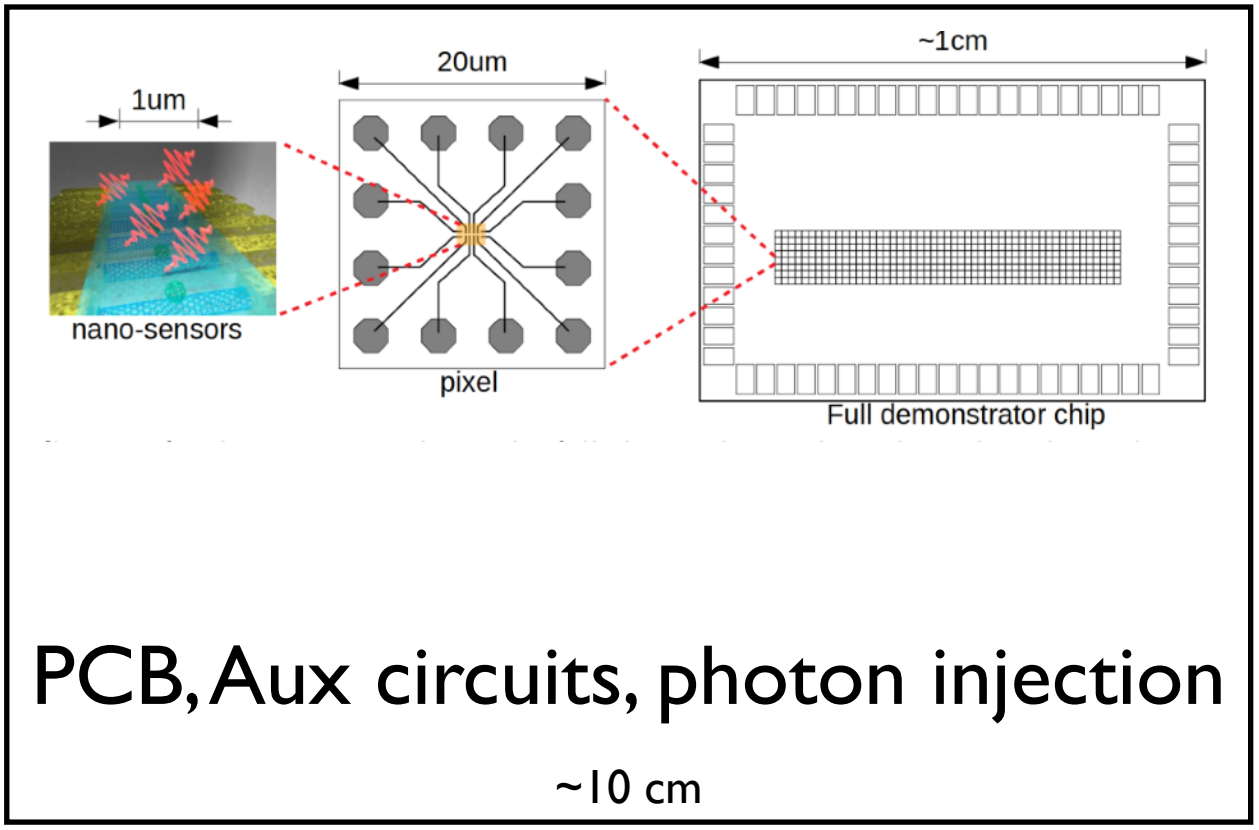
# Nanoscale hybrids Demonstrator circuits and testing

Yuan Mei

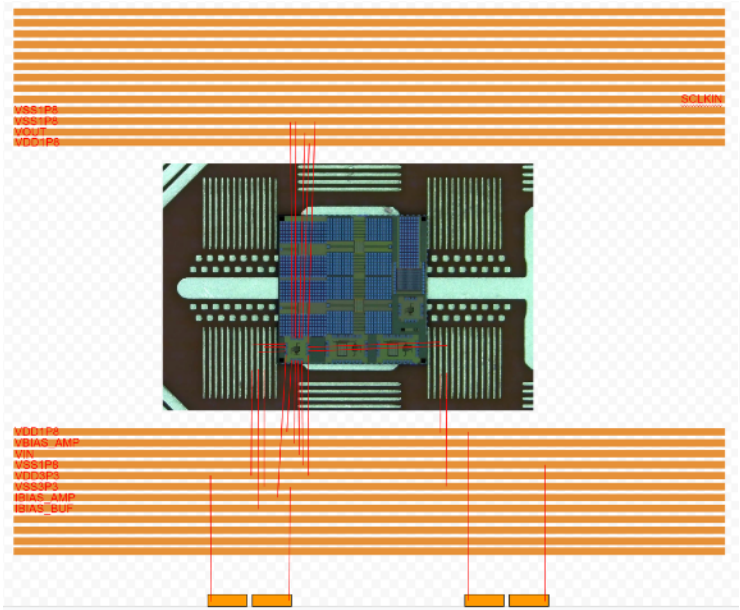
# Demonstrator

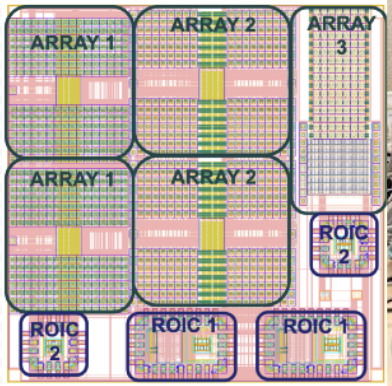


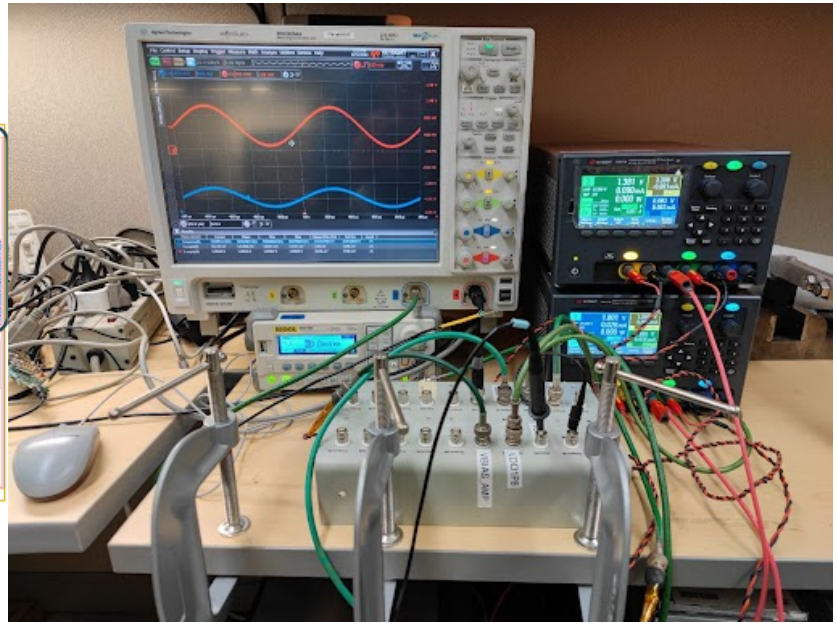


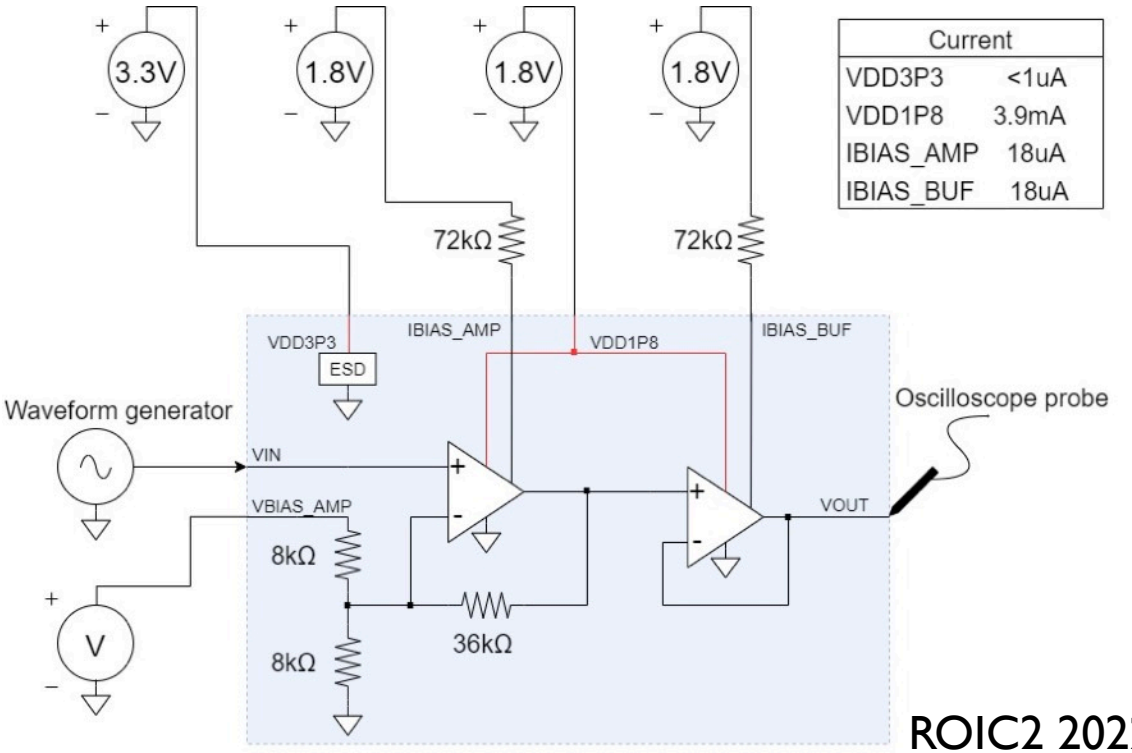

- Photon injection (coupling and calibration)
- CMOS chip powering, biasing, readout, diagnostics
- Through CMOS chip
  - Nanoscale device bias, characterization, readout, etc.

# Early prototype

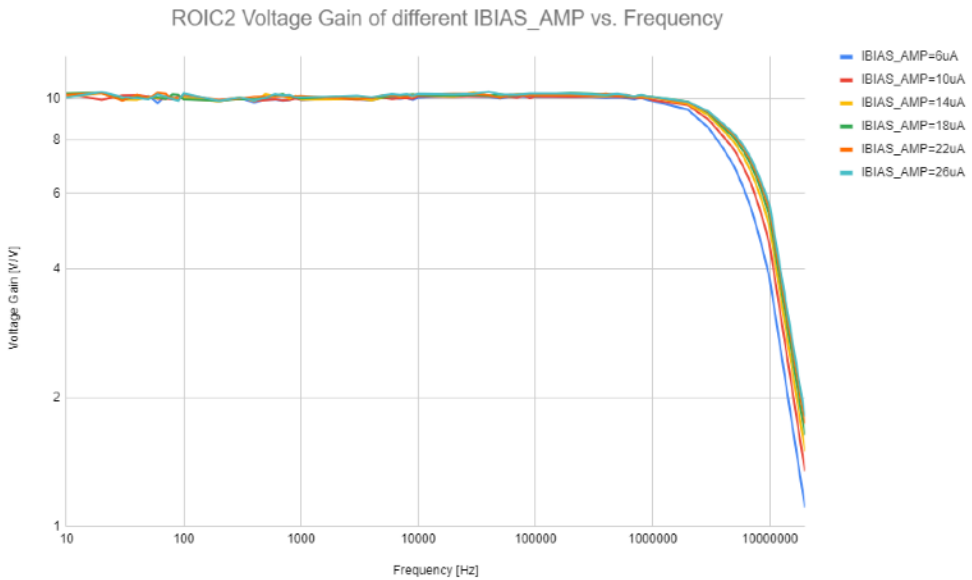


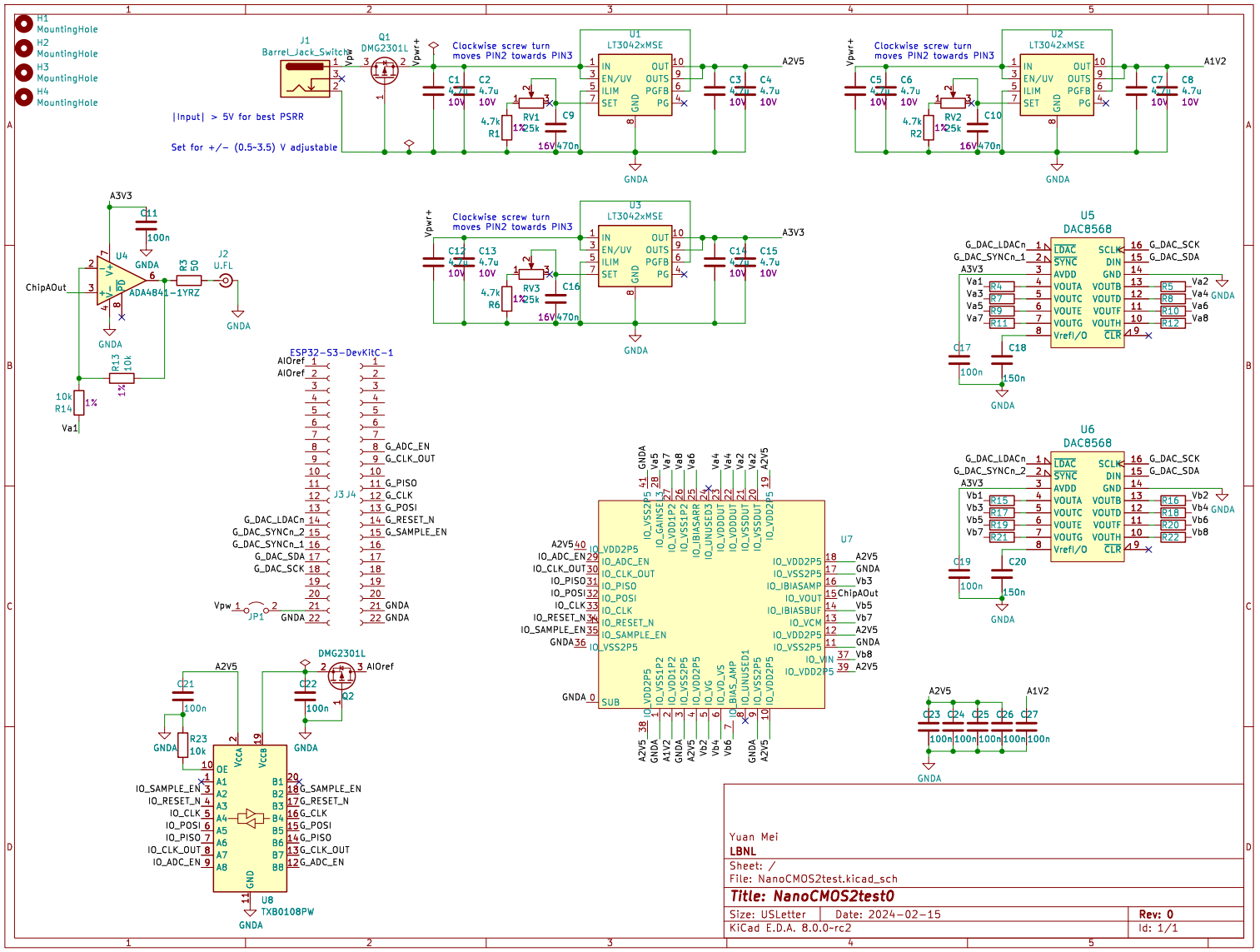


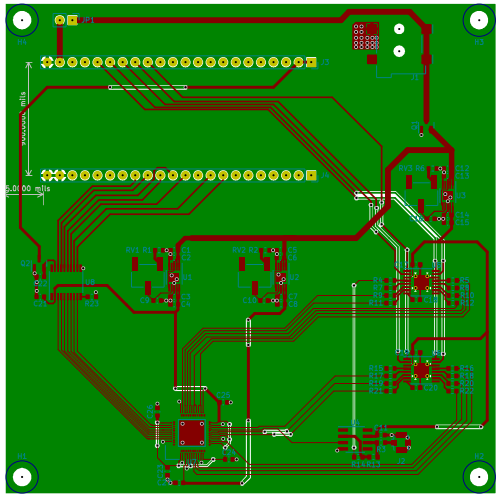

| Current | |
|---|---|
| VDD3P3 | <1uA |
| VDD1P8 | 3.9mA |
| IBIAS_AMP | 18uA |
| IBIAS_BUF | 18uA |

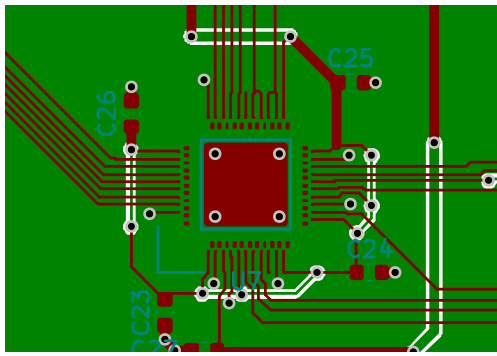



ROIC2 202208, tested by P. Miao

# PCB integrating test functions

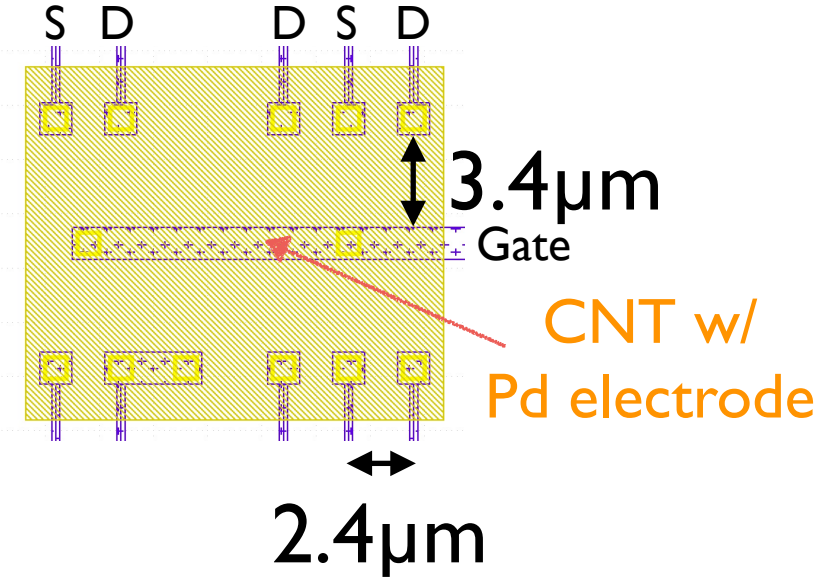


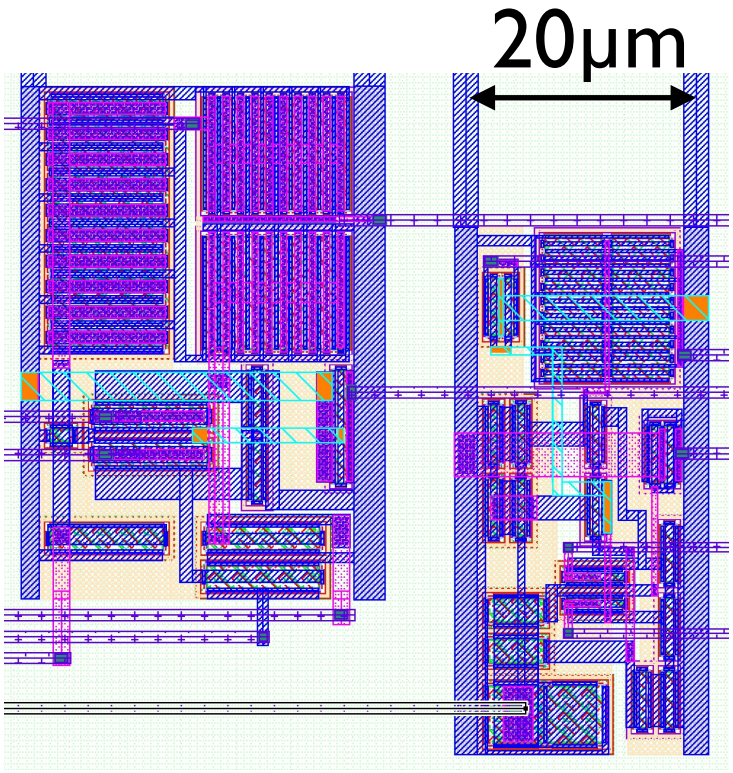



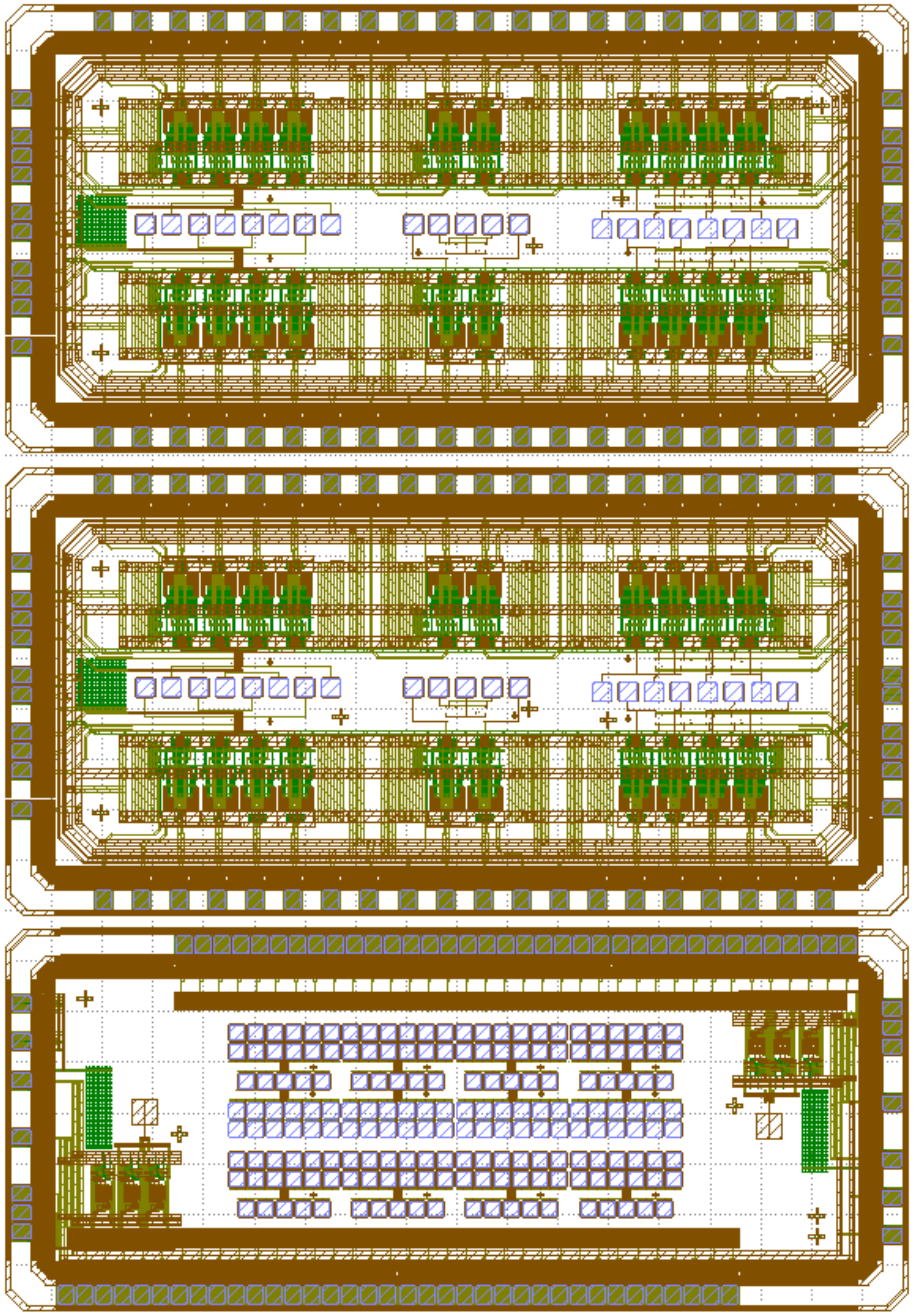



- Microcontroller (MCU) based control system
- Web browser interface (can work wirelessly if desired)
- All biases fully programmable
- Accommodate several chips by wire bonding differently

# Chip by Sky130/NIST program

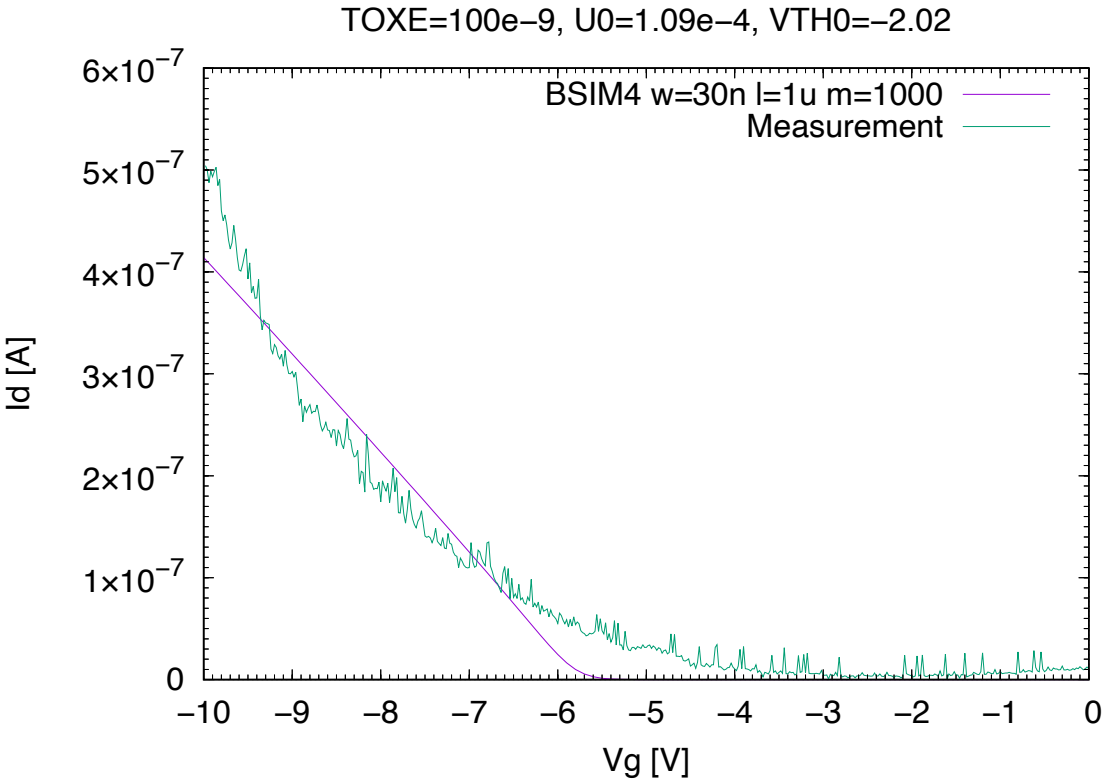


# CNT FET model

## $I_{ds}$ of a single CNT FET is in the range of ~nA




BSIM4 model fit, 1000 devices in parallel

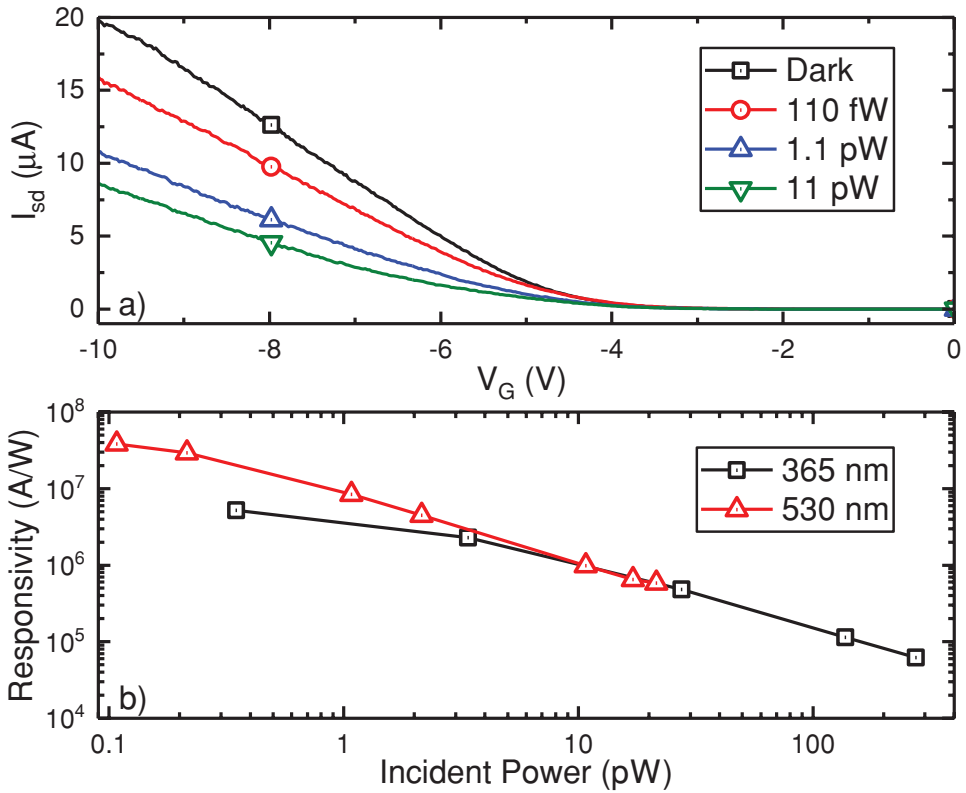


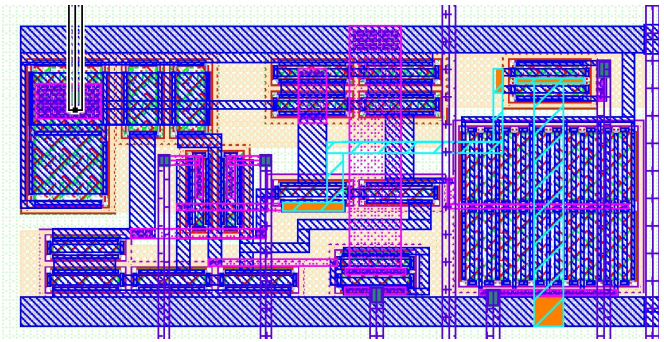

**Figure 2.** a) Transistor transfer characteristics in the dark and under varying intensities of 530 nm light. Measurements were done in vacuum at $V_{SD}$ = 100 mV. Channel length is 300 nm and channel width is 5 µm. b) Responsivity as a function of light intensity for UV illumination (20 µm wide by 200 nm long device channel) and green illumination (5 µm wide by 300 nm long channel).

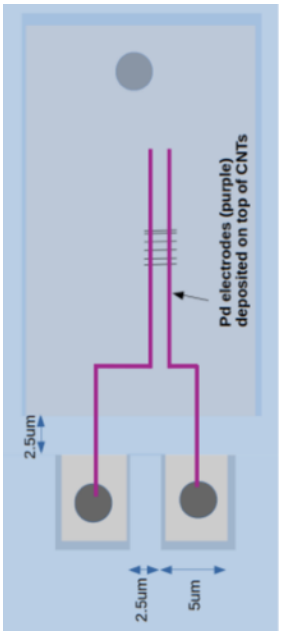


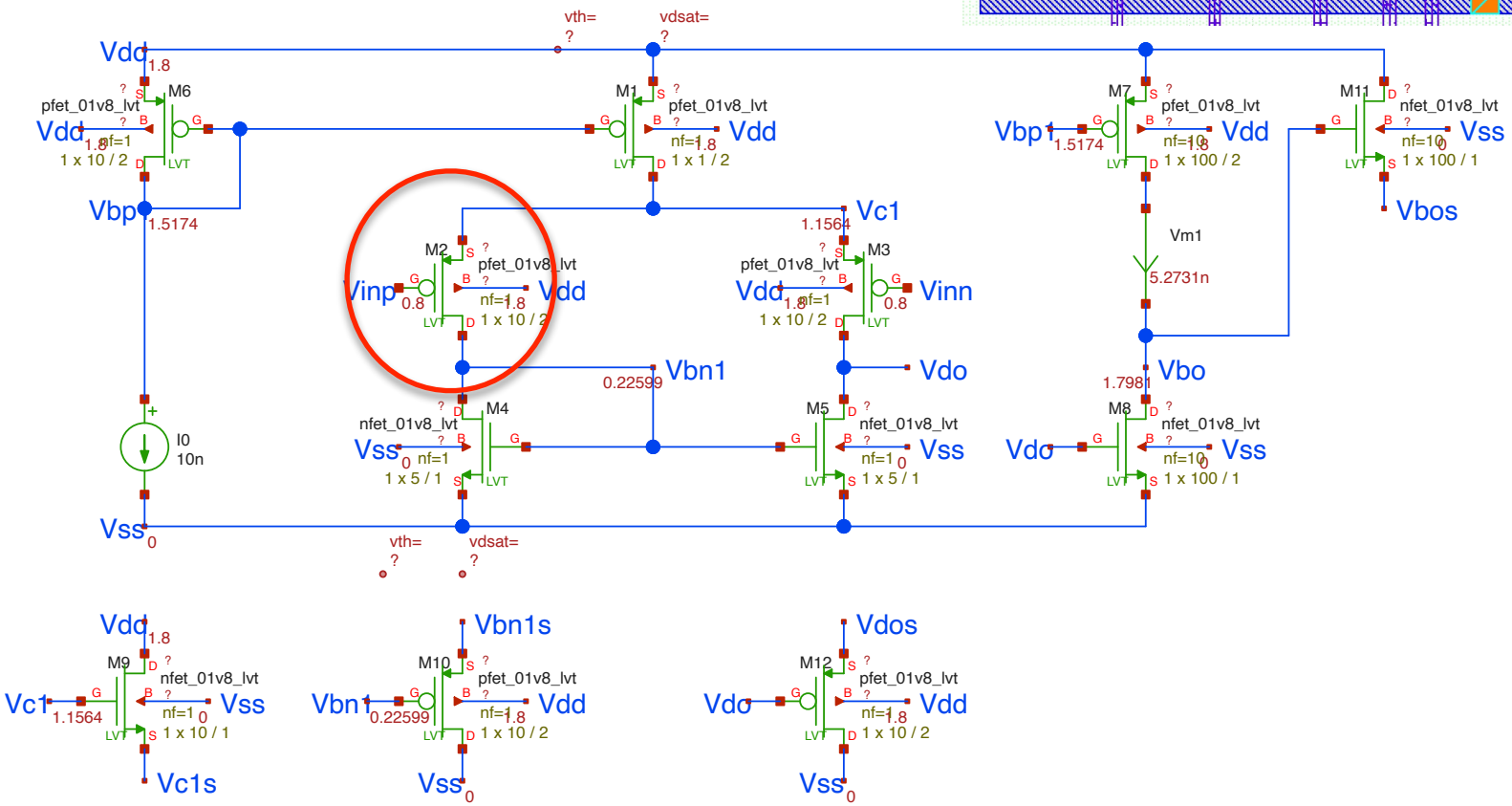
Small 2018, 14, 1802806

# Differential amplifier with CNT input

- Bias at 1.5nA (nominal, for single CntFET) through CntFET
  - Vdd=1.8V, single out-of-chip current bias
- DC gain 31dB (1st stage), 66dB (2 stages). f_0dB = 140kHz
- SF taps around CntFET for Vds measurement.
  - Require external current source and V measurement
- More versions for CntFET bias at 10nA, 100nA, 1uA

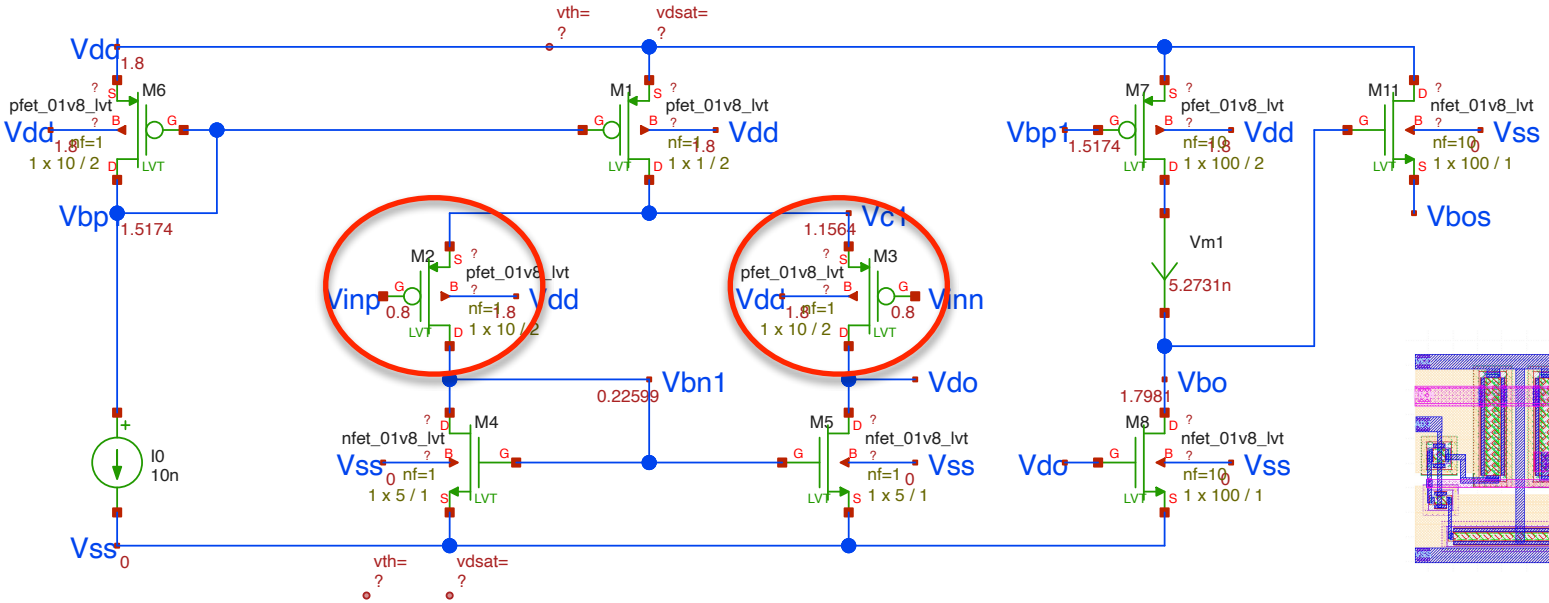


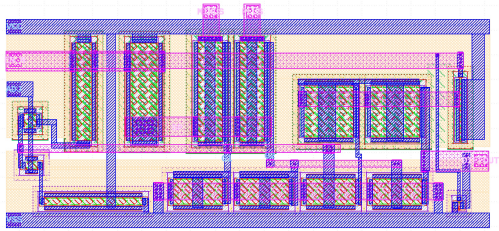


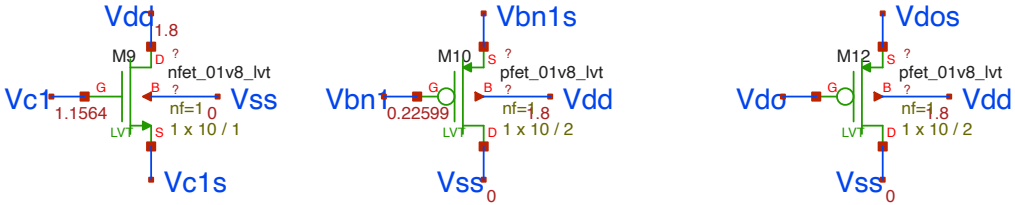



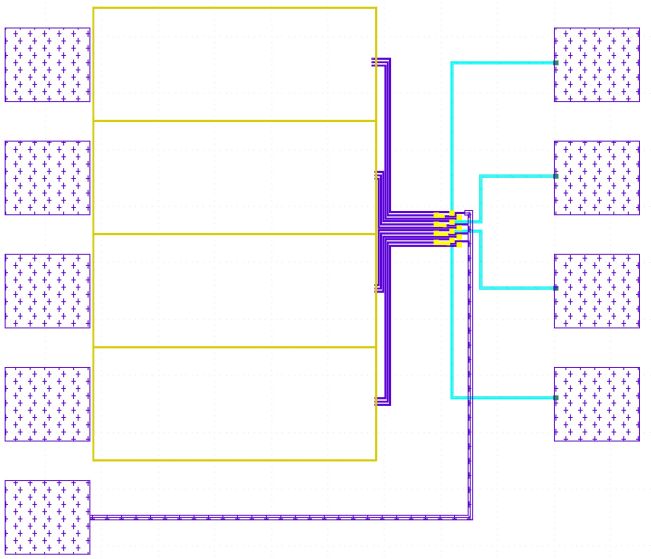
# CntBridgeAmp0

- Replace both input transistors with PADs for connecting to CntFET
- "Center tap" of two CntFETs at node Vc1
- Vc1 and Vbn1 are measured externally via SF



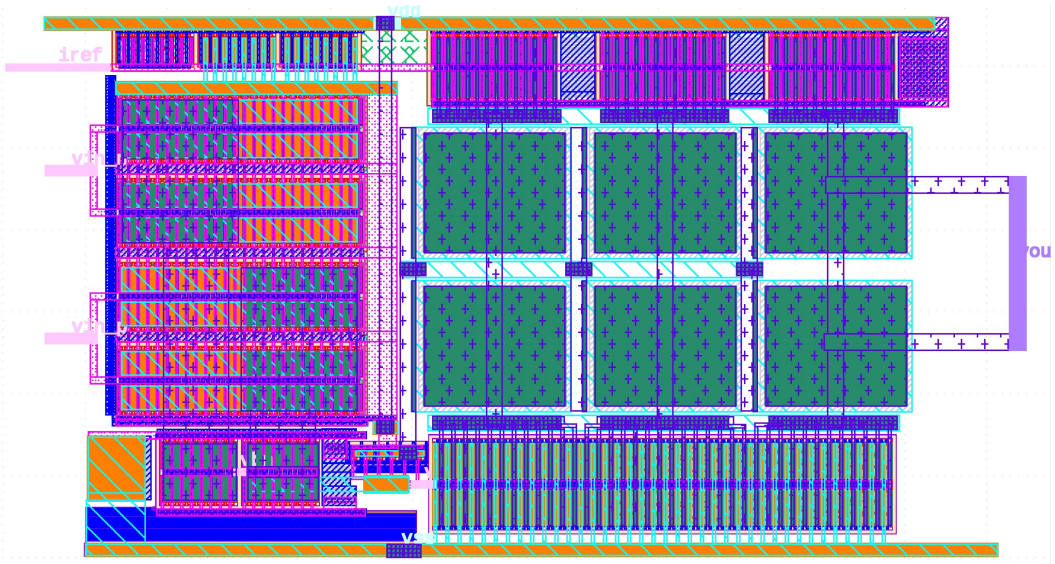



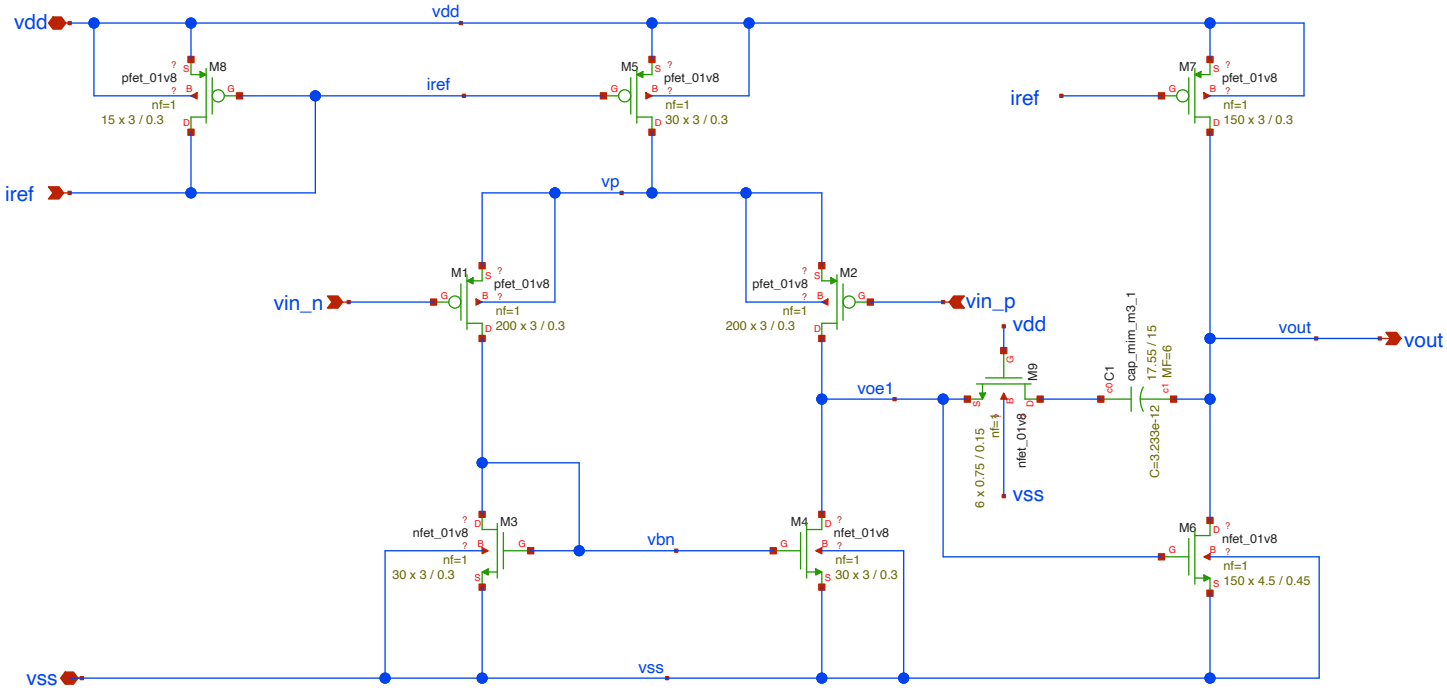


# Voltage buffer/probe driver

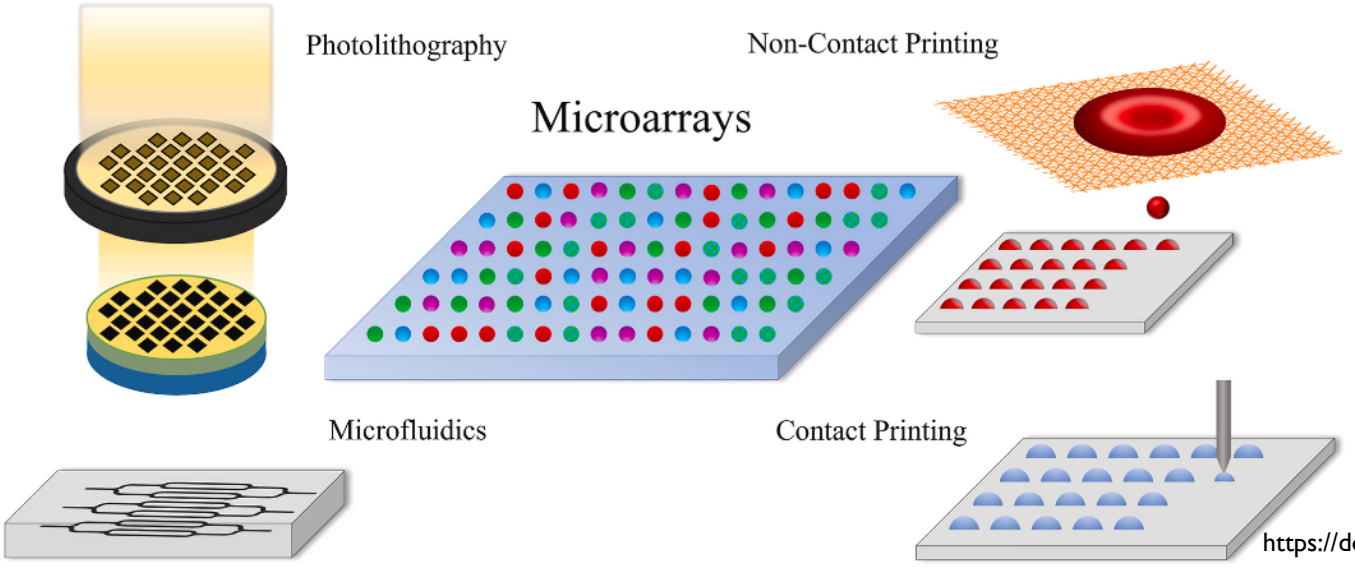
- Open source “Diego” version.
- Vdd=1.8V
- Single external current bias.
- GBW 54.3 MHz, DC gain 60dB
- PM=68deg @ CL=20pF



# An ideal test system (demonstrator)?

- Nano device characteristics vary wildly
  - Design many individual CMOS circuits to cover the parameter space
  - Put these circuits in a array, on easy-to-use readout/control system.
  - Enable high-throughput screening, like chemical assay
  - Getting 1 out of many (N) to work is a success, worry about yield later
    - Increase N by CMOS circuit array (cheap)
- CMOS circuits array must be able to perform
  - Characterization
  - Readout
  - Multiplexing




https://doi.org/10.1016/j.ab.2023.115369

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