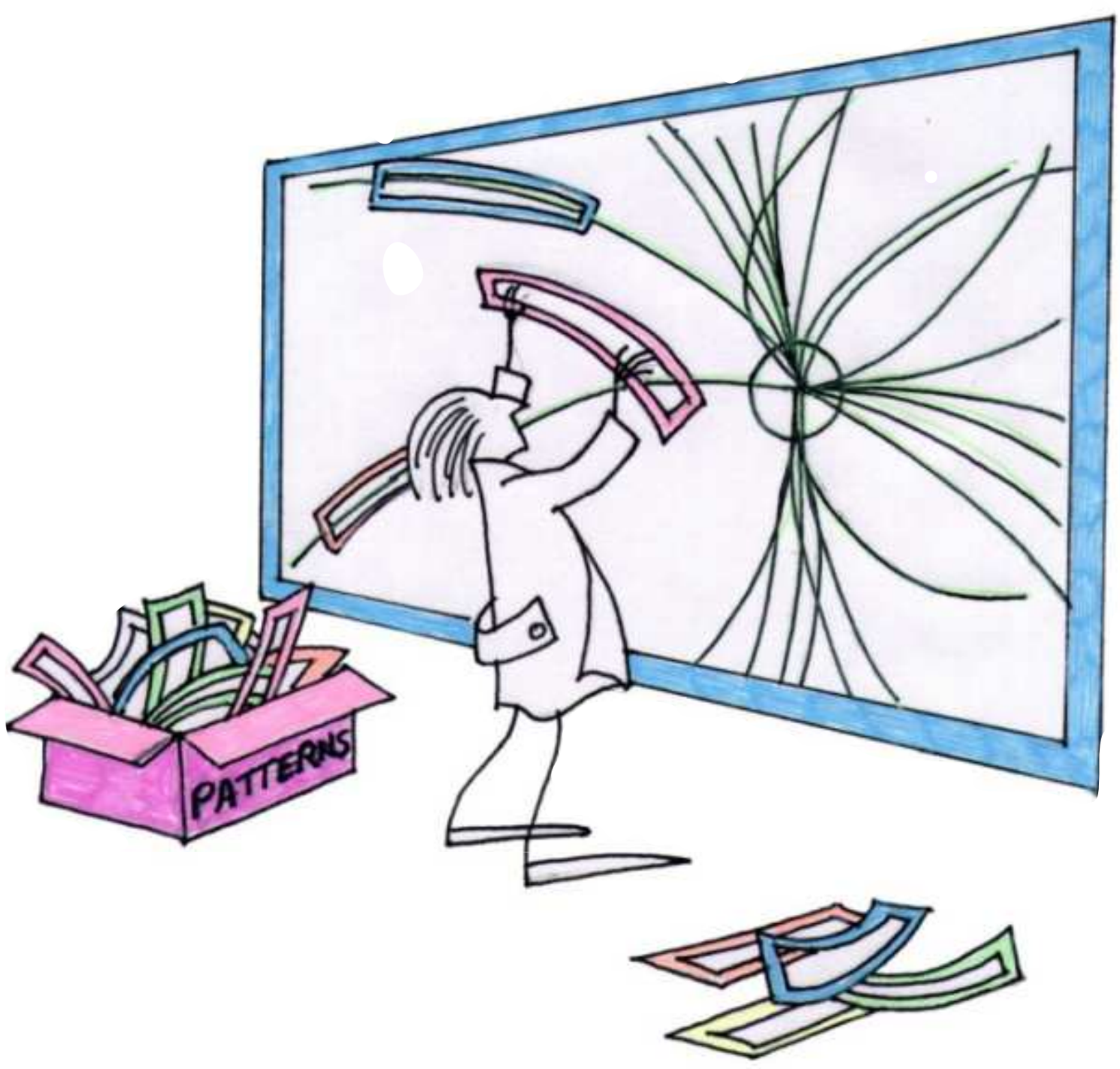
FTK: A HARDWARE BASED TRACK FINDER FOR THE ATLAS TRIGGER



LAUREN TOMPKINS

INSTRUMENTATION BROWN BAG
JUNE 1ST, 2016

Stanford University

OUTLINE

- Why hardware based track finding? Why now?
- How we do it
- Current status and commissioning plan
- Looking to the future

WHY USE TRACKS IN THE TRIGGER?

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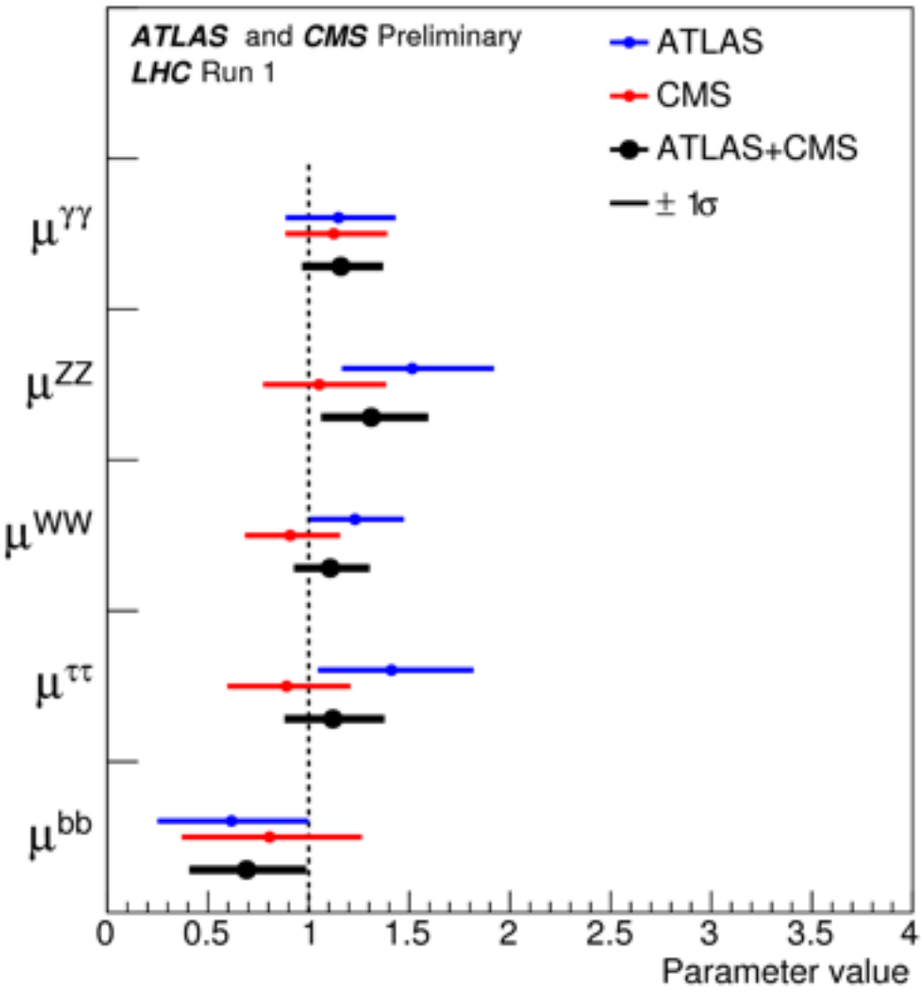
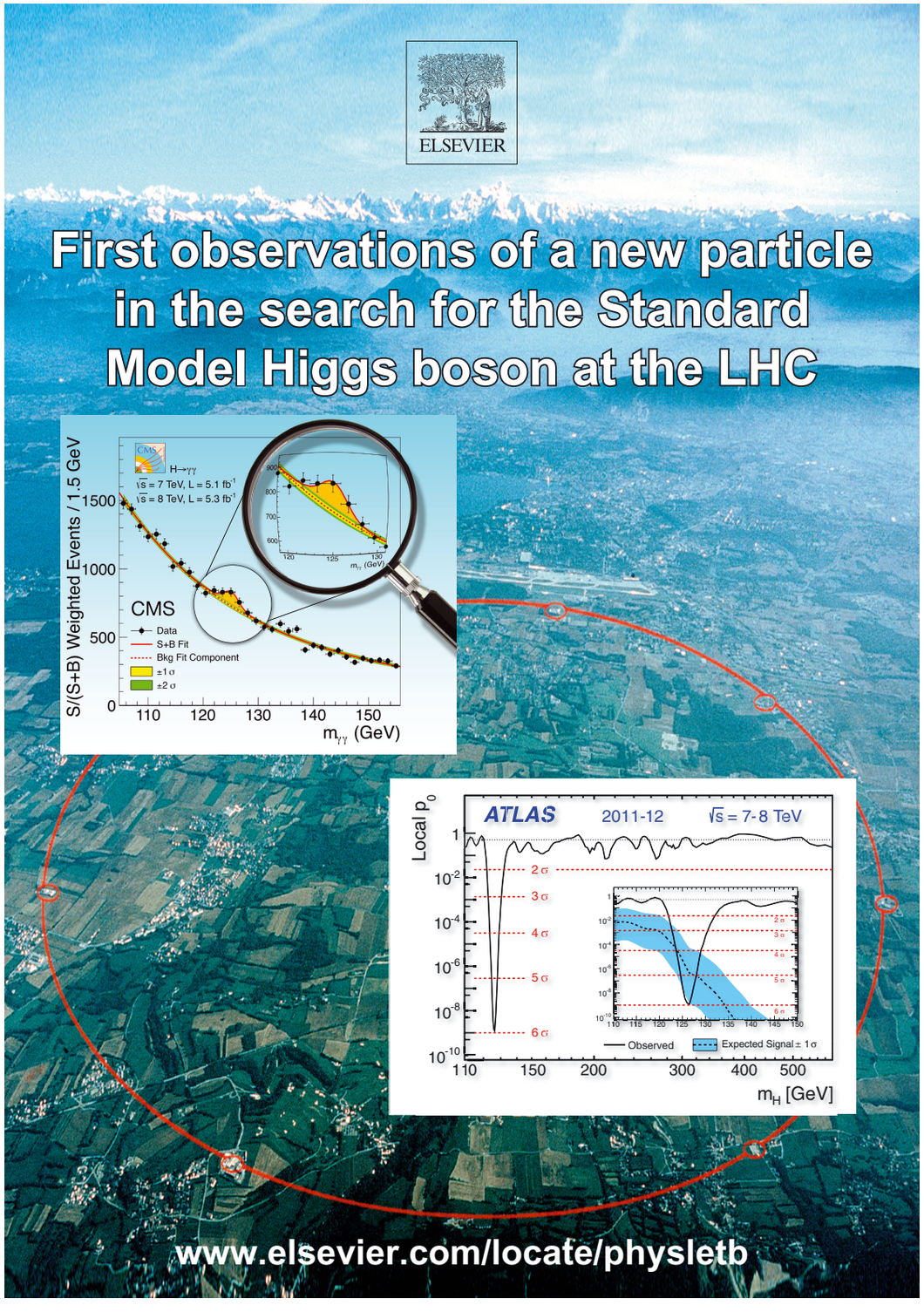
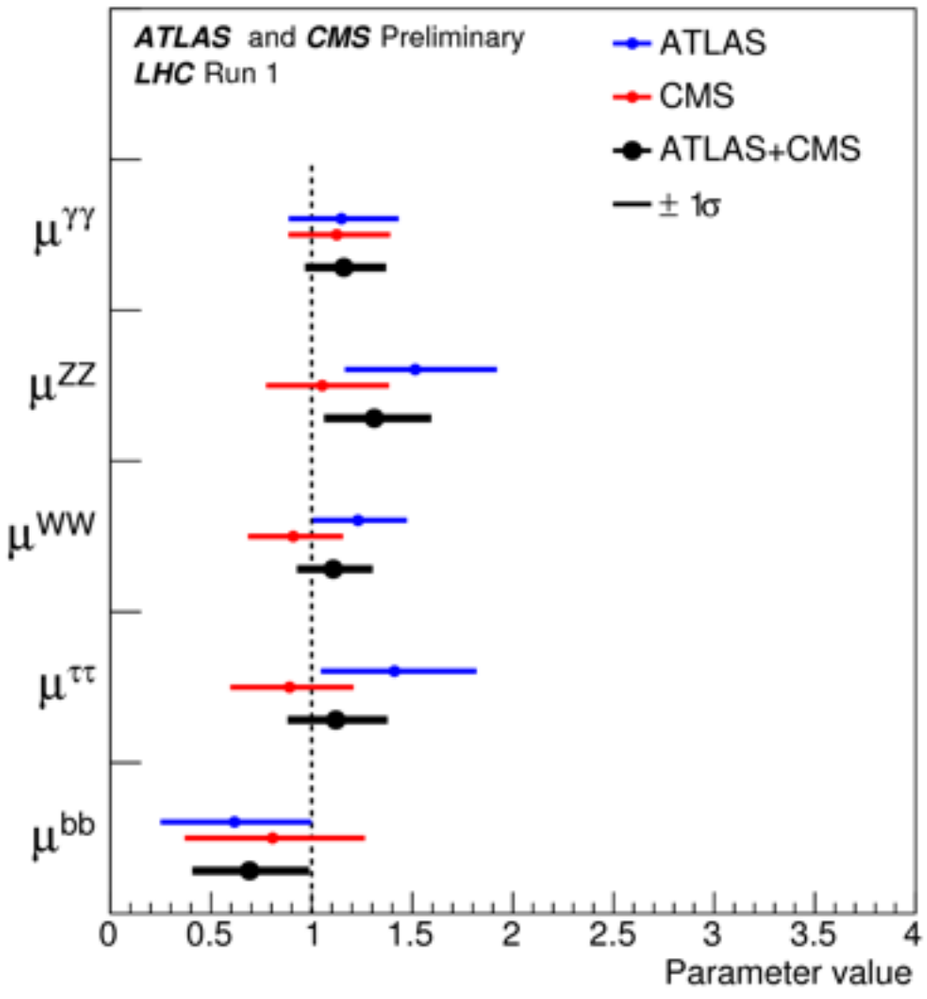
TO DO THE PHYSICS, OF COURSE!



Observed Signal / Expected Signal





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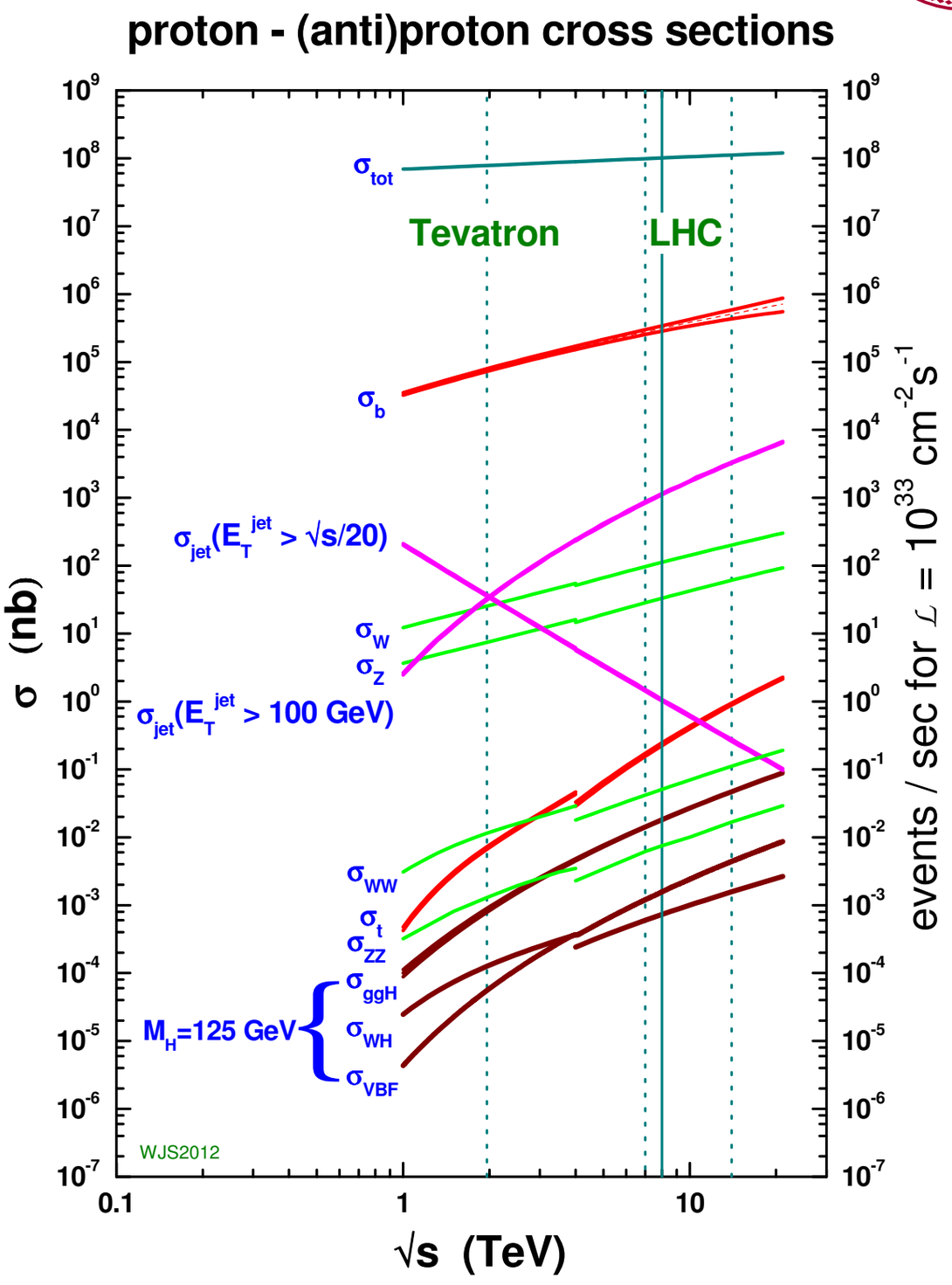

WHAT QUESTIONS ARE WE TRYING TO ANSWER?

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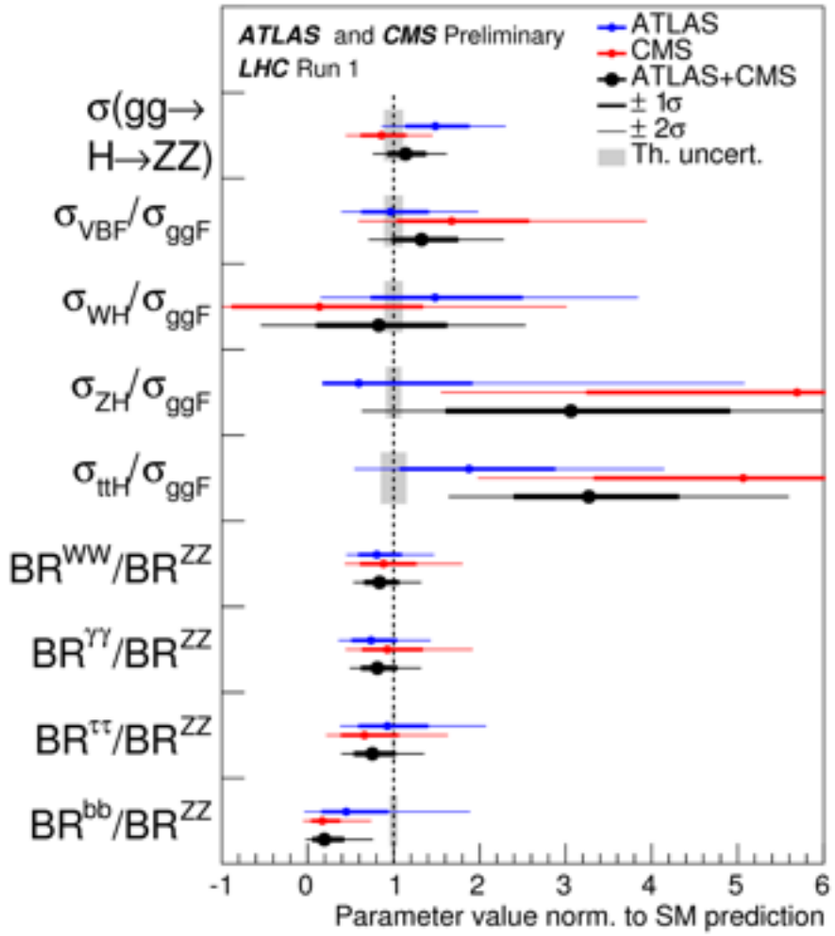
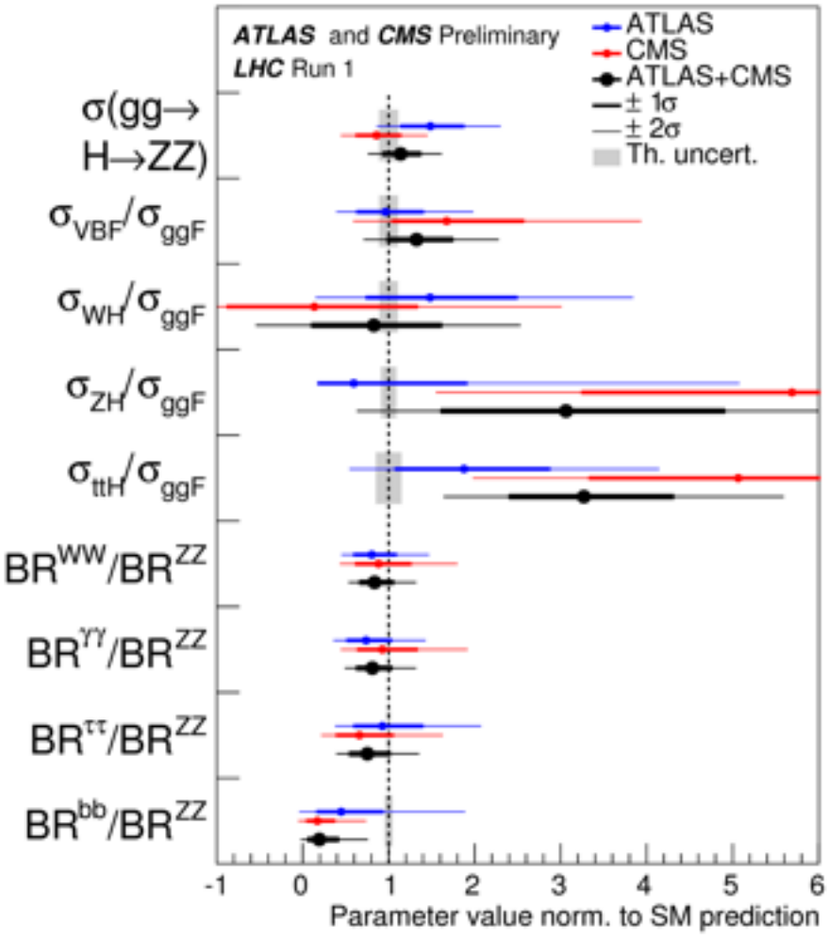
- Is this **really** the Standard Model Higgs Boson?



WHAT QUESTIONS ARE WE TRYING TO ANSWER?

- Is this **really** the Standard Model Higgs Boson?



- Is this the **only** Higgs Boson?

$$V = m_{11}^2 \Phi_1^\dagger \Phi_1 + m_{22}^2 \Phi_2^\dagger \Phi_2 - m_{12}^2 \left(\Phi_1^\dagger \Phi_2 + \Phi_2^\dagger \Phi_1 \right) + \frac{\lambda_1}{2} \left(\Phi_1^\dagger \Phi_1 \right)^2 + \frac{\lambda_2}{2} \left(\Phi_2^\dagger \Phi_2 \right)^2$$
$$+ \lambda_3 \Phi_1^\dagger \Phi_1 \Phi_2^\dagger \Phi_2 + \lambda_4 \Phi_1^\dagger \Phi_2 \Phi_2^\dagger \Phi_1 + \frac{\lambda_5}{2} \left[\left(\Phi_1^\dagger \Phi_2 \right)^2 + \left(\Phi_2^\dagger \Phi_1 \right)^2 \right],$$

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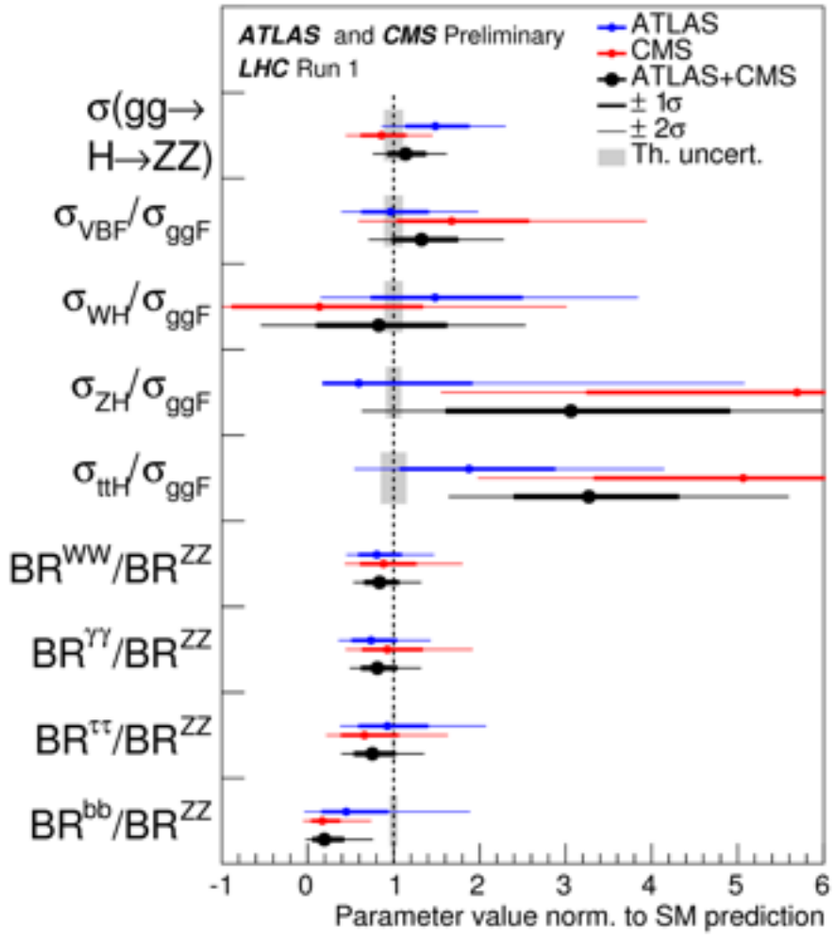

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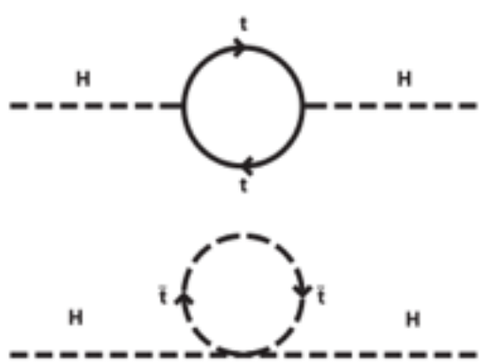
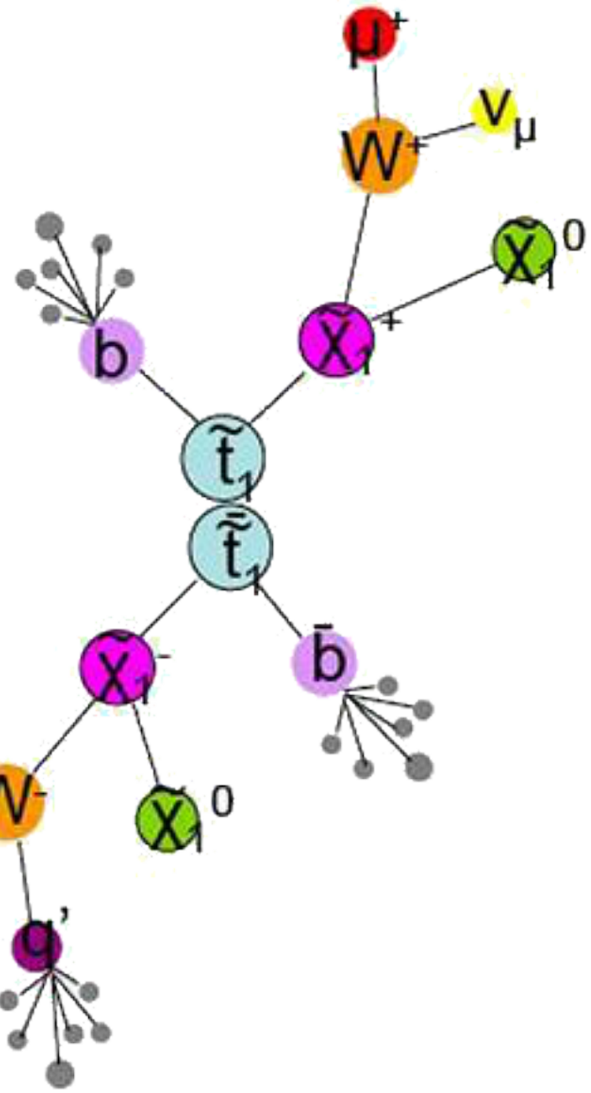
- **Why** is the Higgs mass much lower than the Planck scale?



CARRYING OUT THE PHYSICS PROGRAM

- Need to be able to identify:
  - **3rd generation particles: taus, b-quarks**
    - **Displaced vertices from b-hadron decays**
    - **1- and 3-prong tau decays**
- Leptons from electroweak decays:
  - Isolated electrons and muons
- Jets and Missing Energy
- Tracking is critical!



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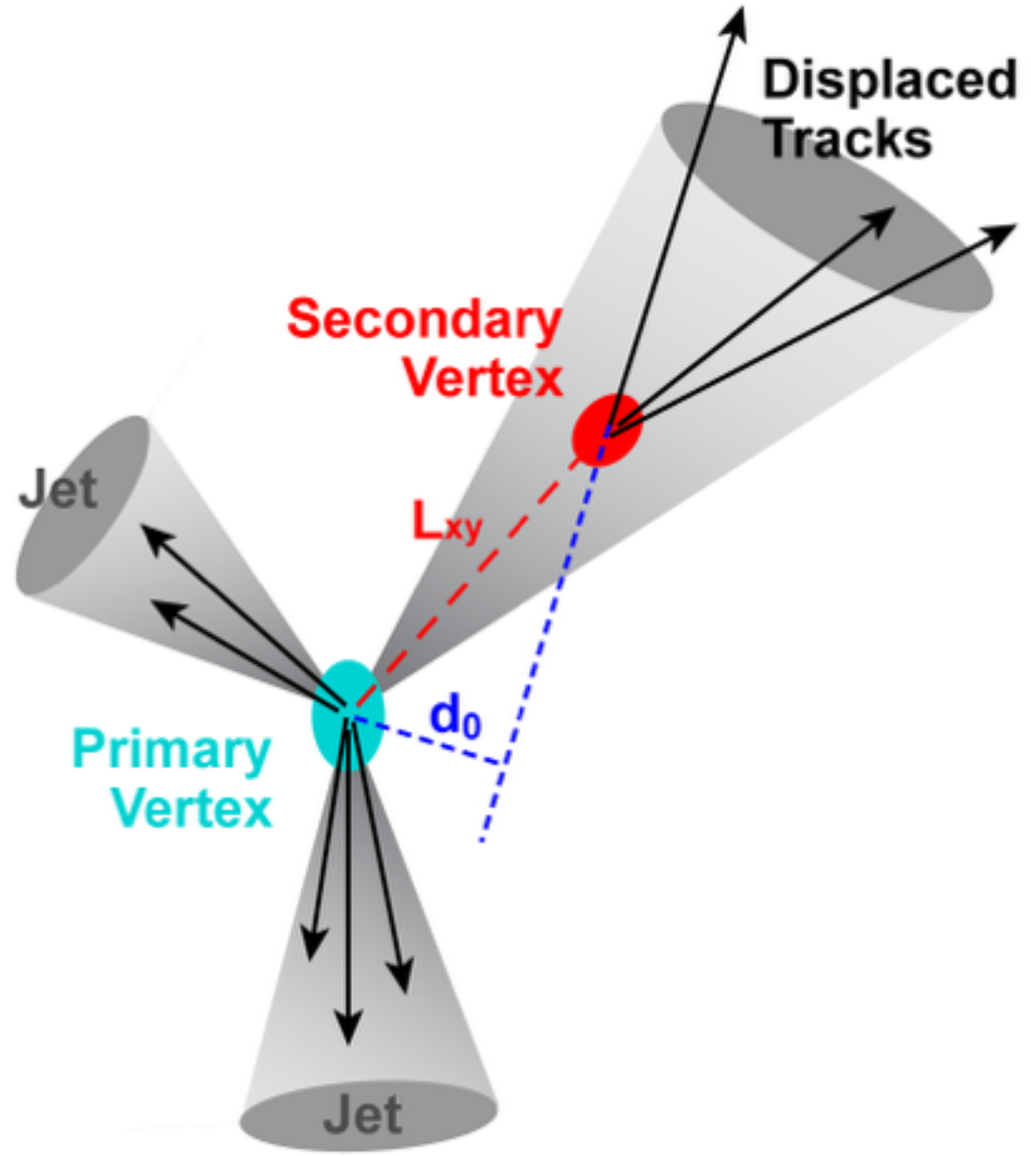

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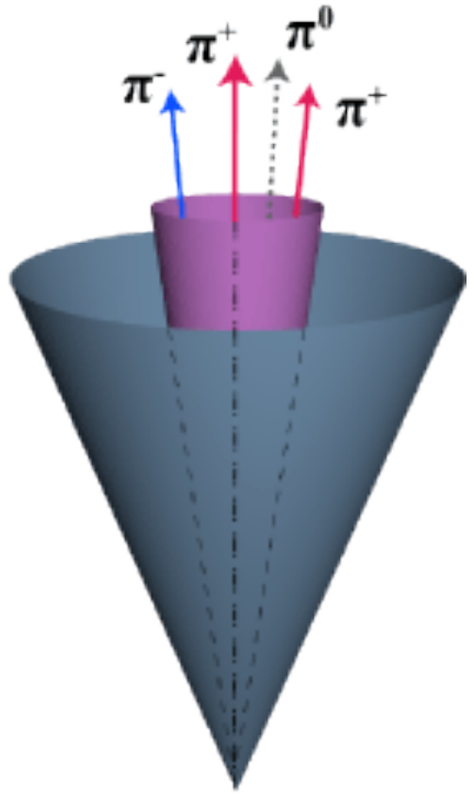

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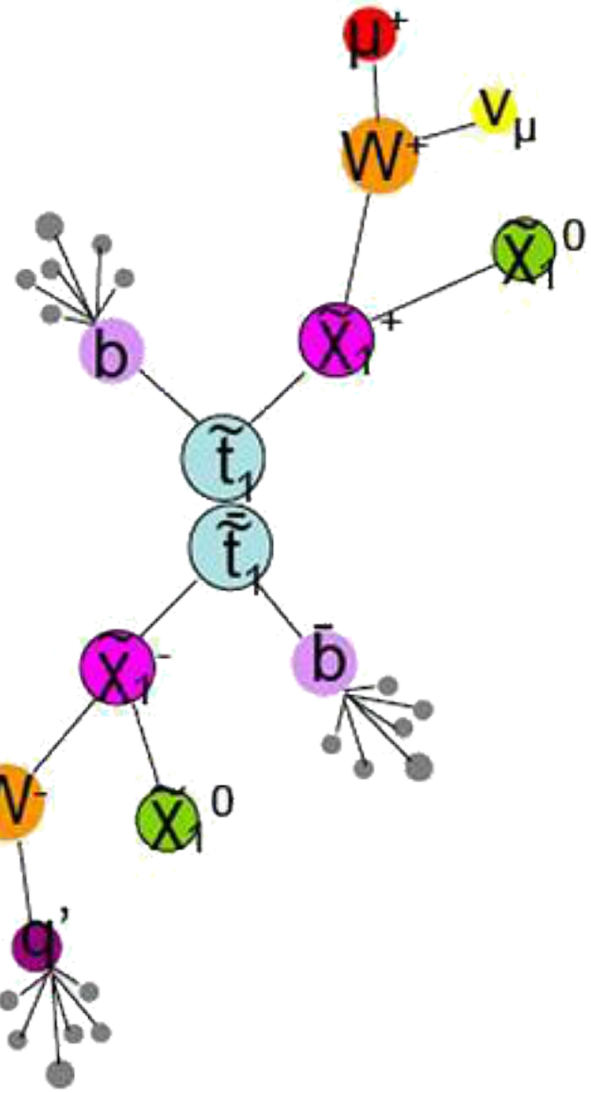
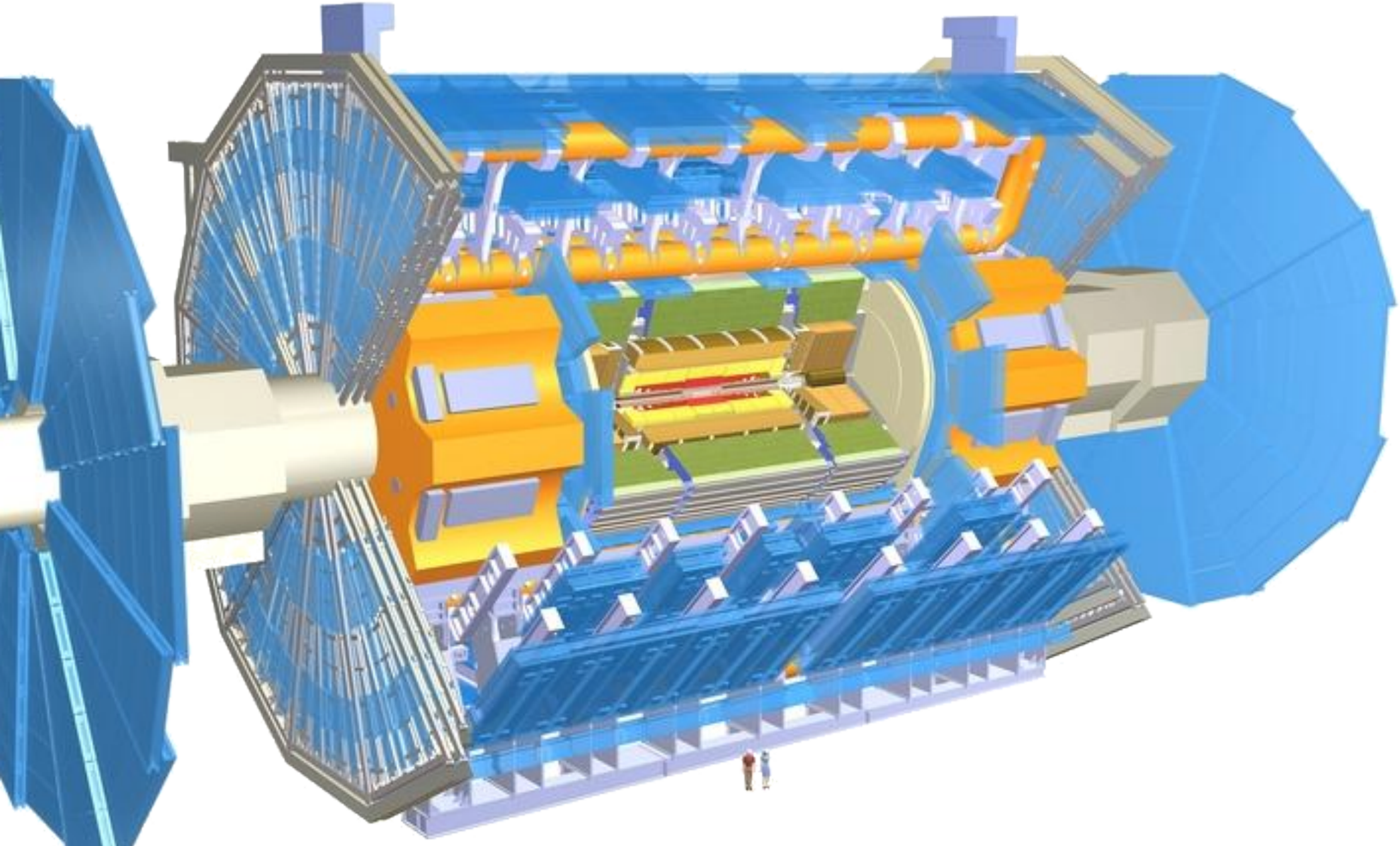
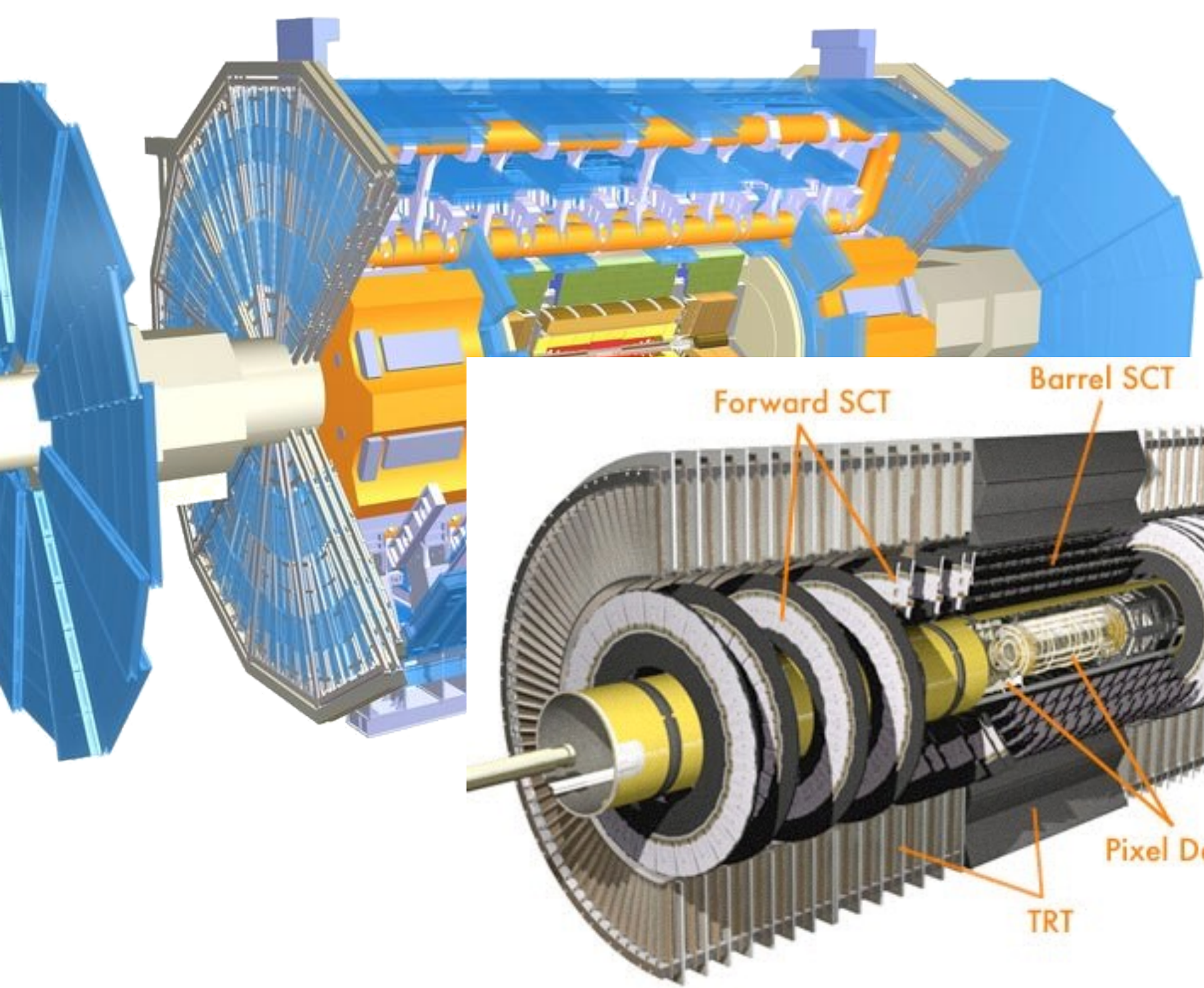
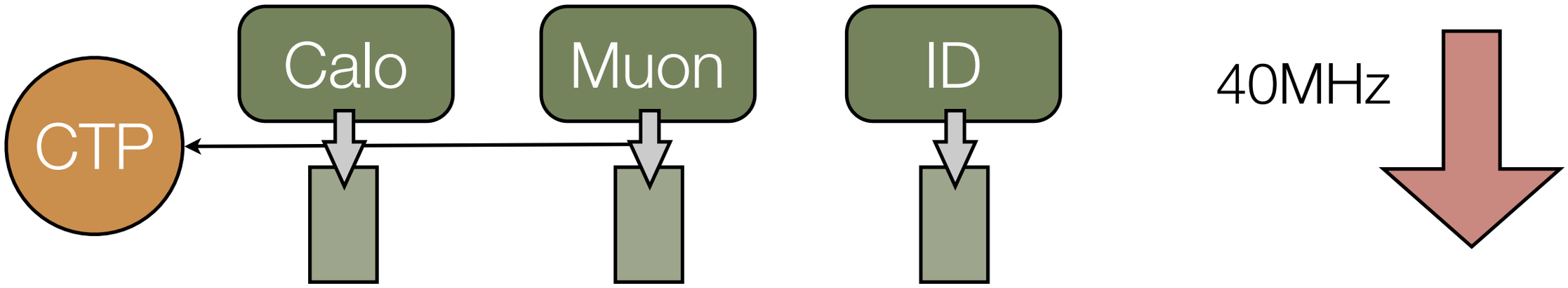





Forward SCT
Barrel SCT
Pixel Detectors
TRT

ATLAS TRIGGER SYSTEM

ATLAS TRIGGER SYSTEM



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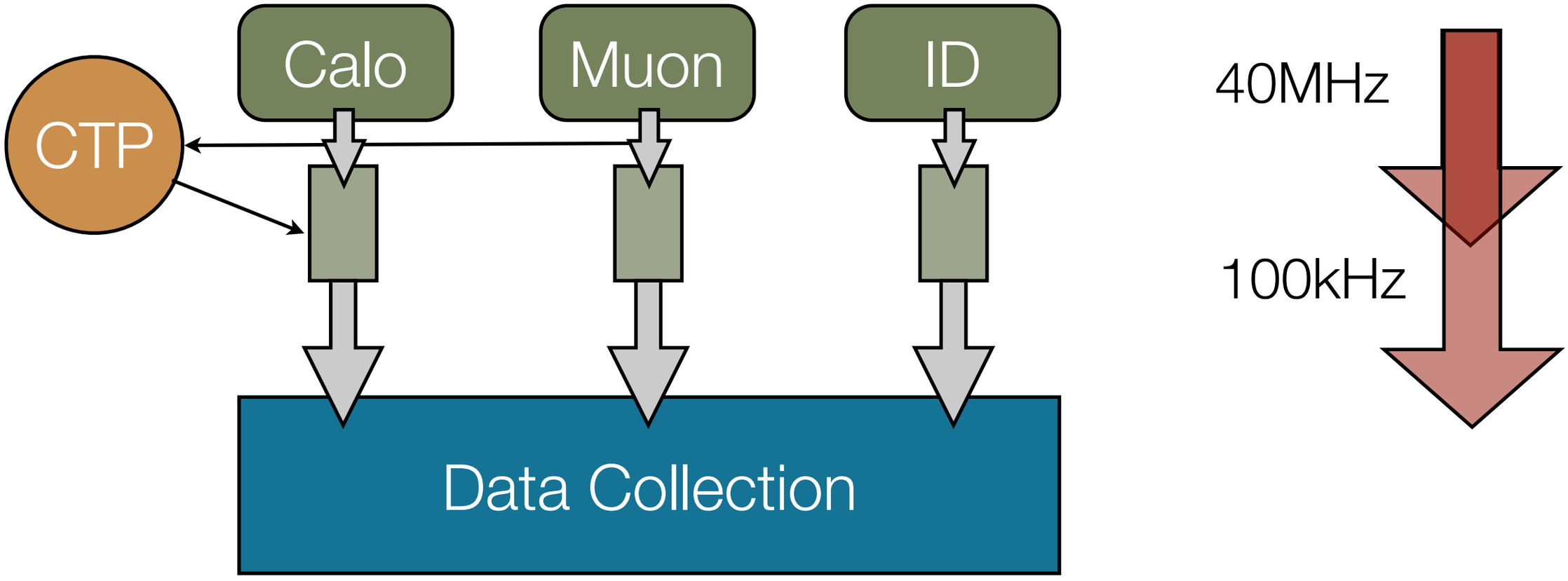

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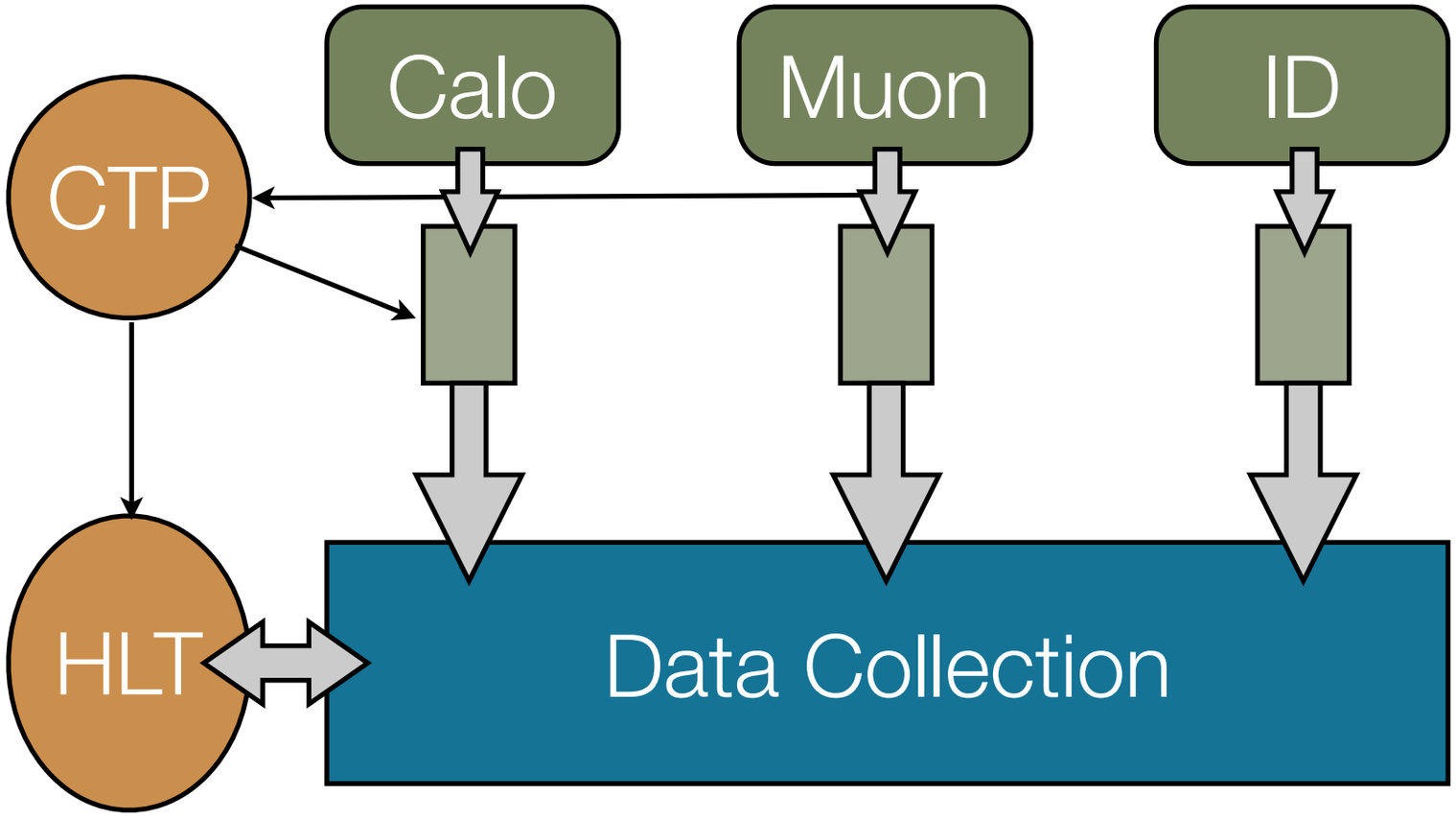

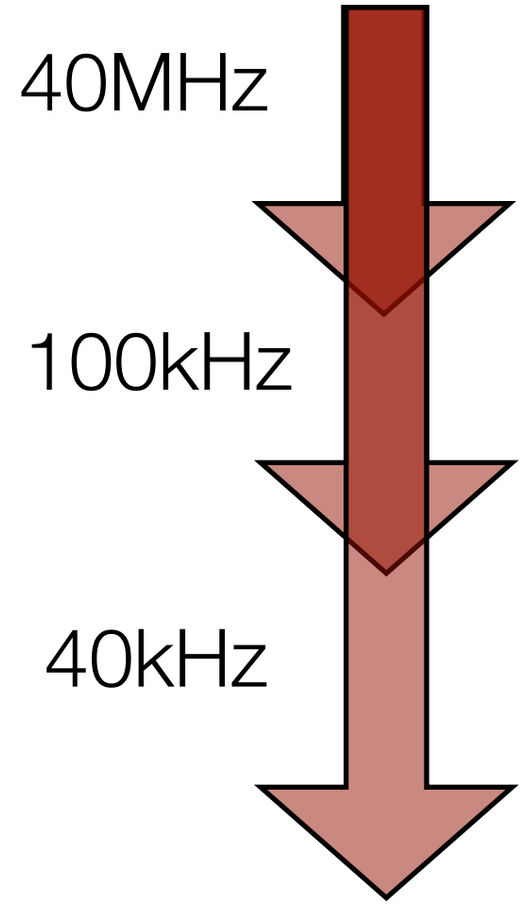

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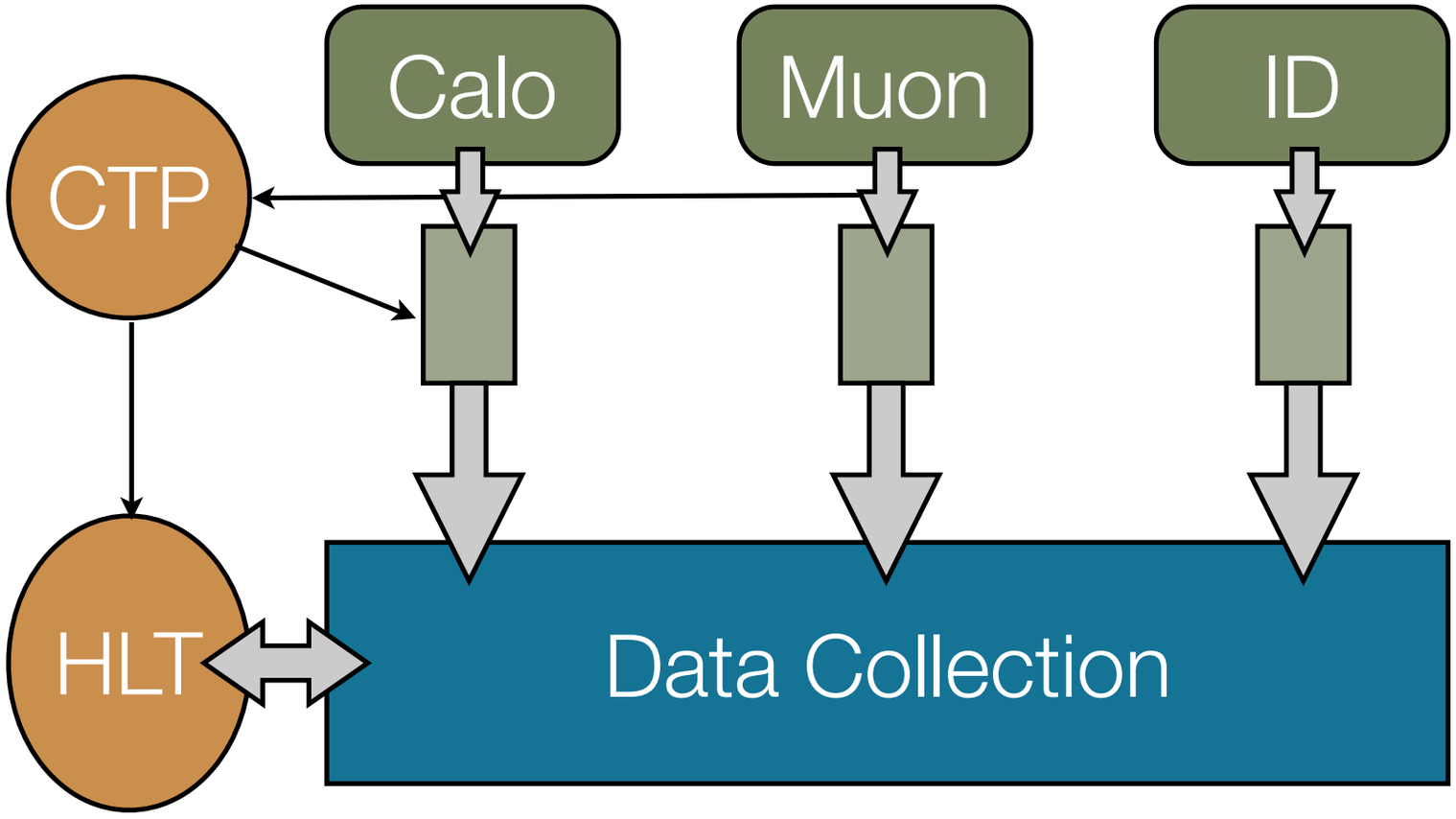

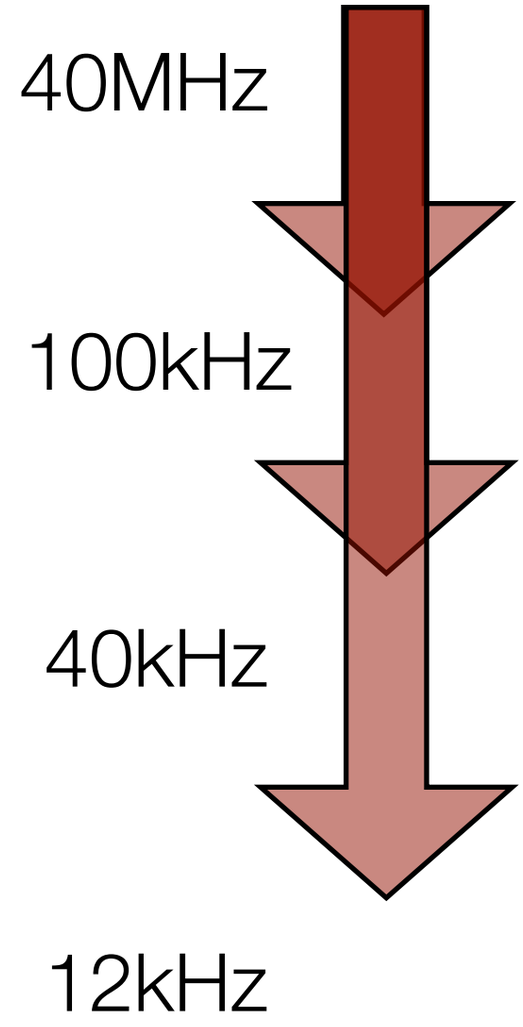

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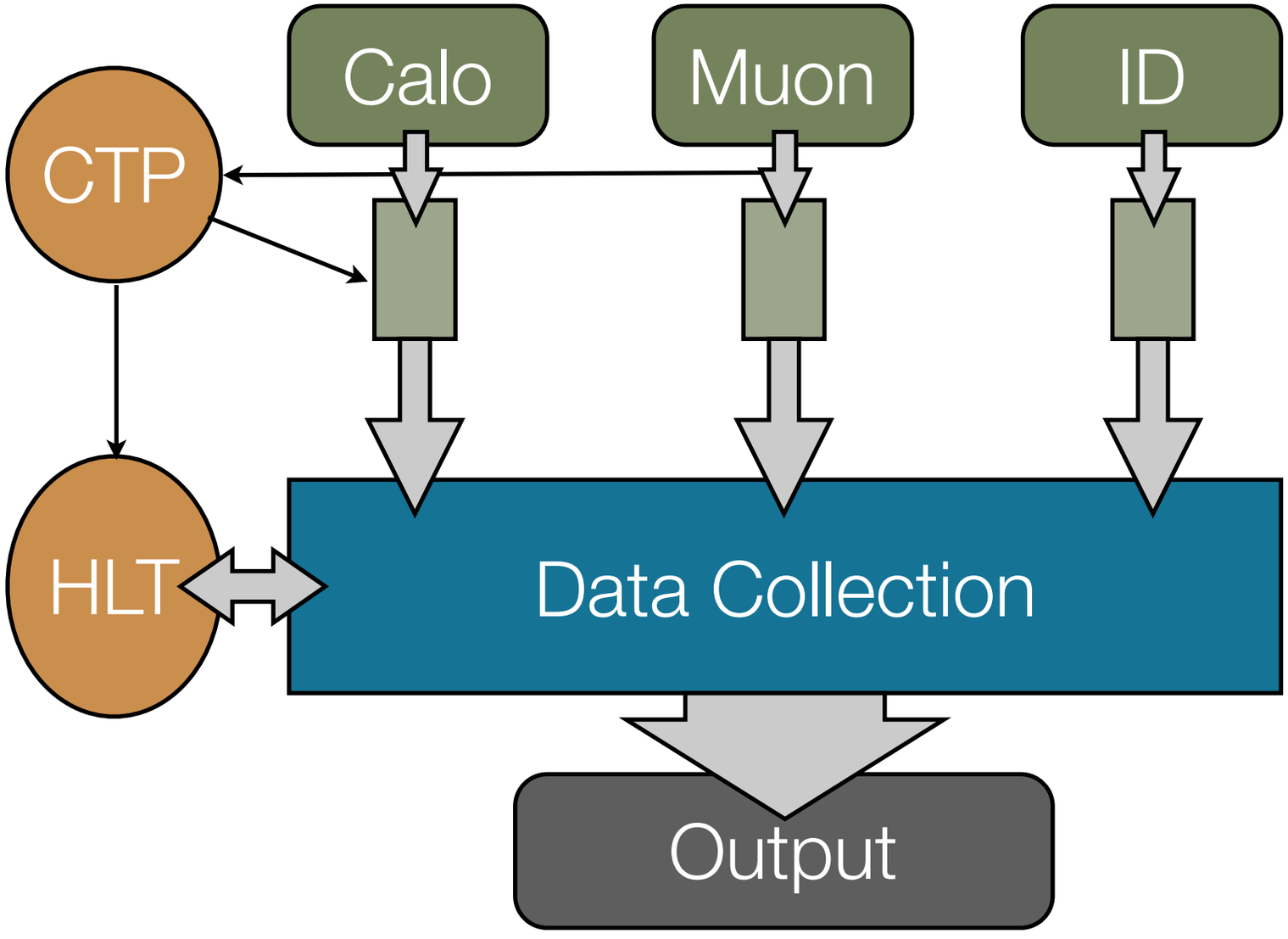

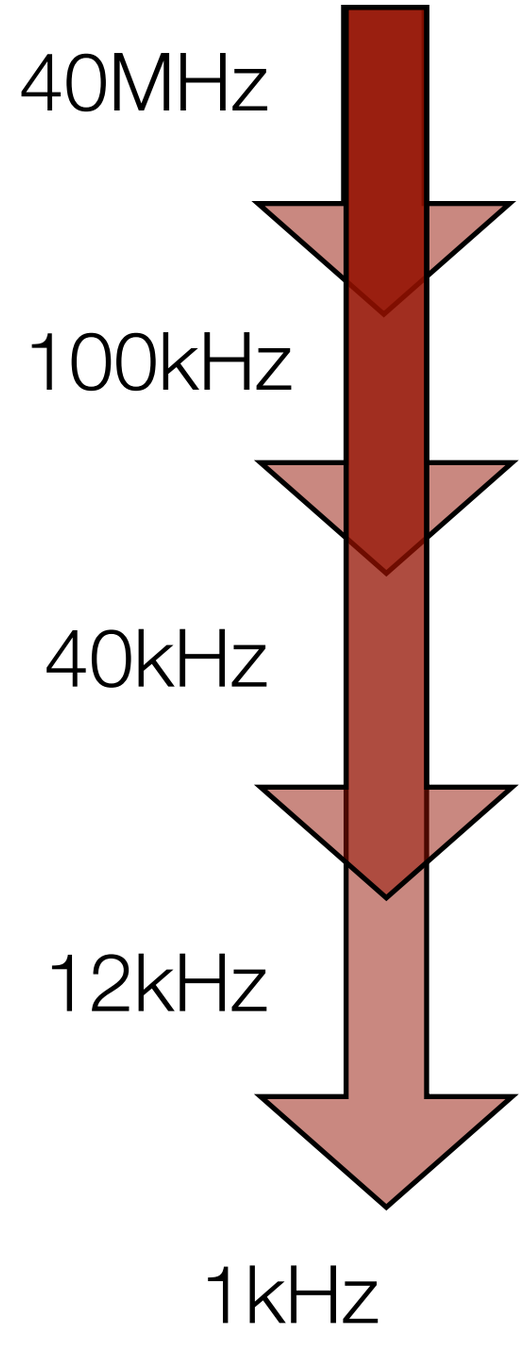

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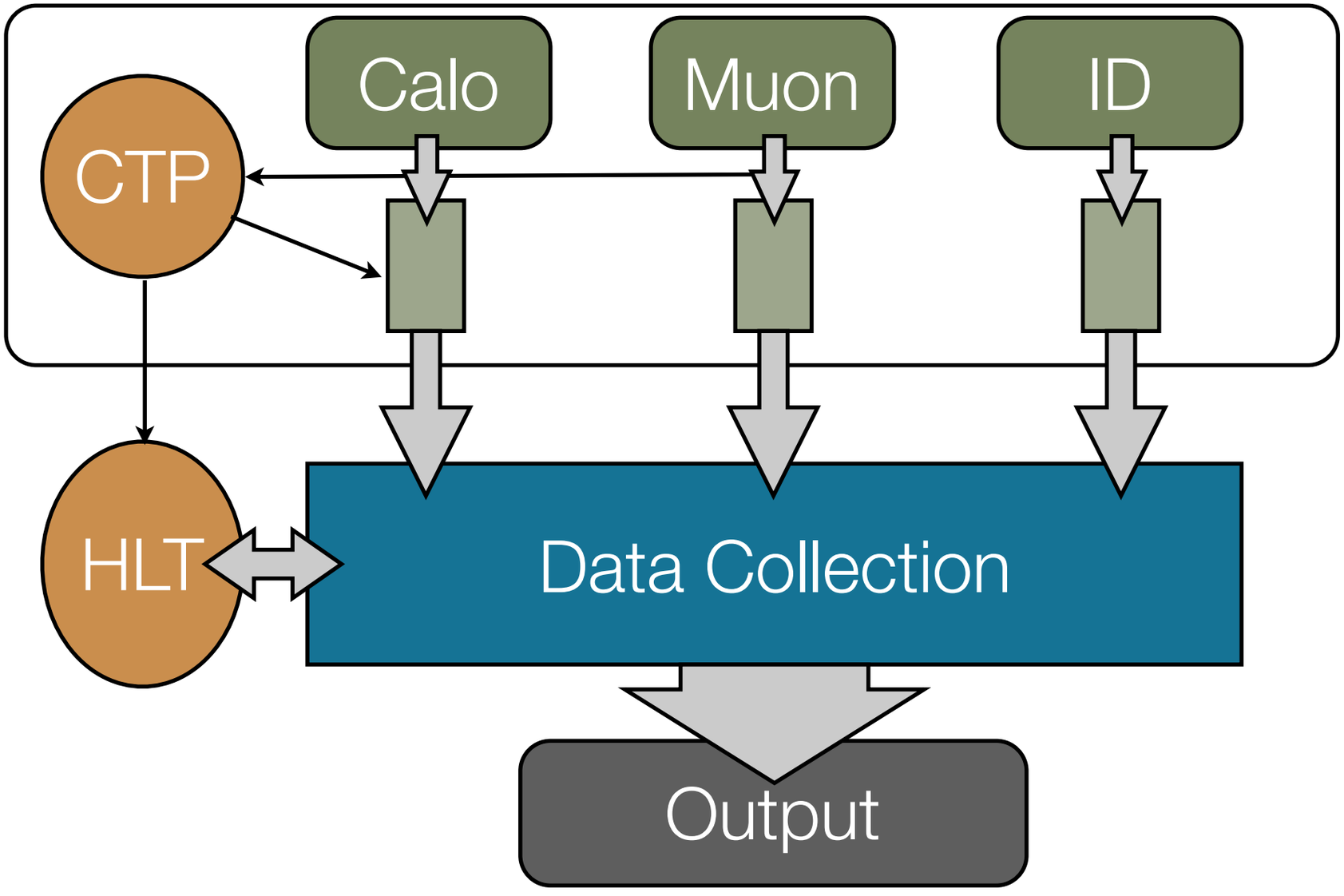

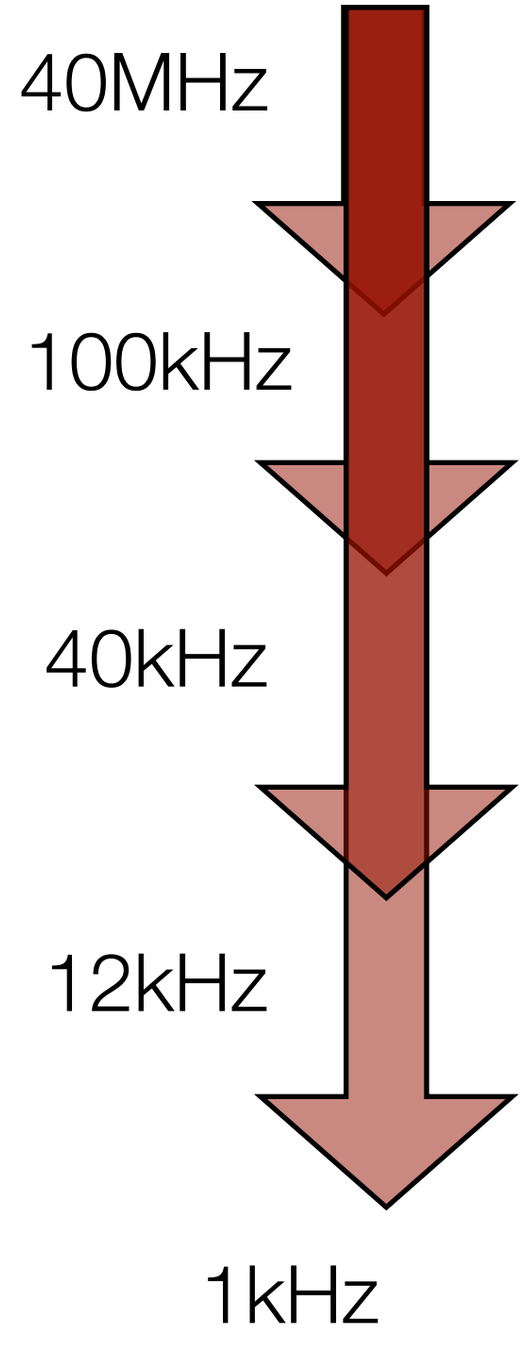

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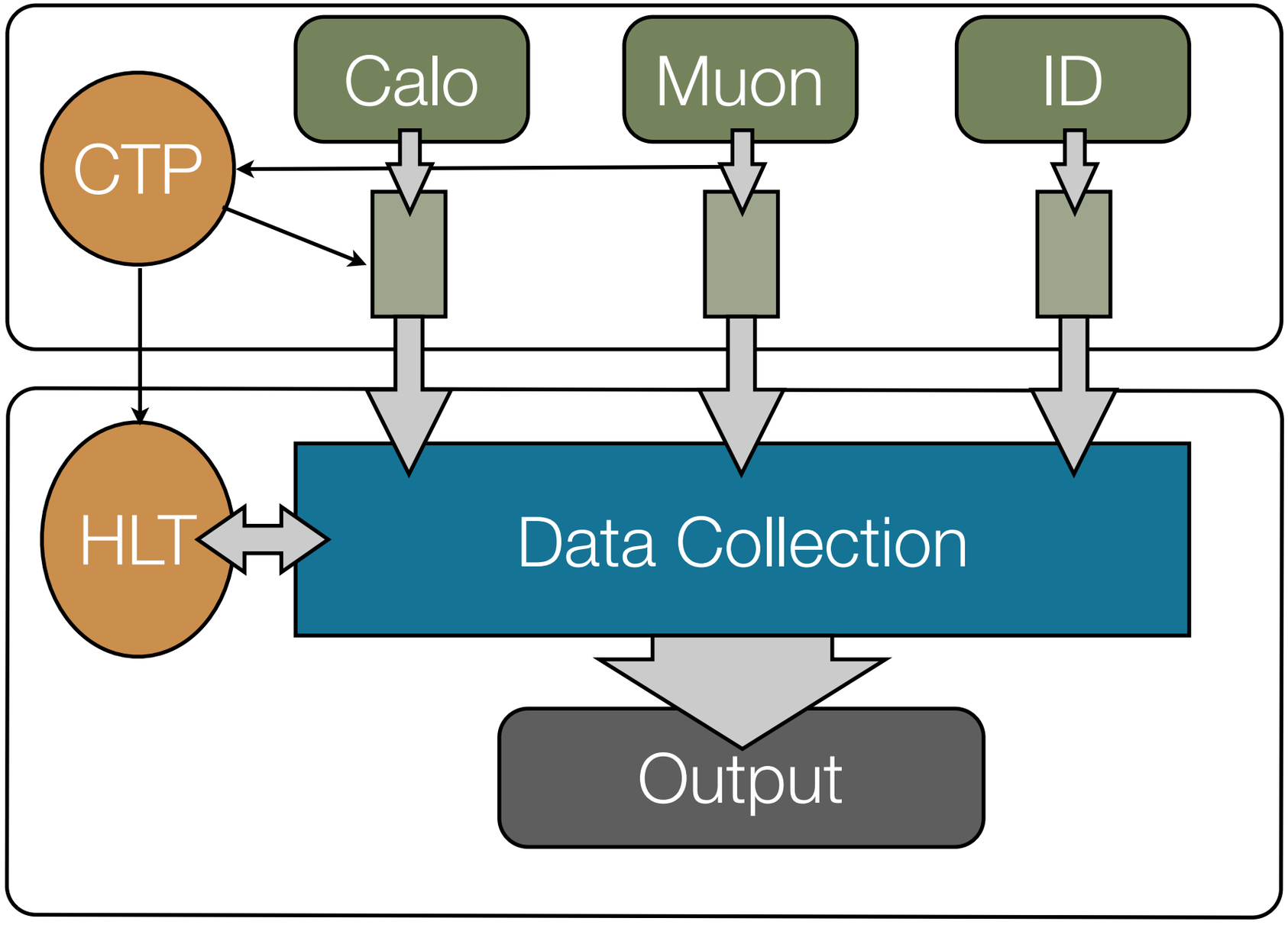
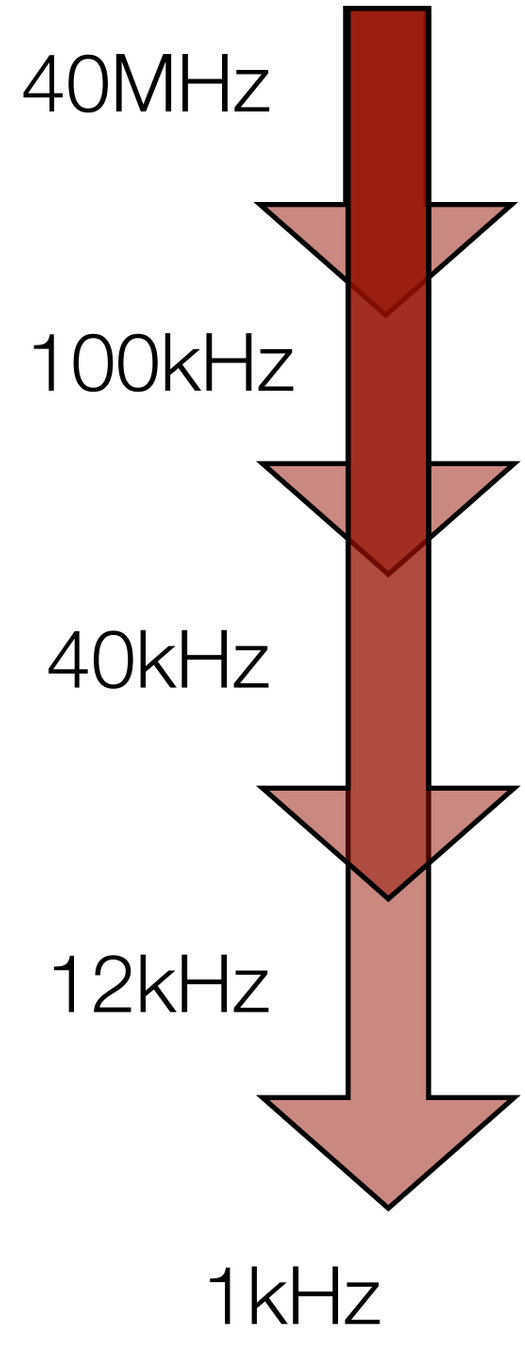
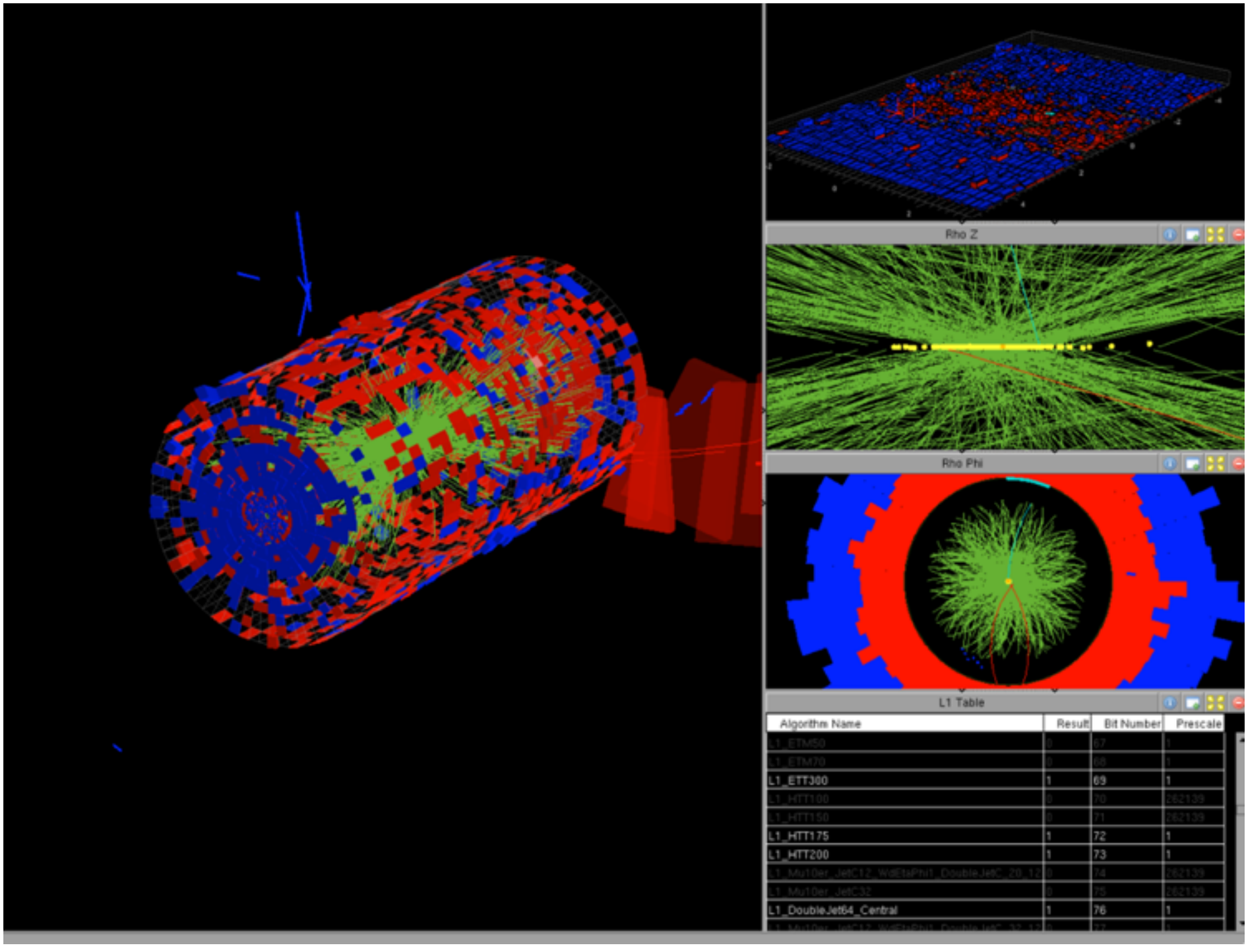




CHALLENGES



CMS, 78 reconstructed vertices

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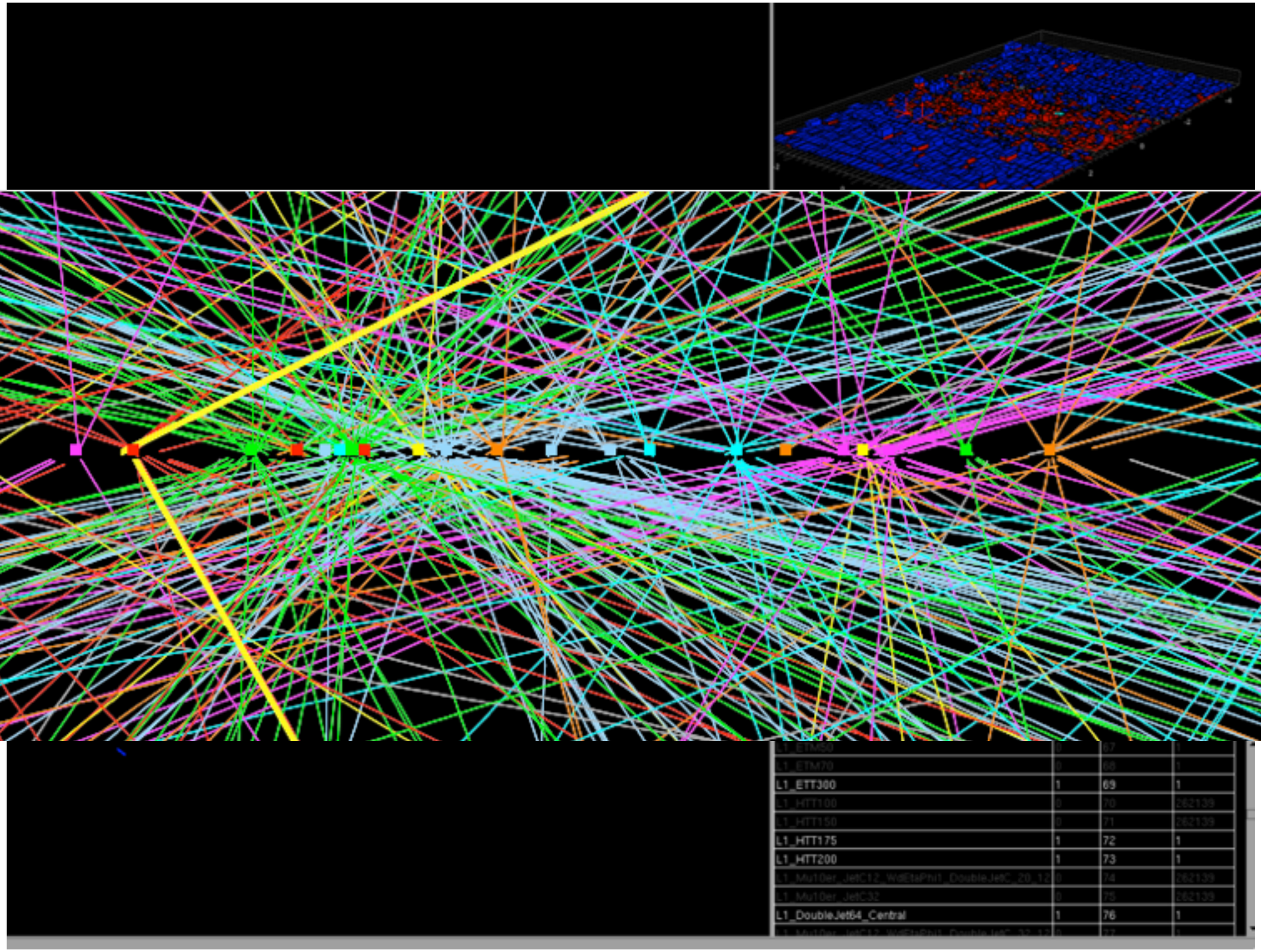

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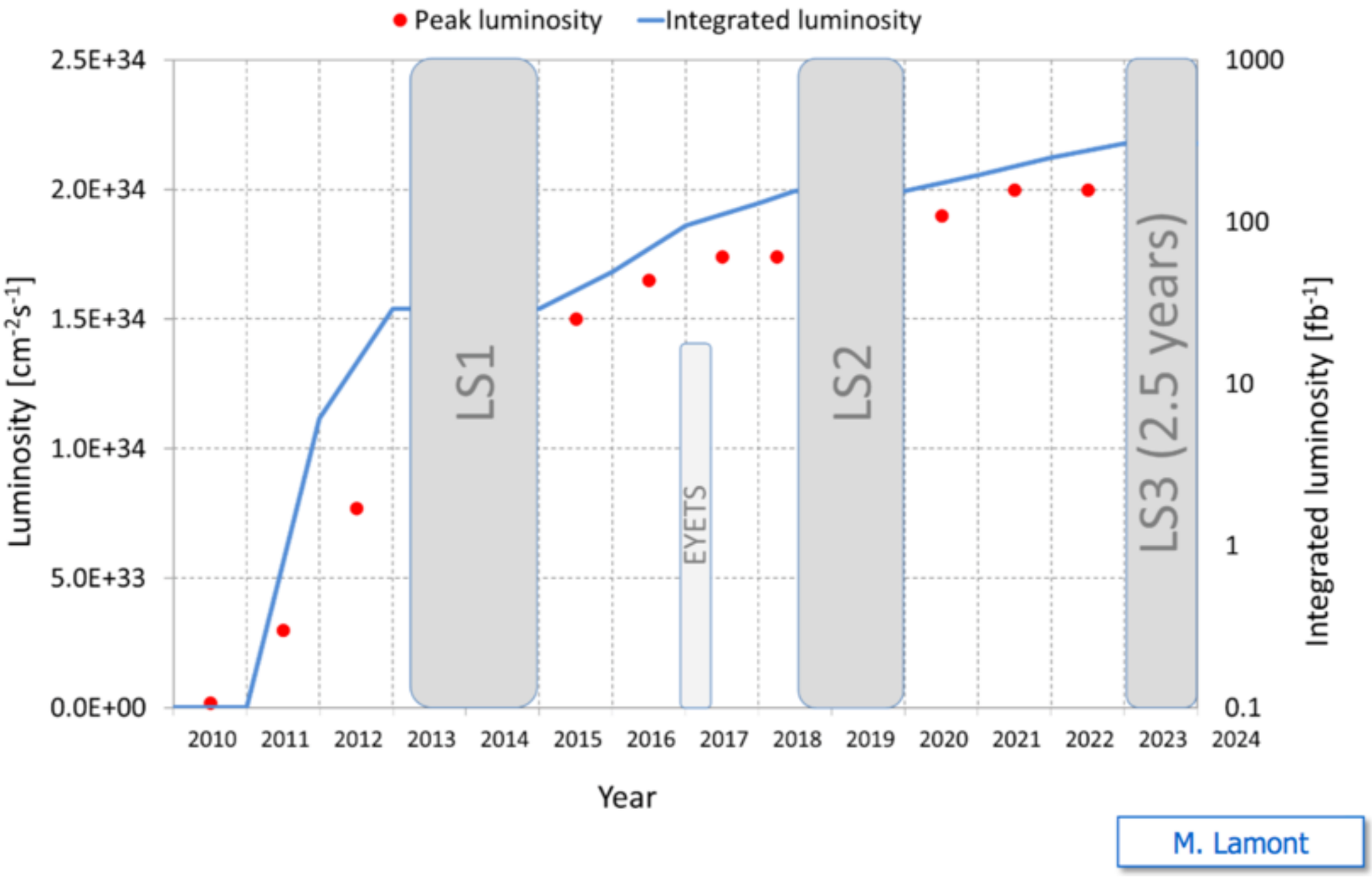
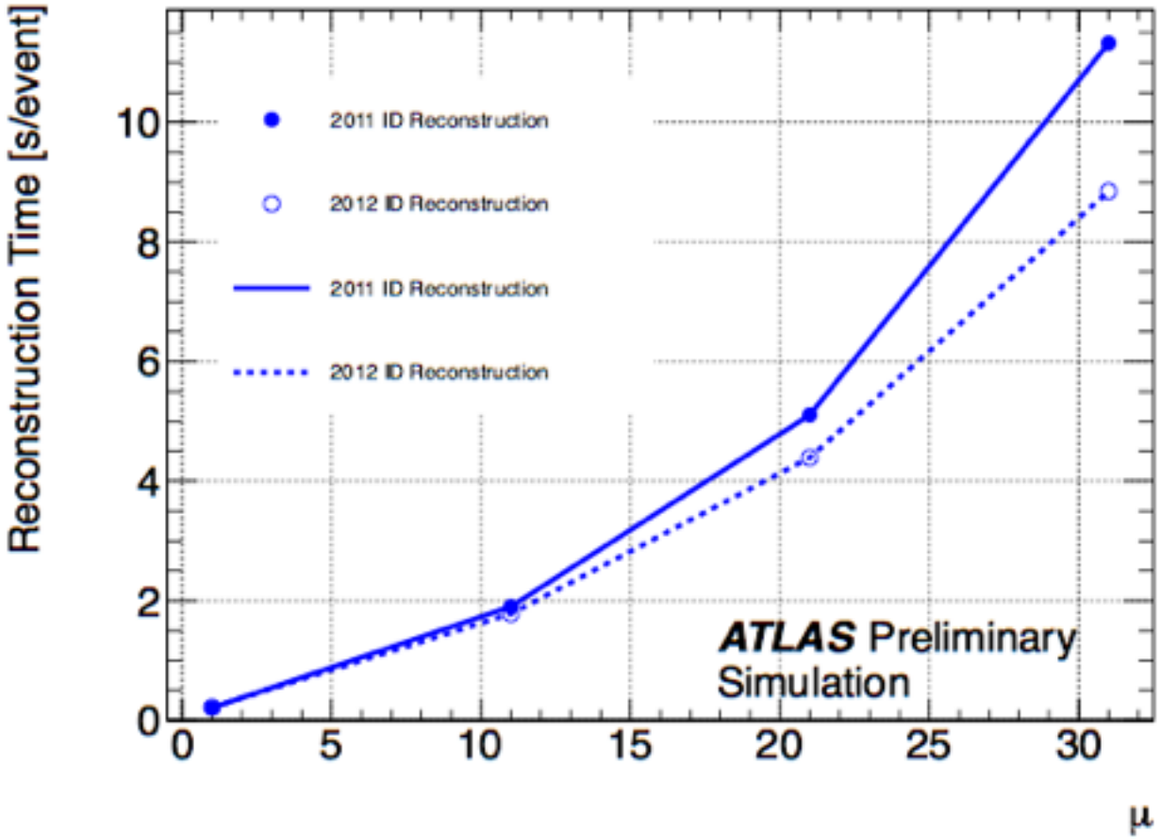
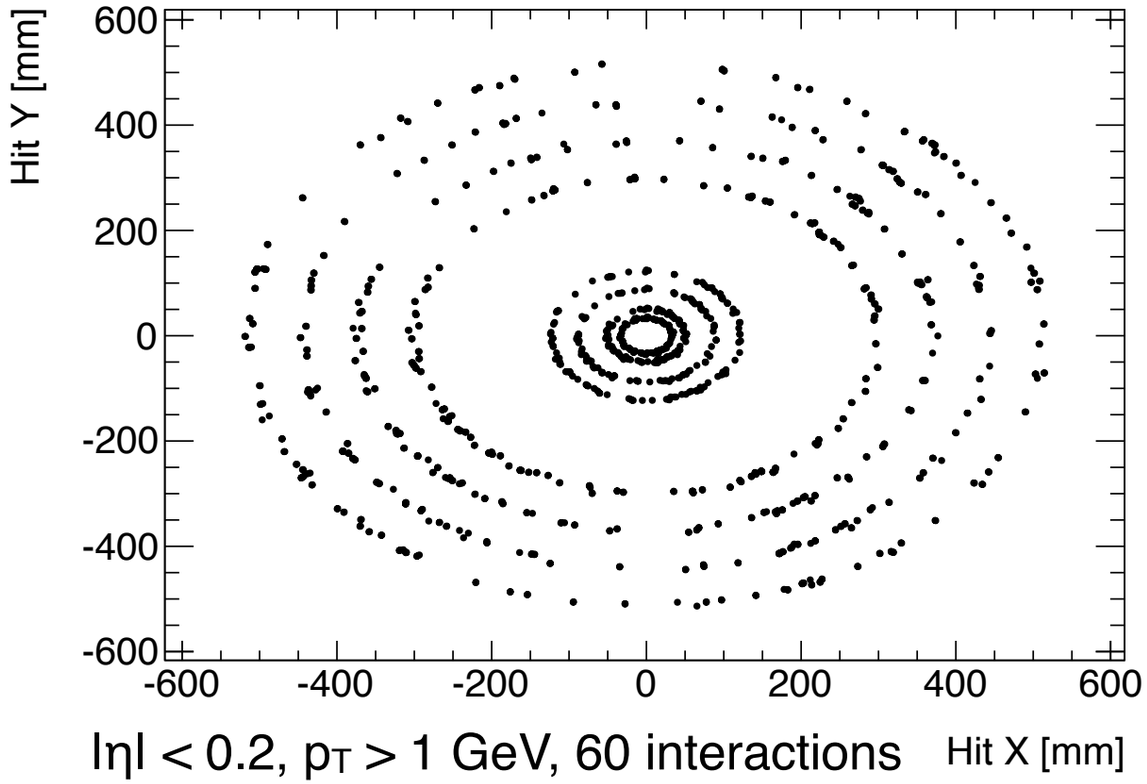
RUN II AND III CONDITIONS



TRACKING AT HIGH LUMINOSITY IS TRICKY

ATLAS-CONF-2012-042





- Huge combinatorial problem, very non-linear with number of interactions
- **Atlas FastTracKer (FTK)** solves these problems with a **hardware based approach**

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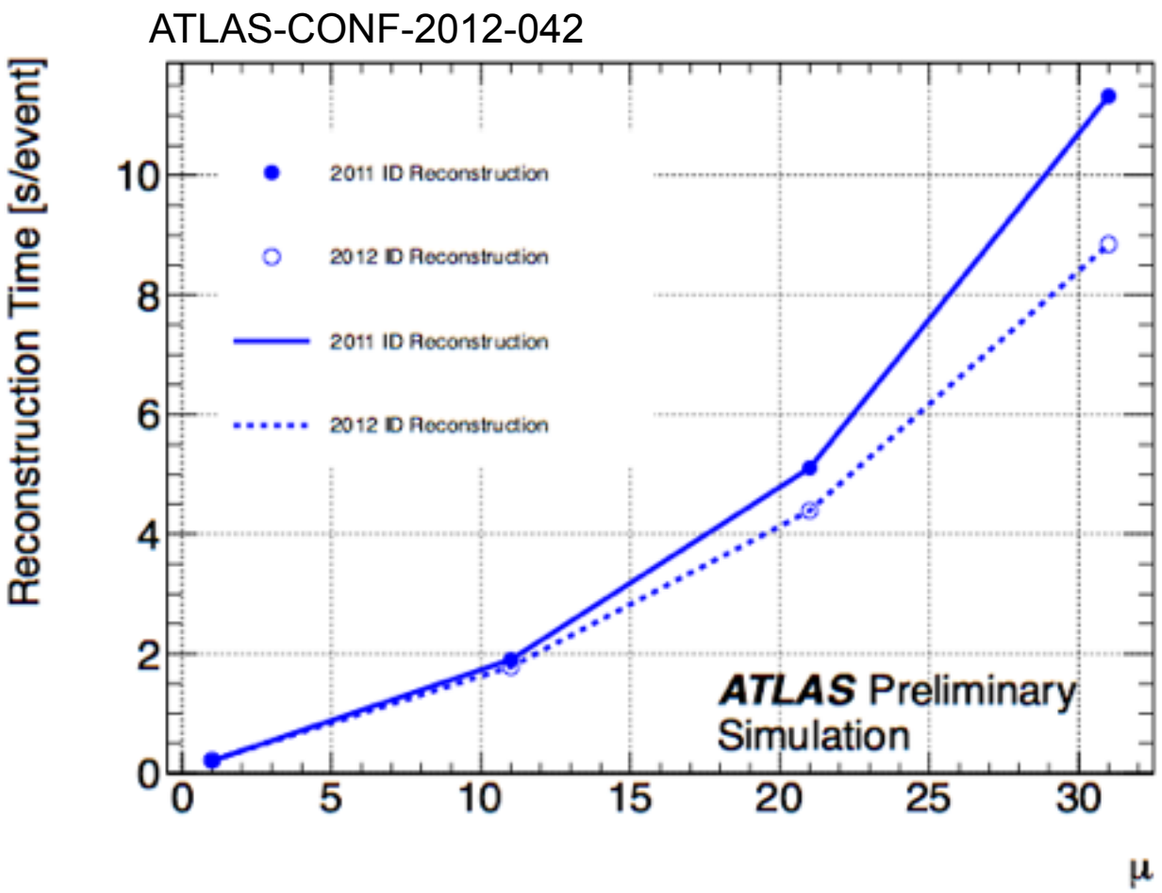

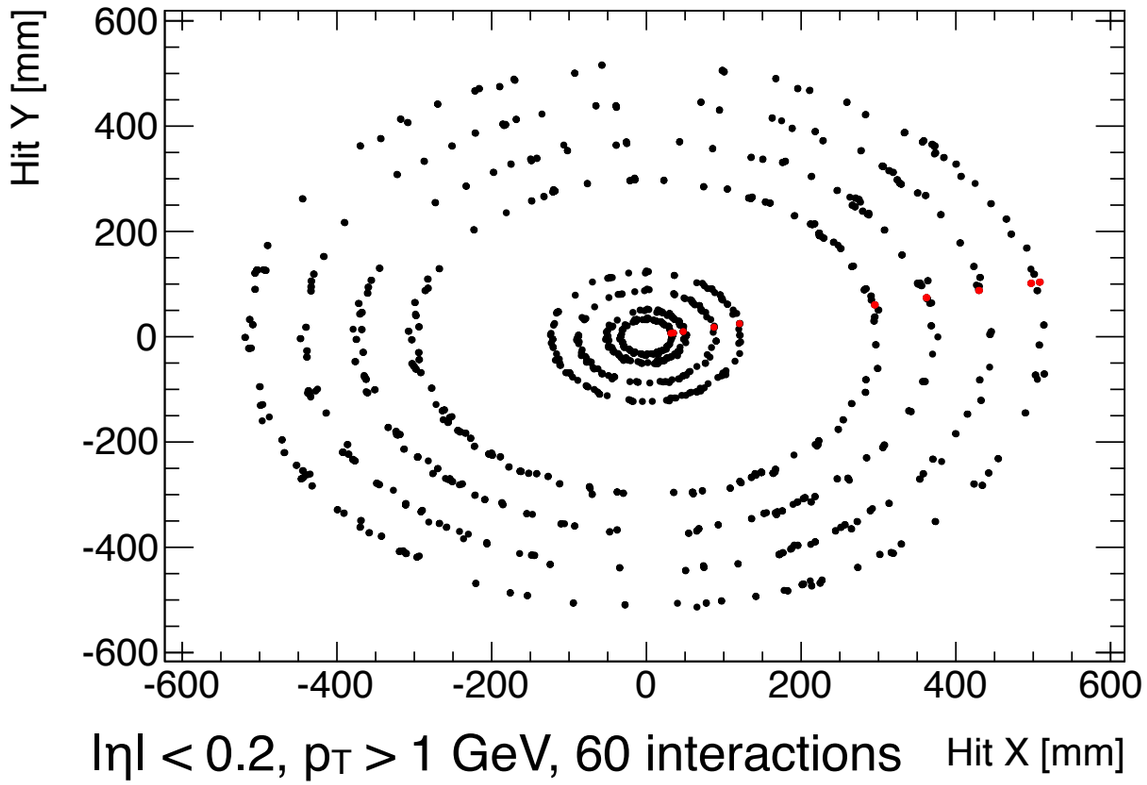

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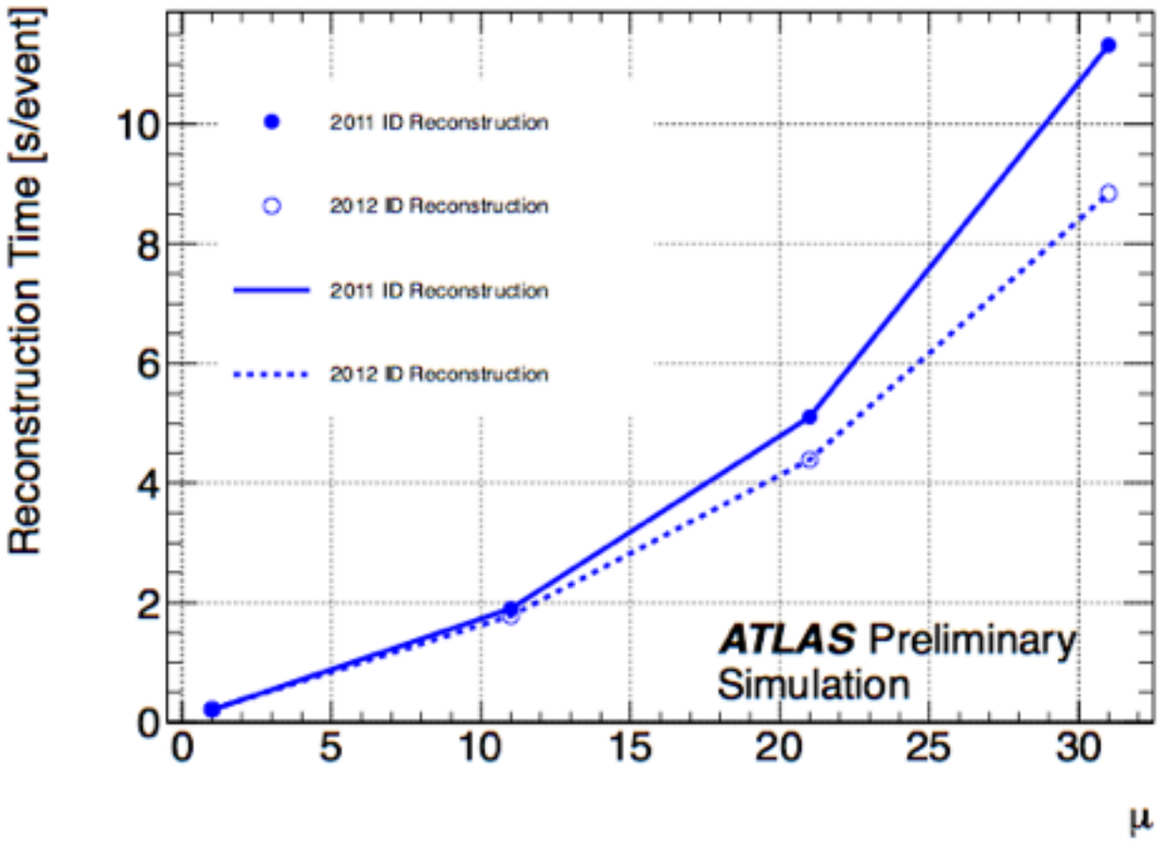

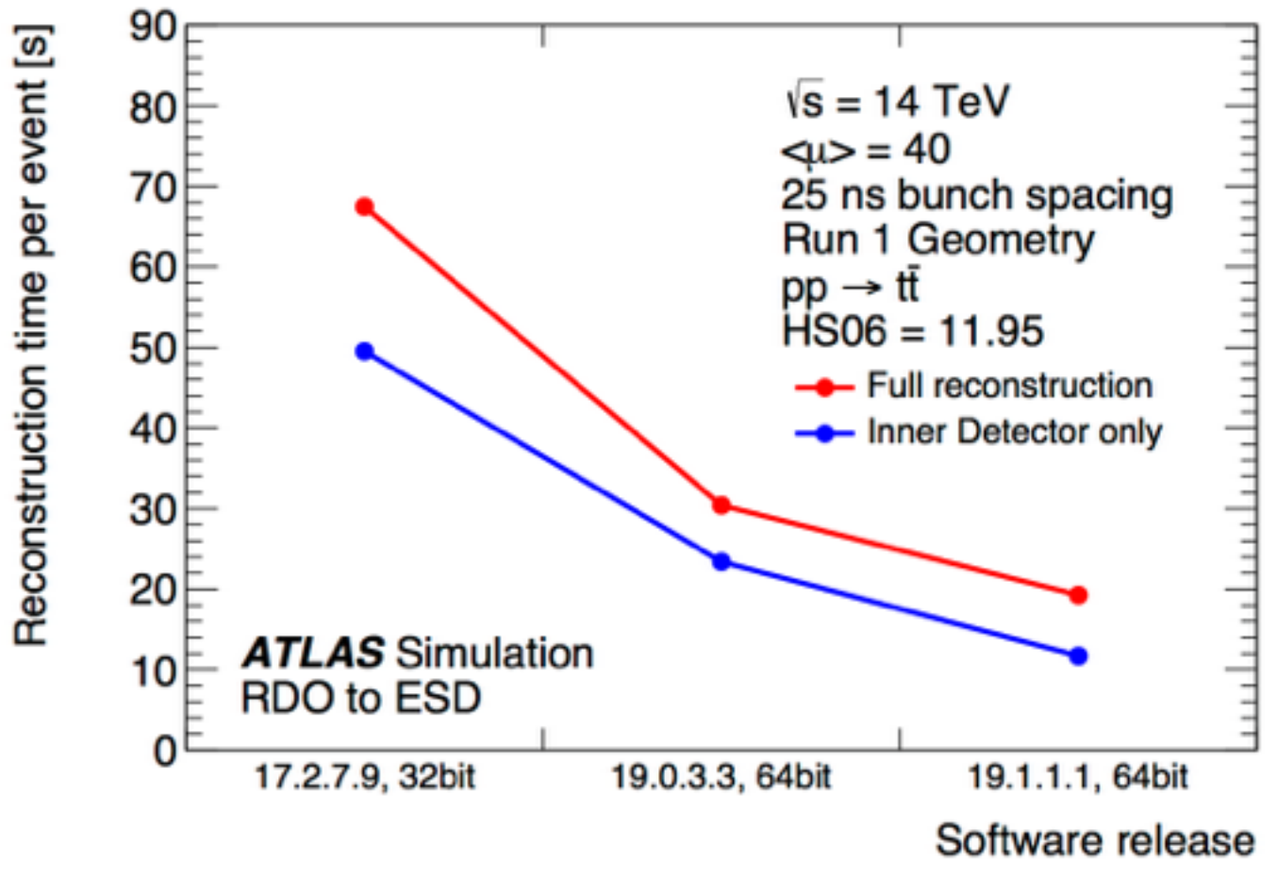

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WHAT DOES A HARDWARE BASED TRACK FINDER LOOK LIKE?

CONCEPTUAL DESIGN

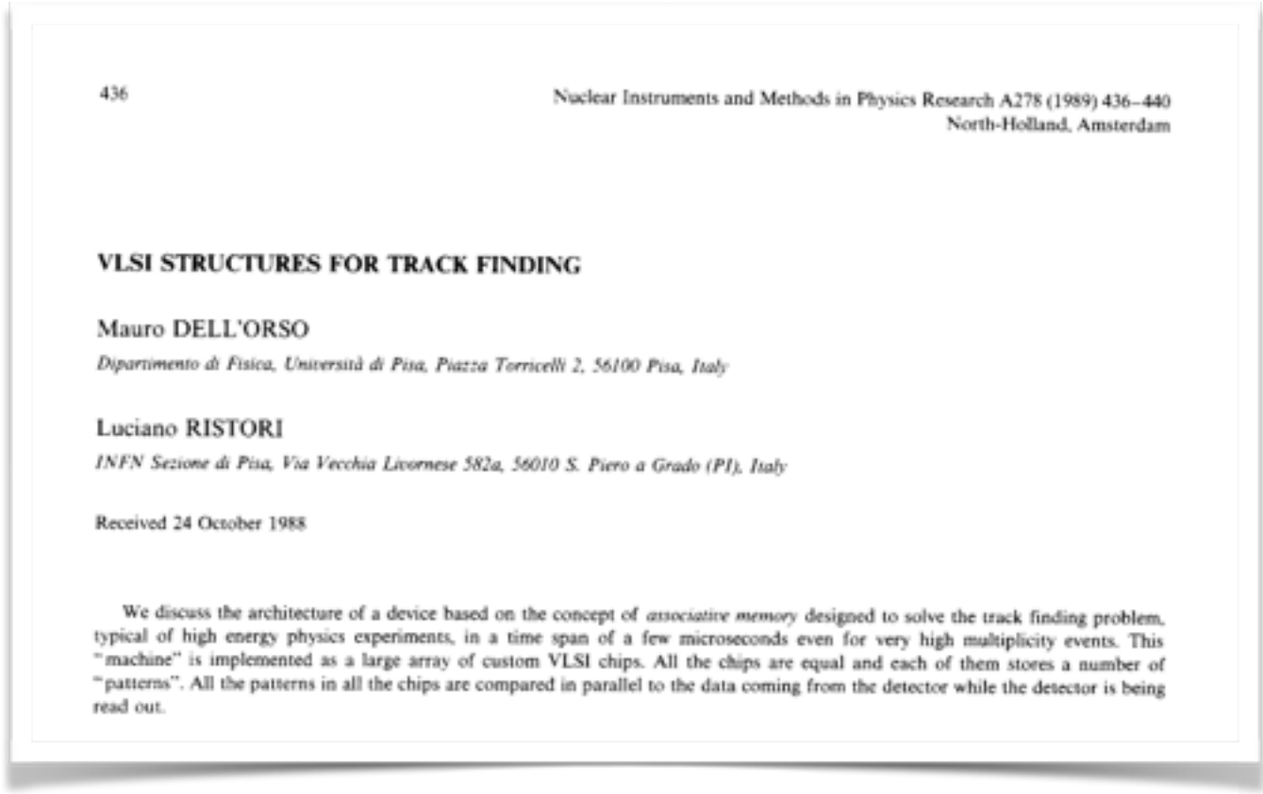
- **Parallelize** the problem: Divide the detector η-ϕ towers

- **Reduce** the data volume: Convert clusters into coarse resolution hits

- **Eliminate** costly loops: Compare hits to pre-stored patterns simultaneously

- **Simplify** algorithms: Use a linearized fit for track candidates

- **Hardware** solution: Implemented in FPGAs or custom ASICs



436 Nuclear Instruments and Methods in Physics Research A278 (1989) 436–440
North-Holland, Amsterdam

VLSI STRUCTURES FOR TRACK FINDING

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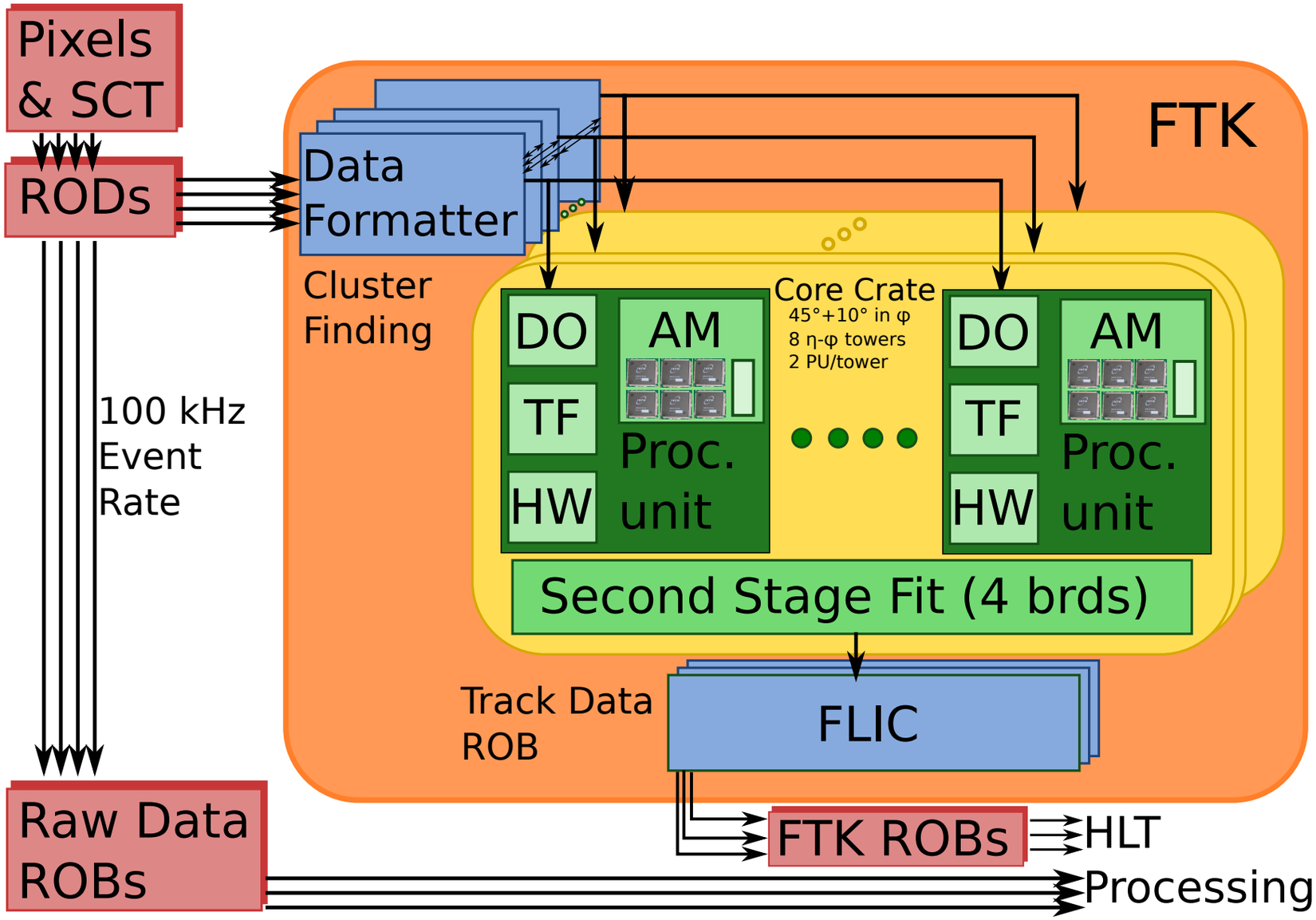
Luciano RISTORI
INFN Sezione di Pisa, Via Vecchia Livornese 582a, 56010 S. Piero a Grado (PI), Italy

Received 24 October 1988

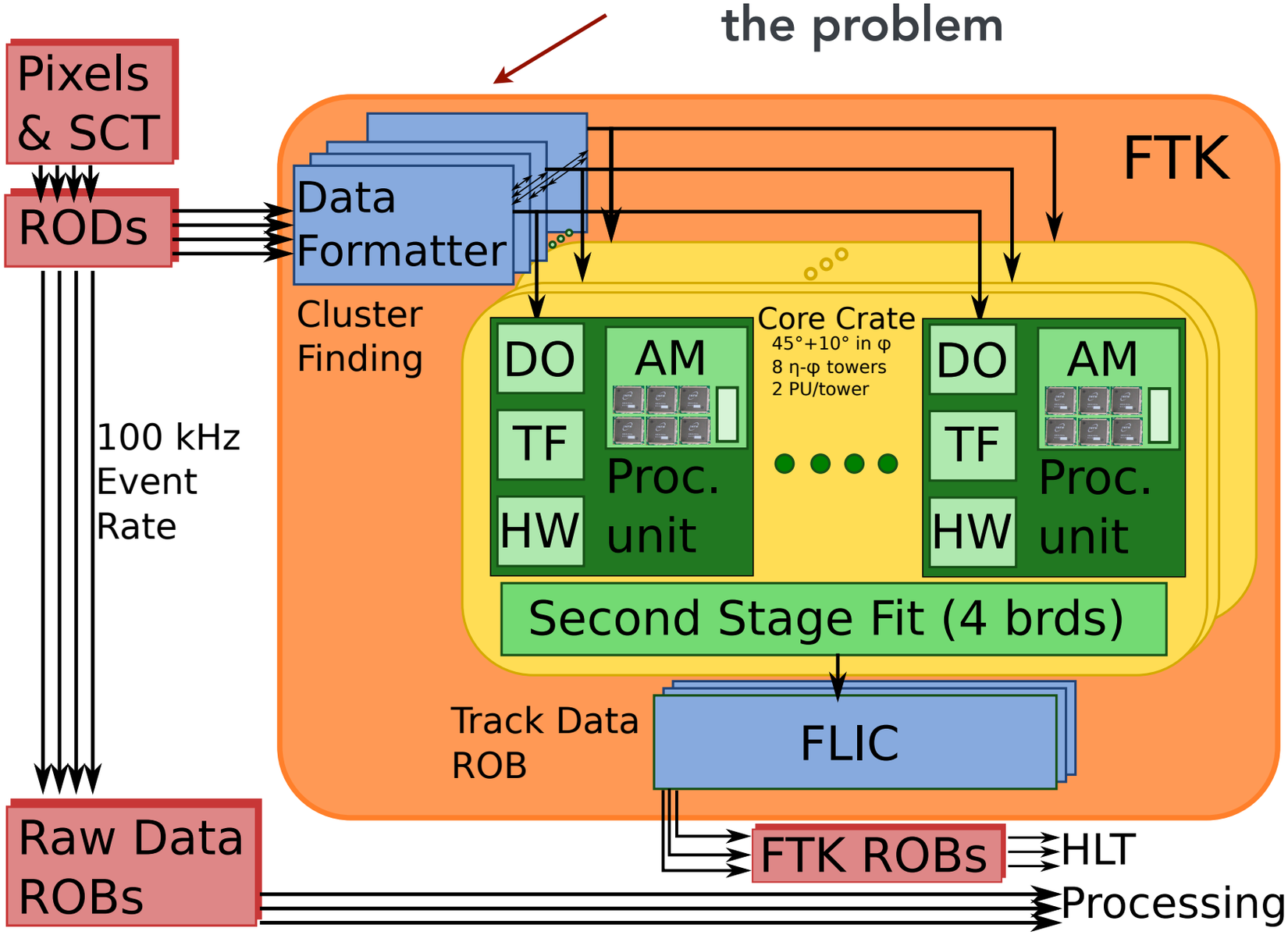
We discuss the architecture of a device based on the concept of *associative memory* designed to solve the track finding problem, typical of high energy physics experiments, in a time span of a few microseconds even for very high multiplicity events. This "machine" is implemented as a large array of custom VLSI chips. All the chips are equal and each of them stores a number of "patterns". All the patterns in all the chips are compared in parallel to the data coming from the detector while the detector is being read out.

SYSTEM ARCHITECTURE



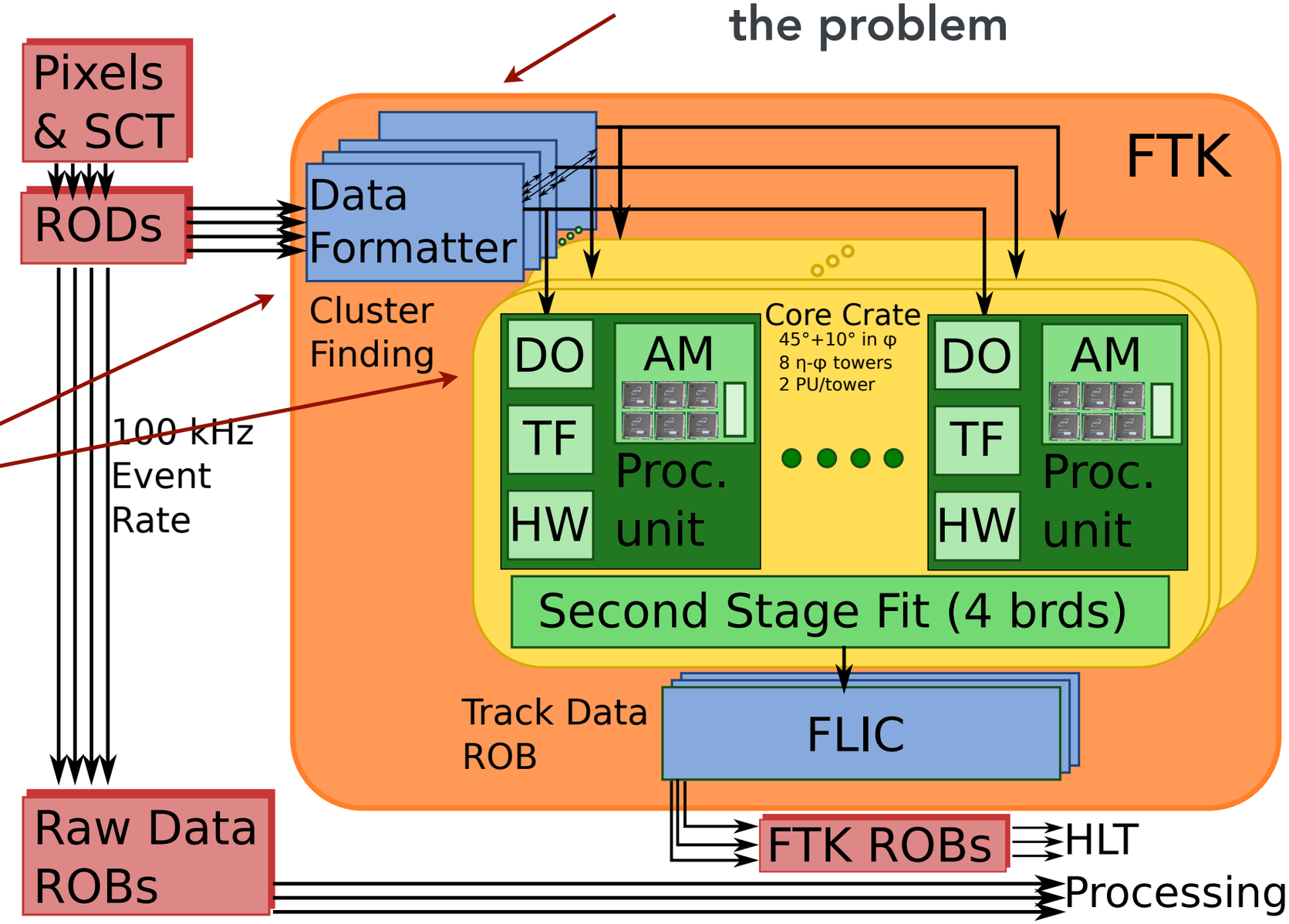
SYSTEM ARCHITECTURE

- **Parallelize the problem**



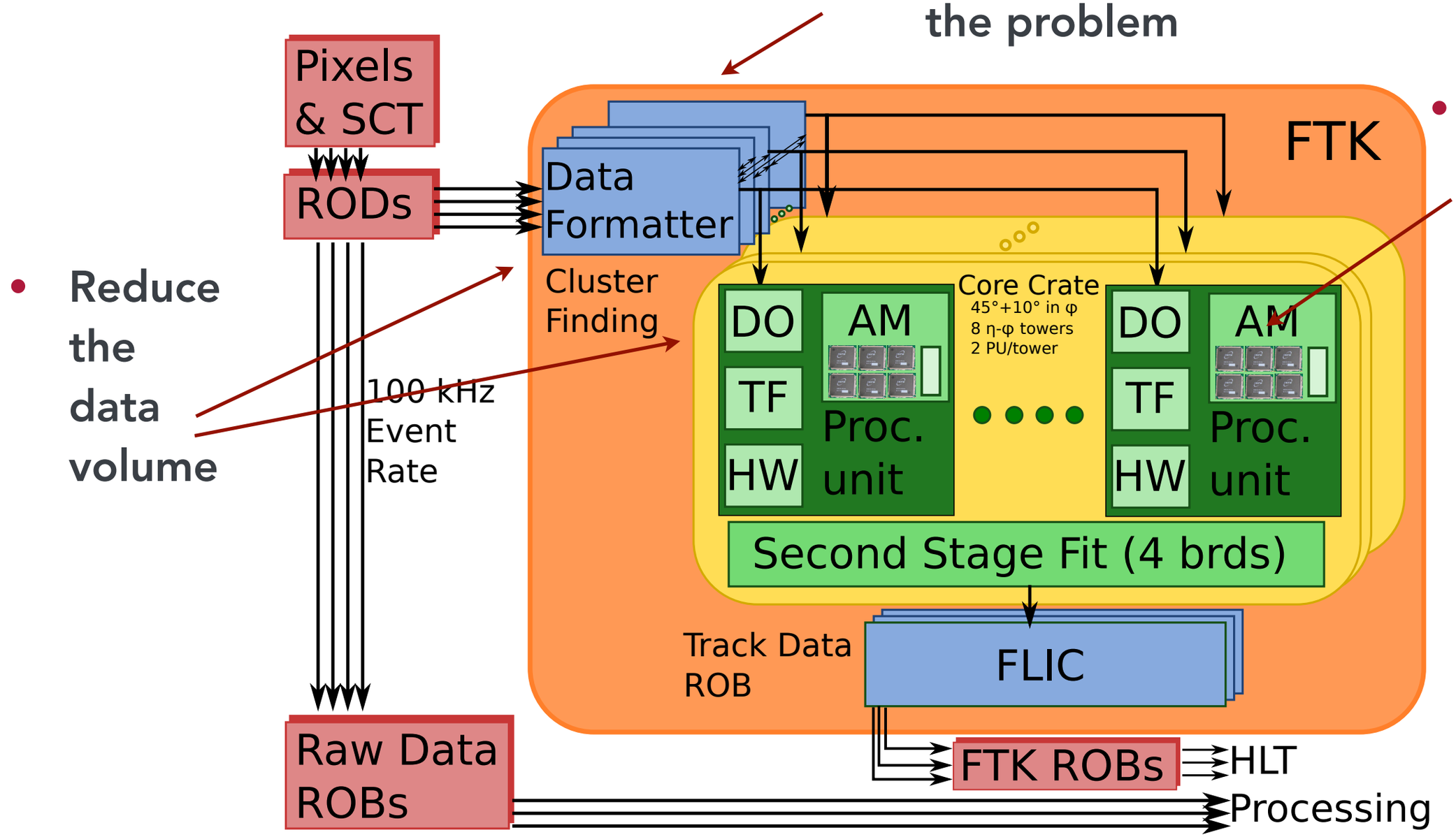
SYSTEM ARCHITECTURE

- Parallelize the problem
- Reduce the data volume



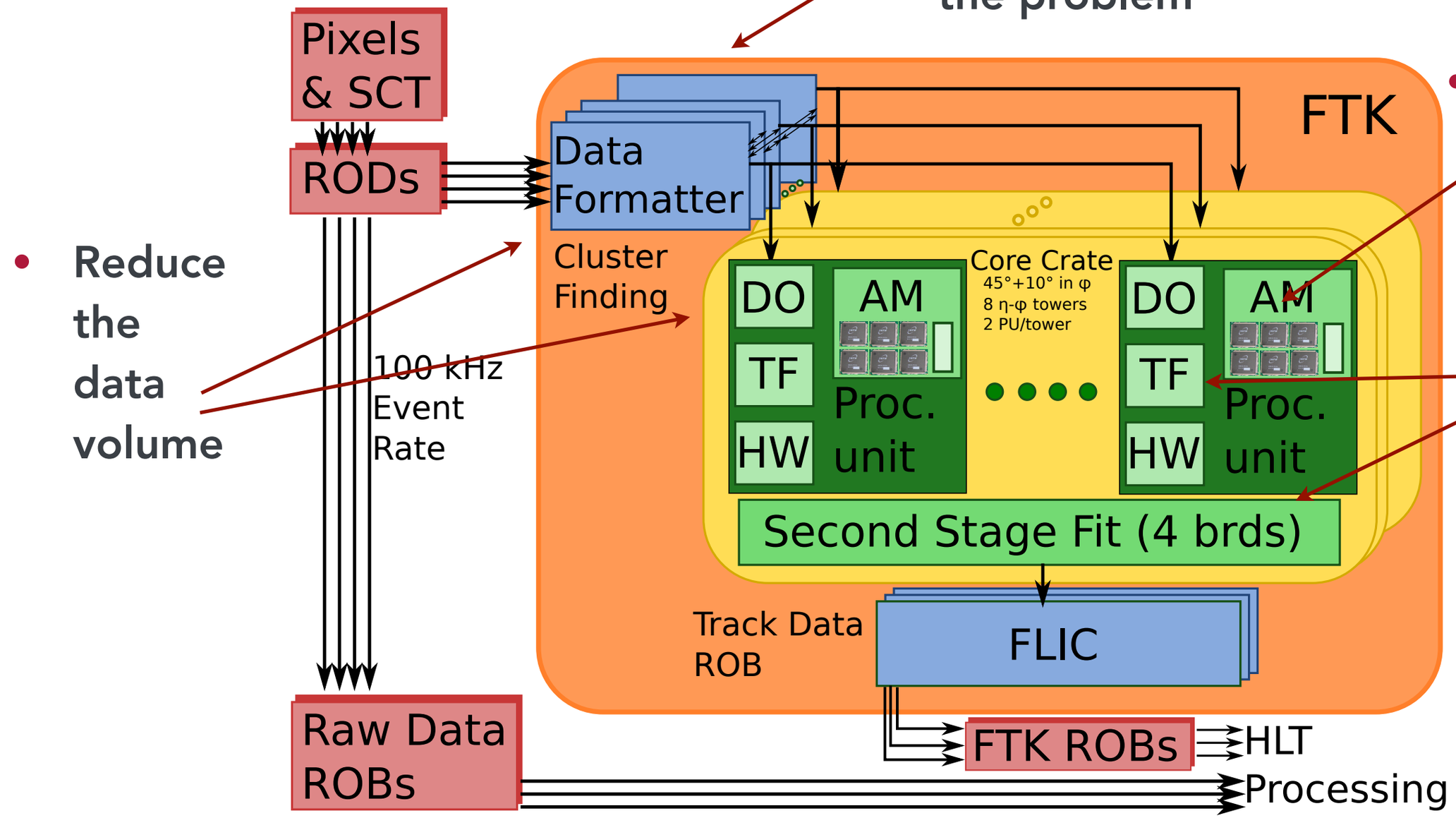
SYSTEM ARCHITECTURE

- Parallelize the problem
- Reduce the data volume
- Eliminate costly loops



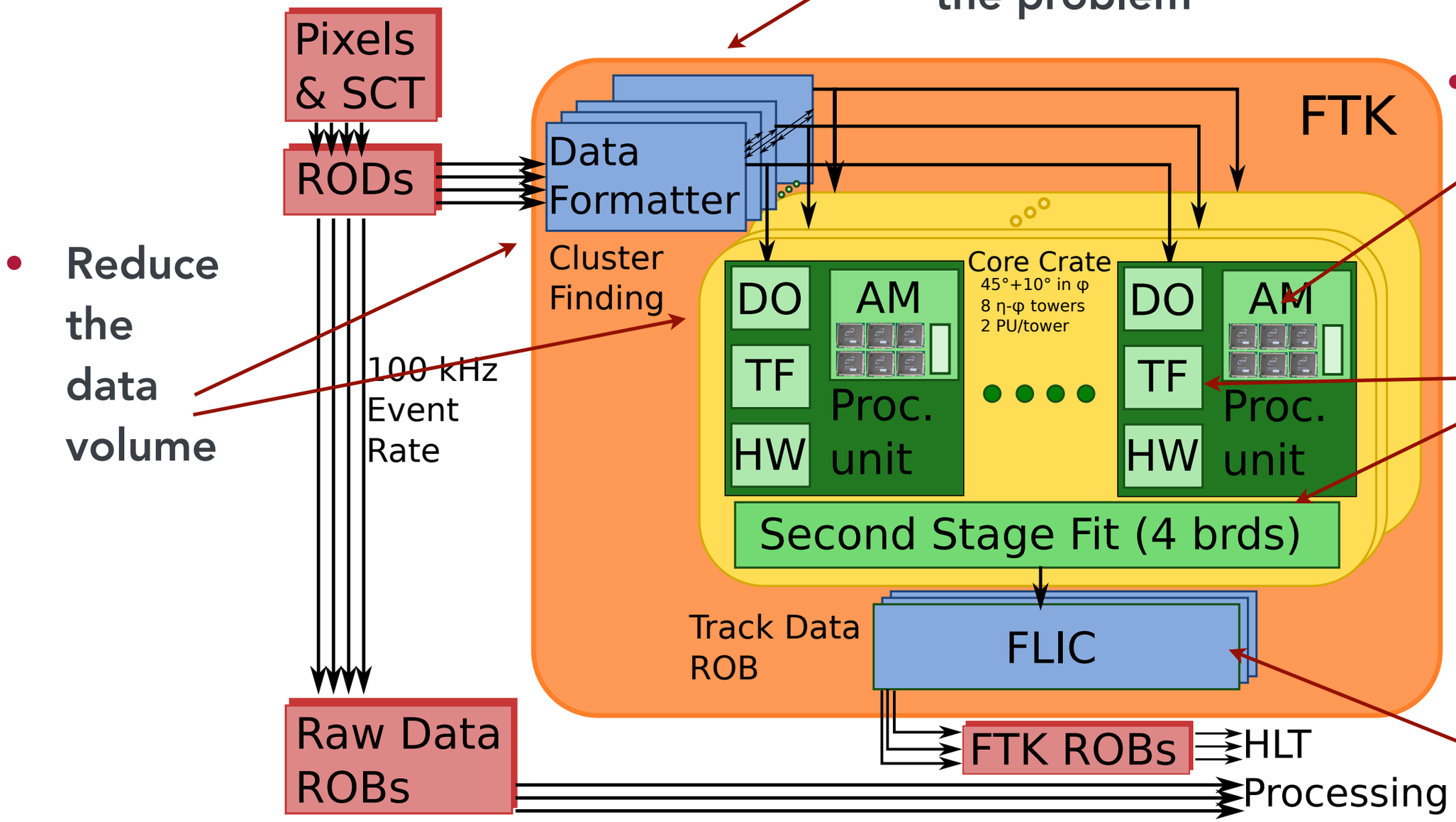
SYSTEM ARCHITECTURE

- Parallelize the problem
- Reduce the data volume
- Eliminate costly loops
- Simplify algorithms



SYSTEM ARCHITECTURE

- **Parallelize the problem**
- **Eliminate costly loops**
- **Reduce the data volume**
- **Simplify algorithms**
- **Available to HLT in O(100μs)**



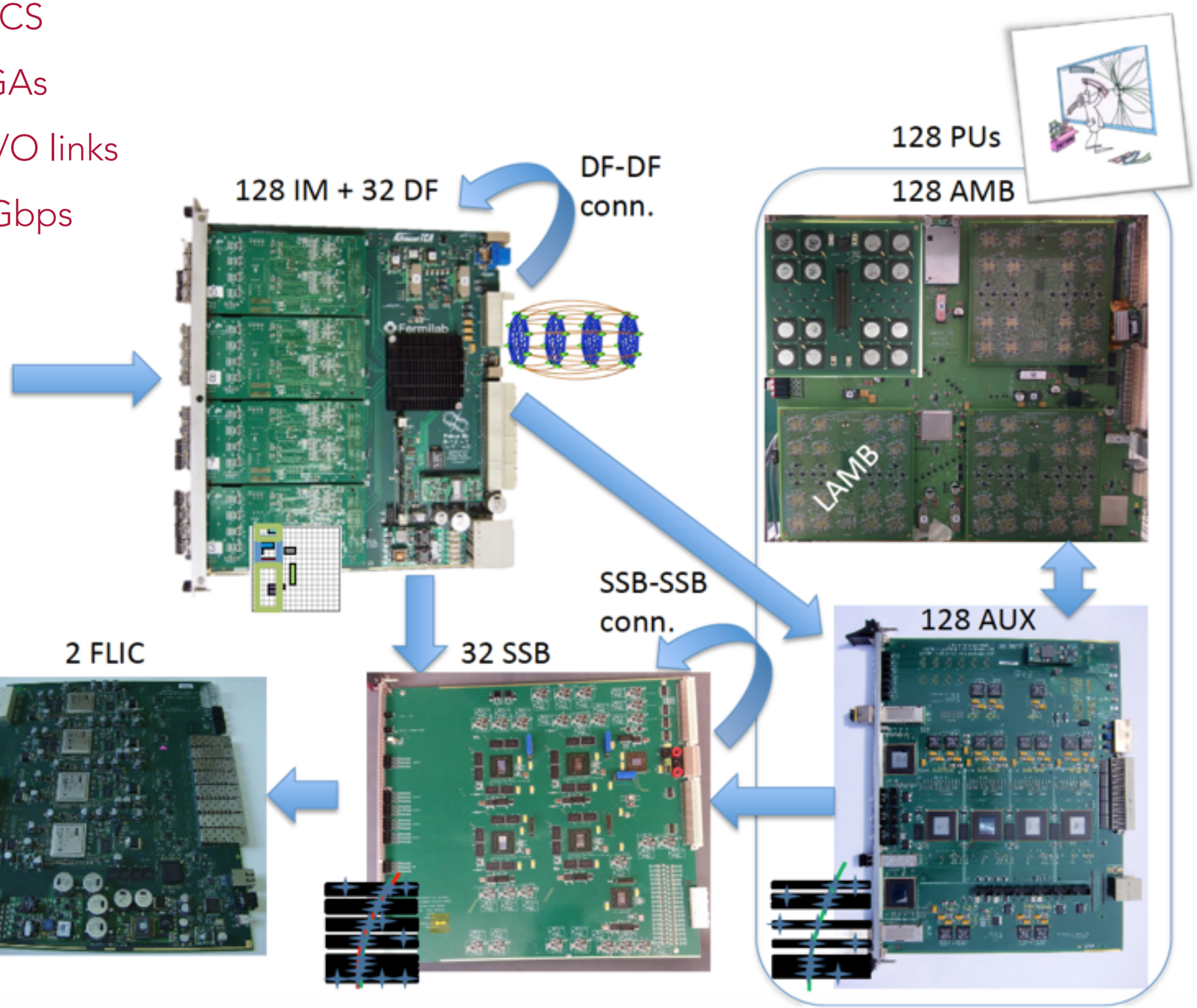
HARDWARE

~8000 ASICS

~2000 FPGAs

Thousands of I/O links

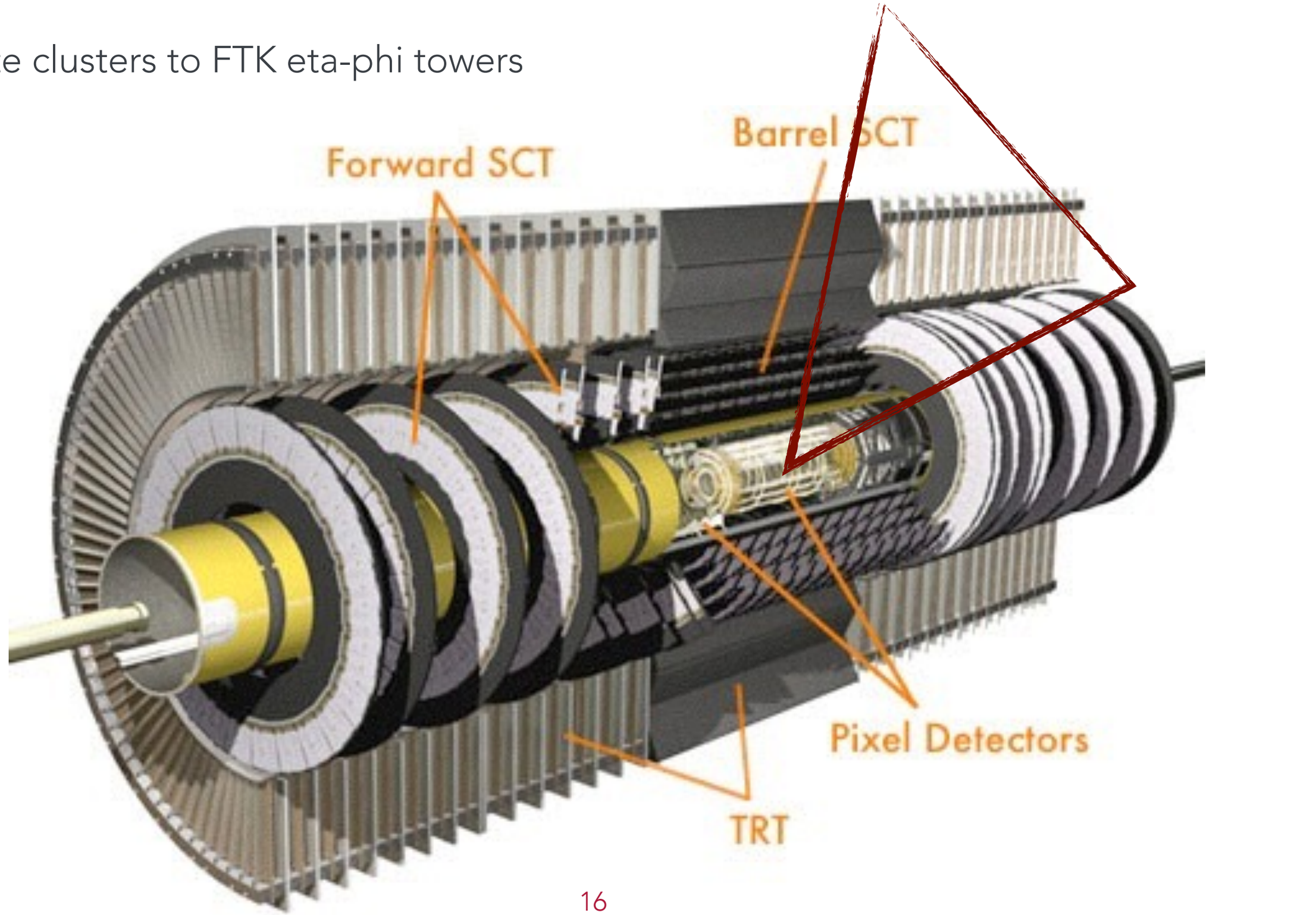
@ up to 10 Gbps



STAGE 1: DATA FORMATTING

- Clustering

- Route clusters to FTK eta-phi towers



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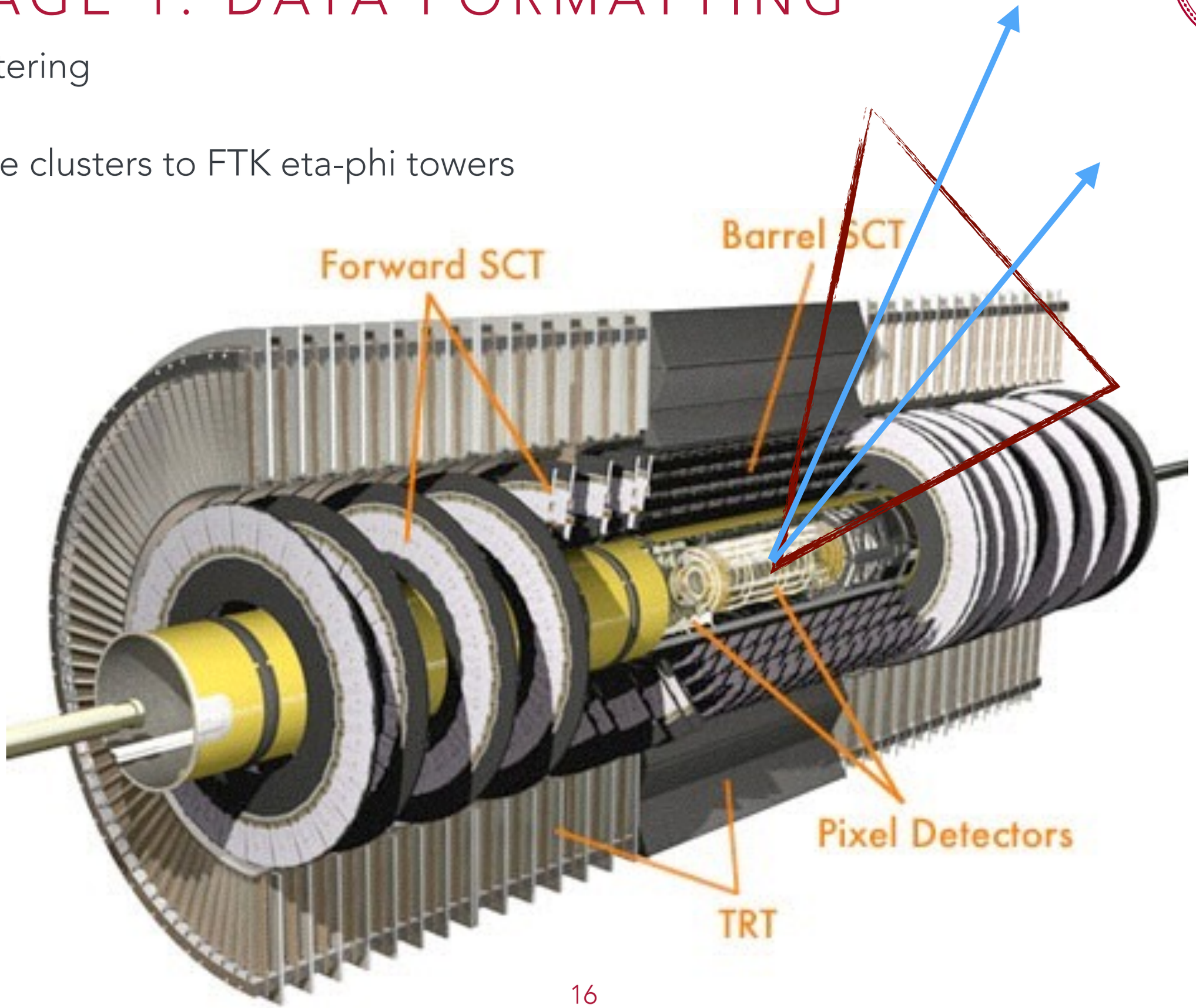
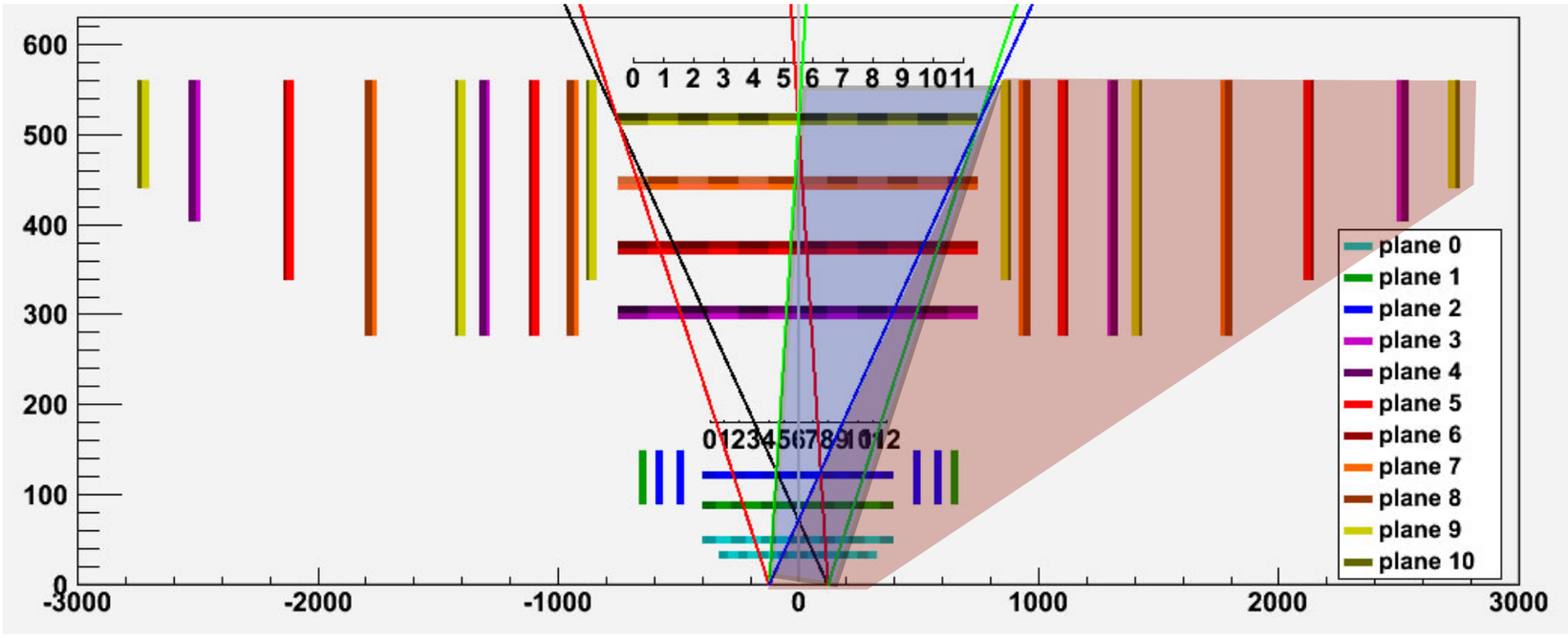
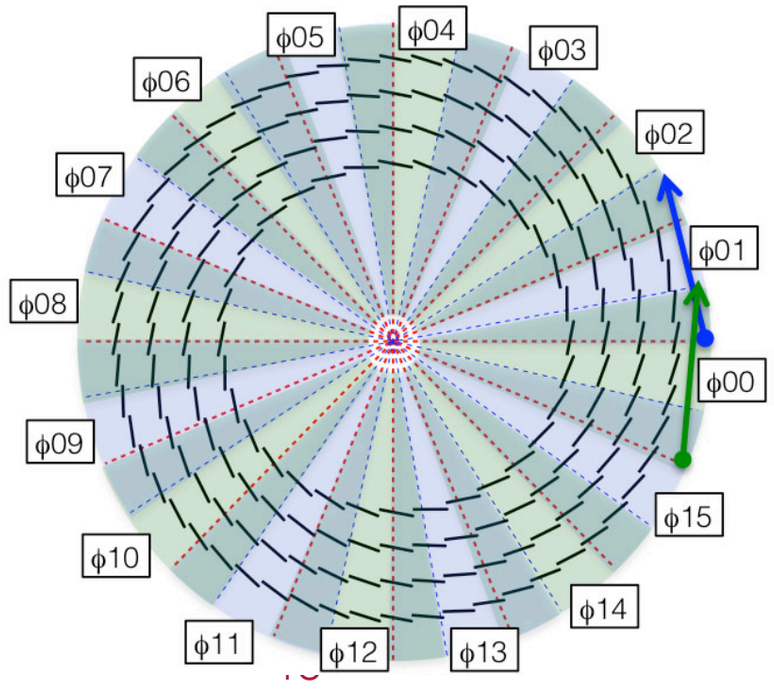


STAGE 1: DATA FORMATTING

- Clustering

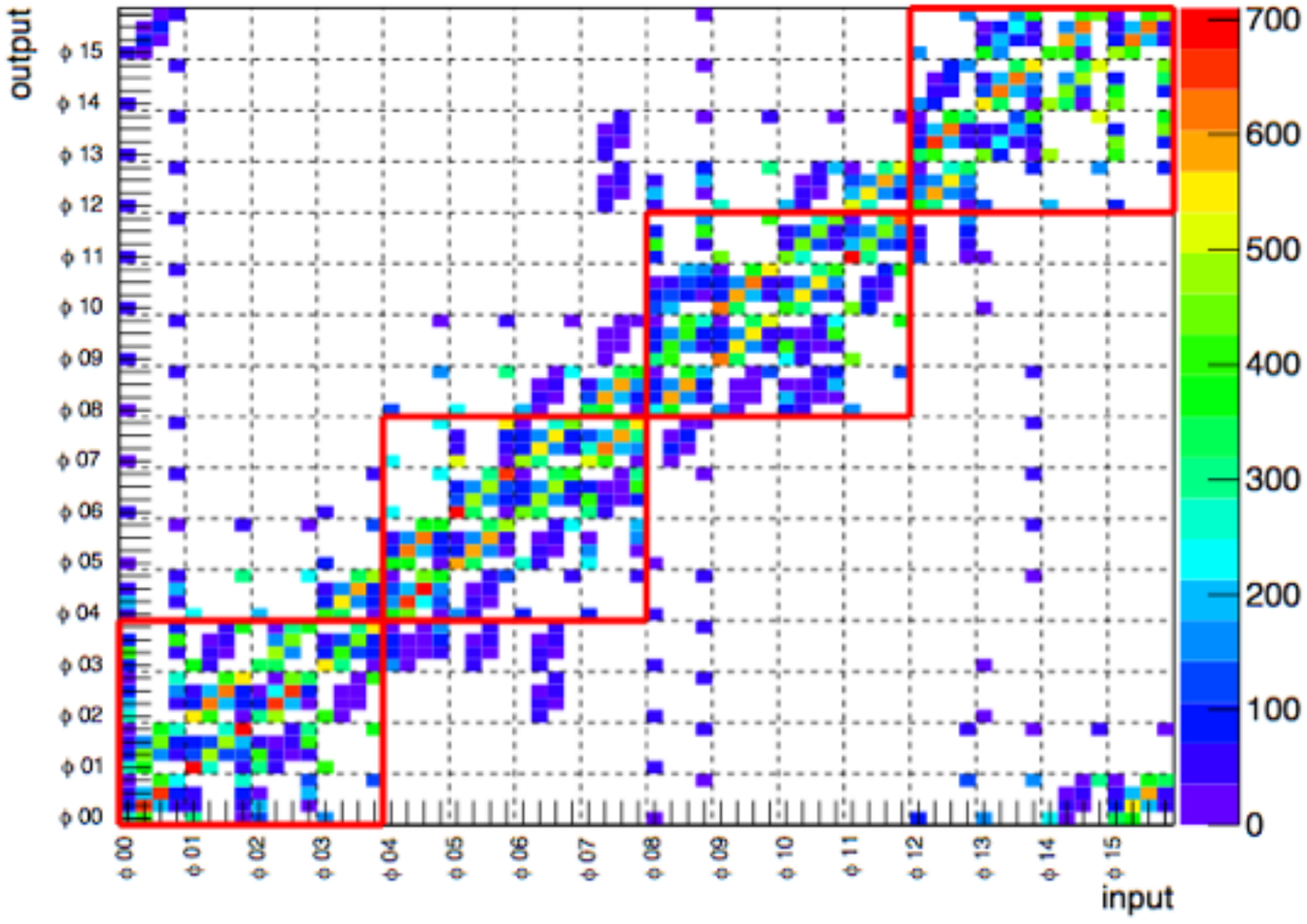
- Route clusters to FTK eta-phi towers





STAGE 1: DATA FORMATTING

- Implemented in ATCA crates with full mesh backplane (40Gbps)
- 32 DF boards in 4 crates
- Inter-board routing determined using greedy search algorithm minimizing tails of routing distribution



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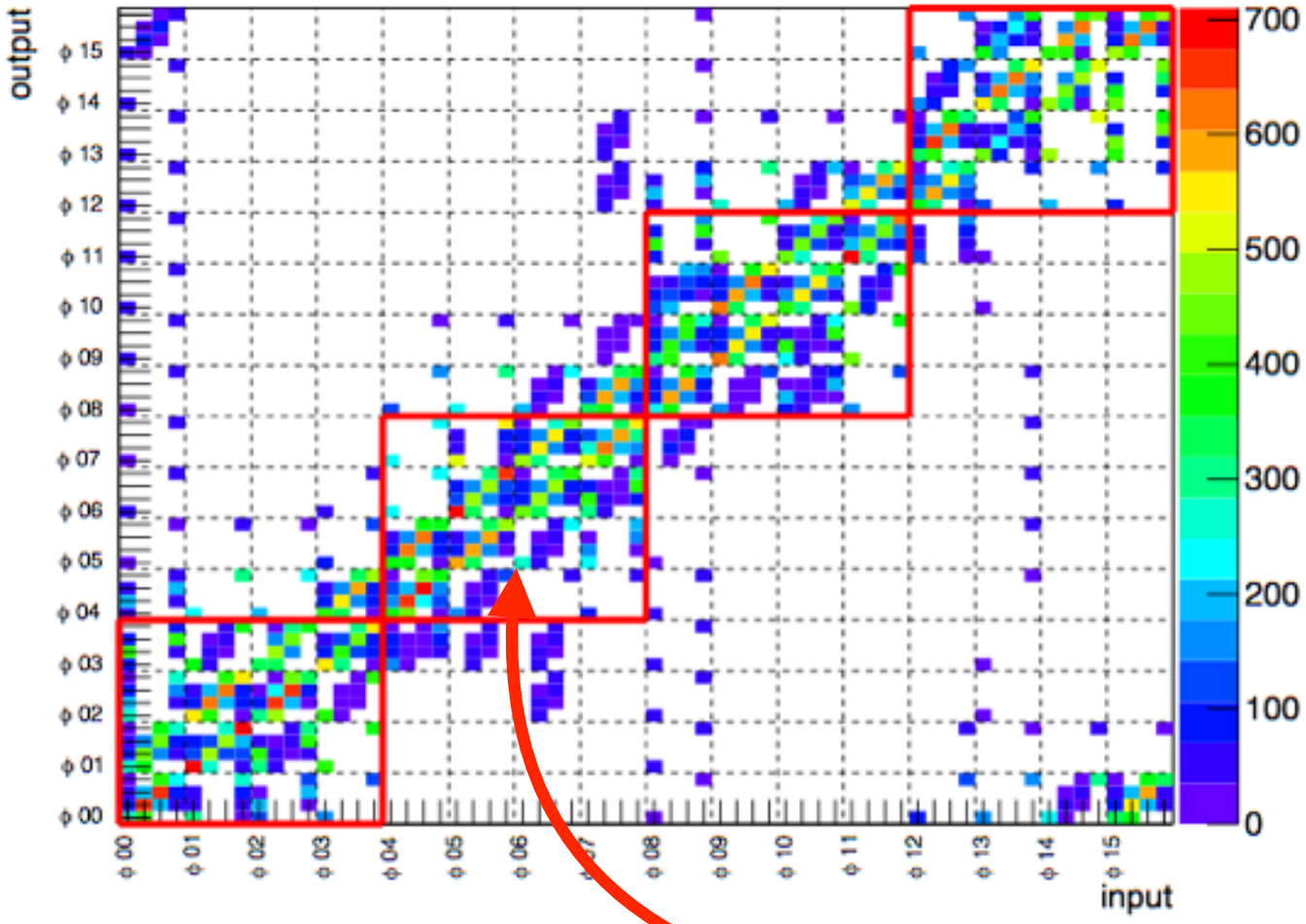

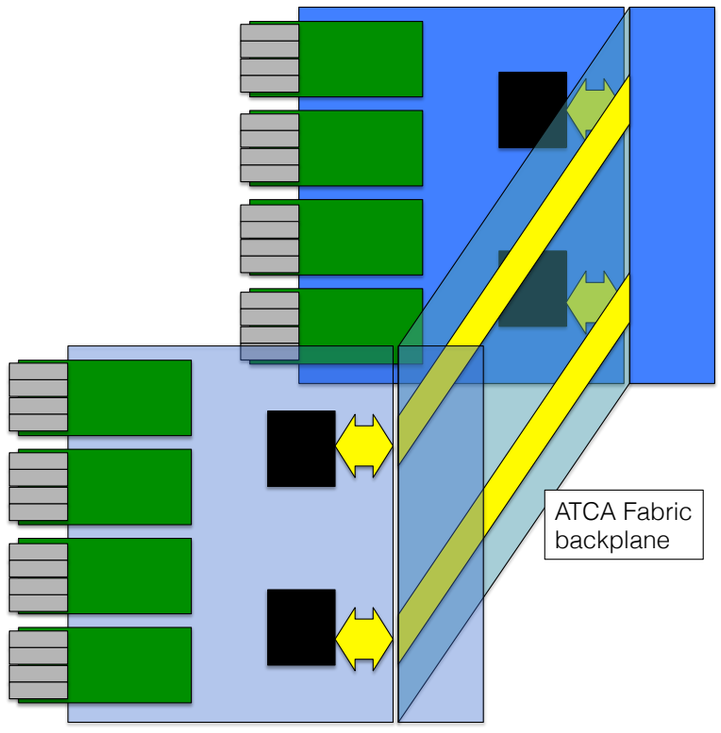

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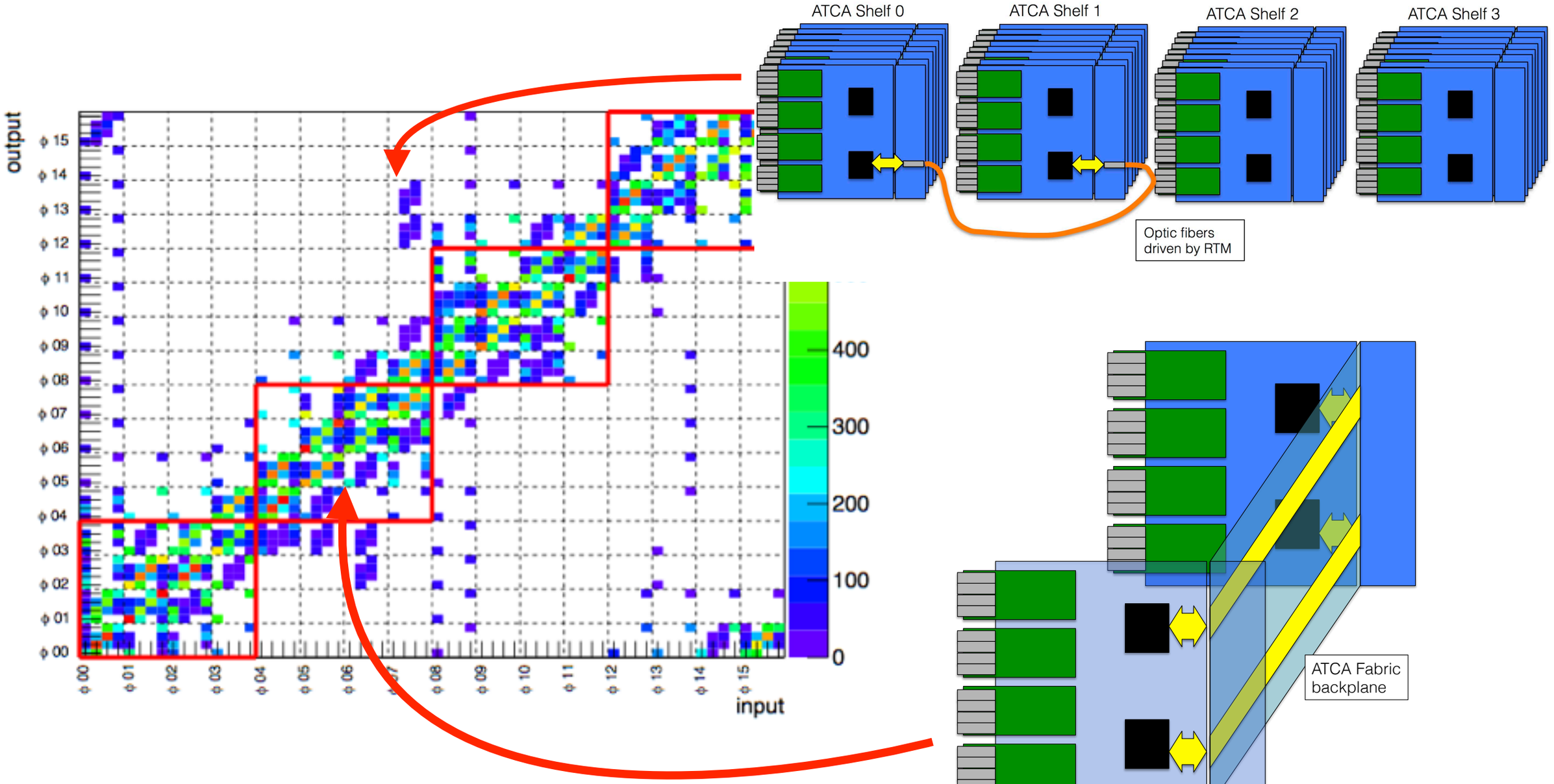

DATA FORMATTER + INPUT MEZZANINE SYSTEM

Pixel/SCT Hits

Cluster Hits

Hits to downstream boards

Fermilab

Distributes clusters to FTK towers

IPMC

To Other DFs

DATA FORMATTER + INPUT MEZZANINE SYSTEM

Hits to downstream boards

Pixel/SCT Hits

Cluster Hits

IM FW

Clustering

- select events based on trigger type
- configure HOLA to respect FTK XOFF
- source internally loaded events for system test

DF FW

IM Hits Receiver

From Other DFs

DF Hits Receiver

Down-stream Router

To AUX/ SSB

Router to other DFs

To Other DFs

To Other DFs

STAGE 2: BINGO
DATA REDUCTION AND PATTERN RECOGNITION

- Hits are ganged together into coarse resolution hits

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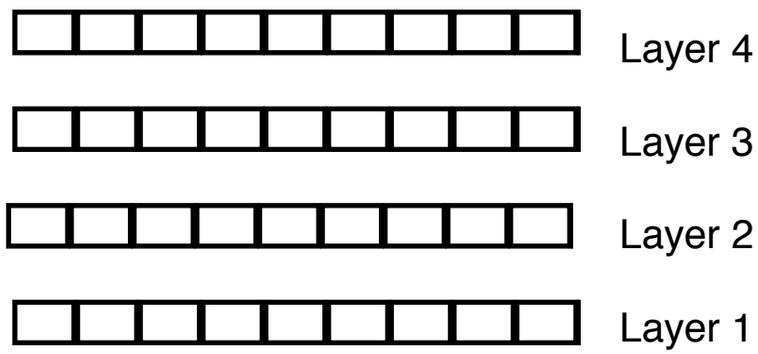

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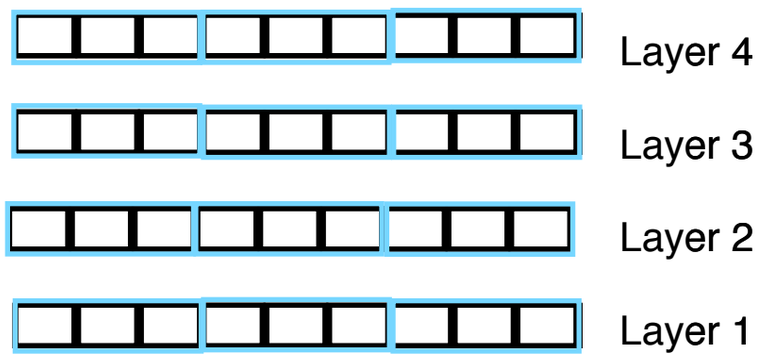

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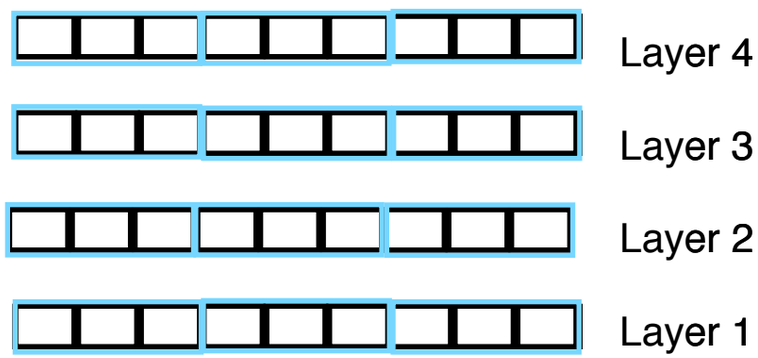

- Hits are ganged together into coarse resolution hits

- All possible patterns of coarse resolution hits determined from simulation

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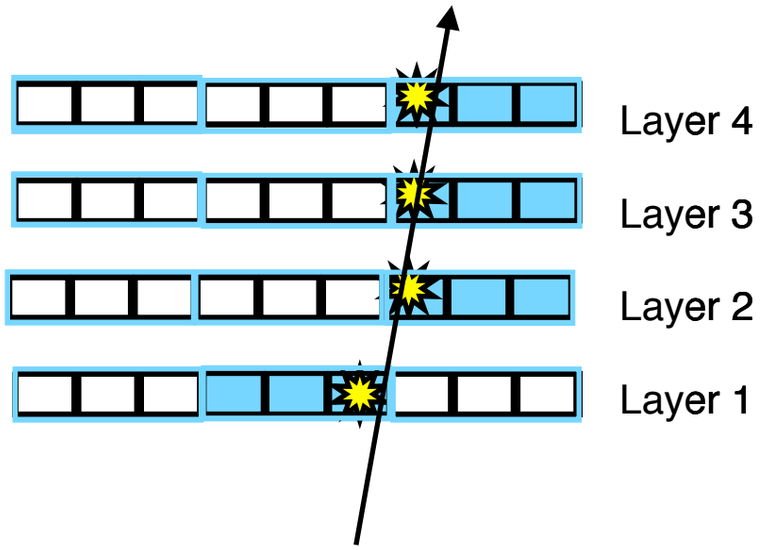

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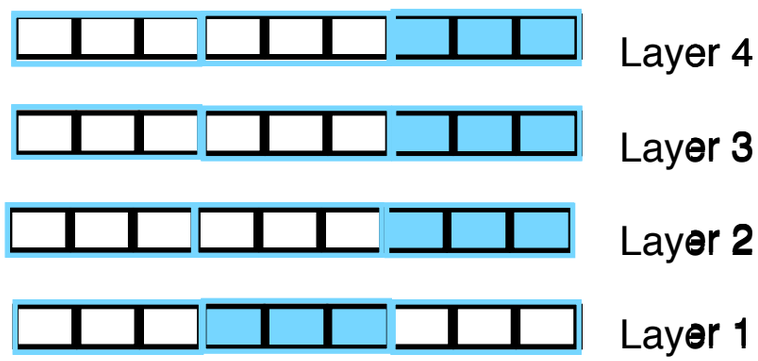

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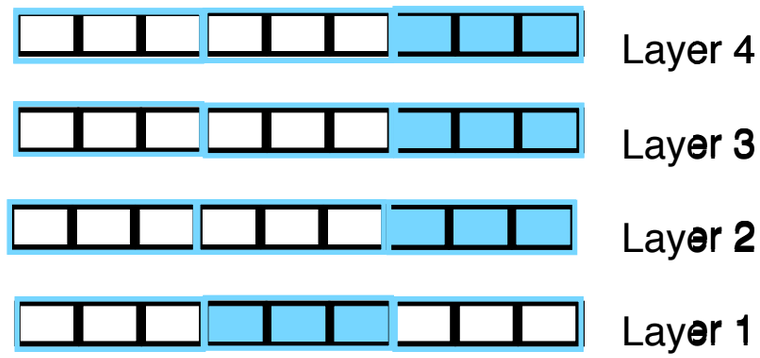

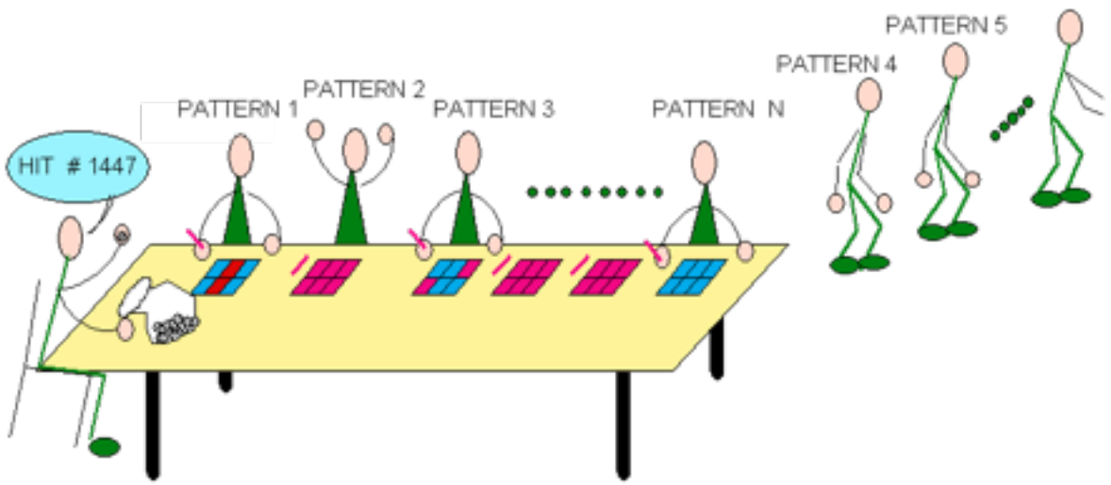

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- Custom associative memory chips are used to **compare hits** to O(10^9) patterns **simultaneously** (bingo cards)

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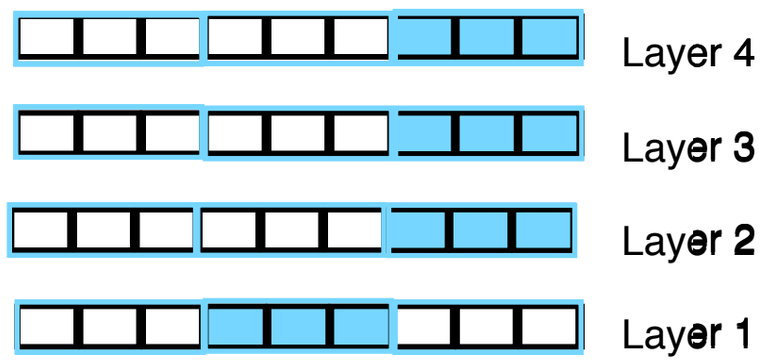

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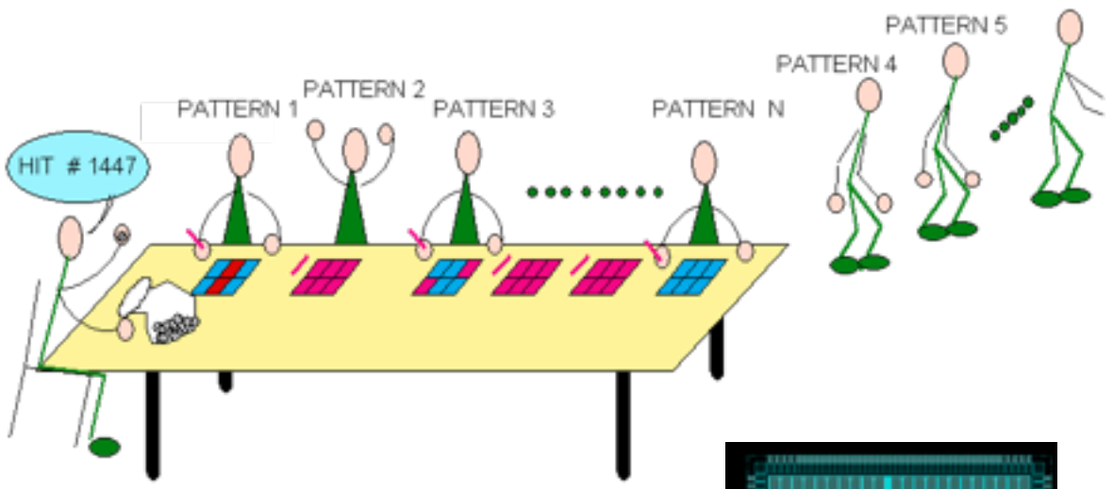

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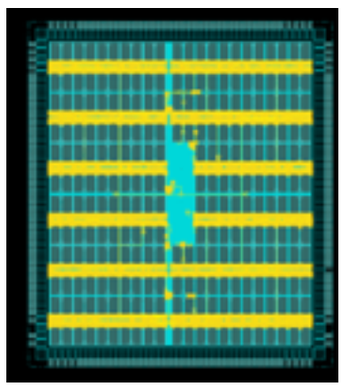
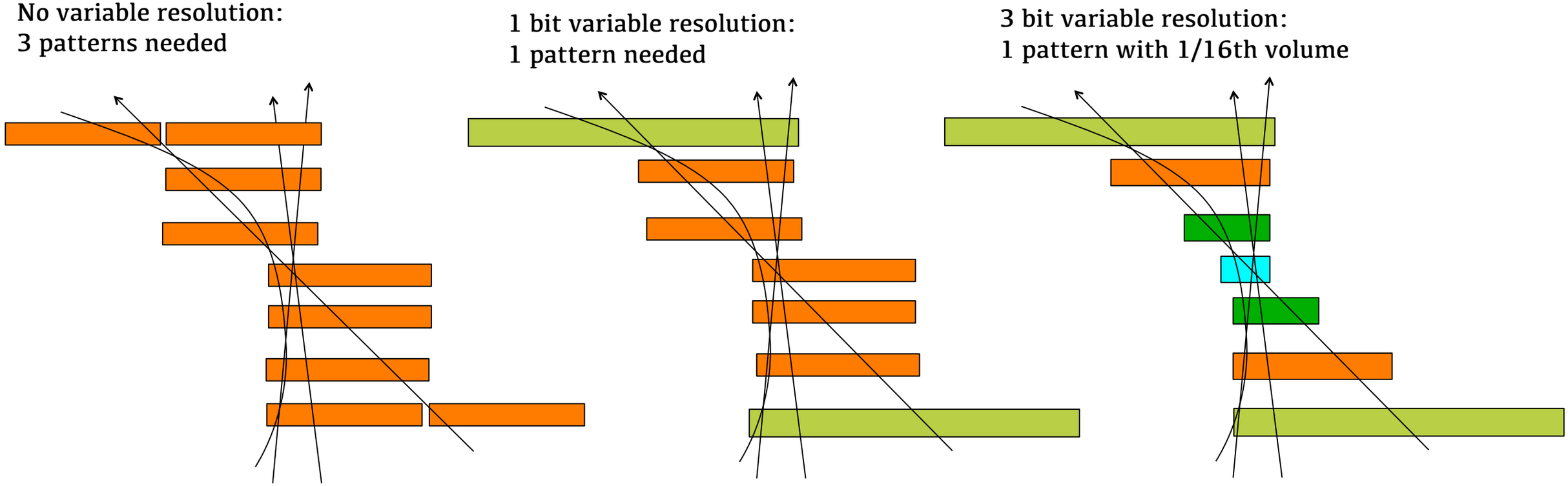


AMChip06

- Custom associative memory chips are used to **compare hits** to $O(10^9)$ patterns **simultaneously** (bingo cards)

REFINEMENTS

- Majority Logic: Only require N out of M layers have a match
  - Gains efficiency
- Variable Resolution Patterns (Don't Care Bits)
  - Reduces the number of patterns and fake matches



- Number of don't care bits set on a layer by layer, pattern by pattern basis

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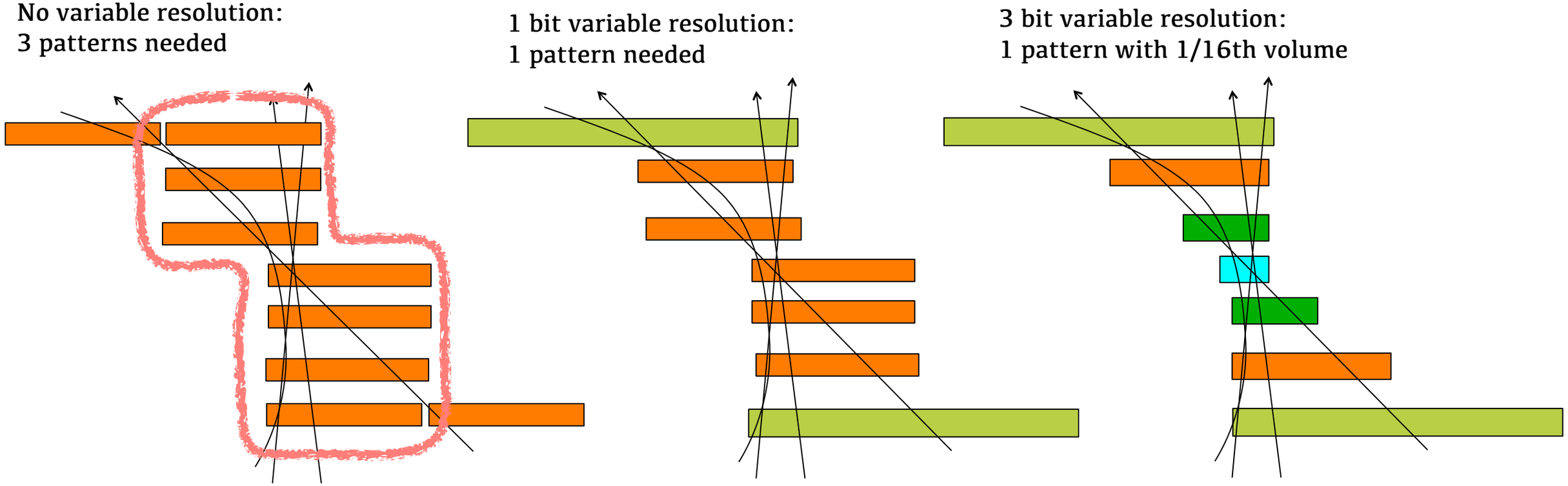

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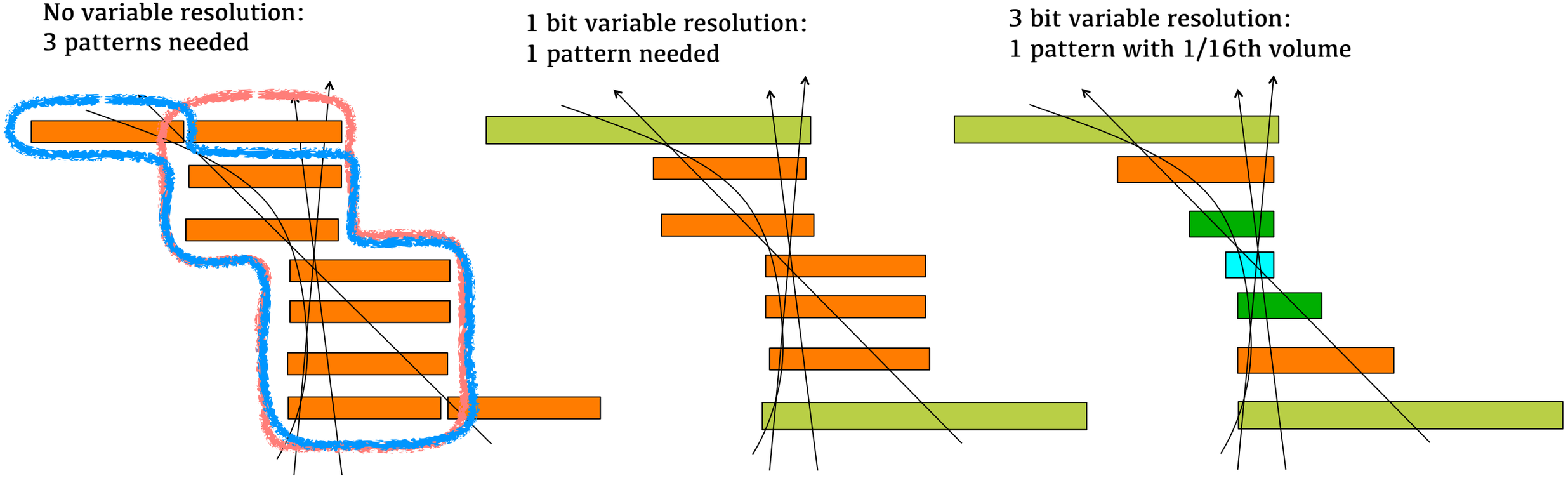

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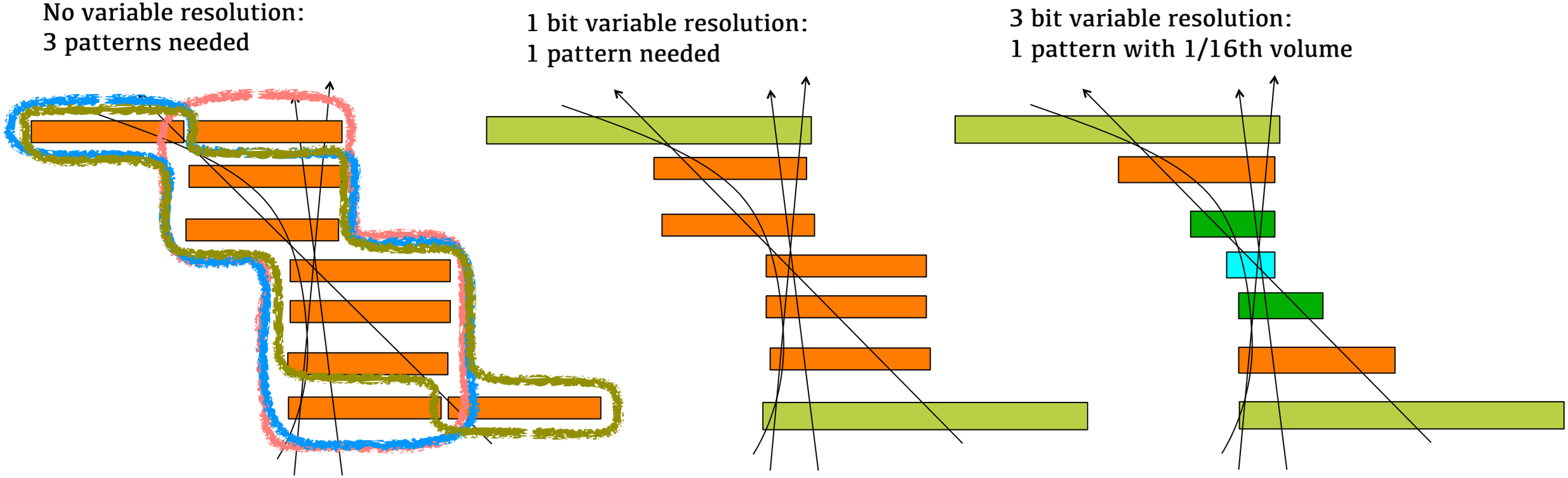

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AMCHIP 06 VITAL STATS

- 65 nm fabrication
- 60mm^2 area
- 2 Gb/s I/O
- 23x23 BGA
- 128k patterns, 400M transistors
- 1.15V, 3.3 A, 3.8 W / chip
- Several hundred chips tested so far, 85% yield

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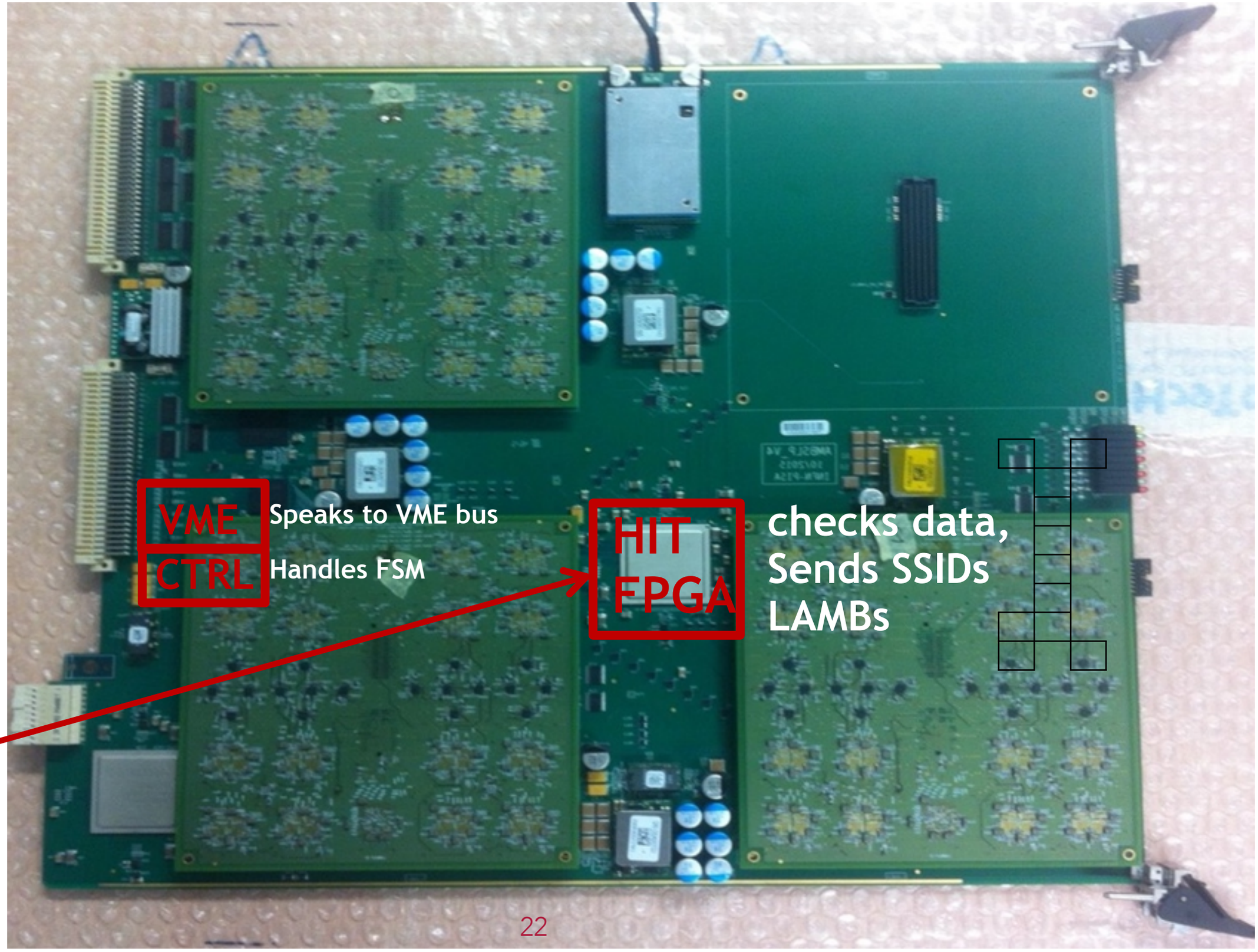
Iphone 6: A8 processor

20nm

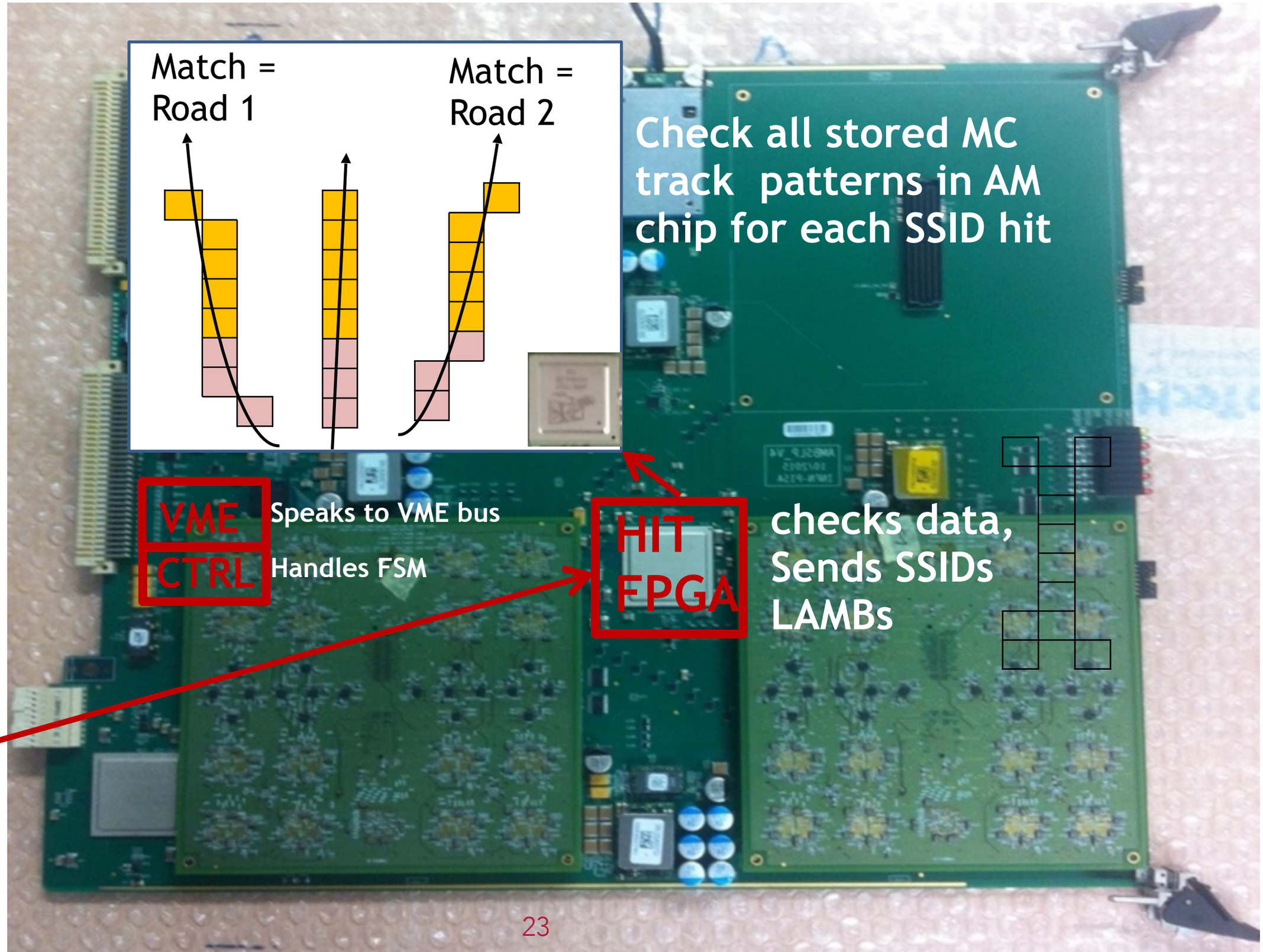
2B transistors

89 mm^2

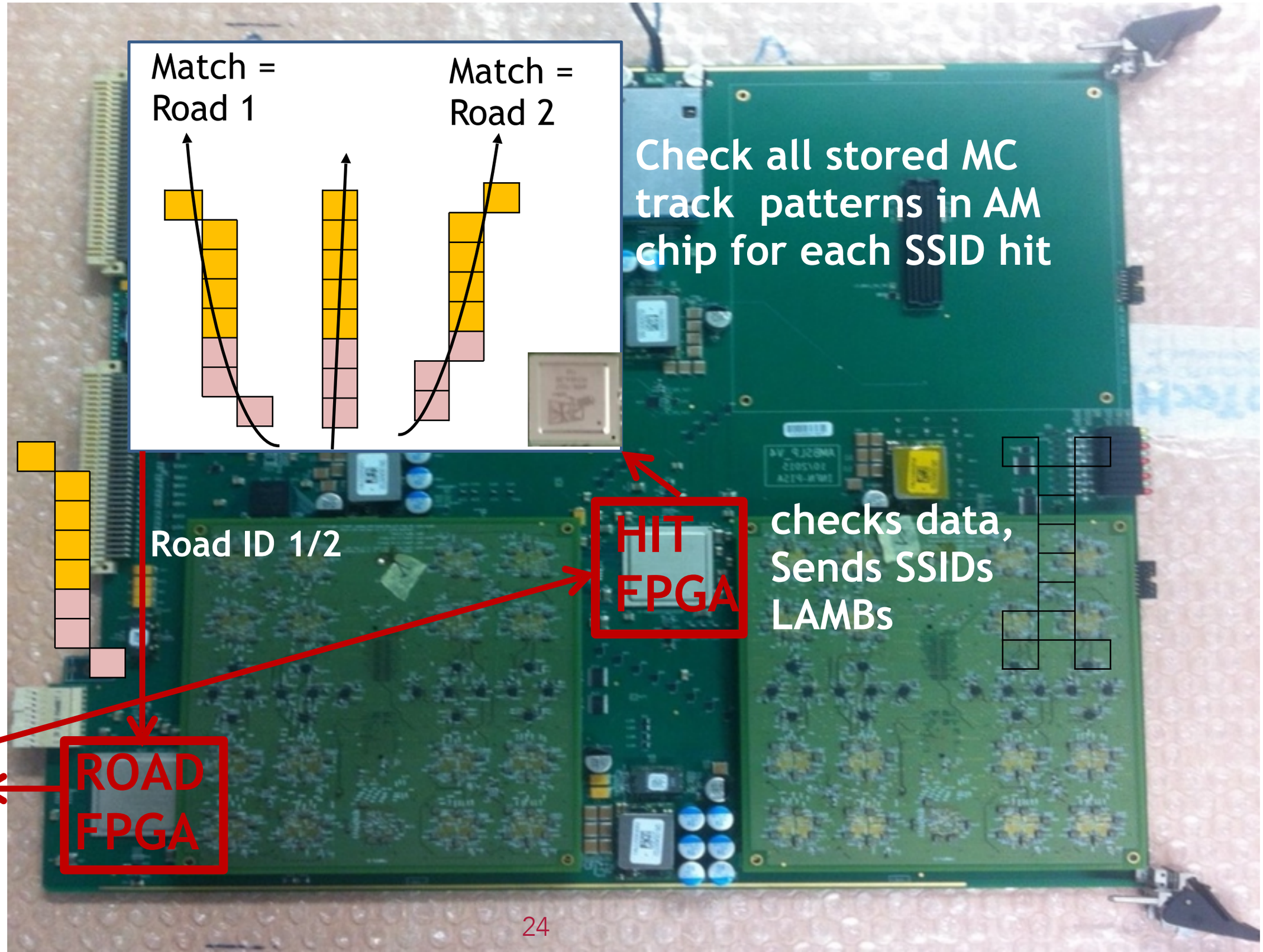
AMB BOARD


VME
CTRL
Speaks to VME bus
Handles FSM
HIT
FPGA
checks data,
Sends SSIDs
LAMBs
SS IDs
from AUX

AMB BOARD

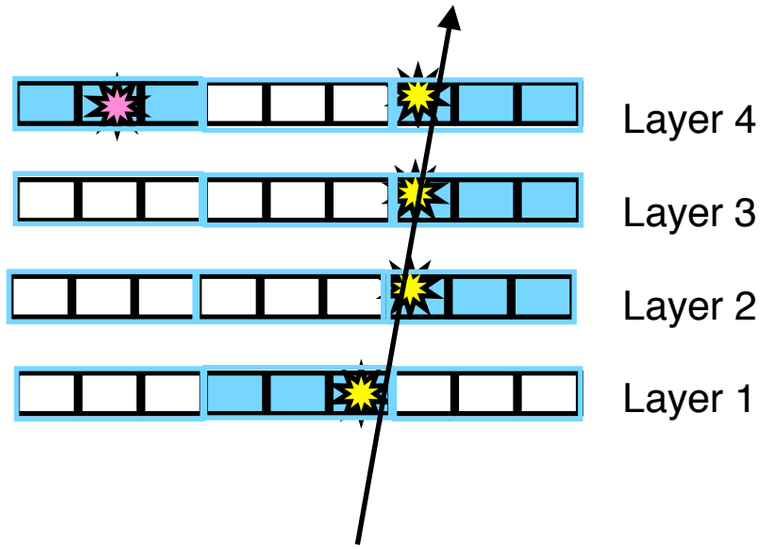

Match =
Road 1
Match =
Road 2
Check all stored MC track patterns in AM chip for each SSID hit
VME
CTRL
Speaks to VME bus
Handles FSM
HIT
FPGA
checks data,
Sends SSIDs
LAMBs
SS IDs
from AUX

AMB BOARD

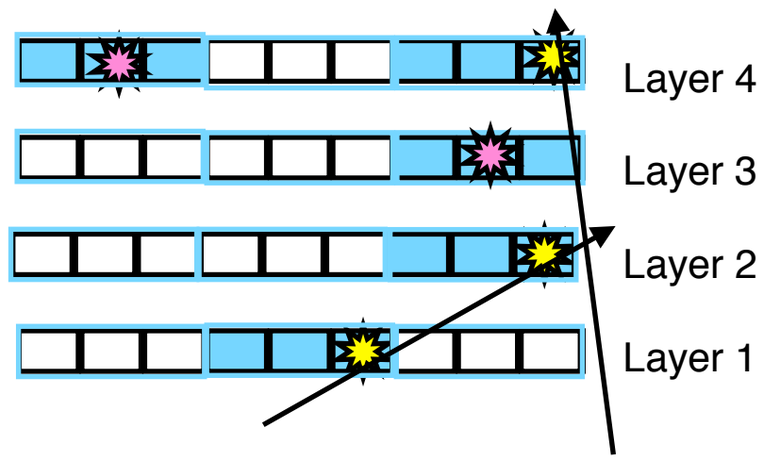

Match =
Road 1
Match =
Road 2
Check all stored MC track patterns in AM chip for each SSID hit
Road ID 1/2
HIT FPGA
checks data, Sends SSIDs LAMBs
SS IDs from AUX
Road IDs to AUX
ROAD FPGA

TRACK FITTING

- Problem: >90% of matched patterns (BINGOs) are from random association of hits

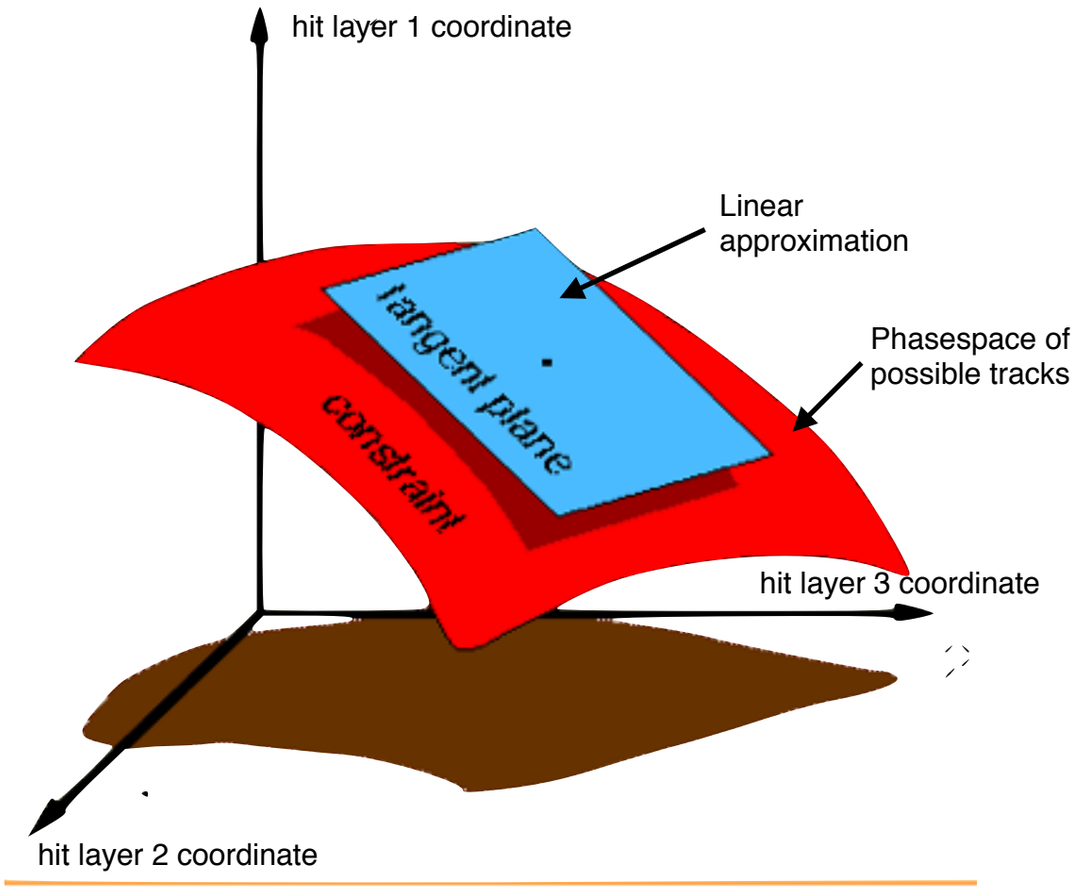


- Solution: check if **full resolution** hits in matched patterns are compatible with a single charged particle



5 PICOSECOND TRACK FITTING

- Linearized fits on FPGAs:
  - Determine phasespace of possible tracks (χ^2)
  - Linear approximation calculated and defined by sector
  - FPGAs multiply and add coordinates by constants to get χ^2
- Keep roads with at least 1 good track
- Fit 1 track / ns (1 track every 5 ps for full system)!



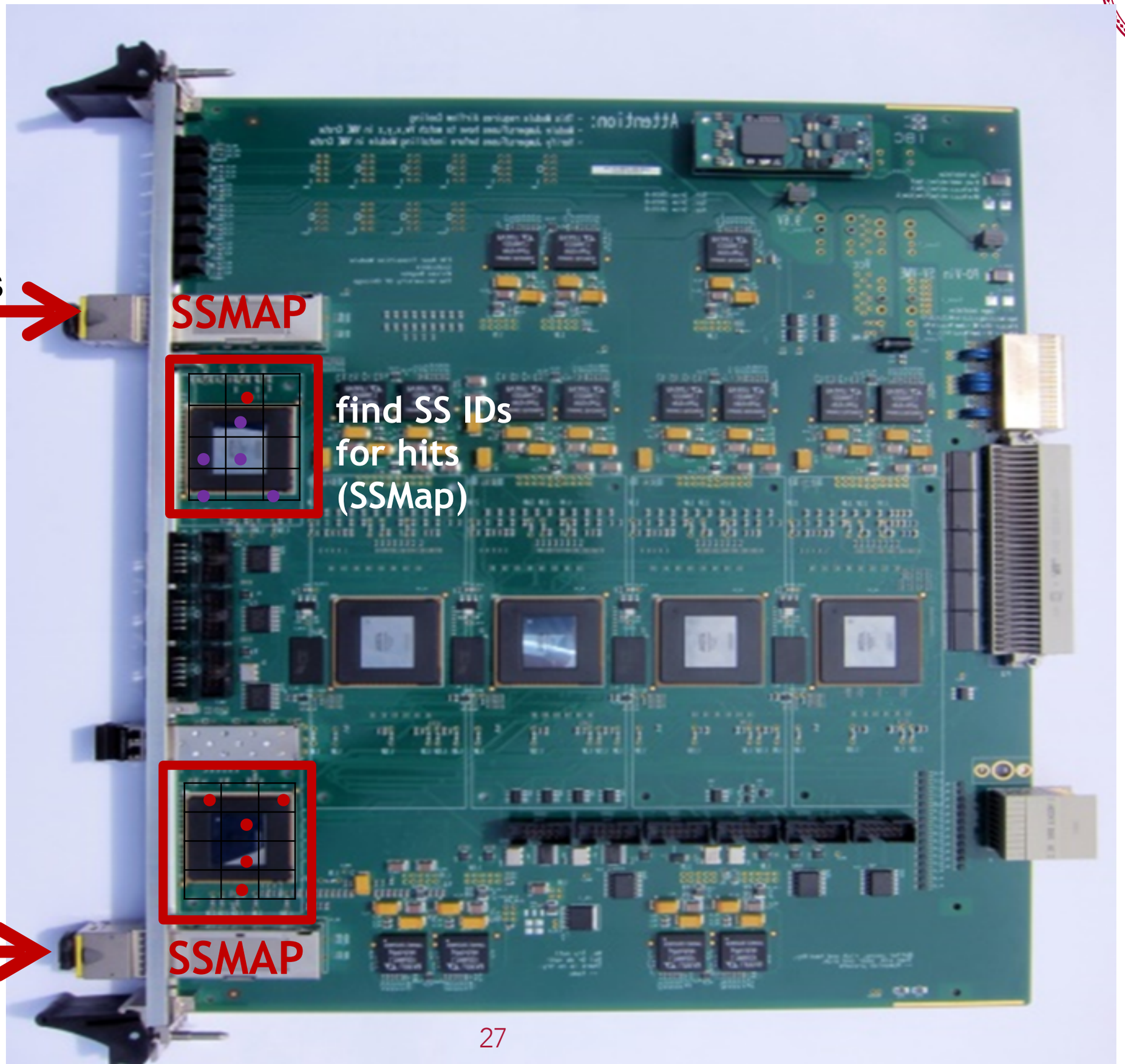
$$\chi_i = \sum_{j=1}^{N_c} S_{ij} x_j + h_i; i = 1, \ldots, N_\chi$$

AUX

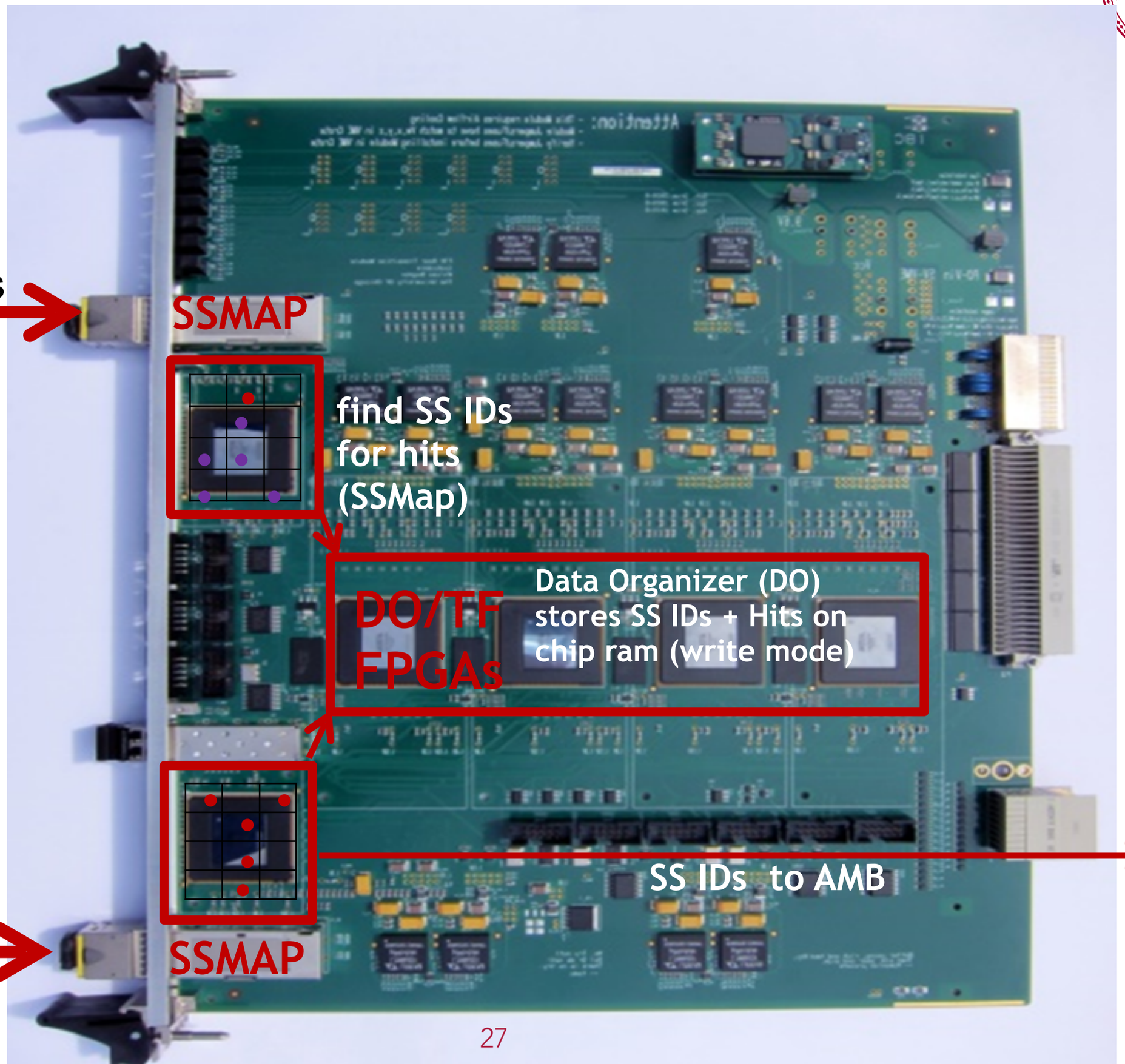
Pix/ SCT Hits from DF

Hits are ganged into groups of pixels/SCT modules called Super Strips (SS)

SCT Hits from DF



AUX



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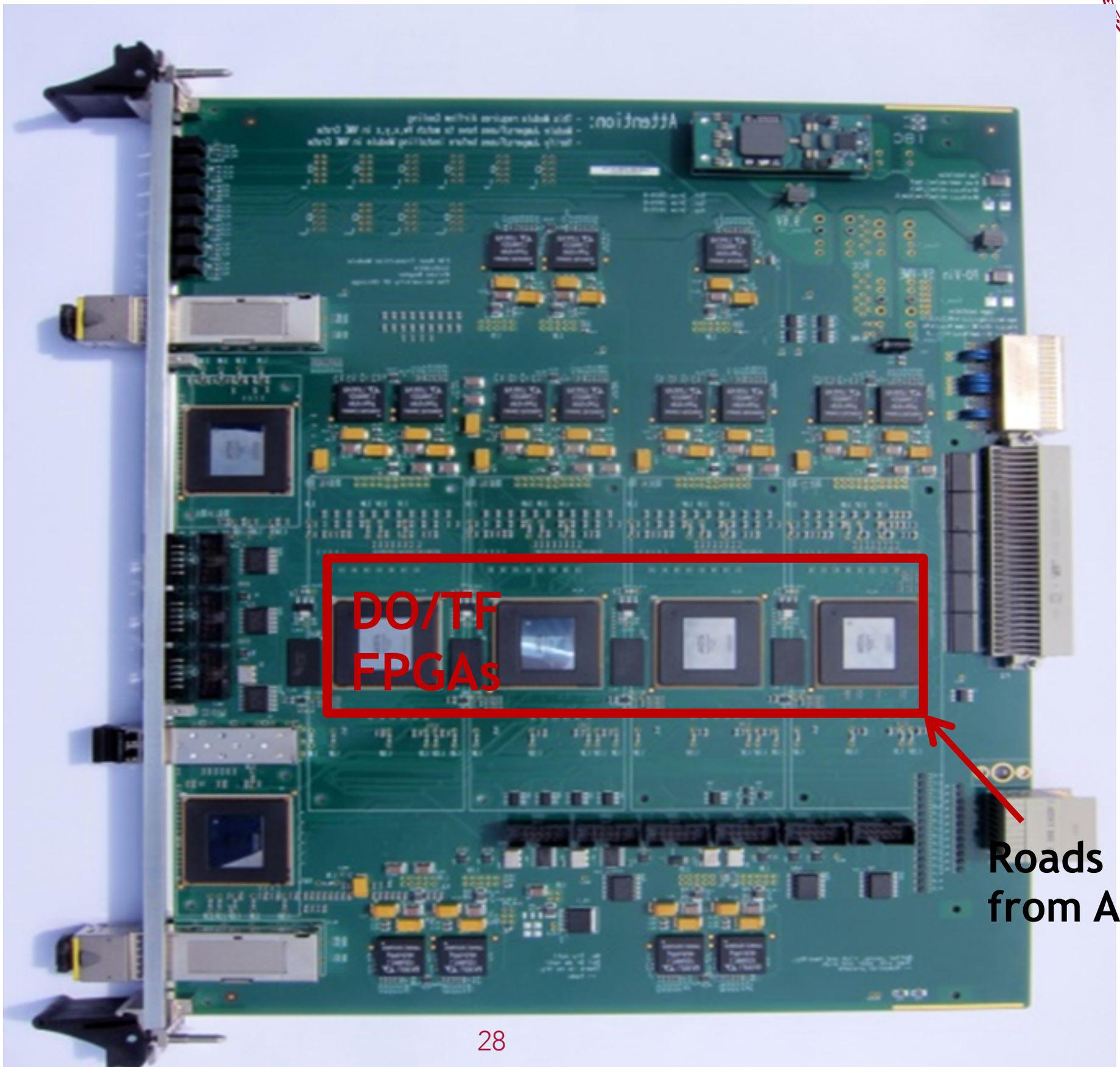
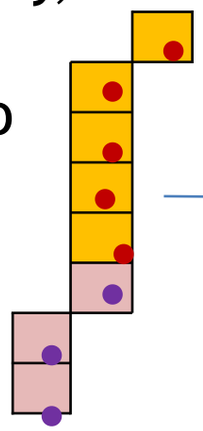


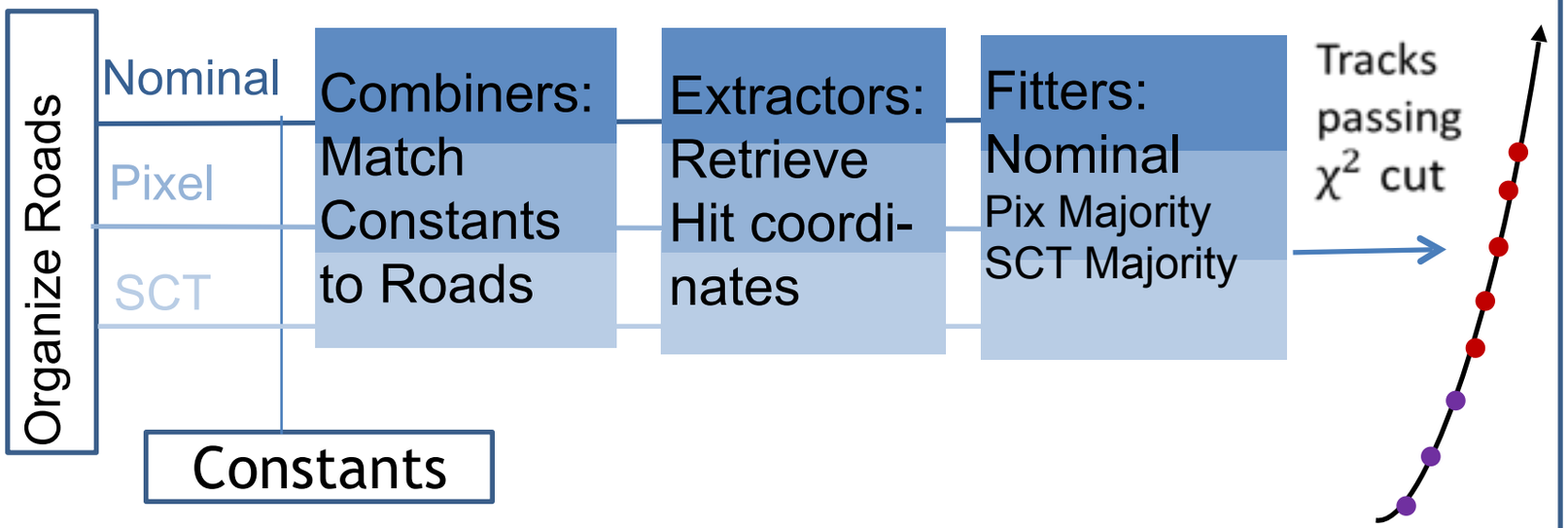
AUX

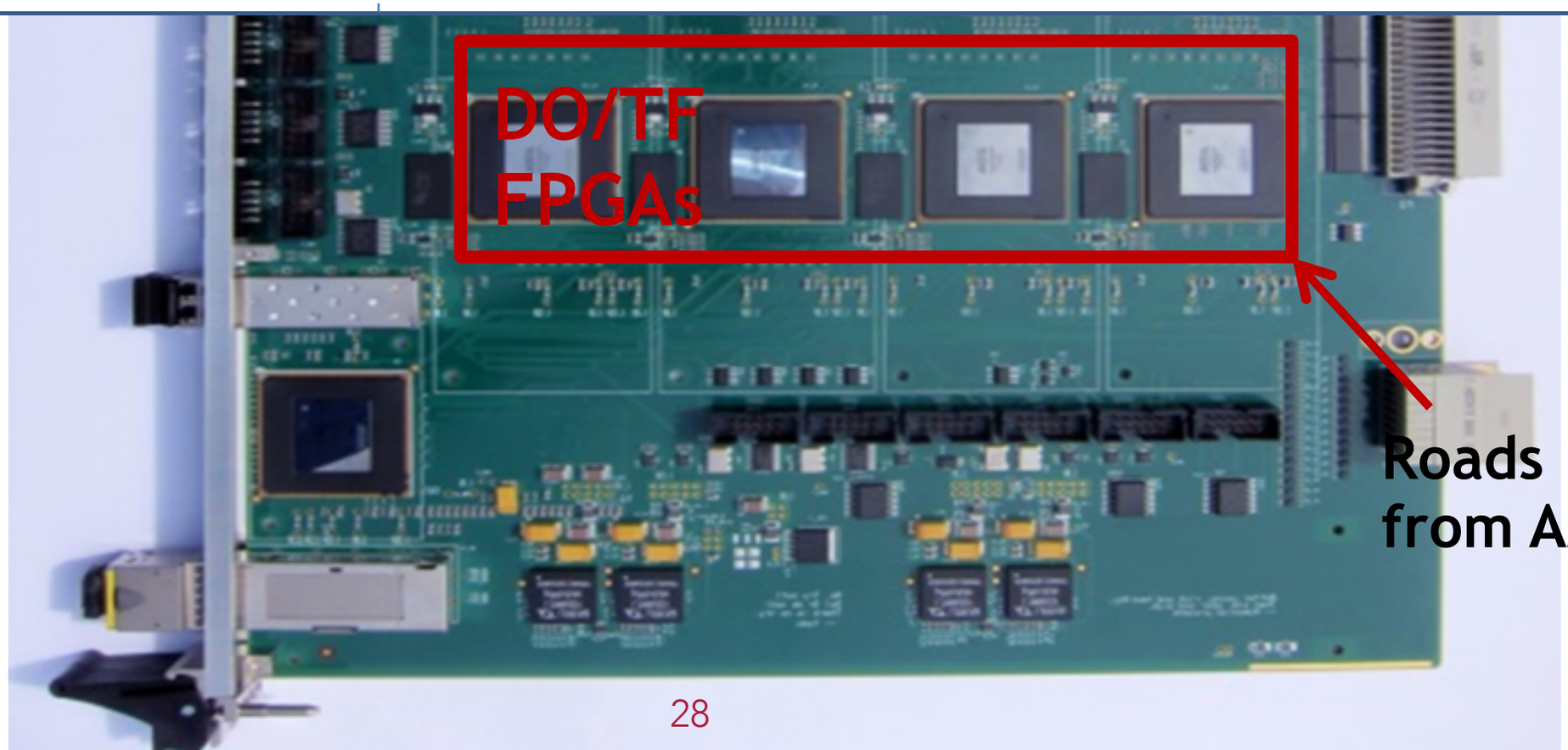
Data Organizer (DO) FW:
Associates roads to SS using ext. memory, sends hits to TF



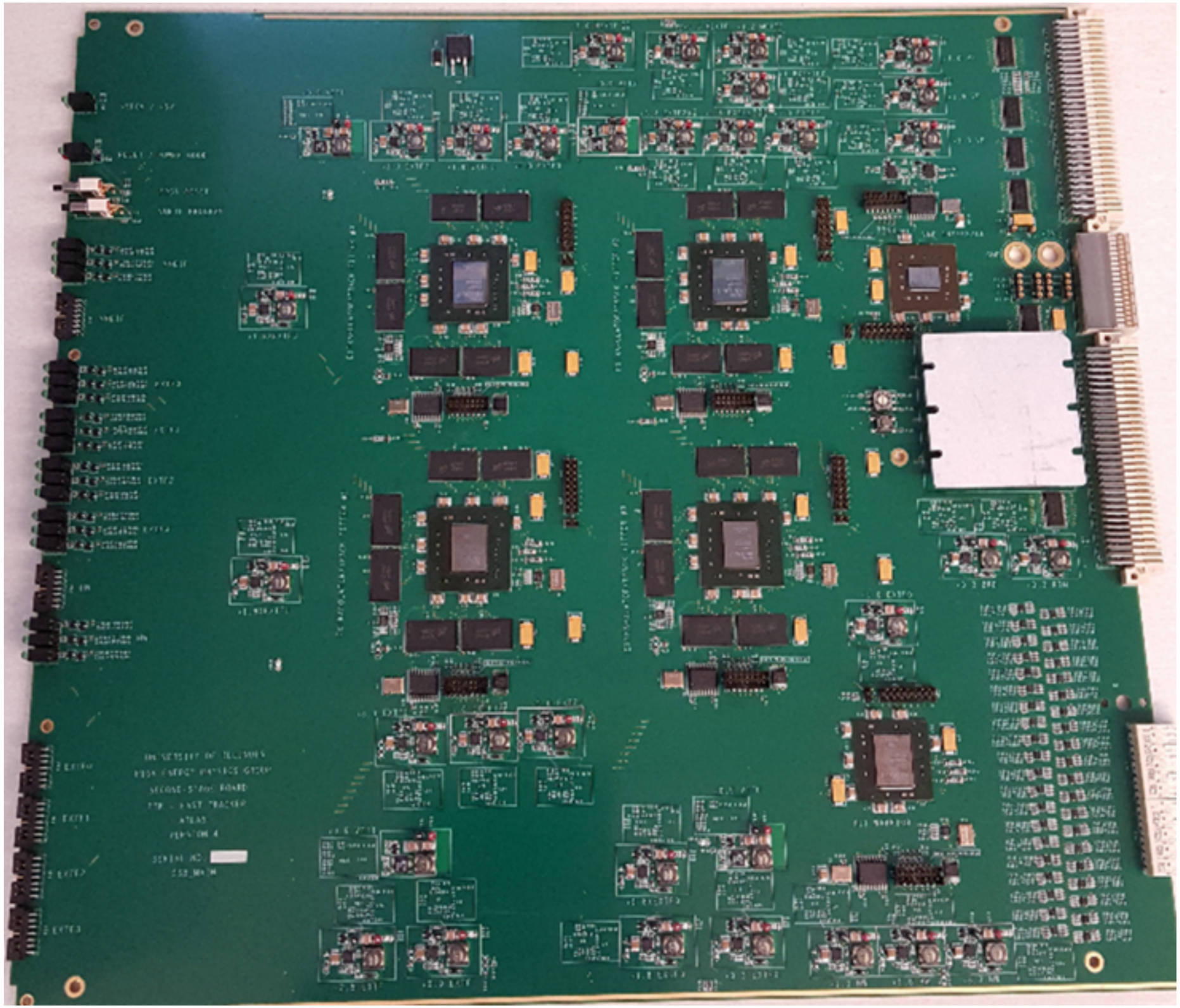
Track Fitter (TF) FW

Allows for 1 missing layer (Pix/SCT majority hit)





FINAL TRACK PRODUCTION



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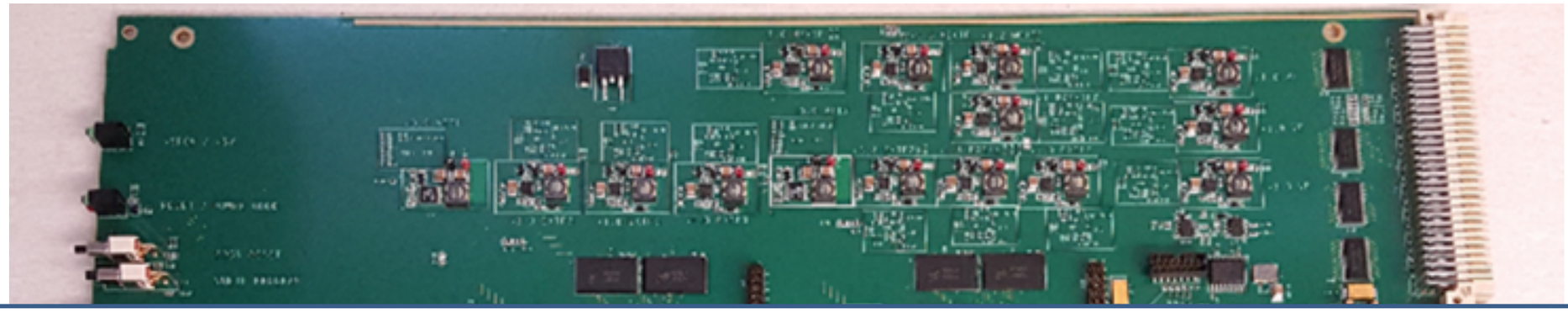
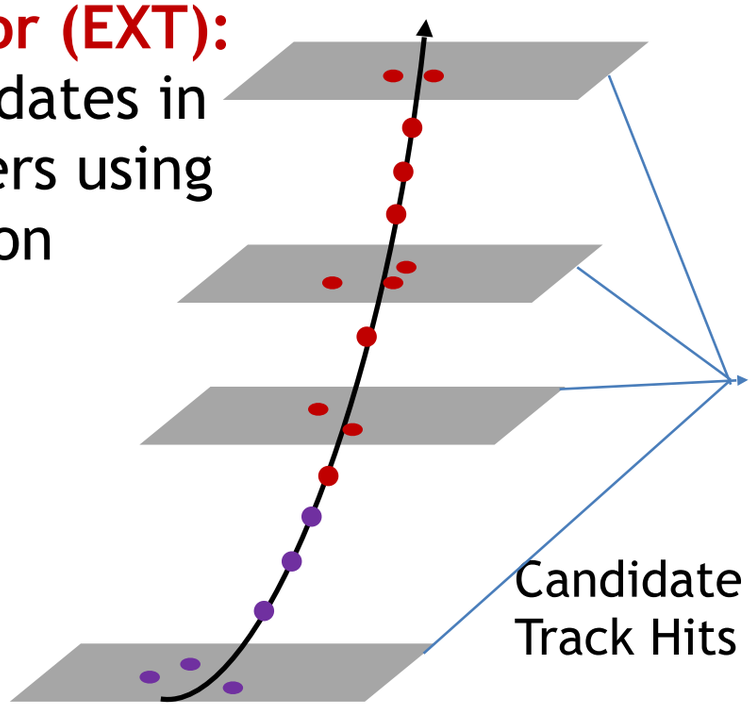
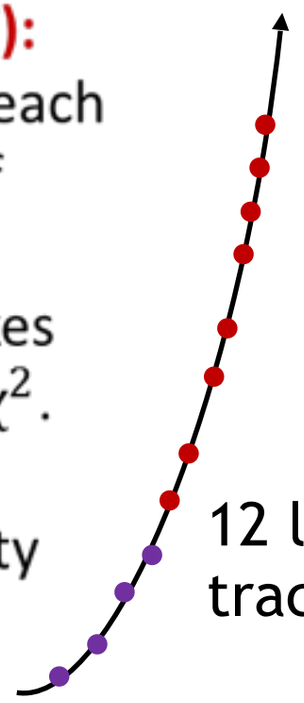
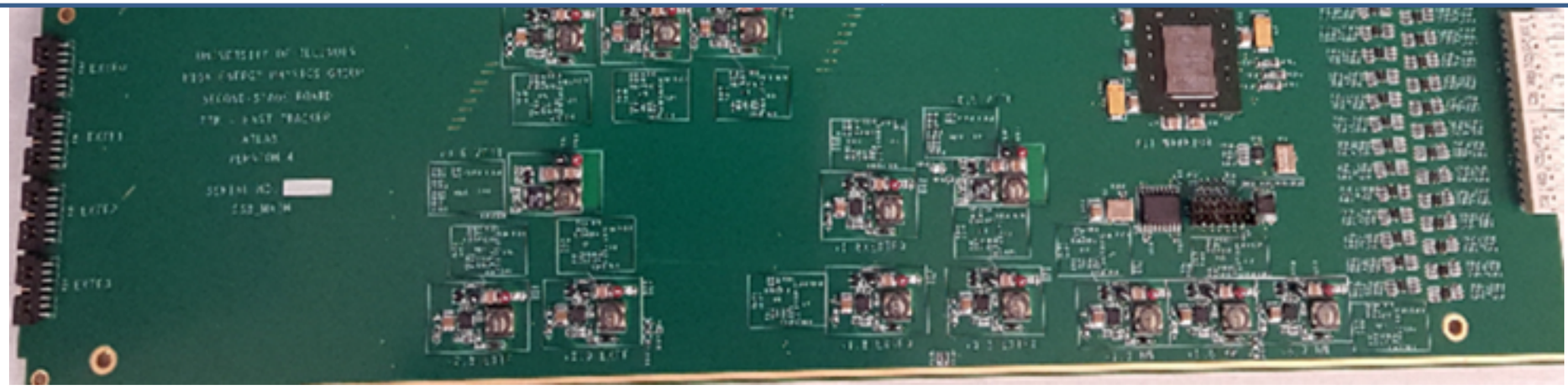


Extrapolator (EXT):
Finds candidates in unused layers using extrapolation constants



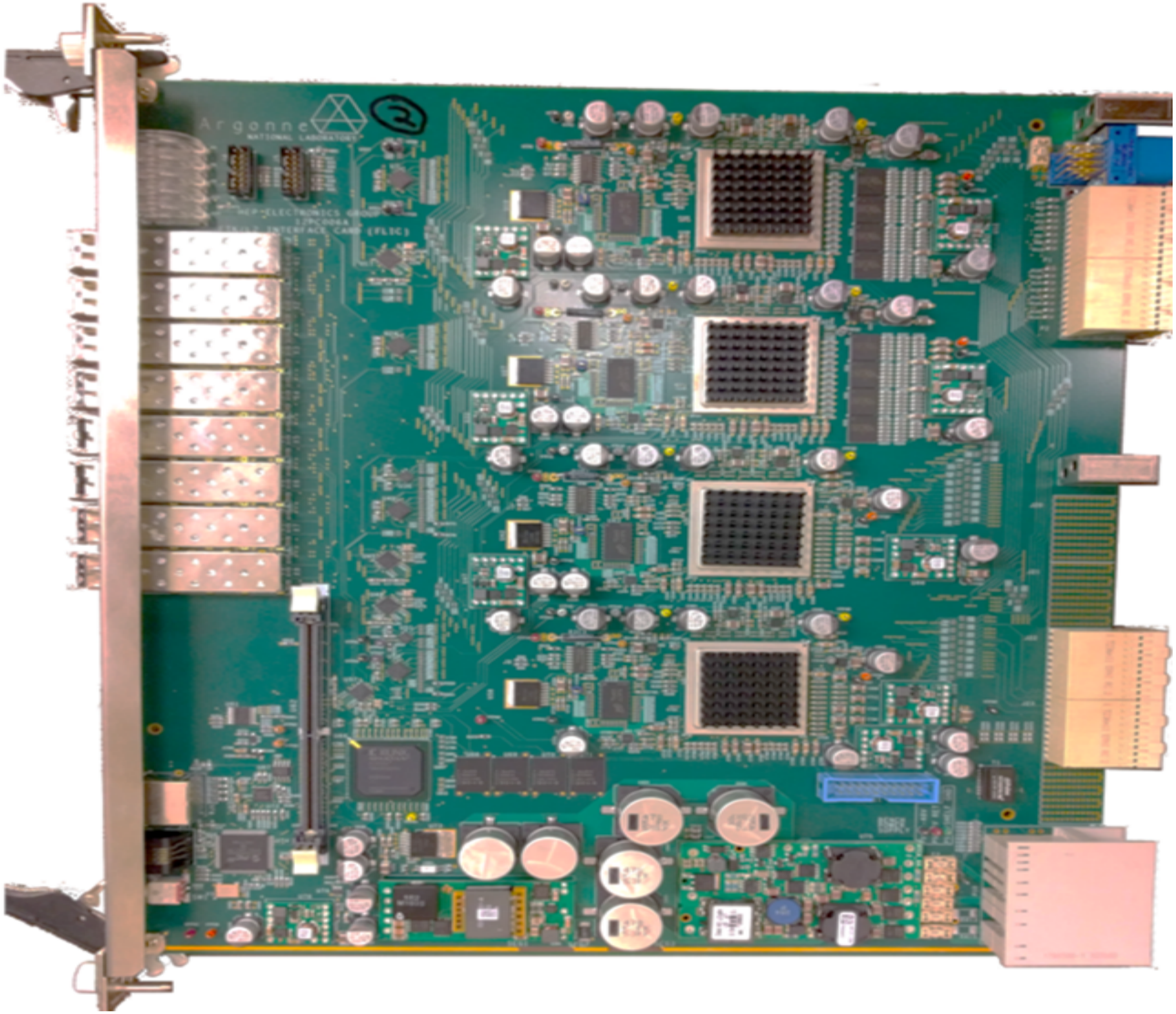
Track Fitter (TF):
Fits track with each combination of possible candidates, takes one with best χ^2. (Nominal and Pix/SCT Majority Fitters)



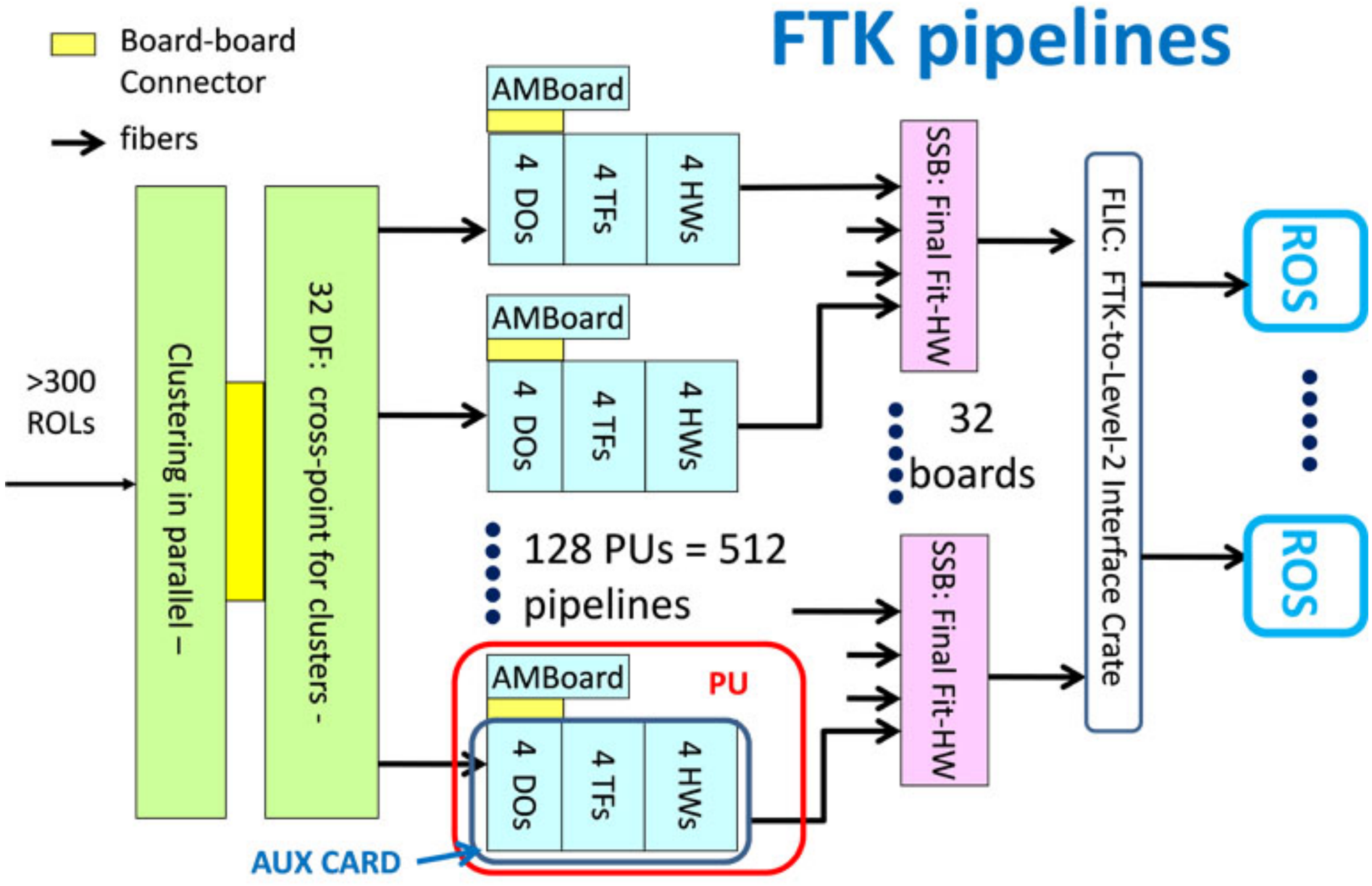


FORMAT FOR HLT: FLIC

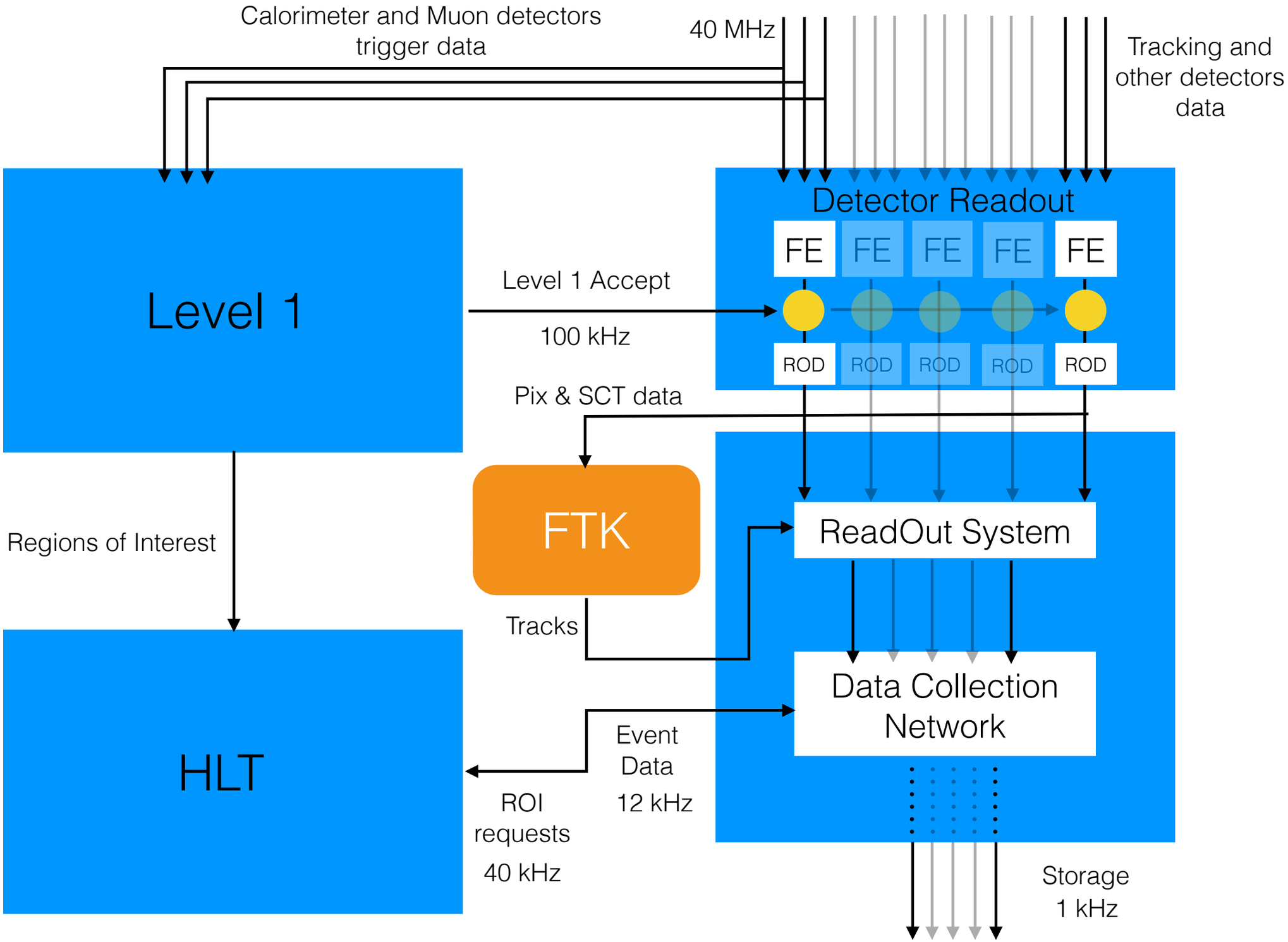
- Merge into event packets
- Include/strip debug & monitoring information



AS A SYSTEM


FTK pipelines
Board-board Connector
fibers
>300 ROLs
Clustering in parallel –
32 DF: cross-point for clusters -
AMBoard
4 DOs
4 TFs
4 HWs
AMBoard
4 DOs
4 TFs
4 HWs
128 PUs = 512 pipelines
AMBoard
PU
4 DOs
4 TFs
4 HWs
AUX CARD
SSB: Final Fit-HW
32 boards
SSB: Final Fit-HW
FLIC: FTK-to-Level-2 Interface Crate
ROS
ROS

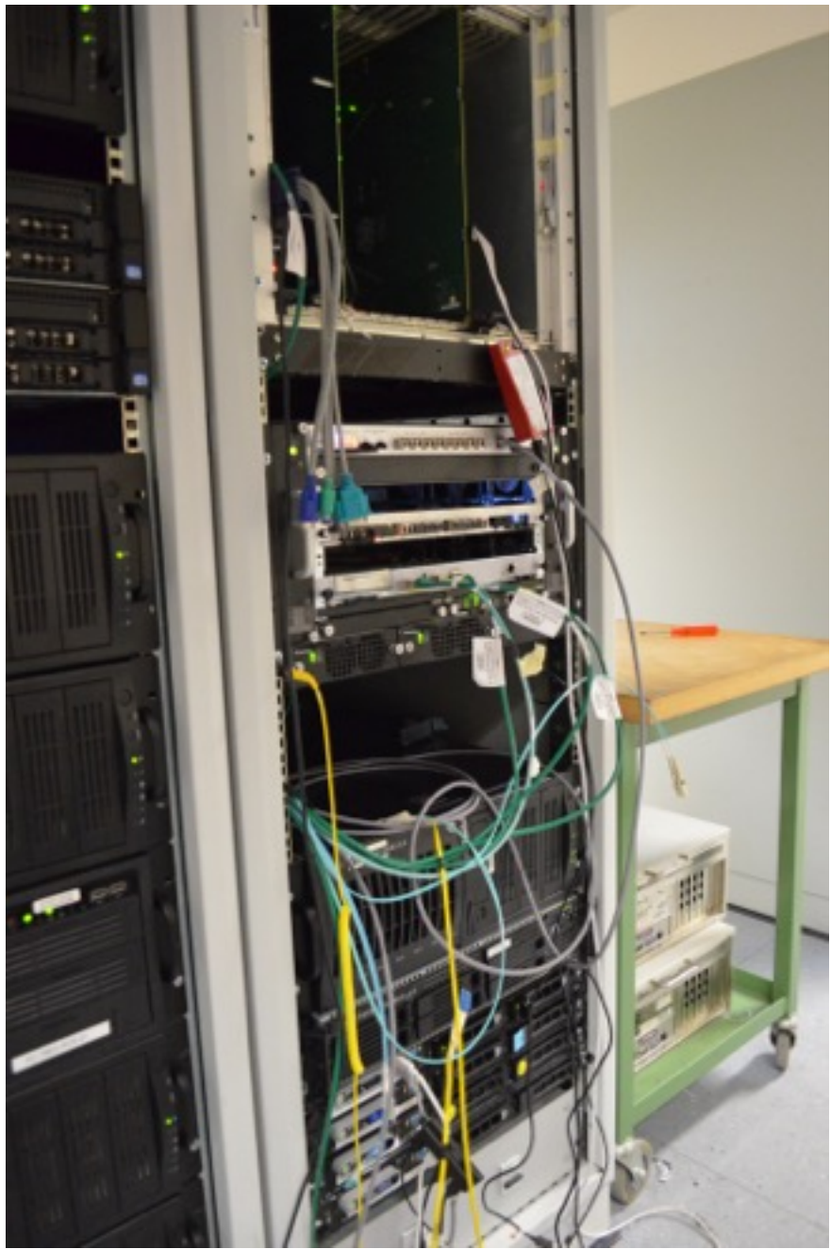
WHERE DOES IT FIT IN?

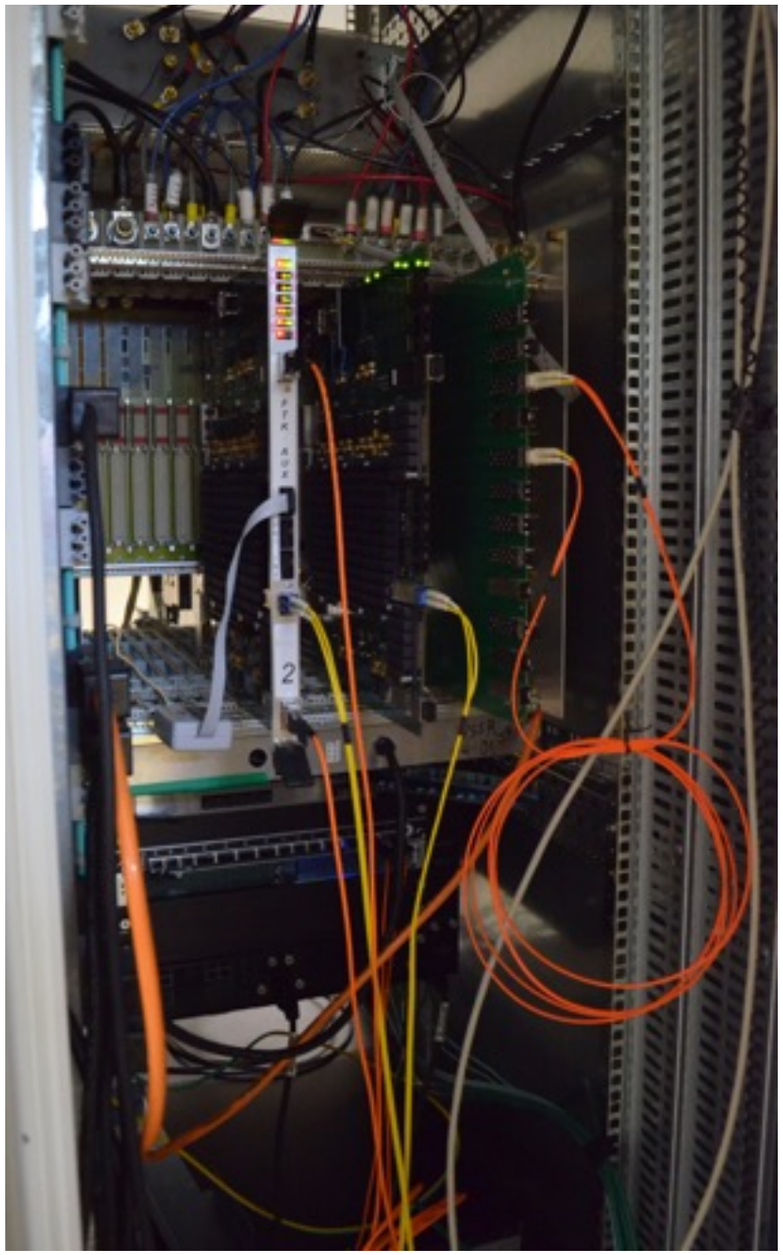


HOW FAR ALONG THE ROAD TO REALITY ARE WE?

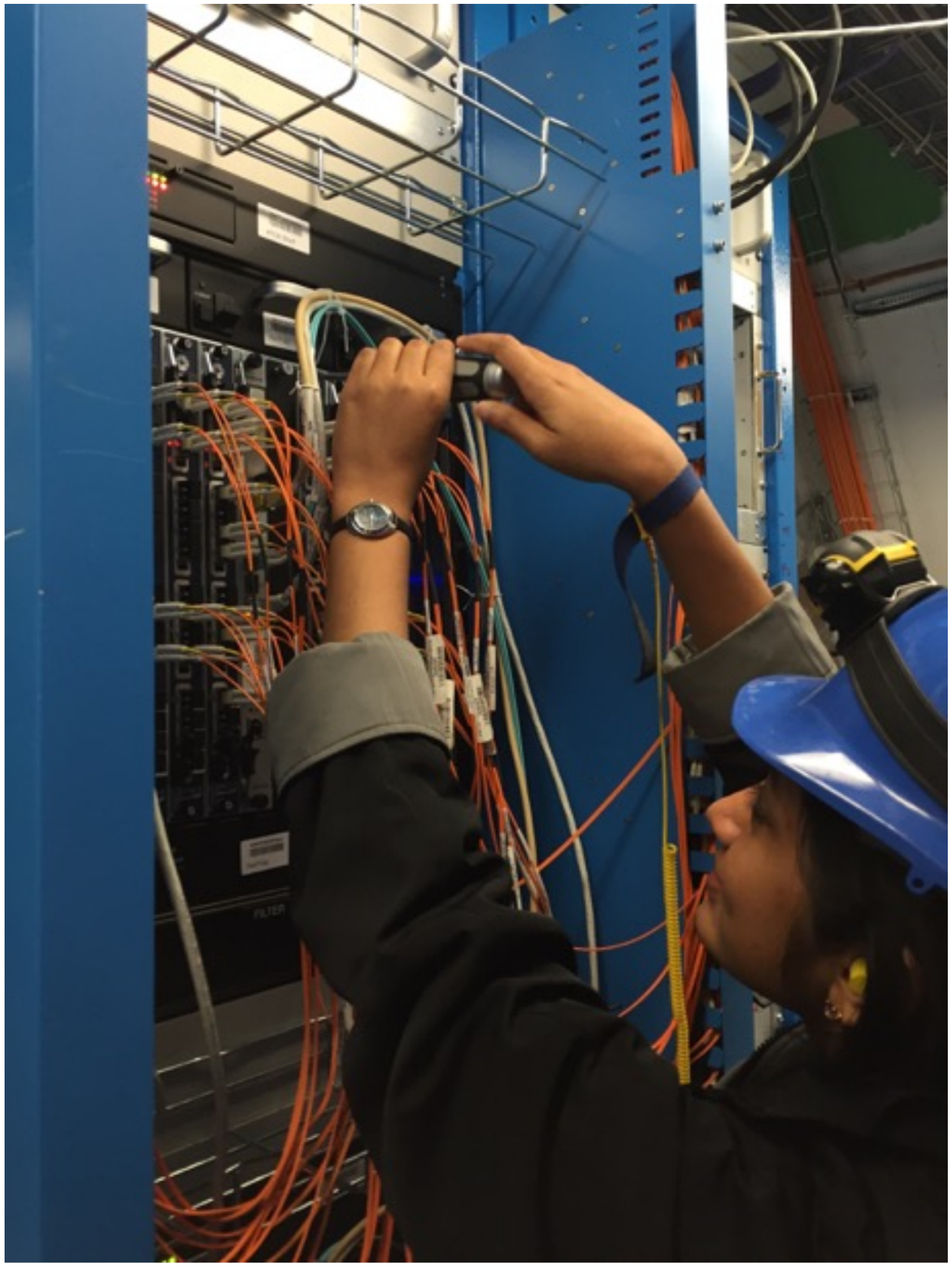
- Initial production of all boards started
  - Some delays for AMB and SSB
- At least one prototype or production board for each board available at CERN for integration tests
- Installation in USA 15 started!
  - One slice including IM+DF+AUX+AMB
  - One full DF Shelf installed*

TEST STAND FOR INTEGRATION @ CERN

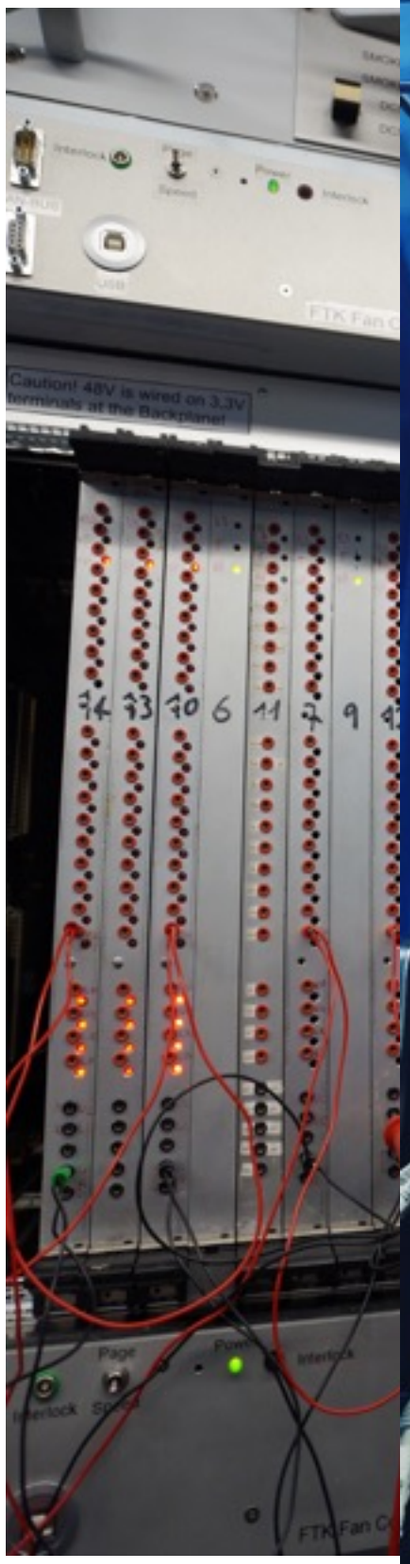




INSTALLATION IN THE COUNTING ROOM

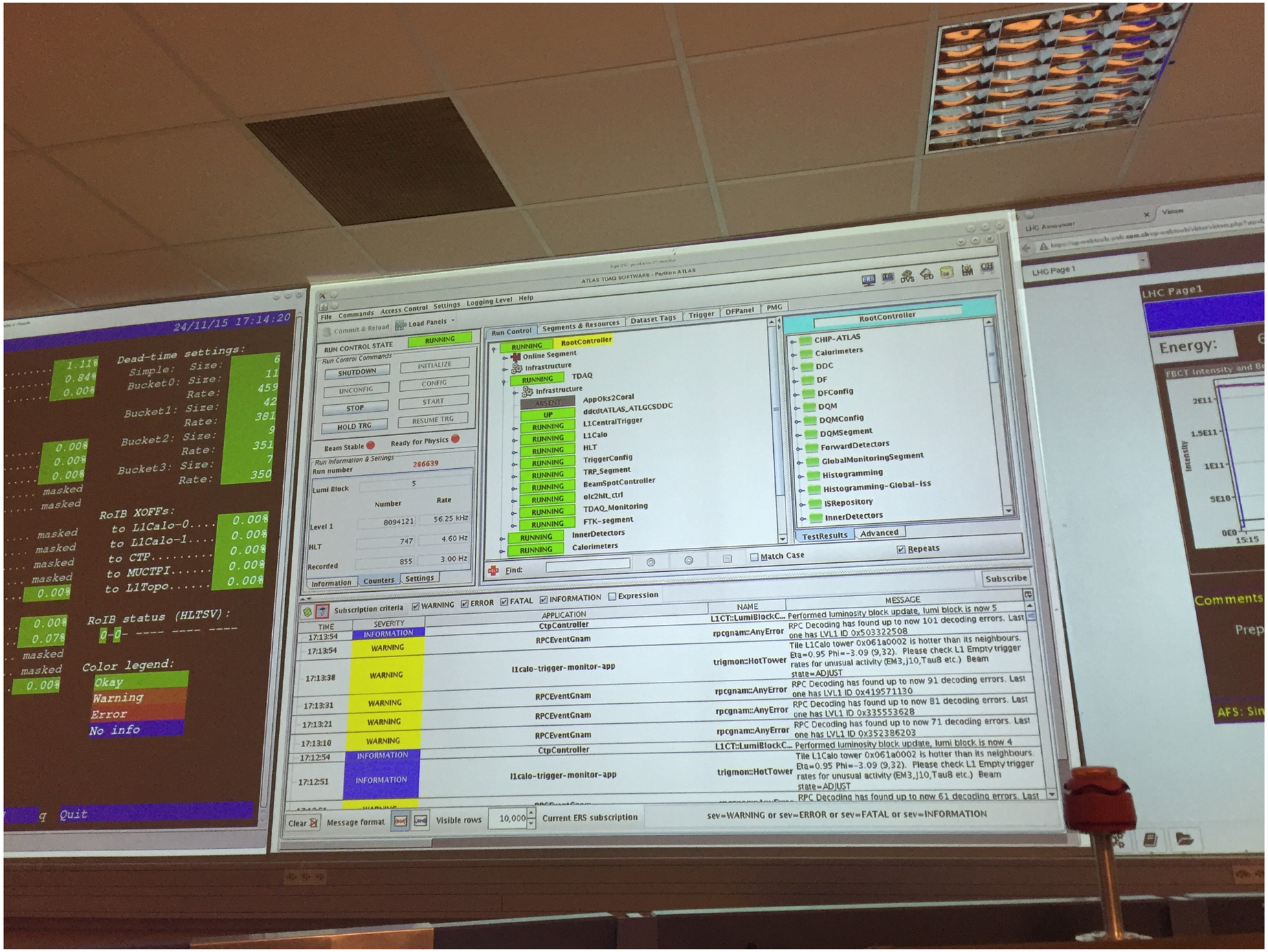


INSTALL OM

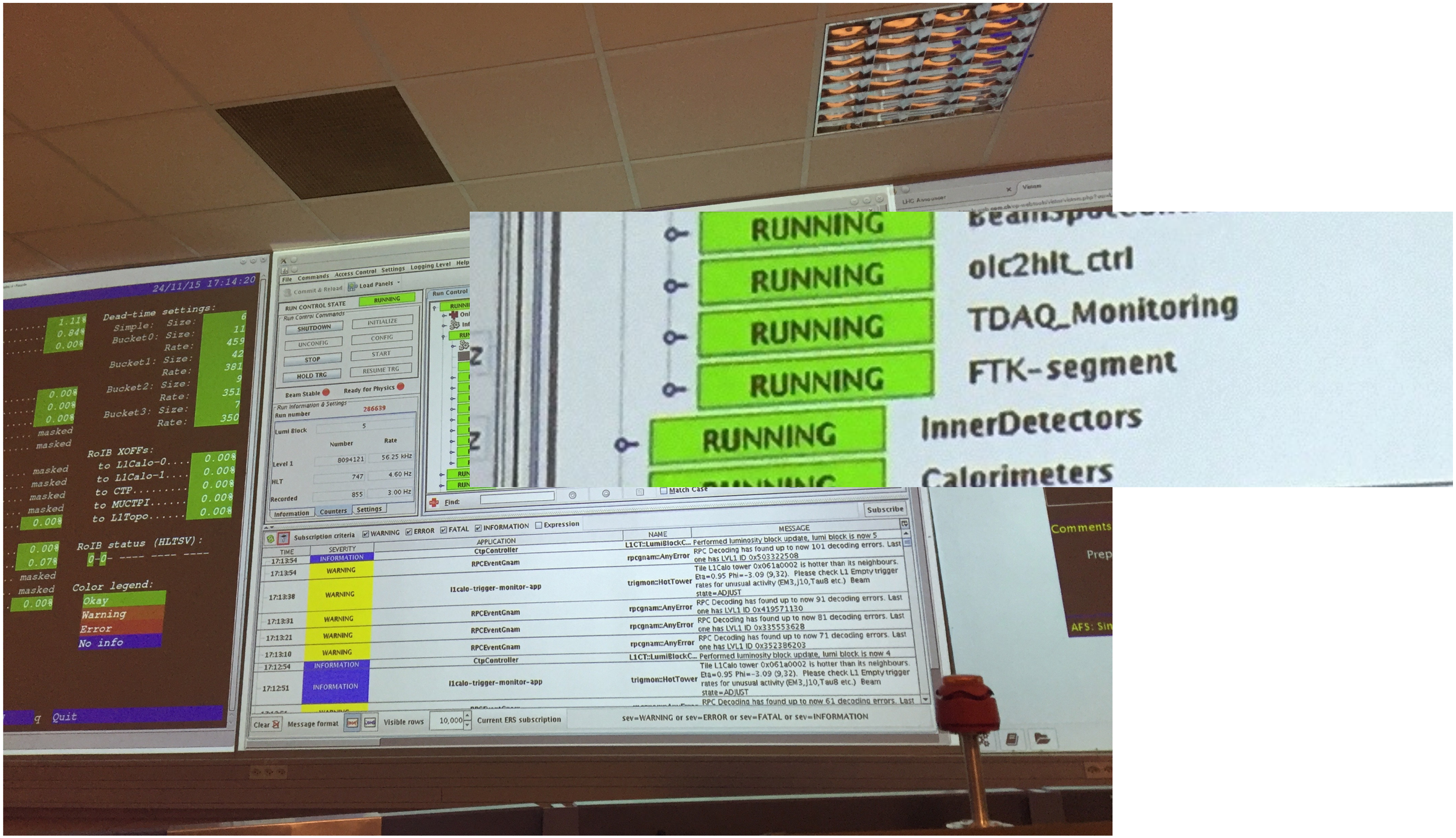

Caution! 48V is wired on 3.3V
terminals at the Backplane!
14 13 10 6 11 7 9
Page
Power
Interlock
Interlock
Speed


ATCA Shelf
ATCA F125

DATA TAKING DURING HEAVY ION COLLISIONS



DATA TAKING DURING HEAVY ION COLLISIONS



CHALLENGES

- Delays in production due to manufacturing issues (AMChip 06, Second Stage Board)
- Infrastructure:
  - New(ish) technologies: ATCA
  - Power consumption in VME racks & limited cooling capacity (14-15kW/rack)
  - Integration into ATLAS DAQ chain (talking to Pix/SCT & ROS)
- Firmware planning/stability/completion
  - Done by students & postdocs with finite institutional lifetimes
- ***Integration of such a heterogenous system!***

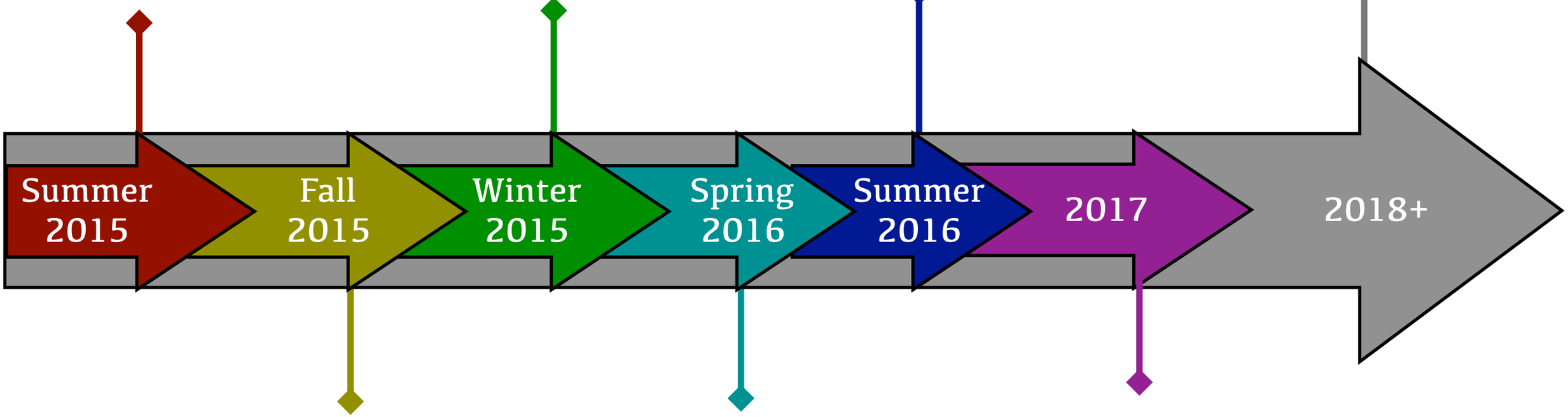
FTK SCHEDULE

First production boards arrive

First integration into ATLAS data stream

Barrel system installed, commissioning starting

Full processing power



Design reviews complete*

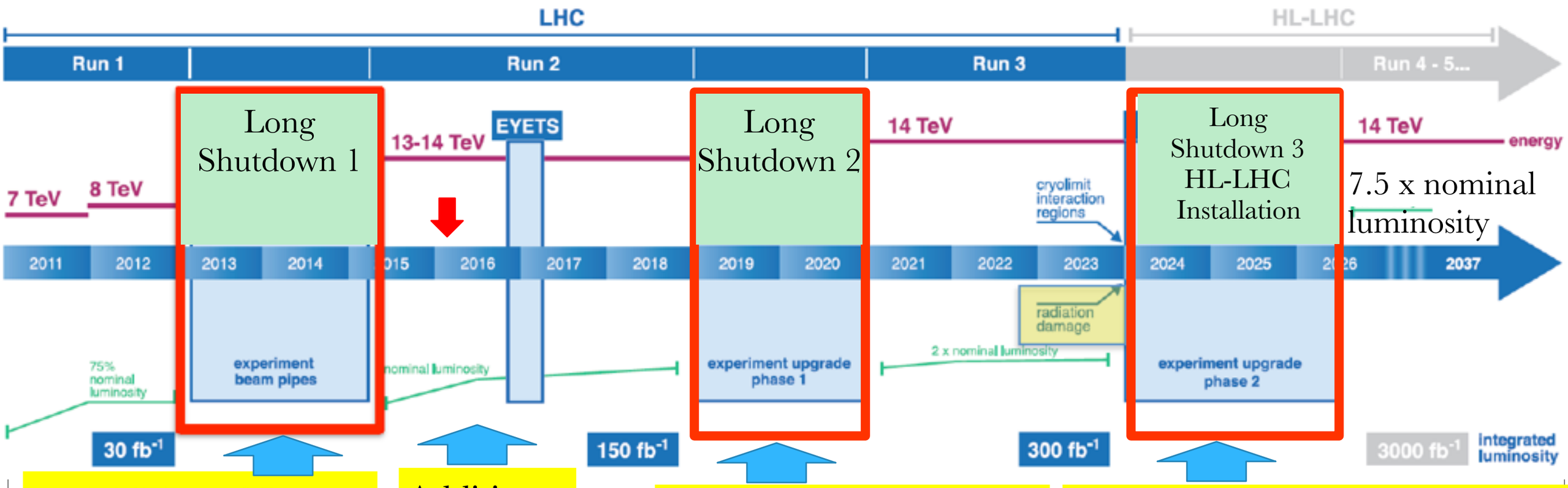
Input/Output Systems Commissioned

Full detector coverage

PLANNING FOR THE FUTURE

THE FUTURE IS NOW

LHC & High Luminosity LHC

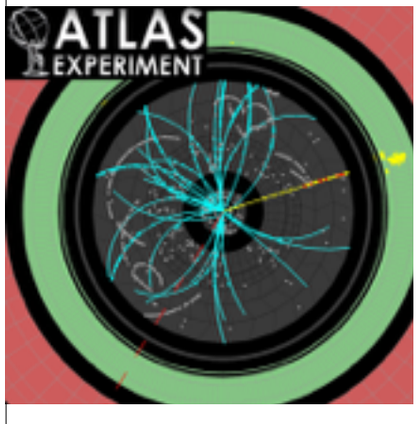


- Addition of Inner pixel layer (IBL)
- Trigger Upgrades

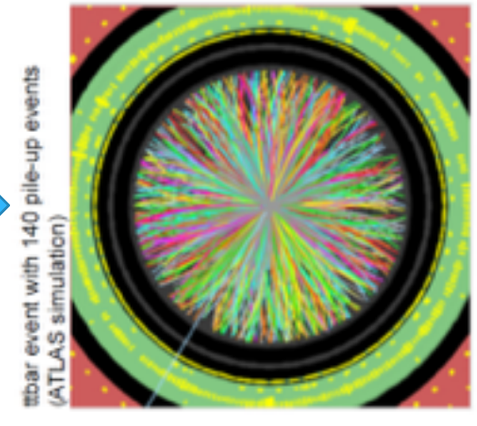
Addition of FTK

Further trigger upgrades
- Concurrent processing on many-core cpu (+ accelerators)

Upgraded ATLAS Detector incl.
- Replacement of Inner Tracker
- Upgraded Trigger



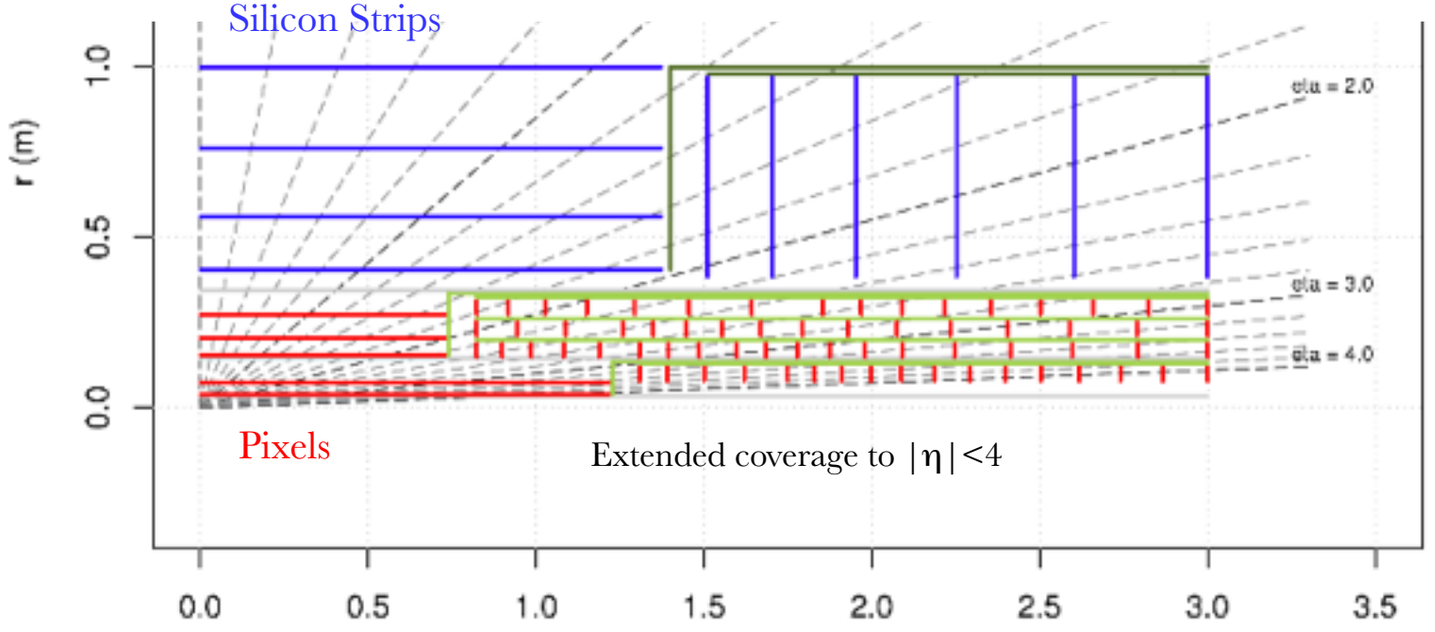
FTK: Fast TracKer: hardware based tracking

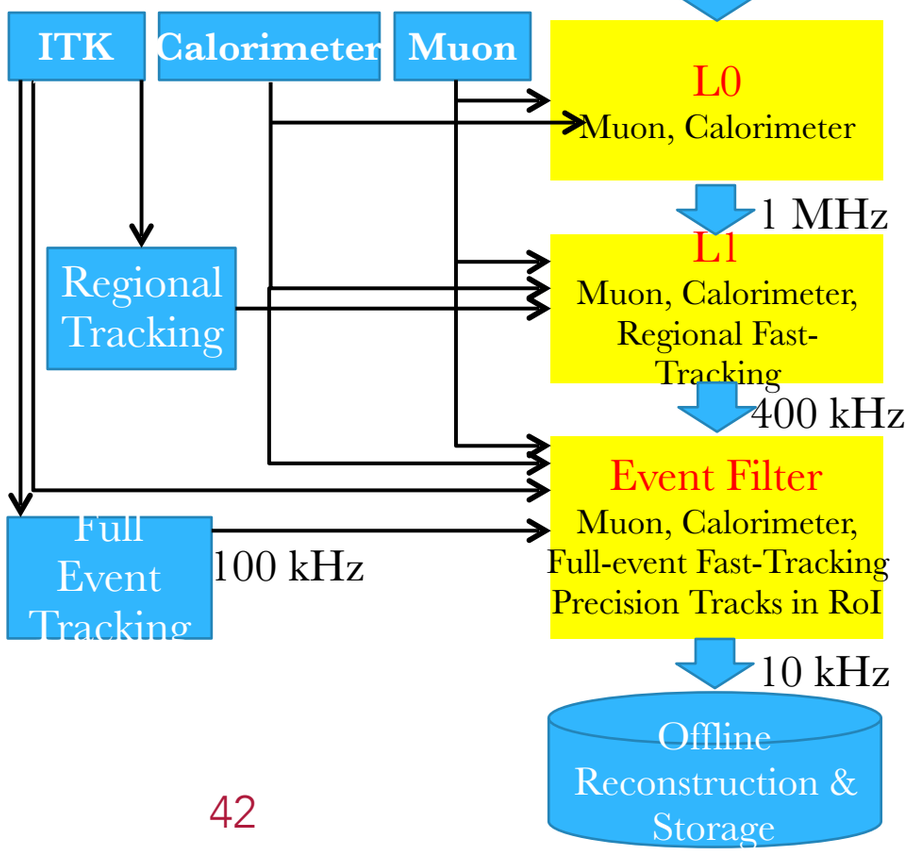


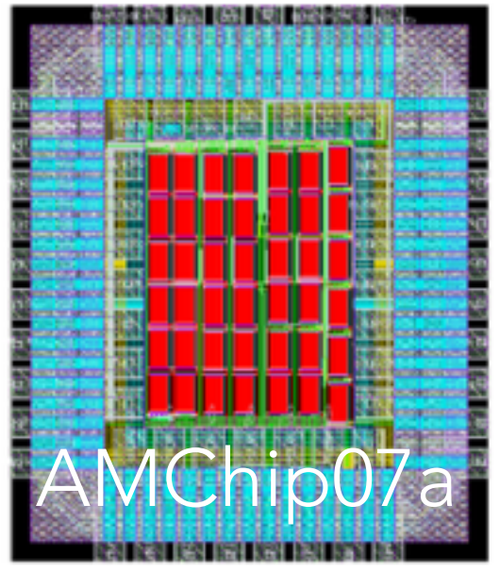
First W->eν 7 TeV collision data.

TRACK TRIGGERING AT HL-LHC

- L=7.5x$10^{34}$$cm^{-2}s^{-1}$, 200 pile-up events
  - ~10 times current highest luminosity
- Critical to measure Higgs couplings, including Higgs self coupling!
- Tracking strategy:
  - Hardware Tracking in RoI at up to 1 MHz
    - AM+FGPA technology
  - Hardware Full Event Tracking at ~100 kHz – selected events: FTK++
    - AM+??
  - CPU/GPU precision tracking in ROI

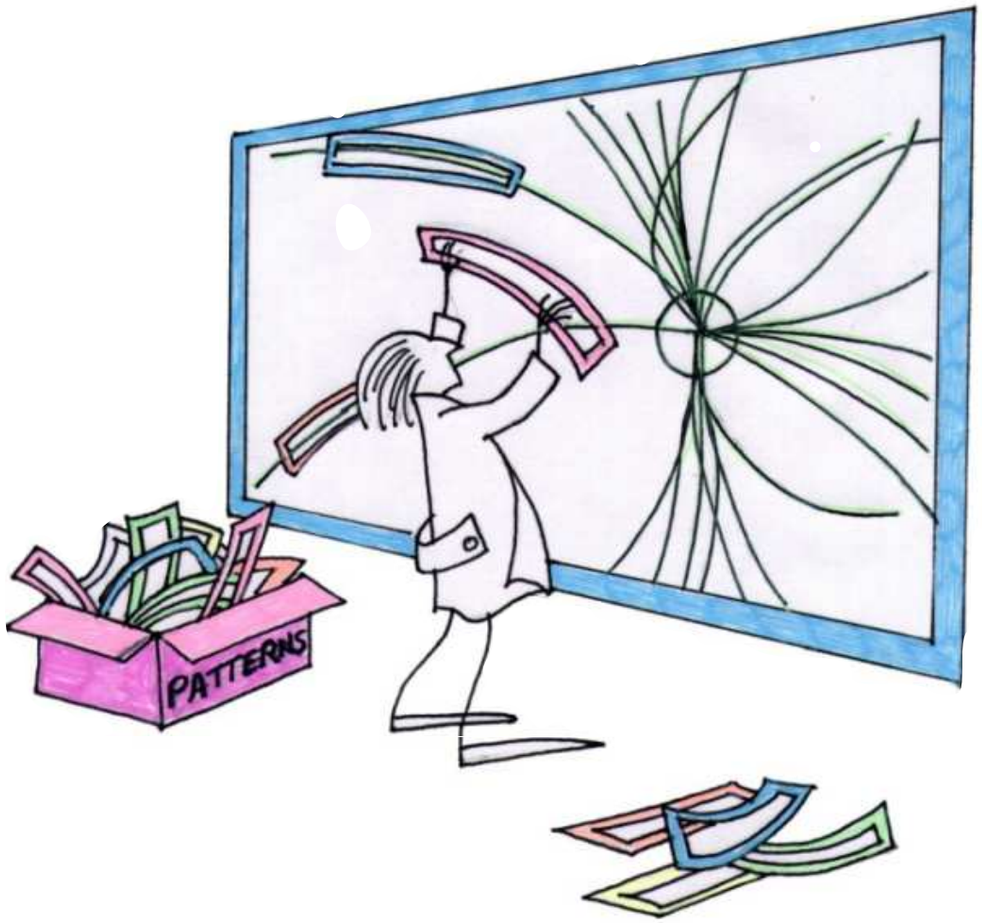




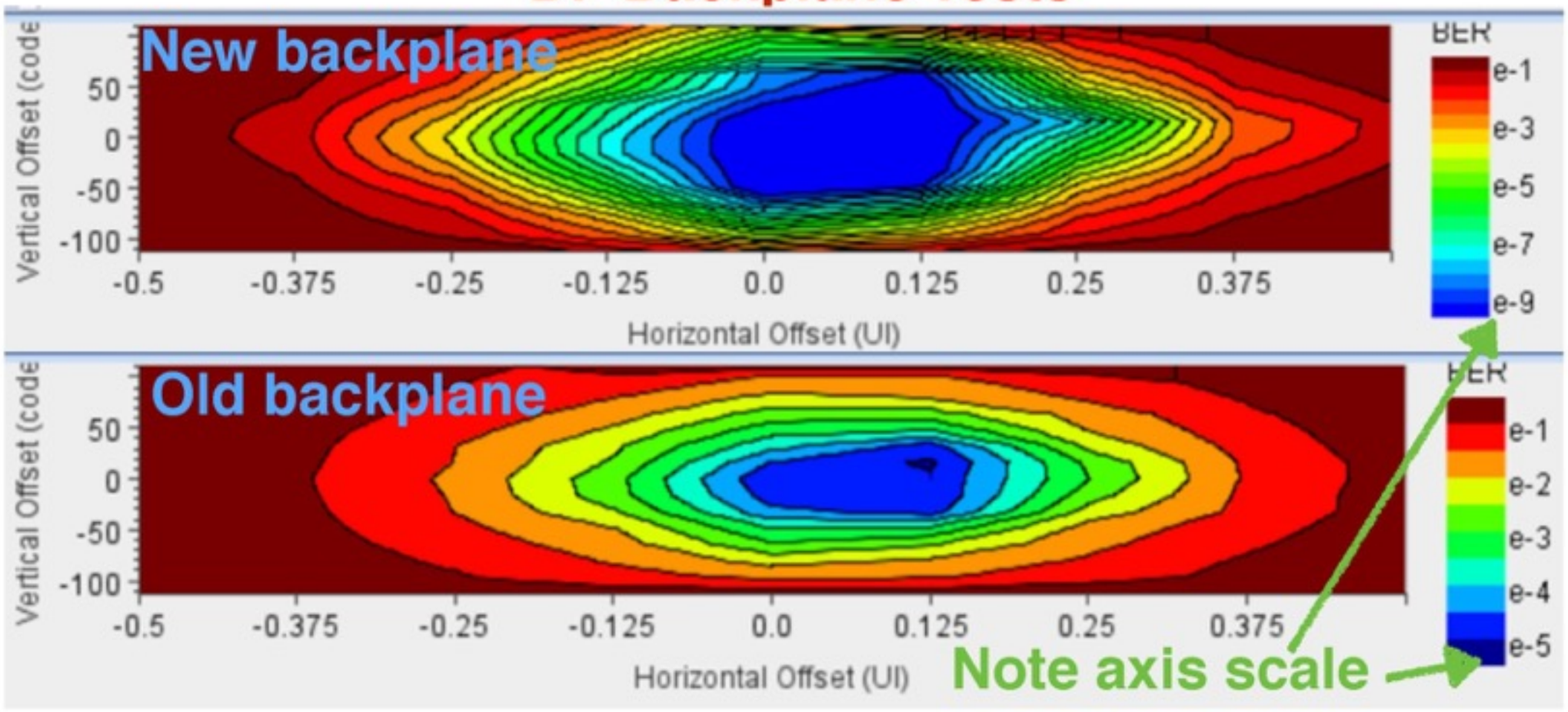


CONCLUSIONS

- LHC Run II & III will have a lot of challenging and exciting physics to be explored
  - Using tracking information in the trigger will increase our sensitivity to heavy flavor objects
- FTK uses a hardware solution to solve the problems of tracking at high luminosity
  - Good performance with respect to offline tracking
  - Trigger chains under development
- Commissioning in 2016, usage in HLT in 2017.



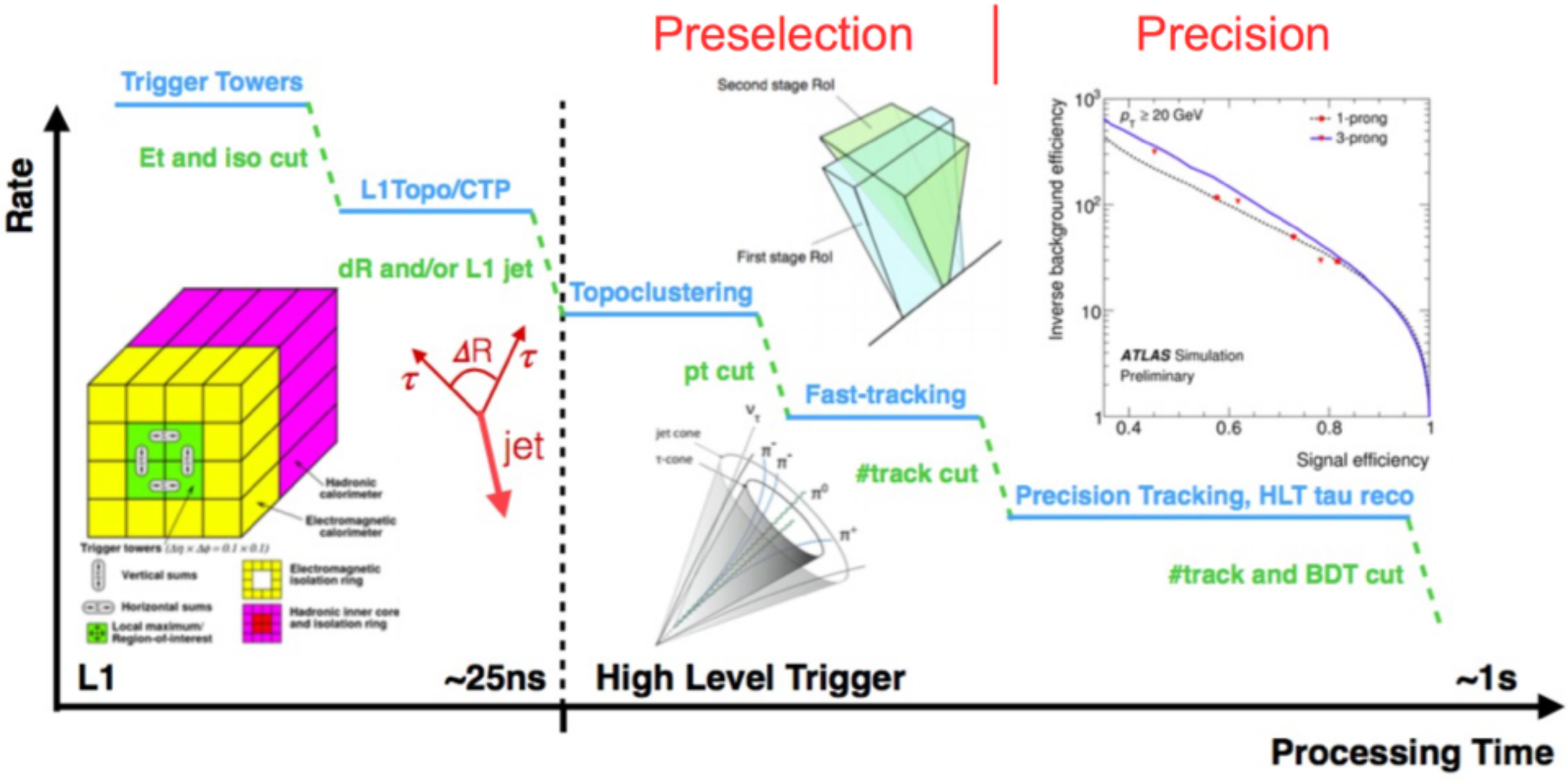
DF Backplane Tests

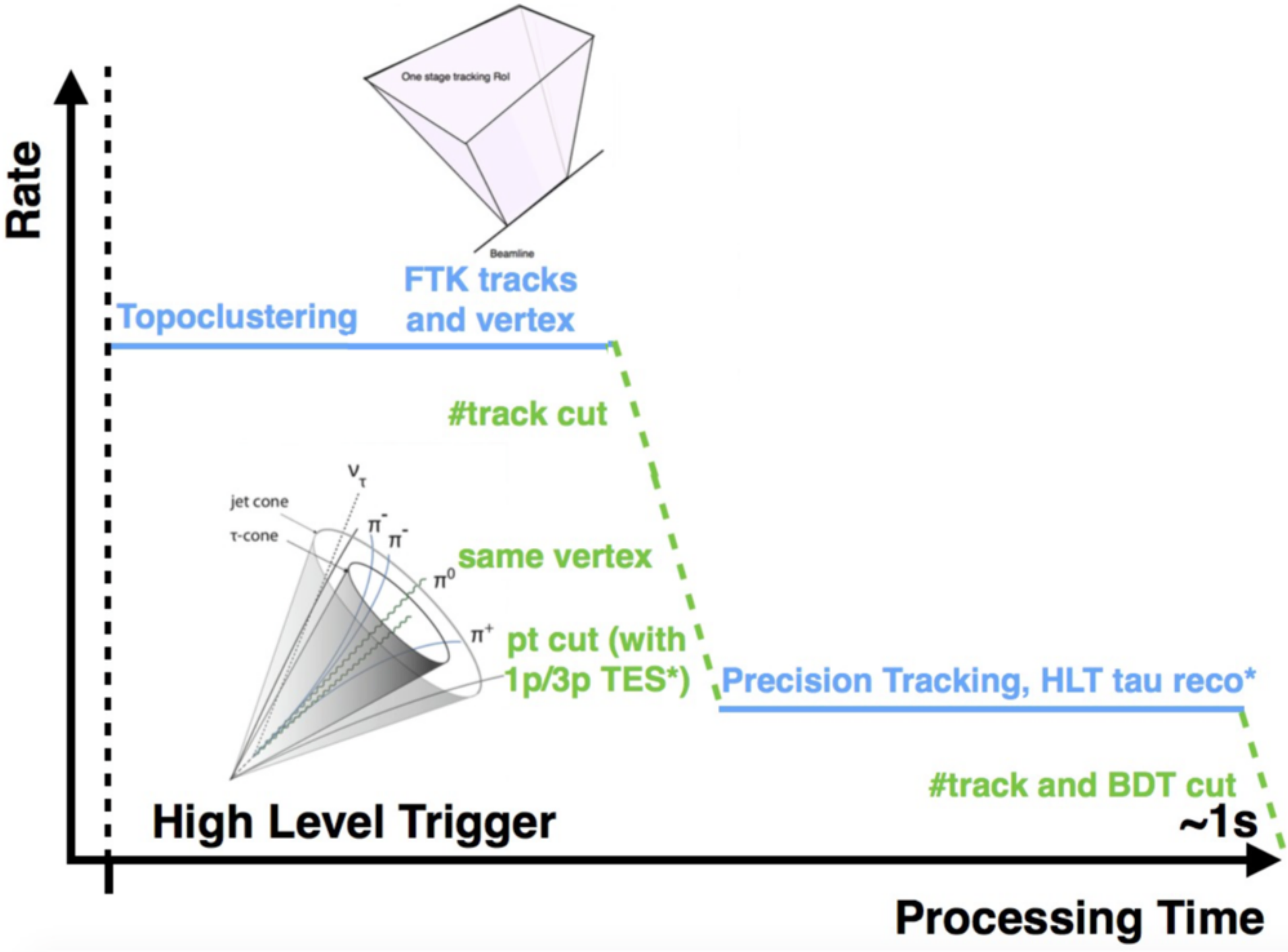


- Large bit error rates in data transferred between boards were seen in previous backplanes built by ASIS
- ASIS delivered new backplane for testing ~2 weeks ago, and came to help test
- Performance was greatly improved in new version
- See above eye scans for an example comparing the two backplanes under the same configuration and board pair, testing transfer rate of 10Gbps

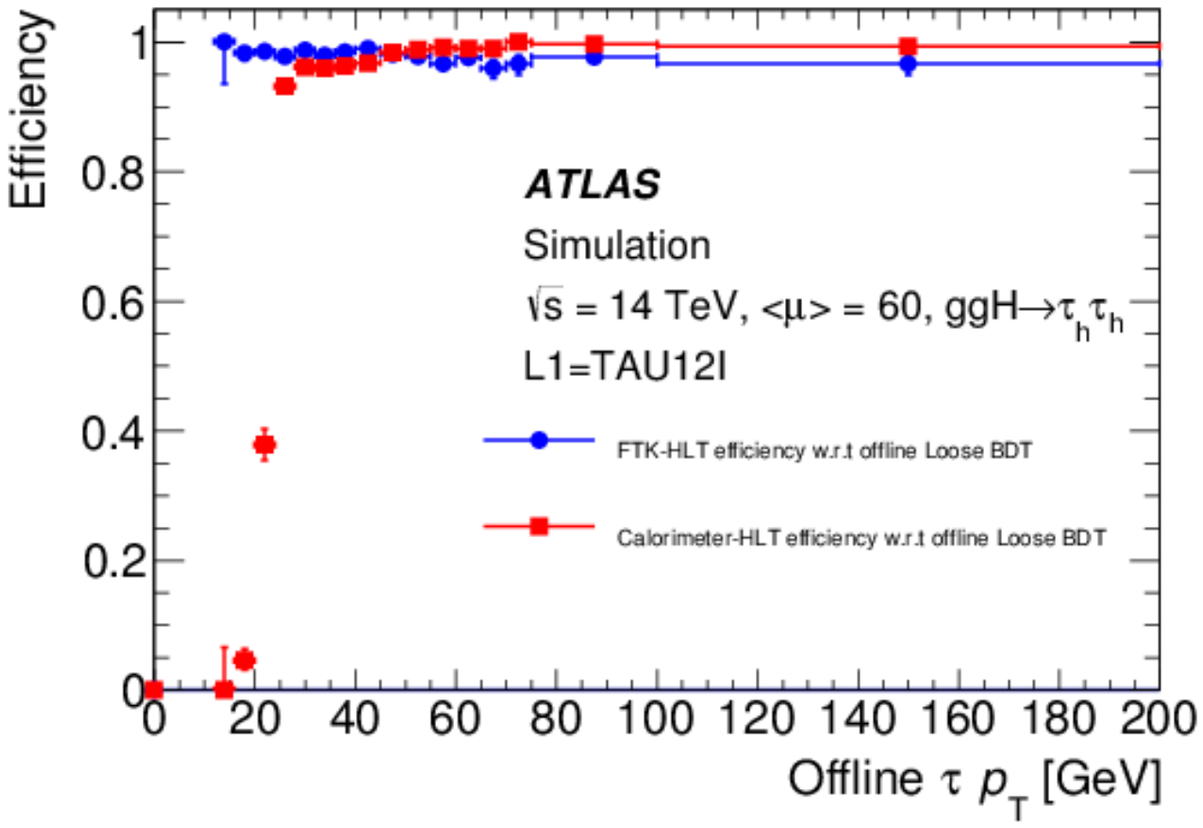
1

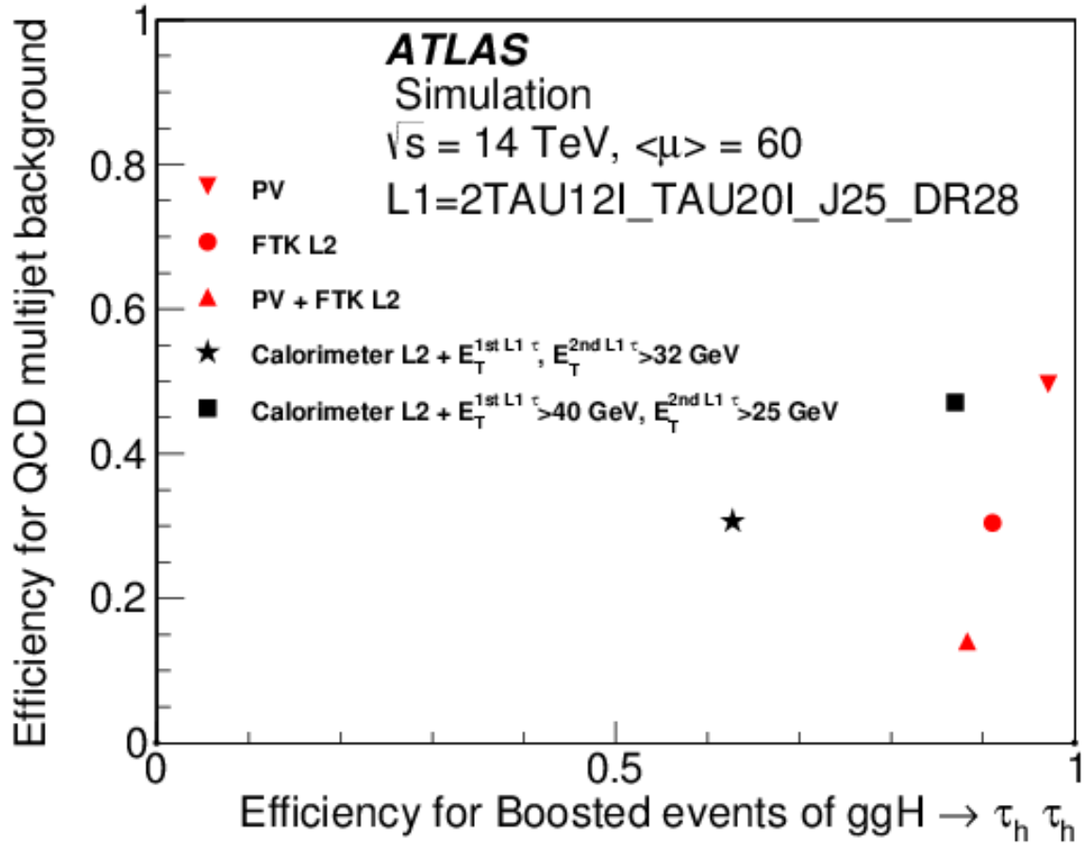
EXAMPLE USES: TAUS



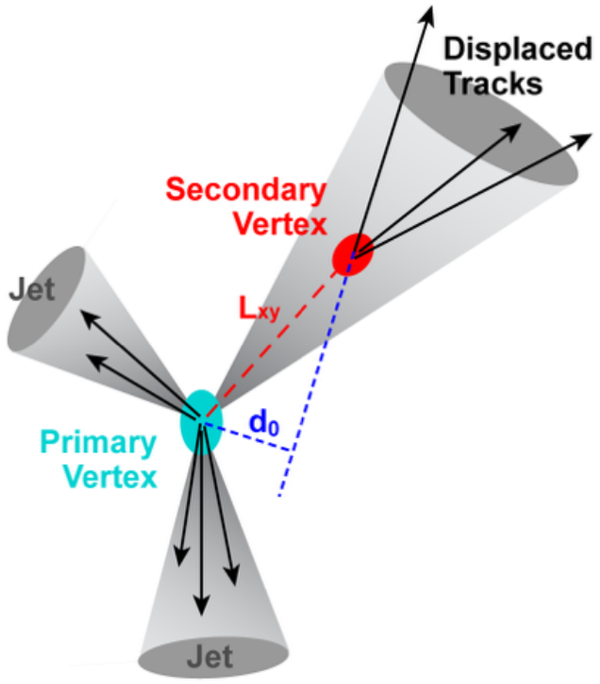

Rate
One stage tracking RoI
Beamline
FTK tracks
and vertex
Topoclustering
#track cut
ν_τ
jet cone
τ-cone
π^-
π^-
π^0
π^+
same vertex
pt cut (with
1p/3p TES*)
Precision Tracking, HLT tau reco*
#track and BDT cut
High Level Trigger
~1s
Processing Time

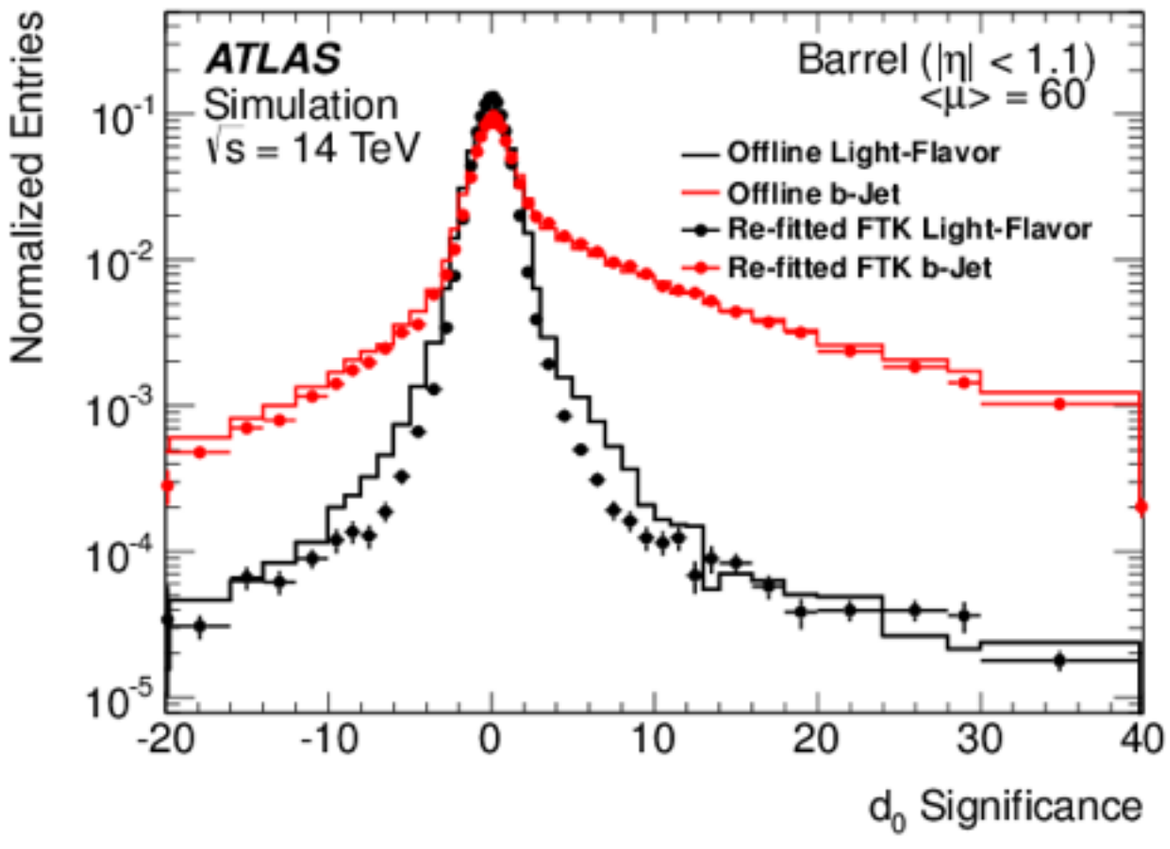
EXAMPLE USES: TAUS

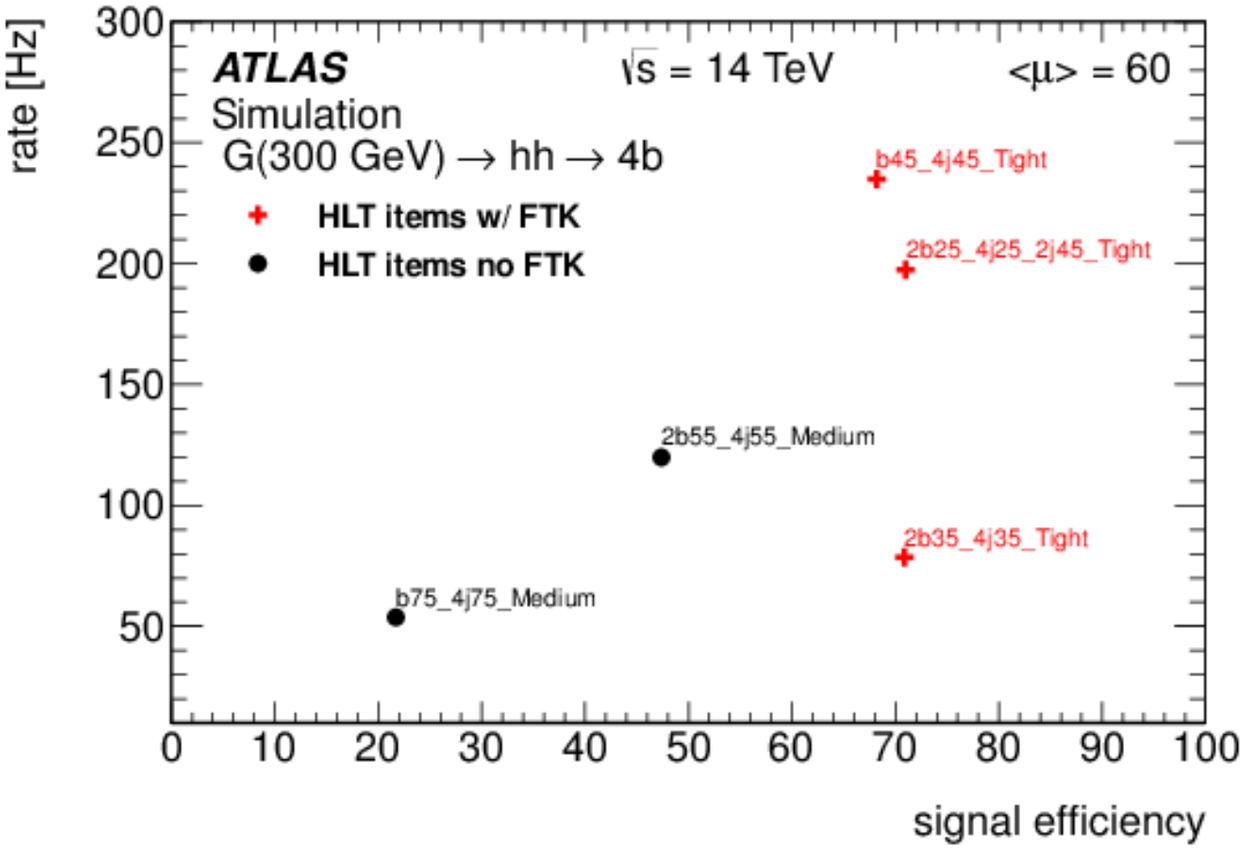




EXAMPLE USES: B-JETS

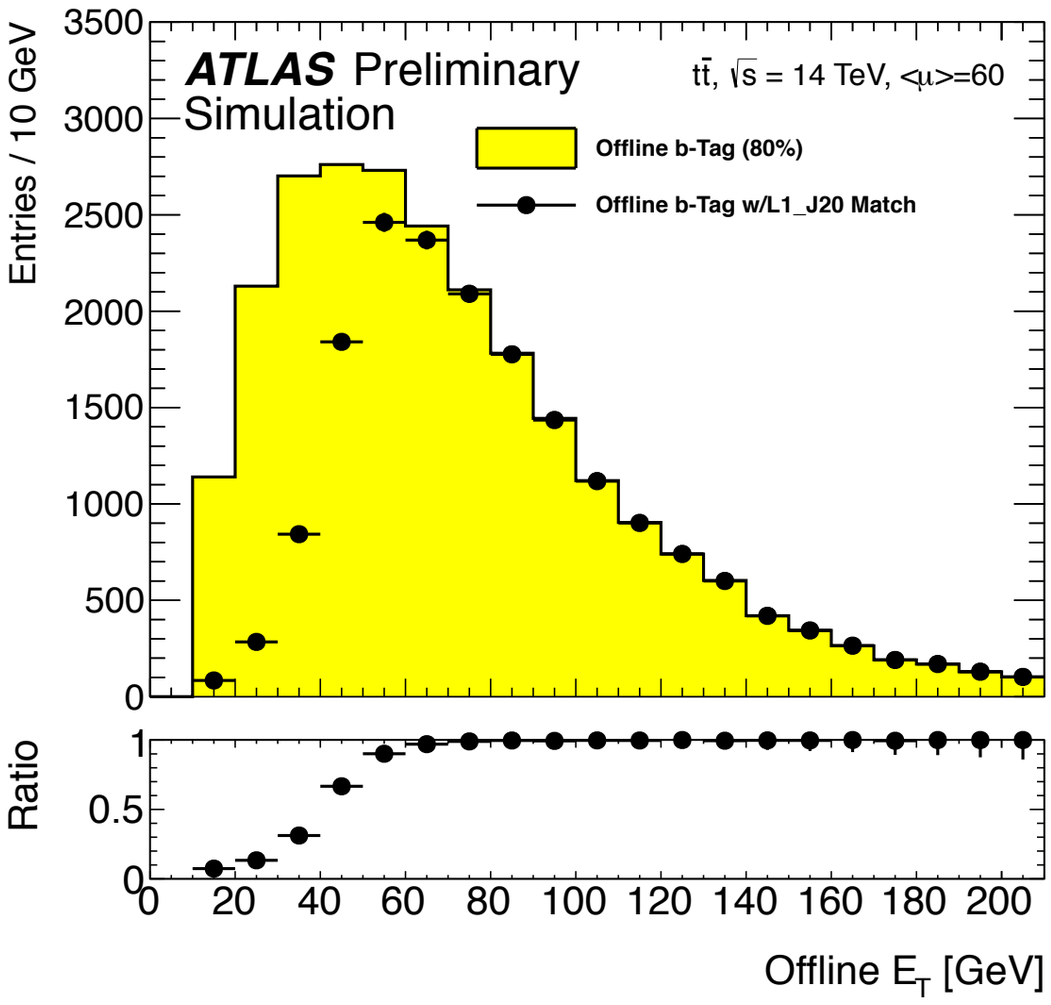




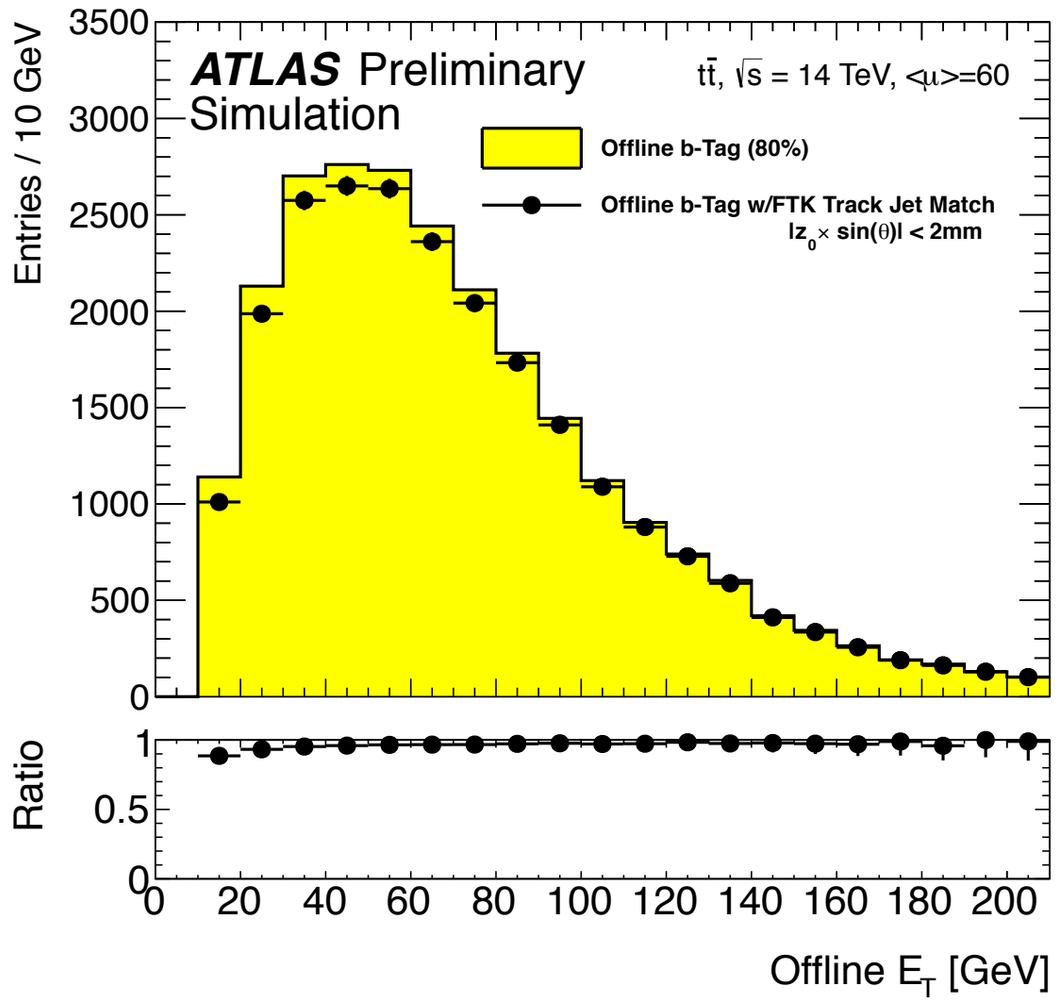


EXAMPLE USES: B-JETS

Calo Jets

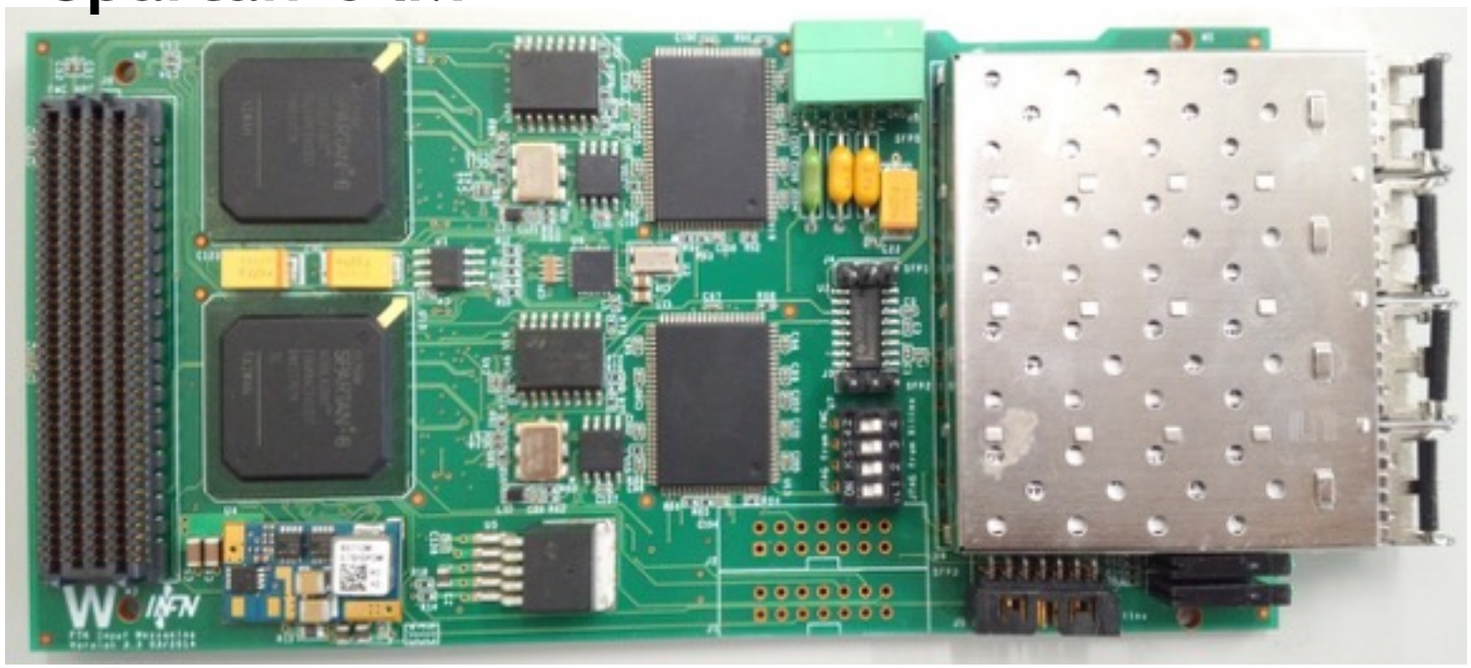


Track Jets



Input Mezzanine board (IM)

Spartan-6 IM

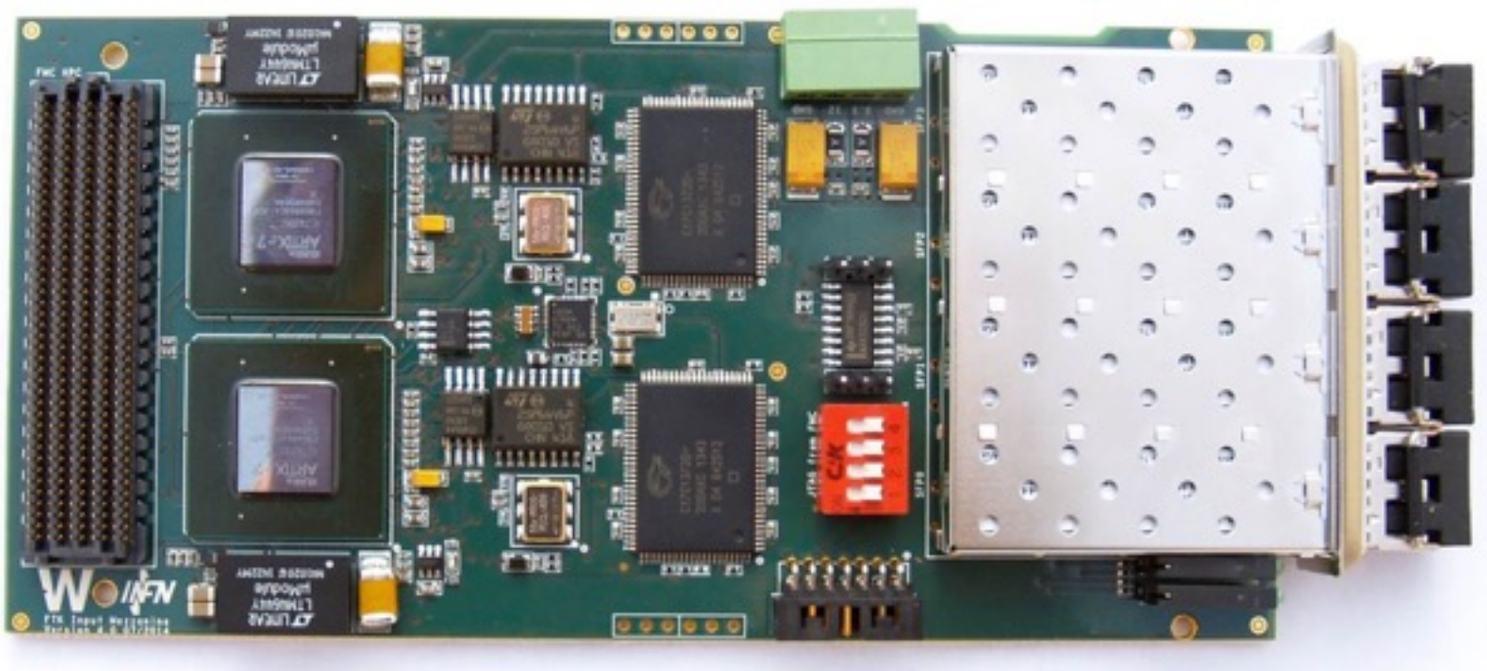


- Total 80 boards are produced.
- 79 boards Pass all test

1 board with patch cable goes to spare

- All boards were delivered to CERN.
- Several boards are already installed to USA15 and used to test.

Artix-7 IM



- All boards will be produced at Nov 23.
- Boards will delivered to CERN after the initial test in this year.
- Several boards are already tested in Real data at CERN

Integration test results

Receive the hit by required speed. **OK**

Process the hit clustering by required speed.**~80 %**

Check IBL

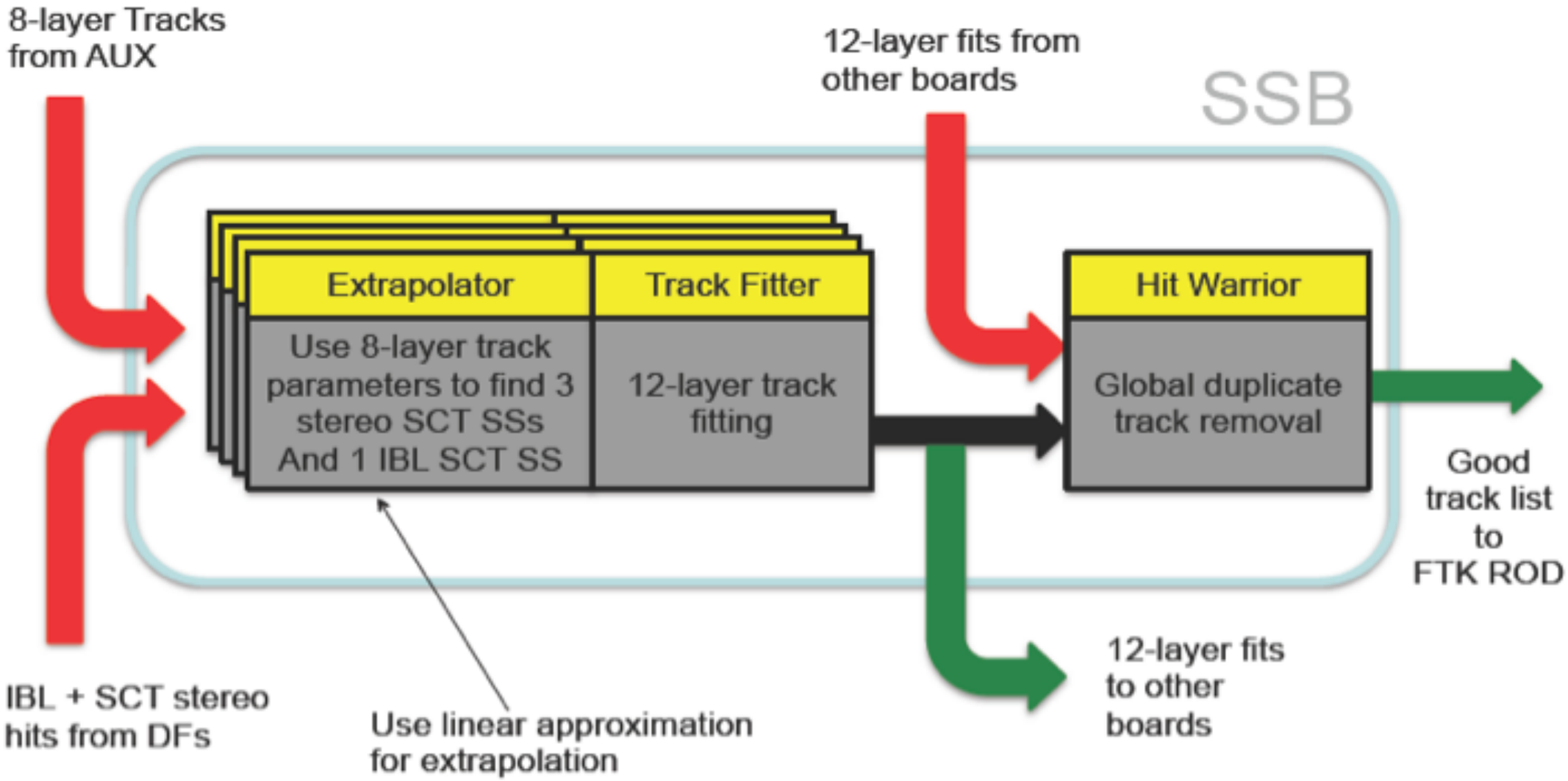
Send the hit to next board (DF) **OK**

Stable data flow. **~80%**

There are still miner bug in data flow for Firm ware side.

->Under Investigation.

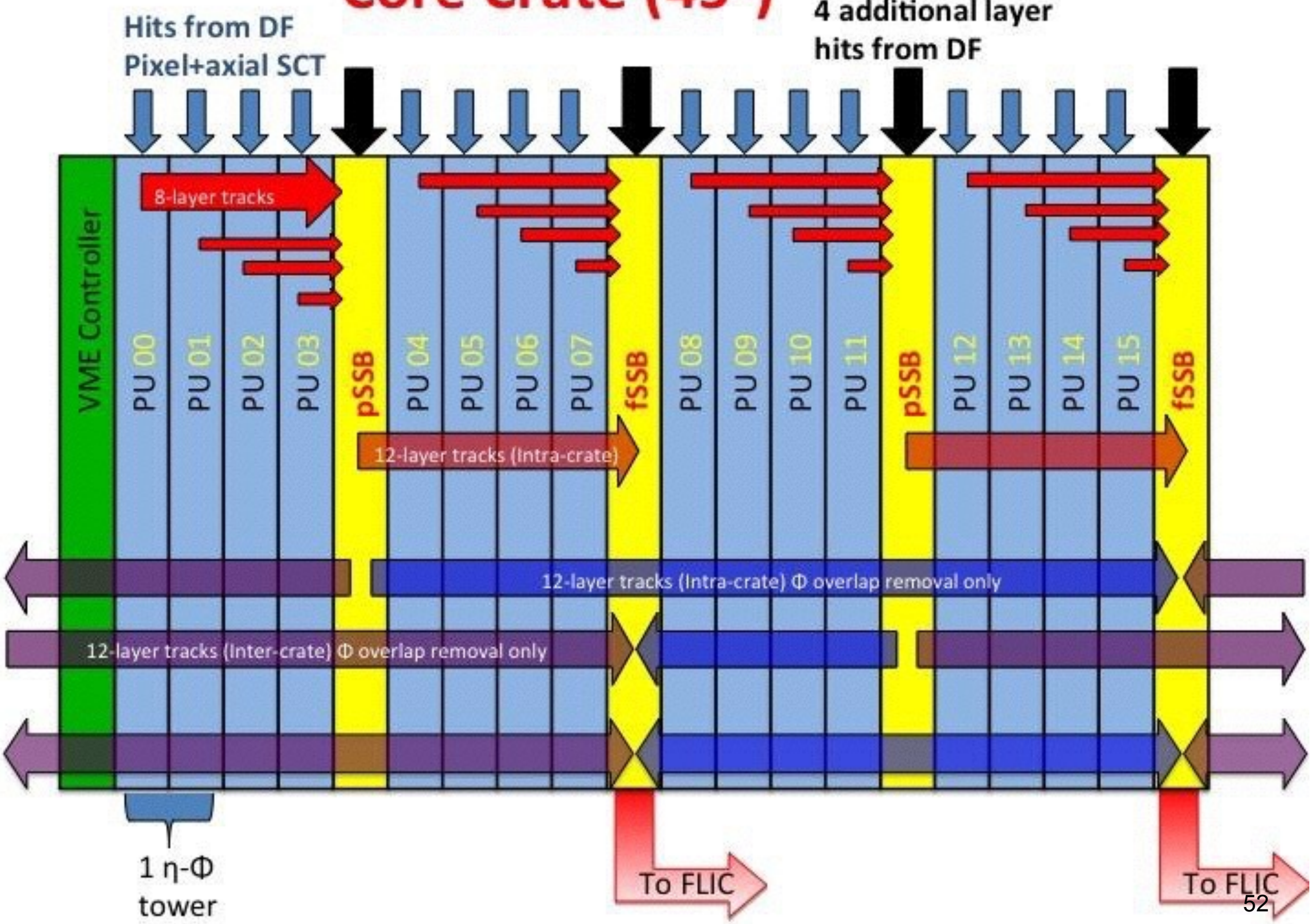
FTK Second Stage: Functions



Each SSB:

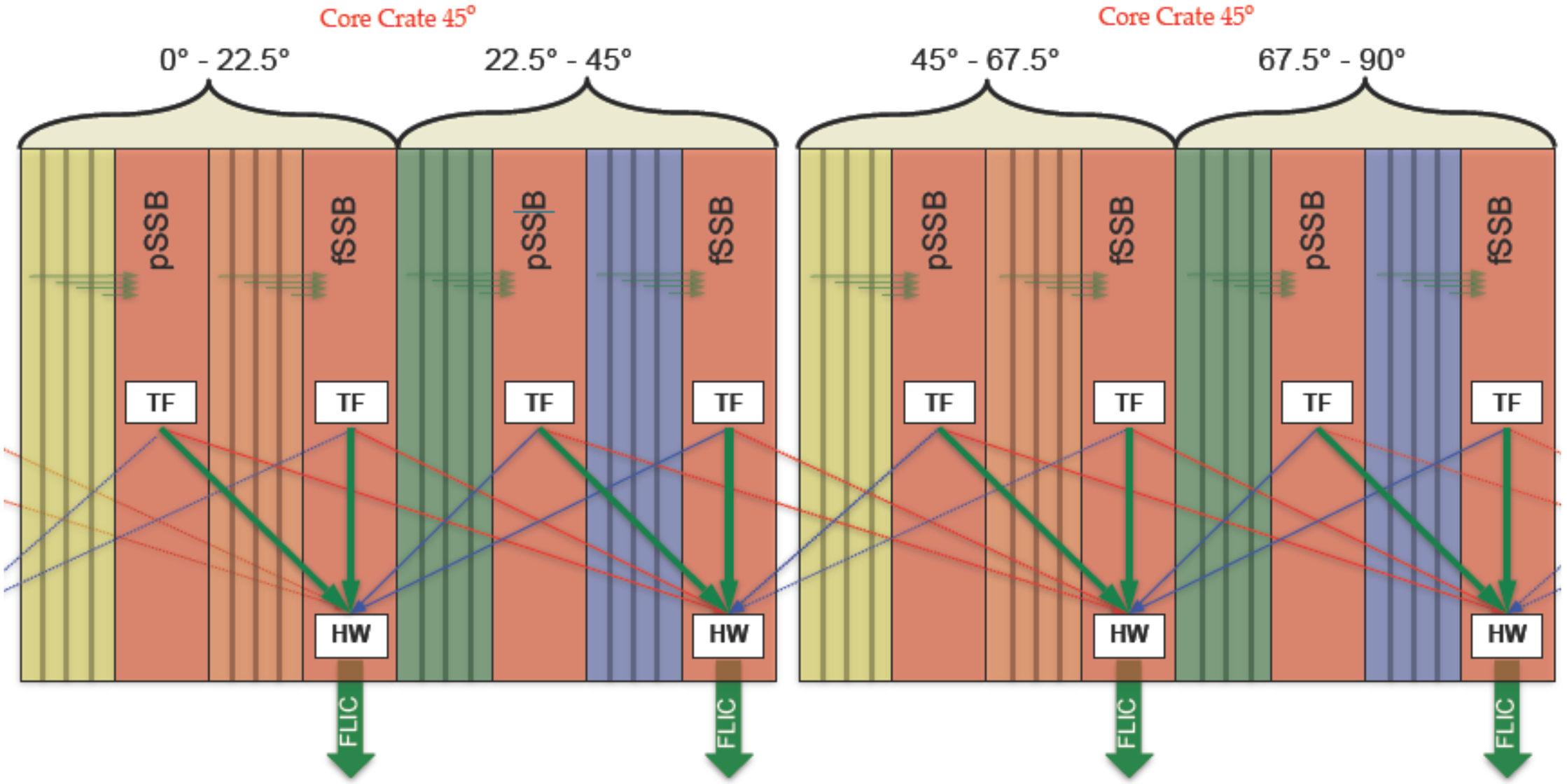
- Receives 8L data from 4 AUX cards
- Receives IBL and stereo SCT hits from DF for 2 η-ϕ towers
- "Extrapolates" 8L fits into layers not used in the 1st stage using pattern constants and retrieves candidate hits from those layers for use in 12L track fitting (*Extrapolator FW*)
- Performs 12L fit (*Track Fitter FW*)
- Receives Intra- and inter-crate SSB 12L track streams and uses these to remove duplicates (*Hit Warrior FW*)
- Merges FTK data within a core crate and outputs data to FLIC

Core Crate (45°)



HW: SSB track flow

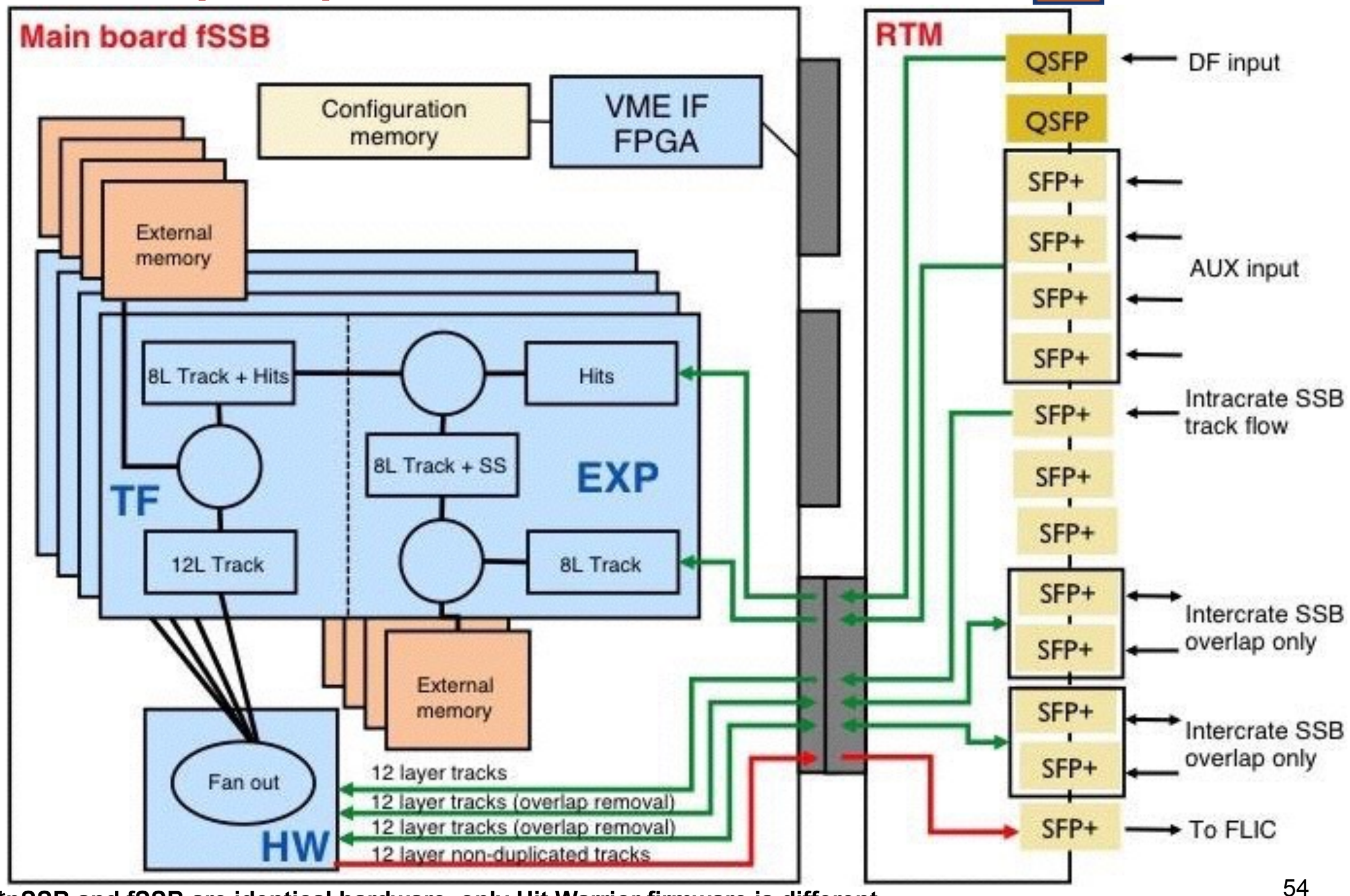
Illinois



Green arrows show the flow of tracks. Tracks flow out of the TF and are merged in the HW.
Red and **Blue** arrows show tracks sent to neighboring φ regions for overlap removal

Final f(SSB)*

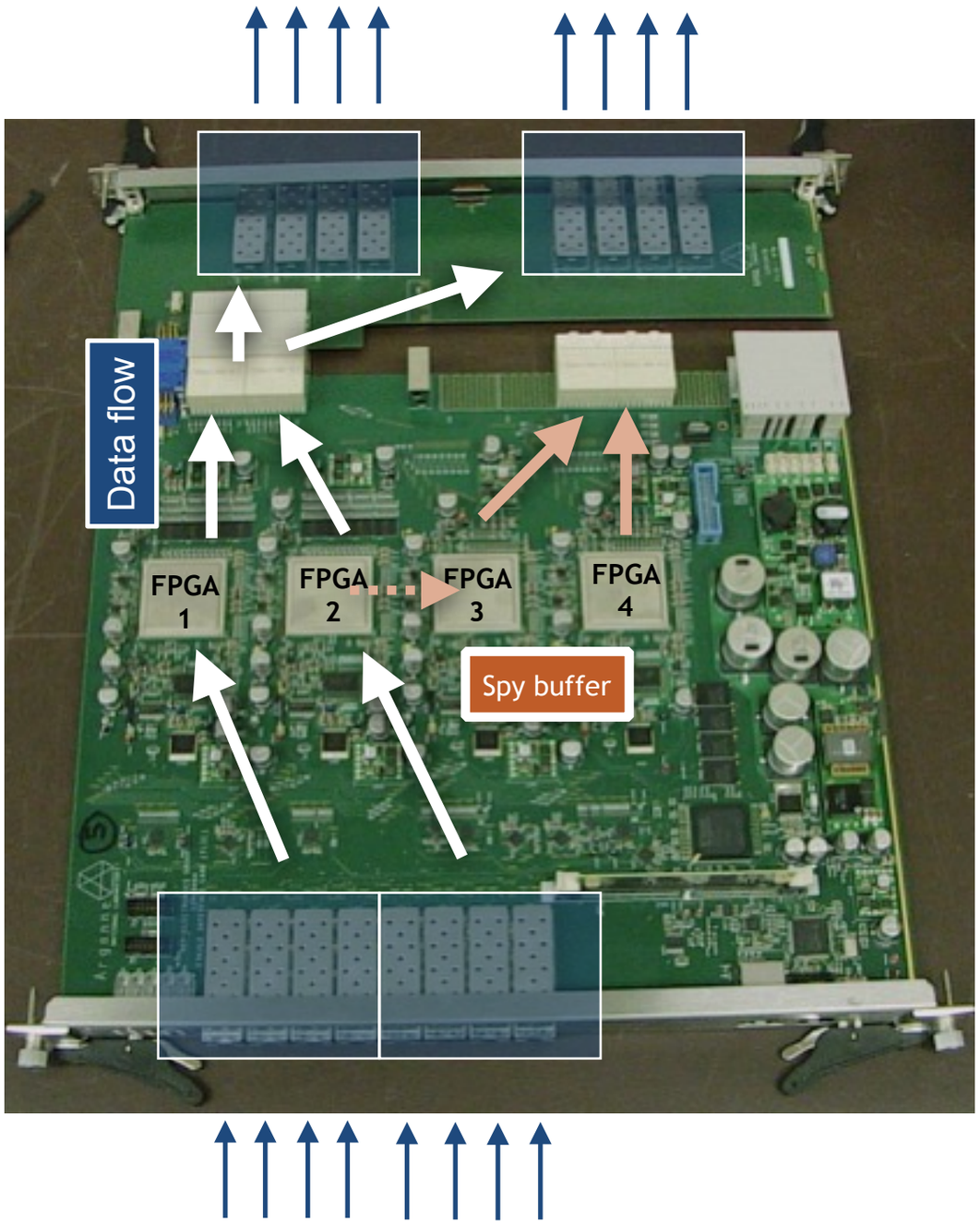
Illinois



*pSSB and fSSB are identical hardware, only Hit Warrior firmware is different

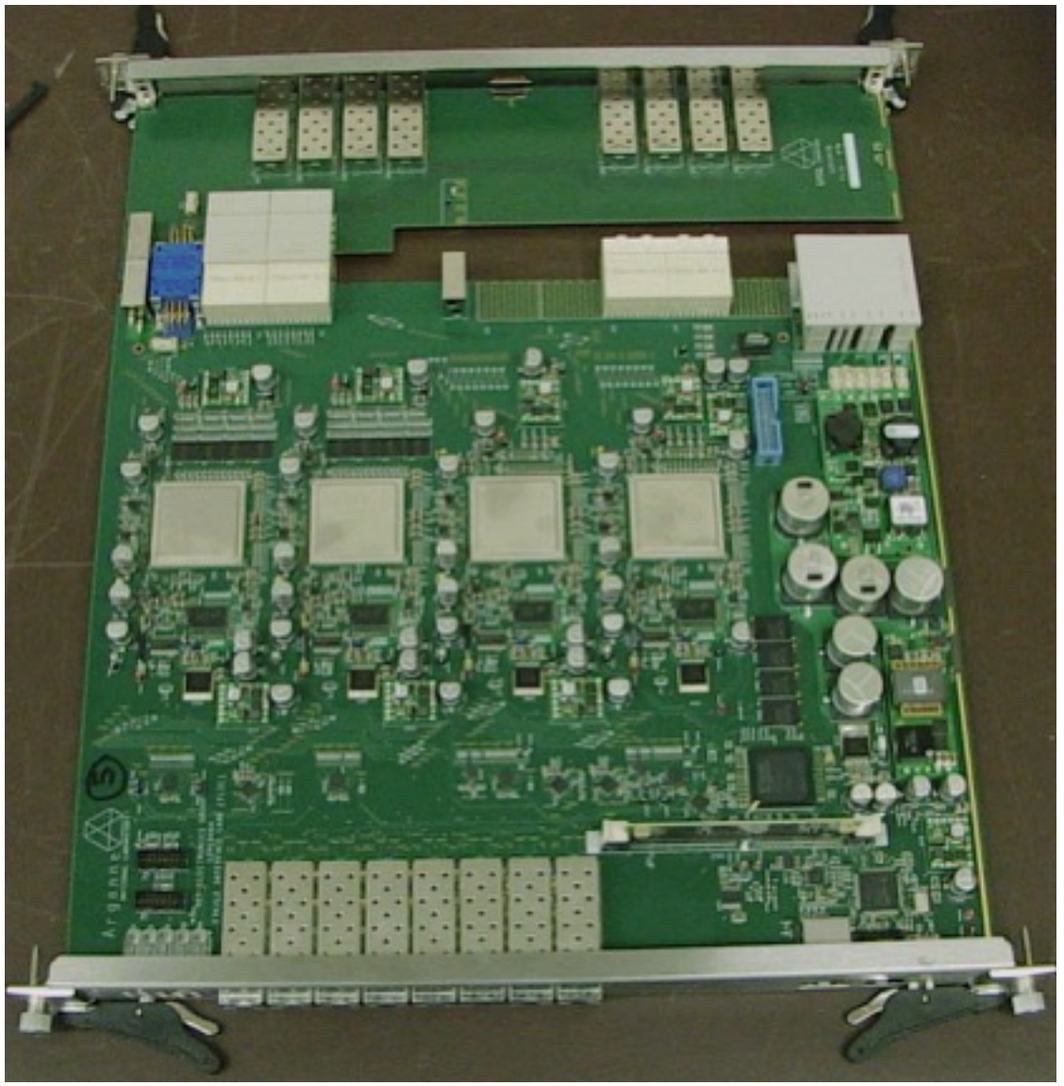
FLIC functionality

- Receive event records from upstream FTK system, 1/16th of the detector per channel
  - Full bandwidth output from the FLIC to HLT
    - Baseline: 300 tracks per event @ 100 kHz
- Convert FTK identifiers to ATLAS global identifiers using SRAM lookup
- Repackage event record into standard ATLAS format
- Communicate with HLT
  - Sends records
  - receives xoff signal and propagates it upstream to FTK
- Monitoring and Processing on ATCA Blades via backplane



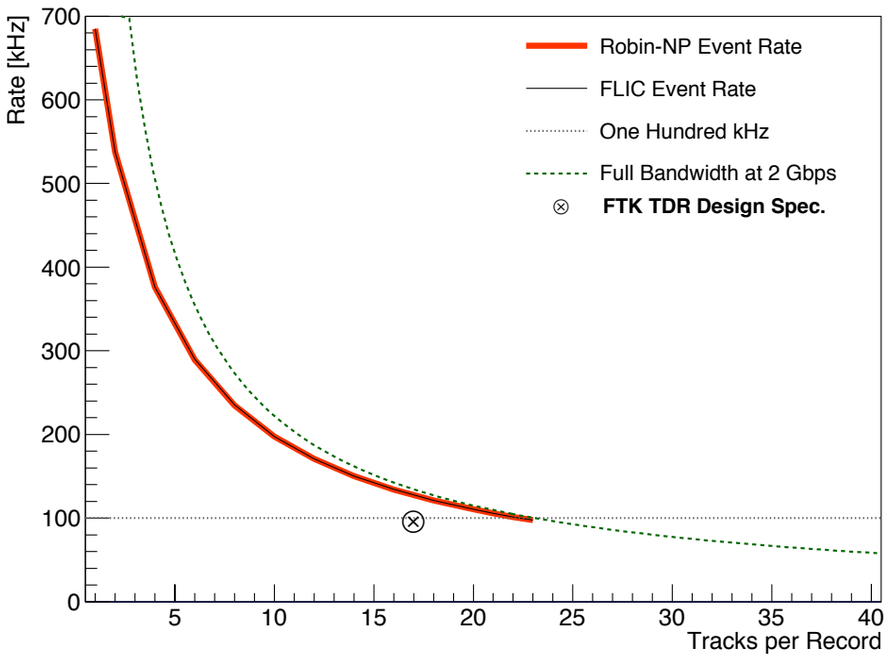
Hardware status

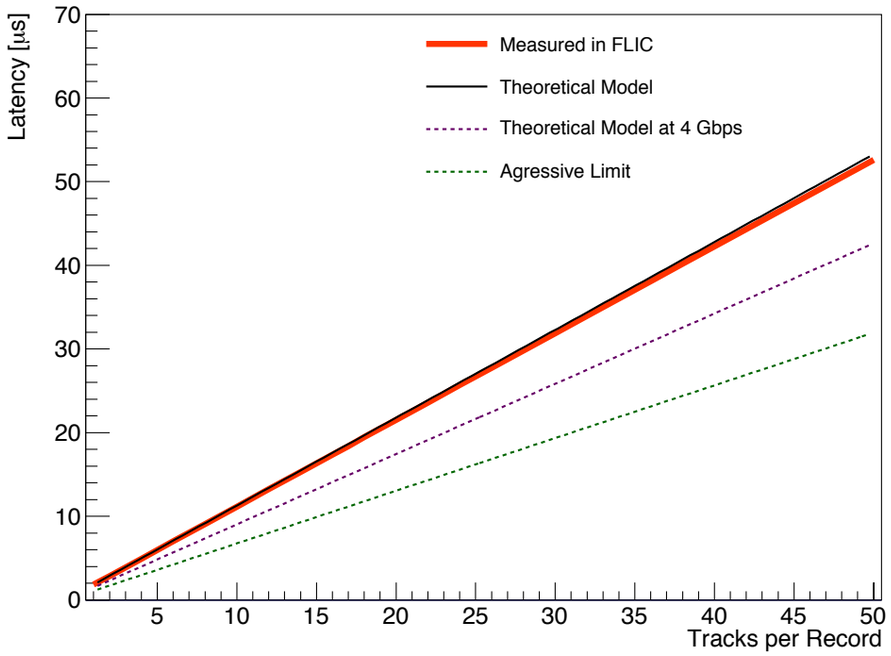
- Prototype boards have been fully tested
  - One send to CERN for integration testing
- Two production boards arrived at ANL in Oct. 2015
  - New front panel, new back panel, IPMC, new SRAM architecture and etc.
  - Firmware updates to fit to the hardware change from the prototype to the production board
  - Currently under lab testing at ANL

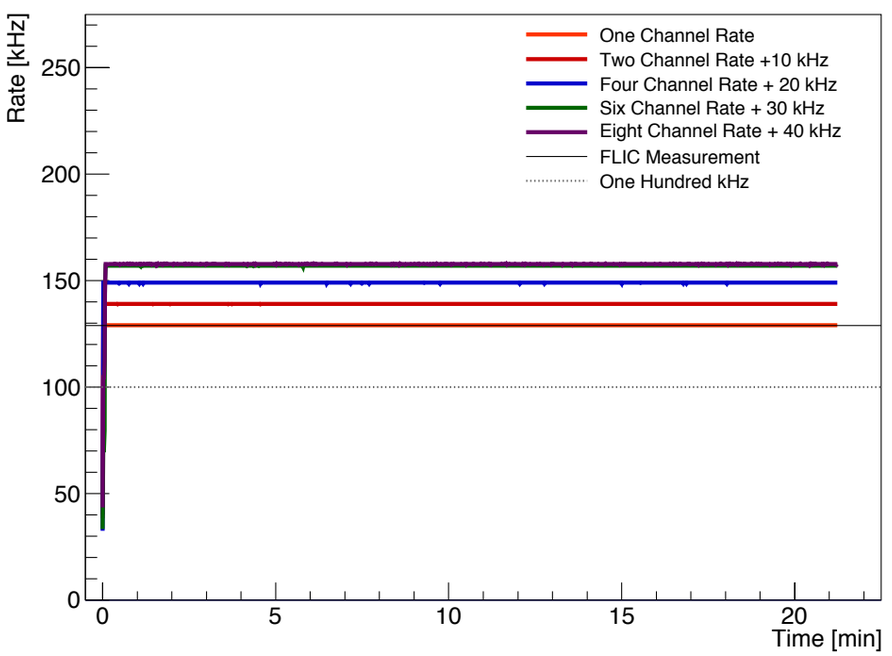


FLIC testing at ANL

- Prototype been fully tested at ANL
  - Latency ~20us, well understood
  - Stable rate above 100 kHz, tested with 1 - 8 channels
    - Rates are shifted to have a better visibility

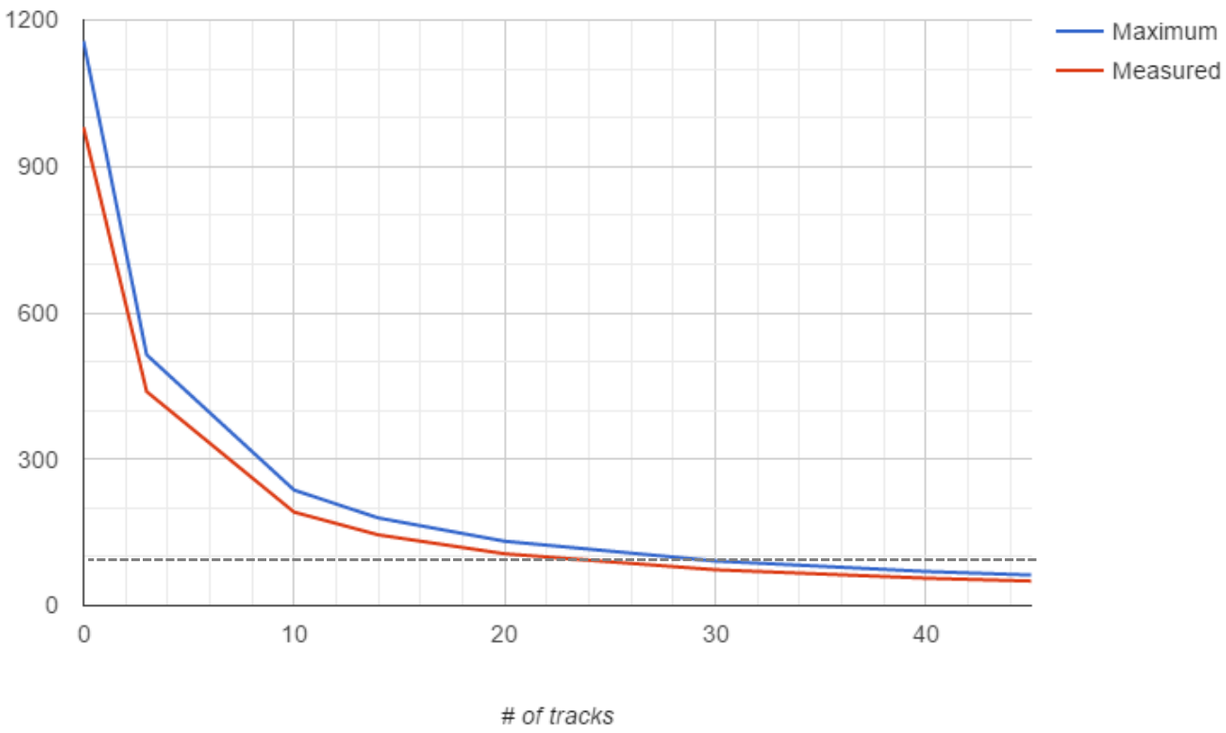


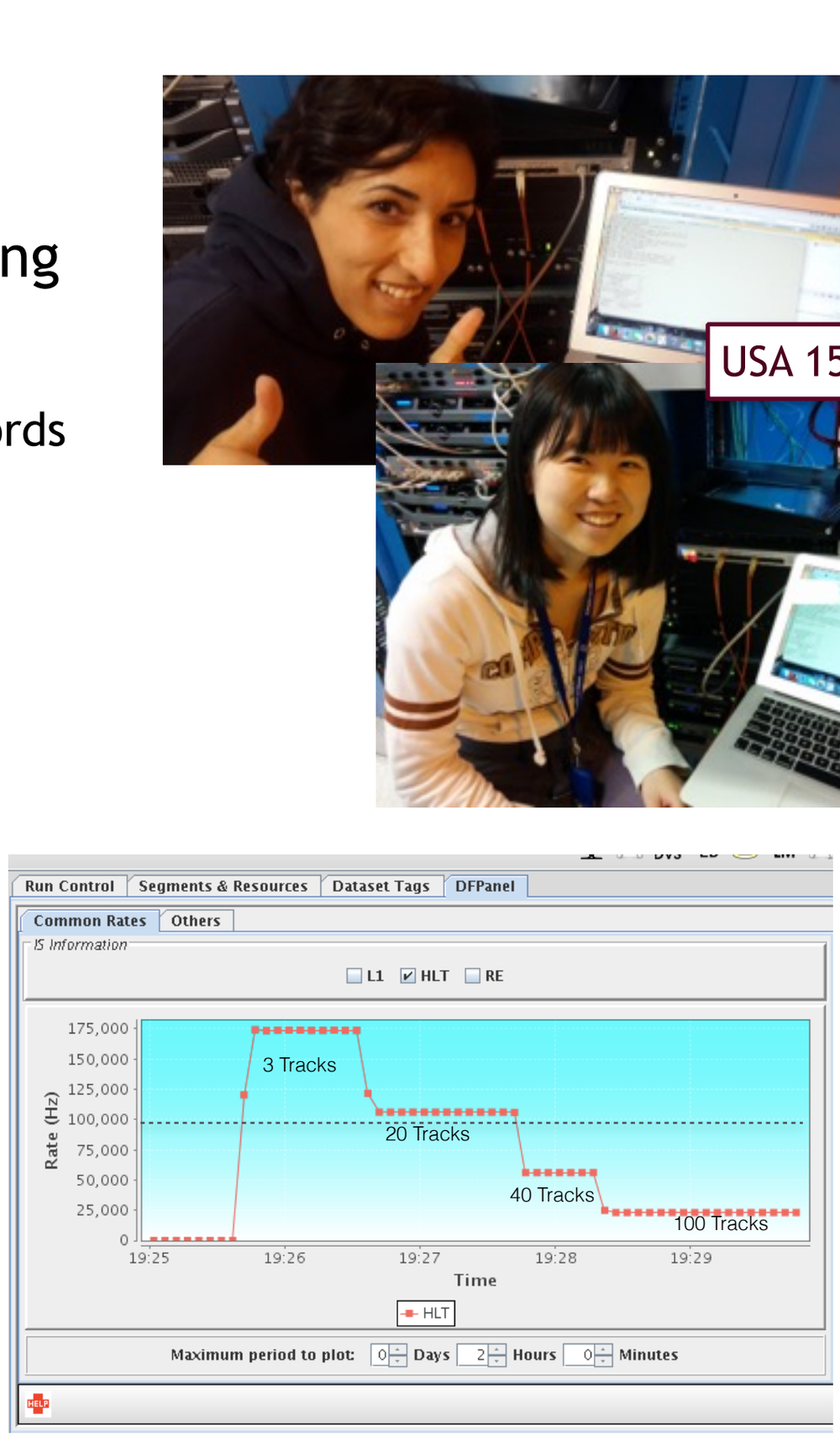




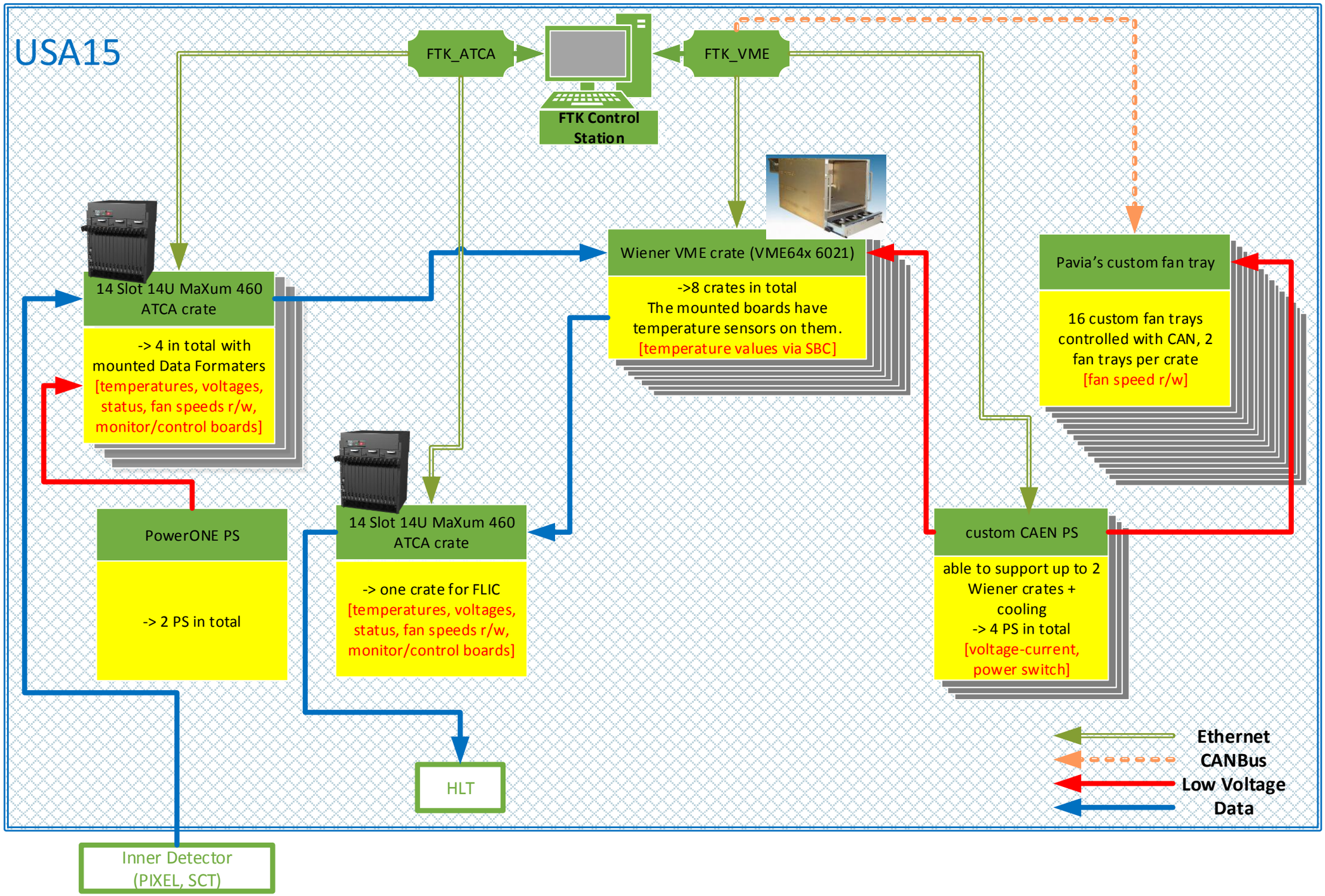
FLIC testing at CERN

- One prototype send to CERN for testing
  - FLIC to ROS rate tested for one channel
    - Rate vs number of tracks per event records (fixed tracks & random delay)
    - Standalone software & ROS partition





DCS


USA15
FTK_ATCA
FTK_VME
FTK Control Station
14 Slot 14U MaXum 460 ATCA crate
-> 4 in total with mounted Data Formaters [temperatures, voltages, status, fan speeds r/w, monitor/control boards]
Wiener VME crate (VME64x 6021)
->8 crates in total
The mounted boards have temperature sensors on them.
[temperature values via SBC]
Pavia's custom fan tray
16 custom fan trays controlled with CAN, 2 fan trays per crate
[fan speed r/w]
PowerONE PS
-> 2 PS in total
14 Slot 14U MaXum 460 ATCA crate
-> one crate for FLIC
[temperatures, voltages, status, fan speeds r/w, monitor/control boards]
custom CAEN PS
able to support up to 2 Wiener crates + cooling
-> 4 PS in total
[voltage-current, power switch]
HLT
Inner Detector (PIXEL, SCT)
Ethernet
CANBus
Low Voltage
Data

EXAMPLE USAGE OF LAB 4 TESTSTAND

- Controlled environment lets us test FW limits in interaction between two boards