LBNL, Berkeley, August 19, 2016

Depleted CMOS Pixels R&D (for LHC - pp Experiments)

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SILAB
Silizium Labor Bonn

LHC pixel detectors

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- complex signal processing already in pixel cell possible
  - zero suppression
  - temporary storage of hits during L1 latency
- radiation hard to >10^{15} n_{eq}/cm^2
- high rate capability (~MHz/mm^2)
- spatial resolution ~ 10 – 15 µm

PRO

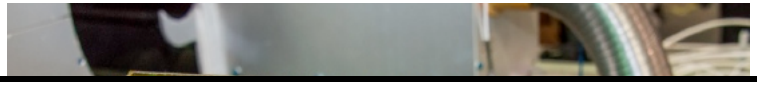
… but also

- relatively large material budget: **3.5-1.5% X_0** /layer in ATLAS/CMS
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
- complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - as a result: expensive

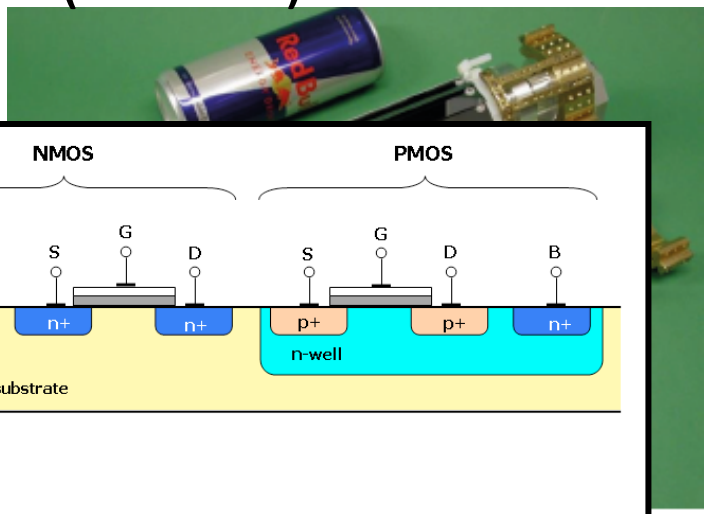
CON

(Semi)-Monolithic Pixel Detectors

STAR / RHIC MAPS



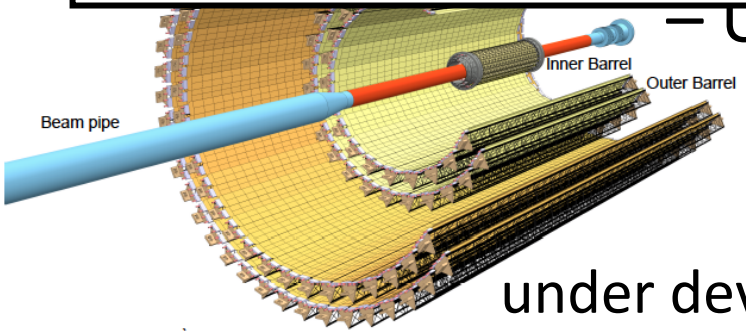
(Belle II) DEPFET



- Use commercial CMOS technology
  - mature (world market)
  - cheap in comparison
- Monolithic (i.e. one sensor/chip entity)
  - avoids hybridization
  - wafer scale processes
  - large modules possible when stitching over reticles is employed
- Can (in principle) have very small pixels
  - o (25 x 25 µm²)

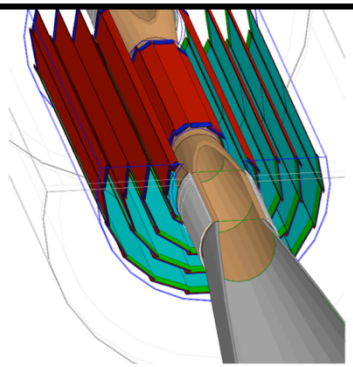
M

– Upgrade



total area
~10 m²

under development
target: 2018



total area
? m²

current
baseline

Rate and Radiation Levels

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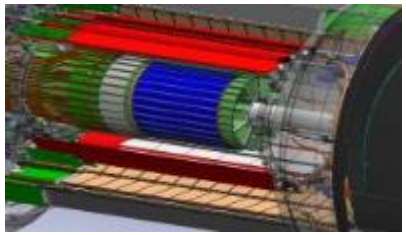
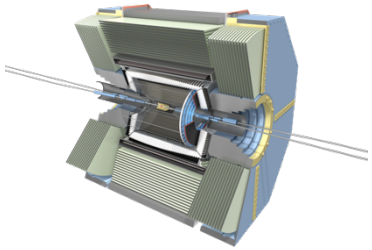
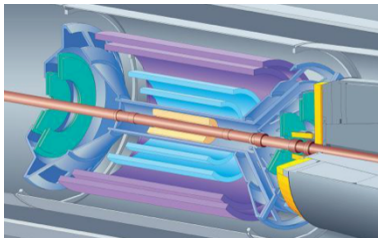
STAR



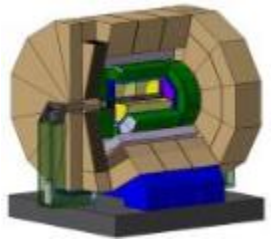
Belle II



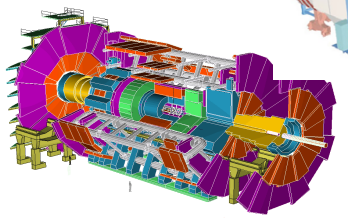
ALICE-(HL)-LHC

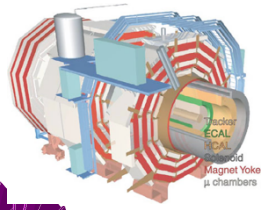


ILC



ATLAS





CMS

Numbers for innermost layers (r ≈ 5cm,) -> scale by 1/10 for typical strip layers (r > 25 cm)

	STAR	Belle II	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
						Outer	Inner
BX-time (ns)	110	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	10	250	1 000	1 000	10 000
Φ (n_{eq}/cm^2)	few 10^{12}	2 x 10^{12}	> 10^{13}	10^{12}	2x10^{15}	10^{15}	2x10^{16}
TID (Mrad)*	0.2	20	0.7	0.4	80	50	> 1000

Monolithic Pixels

Hybrid Pixels

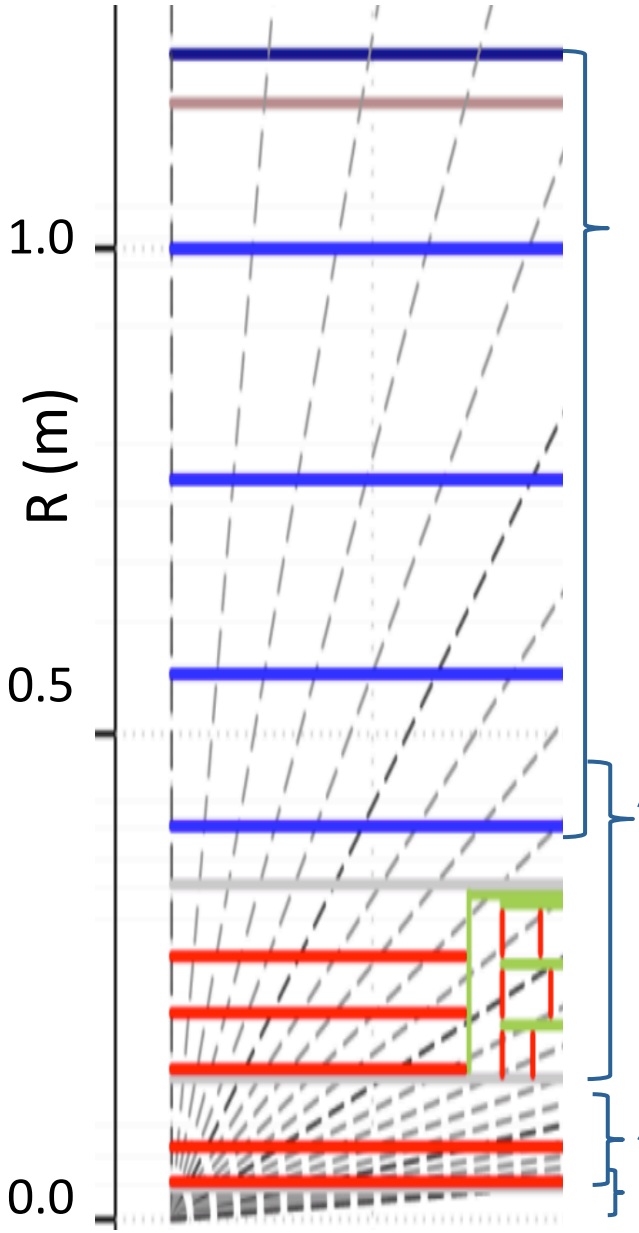
*per (assumed) liftetime
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

in need for
- much less material
- higher resolution
- thinner strips & monolithic pixels

state of the art
- large area strips
- hybrid pixels

- even larger area
- radhard sensors
- higher rates R/O
- **CMOS pixel R&D**

Current ATLAS ITk targets ...

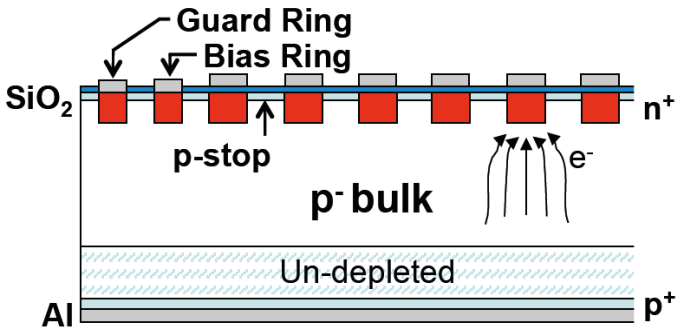


strips

outer pixel

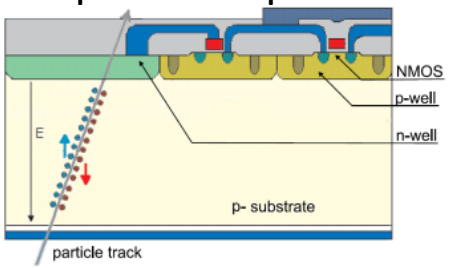
inner pixel

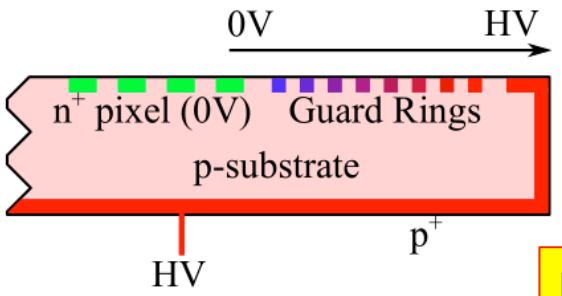
innermost pixel



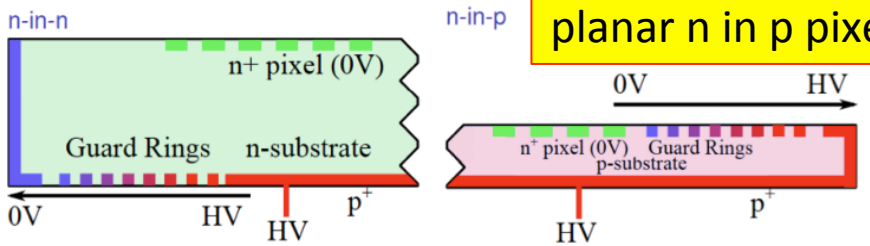
n in p
strip modules

depl. CMOS pixels

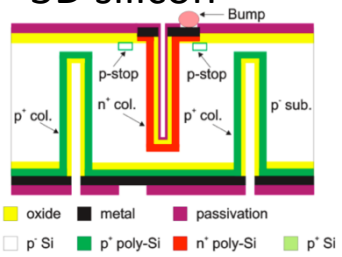




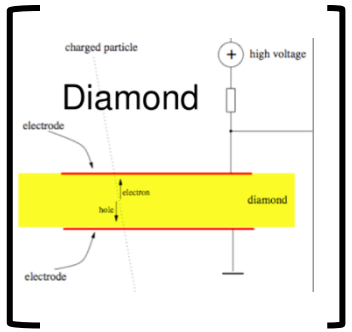
large modules
planar n in p pixels / CMOS?



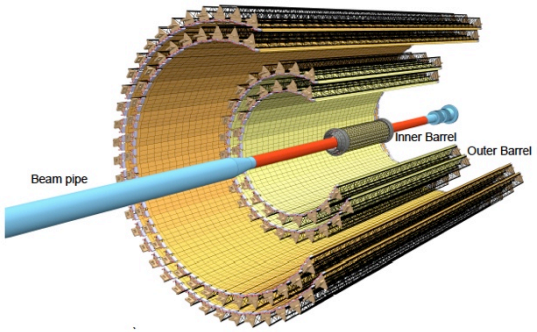
3D silicon



dedicated
rad.-hard
detectors

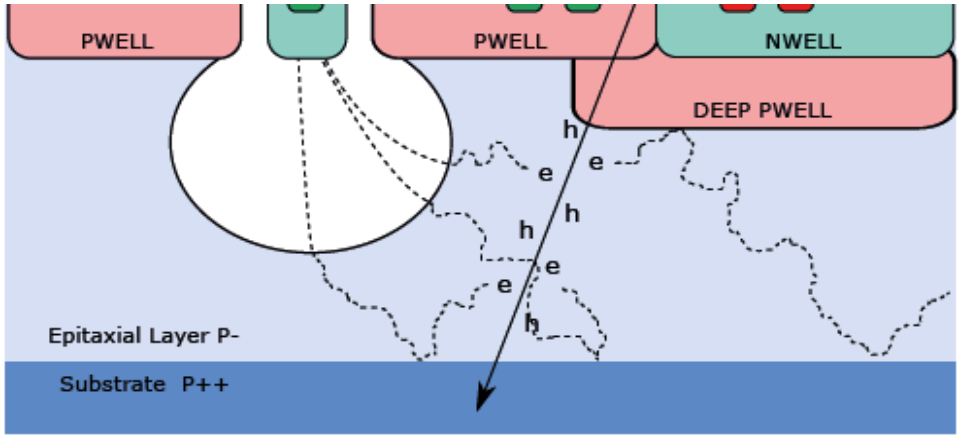


ALICE ITS: CMOS pixel: TowerJazz 0.18µm imaging process



- 3 inner (r < 2.1 cm) + 4 outer (r < 40 cm) layers
- ~ 10 m^2
- low material (0.3% X_0 inner barrel, 0.8% X_0 outer barrel)

from L. Musa 2015



Tower Jazz 0.18 µm CMOS

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

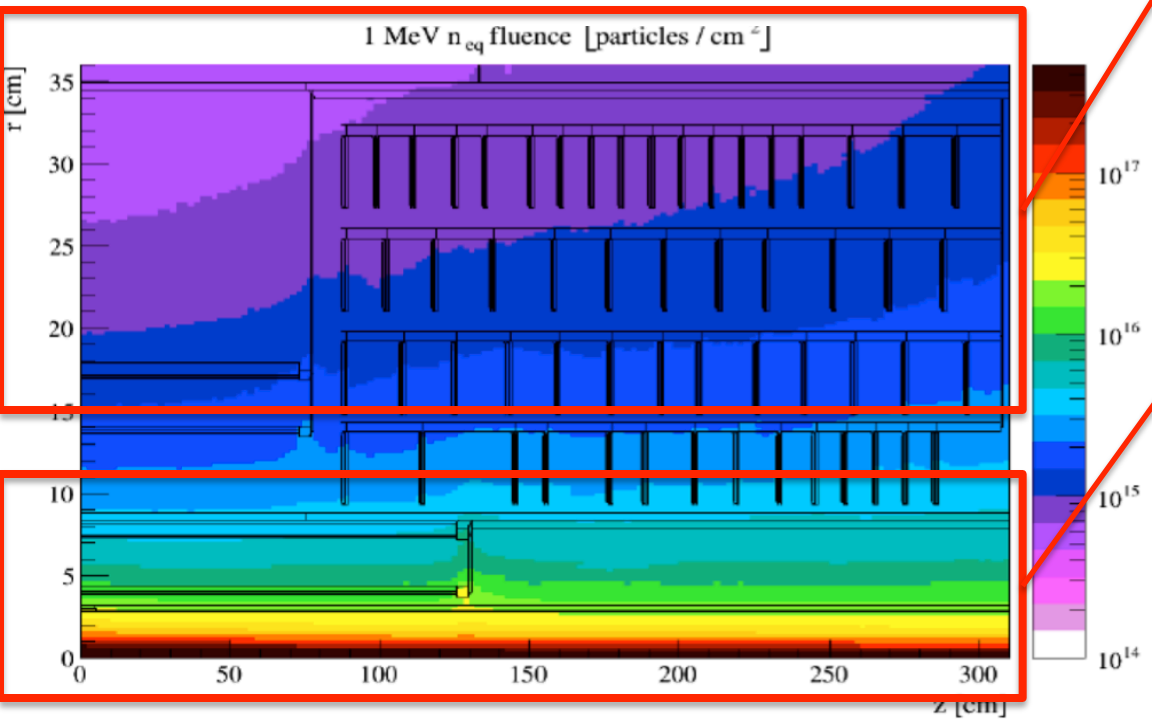
- Gate oxide 3nm

➔ Circuit rad-tolerant

- high resistivity (> 1kΩ cm) epi-layer (p-type, 20-40 µm thick) on p-substrate
- very small n-well diodes => small C_{in}
- moderate reverse bias => increase depletion region around Nwell collection diode
- quadruple well process => shield Nwells by deep Pwells => full CMOS
- radiation tolerance to 700 krad / fluence $10^{13}/n_{eq}/cm^2$ (= 1/1500 of HL-LHC-pp)

High Luminosity LHC Environment - Specs

- Set by LHC radiation levels, hit rates and bunch structure
  - 25ns
  - L1 trigger rates



- **Outer layers**
  - Occupancy 1-2 MHz/mm^2
  - NIEL ~ 10^{15} n_{eq}/cm^2
  - TID ~ 50 Mrad
  - Larger area O(10m^2)
- **Inner layers**
  - Occupancy 10-30 MHz/mm^2
  - NIEL ~ 10^{16} n_{eq}/cm^2
  - TID ~ 1 Grad
  - Smaller area O(1m^2)

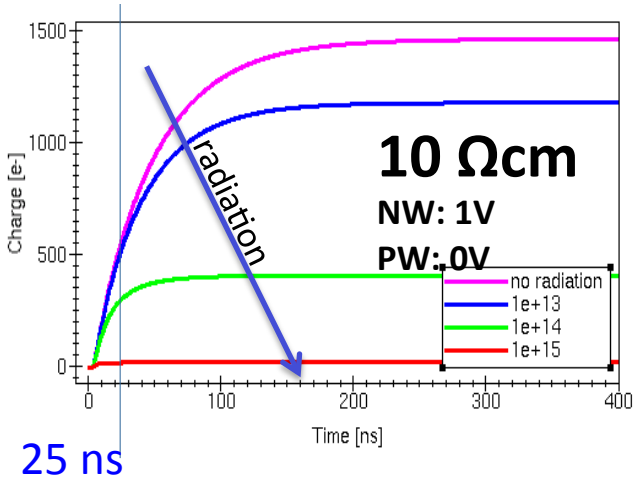
CMOS Pixels for HL-LHC -> DMAPS

- driven by the need/hope for
  - low cost large area detectors … more pixel layers in trackers …. commercial adv.
  - less material … ? less power … this is not at all clear
- but facing the rate/radiation challenges of the HL-LHC
- **goal:** some (40 – 80 µm) depletion depth for …
  - fast charge collection (< 25ns "in-time" efficient)
  - a reasonably large signal ~4000 e-
  - not too large a travel distance to avoid trapping (rad hardness)

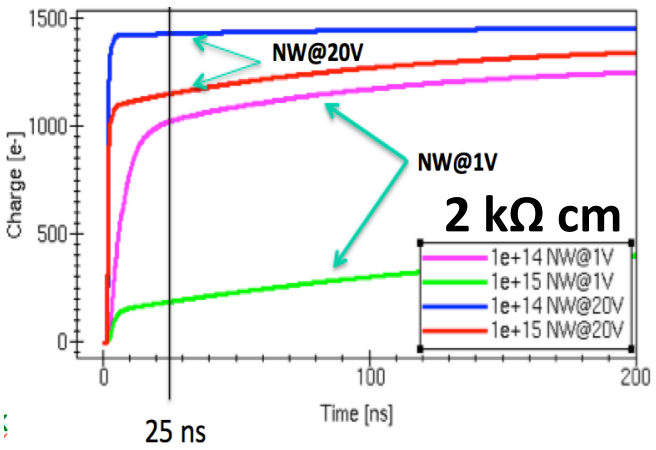
$$d \sim \sqrt{\rho \cdot V}$$

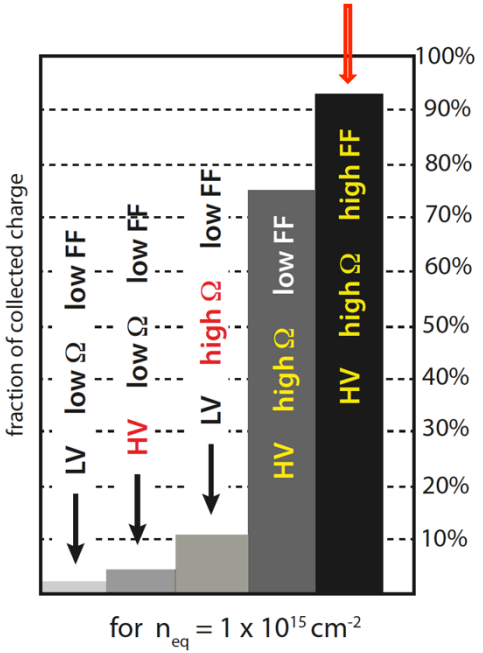
- **need**

low resistivity, low voltage



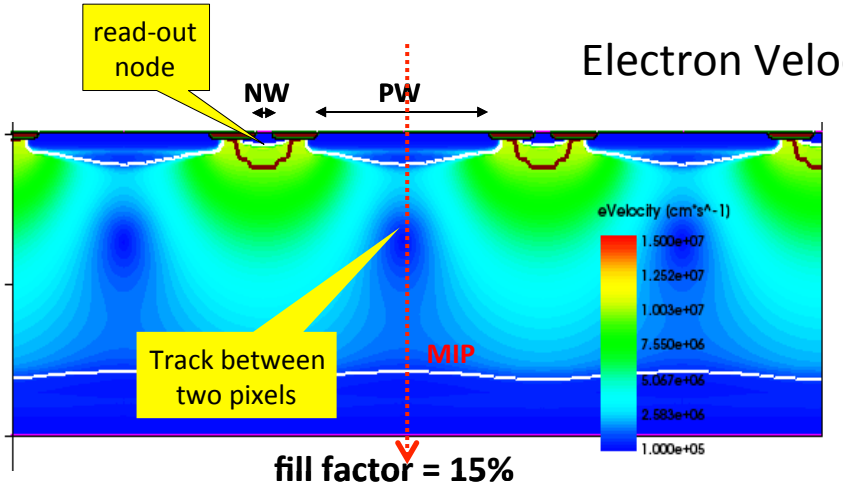
high res. plus (high) voltage



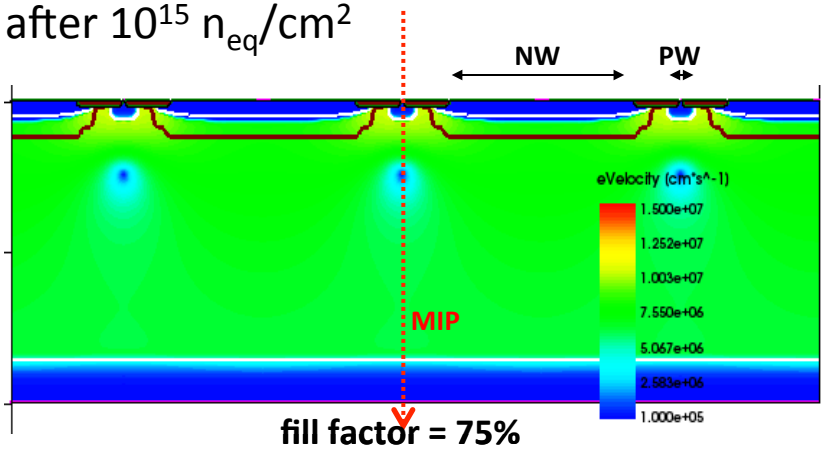


from Tomasz Hemperek

The question of the the fill factor

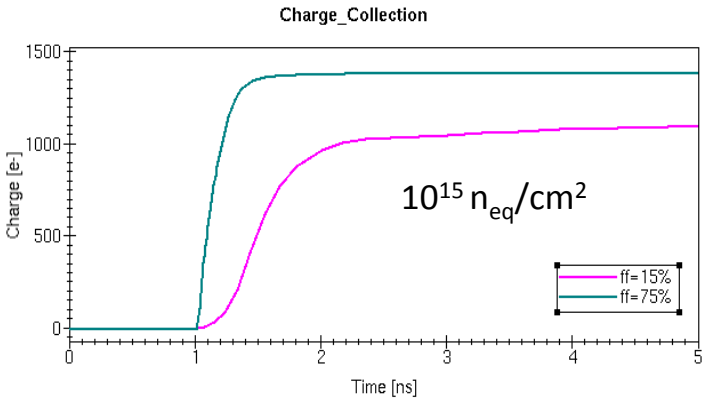


Electron Velocity after 10^{15} n_{eq}/cm^2



Charge collected within the first 10ns:

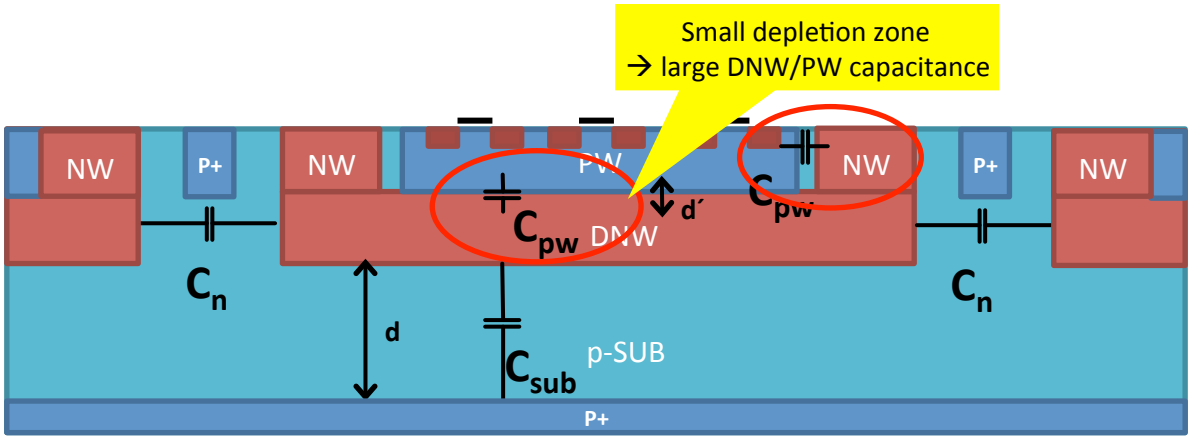
Fill factor	CCE after n_{eq}/cm^2		
	no radiation	10^{15}	$5 \cdot 10^{15}$
15%	99%	75%	25%
75%	100%	93%	67%



Simulation parameters:

- Pixel pitch: 20µm
- NW - bias: +20V
- Substrate: 2k Ohm cm, 20µm thick

Detector Capacitance



Large Fill Factor collecting node has a double junction: DNW/SUB and DNW/PW

- Backplane capacitance C_{sub} (DNW to substrate)
  - Depends on depletion depth (substrate resistivity, bias voltage)
- Inter-pixel capacitance C_n
  - Depends on fill factor and p-implant ('p-stop') geometry

} same as for std. Hybrid Pixels

- DNW to P-well capacitance C_{pw}
  - Depends on **electronics circuit area** and **DNW/PW junction** width → additional capacitance for Active Pixels

Consequences of the additional interwell capacitance

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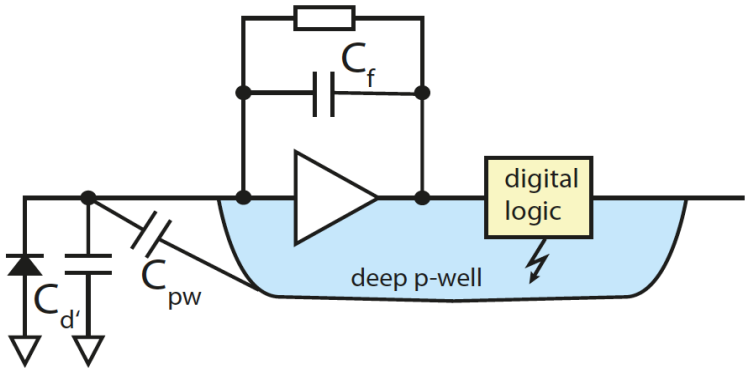
- larger total detector capacitance: $\mathbf{C_d} = C_{d'} + C_{pw}$

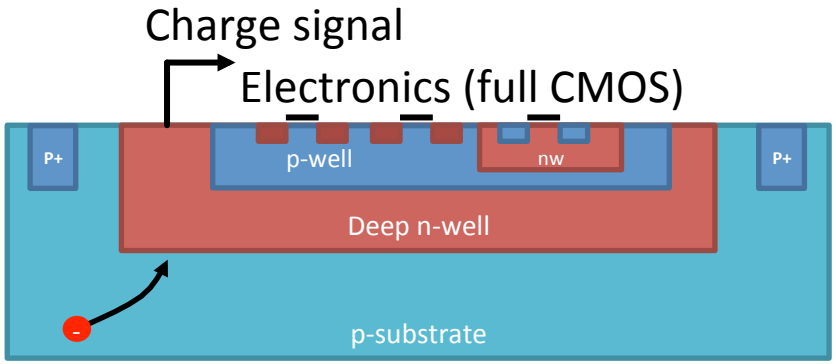


- noise $ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$
- timing $\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$

need to increase g_m to compensate
=> increased power ($g_m \propto I_d$)

- cross talking into sensor
  The PW/DNW capacitance C_{pw} directly couples into the sensor (the CSA imput node).
  Even with careful layout and low noise digital circuitry the operation threshold can be affected.
  For example: for C_{pw} = 100 fF, ΔV_{pw} = 1mV => $Q_{x\text{-}talk}$ = 625 e^-

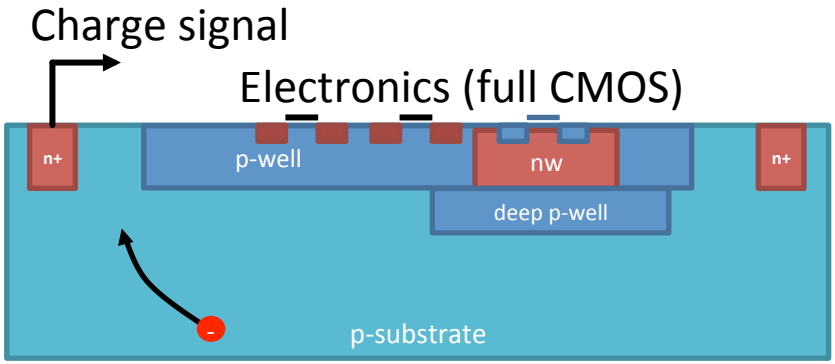
Design considerations: the charge collection (R/O) node



Electronics **inside** charge collection well

- Collection node with **large fill factor**
  → no low field regions
- on average **short(er) drift** distance
- **Large** sensor **capacitance** (DNW/PW junction!)
  → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

=> radiation tolerant
but larger C => noise, timing, power affected



Electronics **outside** charge collection well

- Very **small sensor capacitance** → low power
- Less radiation hard (longer average drift distances)
- Full CMOS with additional deep-p implant

=> low noise & low power (small C)
but less radiation tolerant

Enabling technologies

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"High" Voltage add-ons

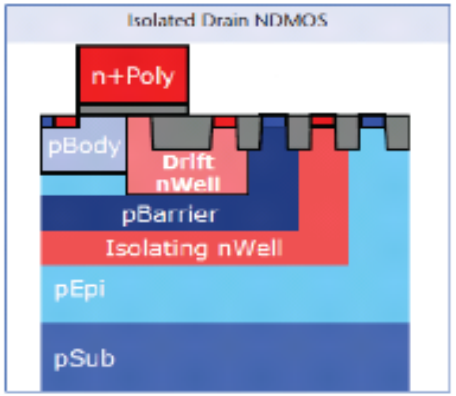
Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).

"High" Resistive Wafers

8" hi/mid **resistivity** silicon wafers **accepted/qualified by the foundry**. Create depletion layer due the high resistivity.

Technology features (130-180 nm)

Radiation hard processes with **multiple nested wells**. Foundry must accept some process/DRC changes in order to optimize the design for HEP.



from: www.xfab.com

Backside Processing

Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.

ATLAS: (1) Demonstrator program: active CMOS Pixel plus R/O Chip (still hybrid)
(2) R&D towards full monolitic DMAPS devices

BUT

- Industry does not care about particle detection (except photons)
  - they use cheap low resistive substrate Si (not depletable) … Q-coll by diffusion (slow)
  - some (CMOS camera) technology have a relatively thick epitaxial layer (~15 µm)

  ⇒ try to exploit special technology features to make detectors
  multiple wells, some (thin) depletion layer, backside contacts => optimize Q-coll.

Current **DMAPS** explorations

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- HV/HR technologies
  - HV CMOS
    - AMS 350 nm (Karlsruhe)
    - **AMS 180 nm (Karlsruhe)**
  - HR CMOS
    - **LFoundry 150 nm (Bonn, CPPM, IRFU** also **SLAC,** soon **KIT)**
    - Global Foundry 130 nm (CPPM, KIT)
    - ESPROS 150 nm (Bonn)
    - Toshiba 130 nm (Bonn)
    - **TowerJazz 180 nm (CERN** also Bonn/Strasbourg**)**
    - IBM T3 130 nm (LBNL)
    - STM 180 nm (INFN)
- SOI – CMOS Pixel
    - **XFAB 180 nm (Bonn)**

this talk

Route so far towards a DMAPS pixel sensor for ATLAS

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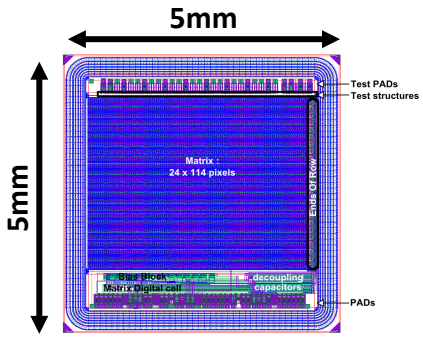
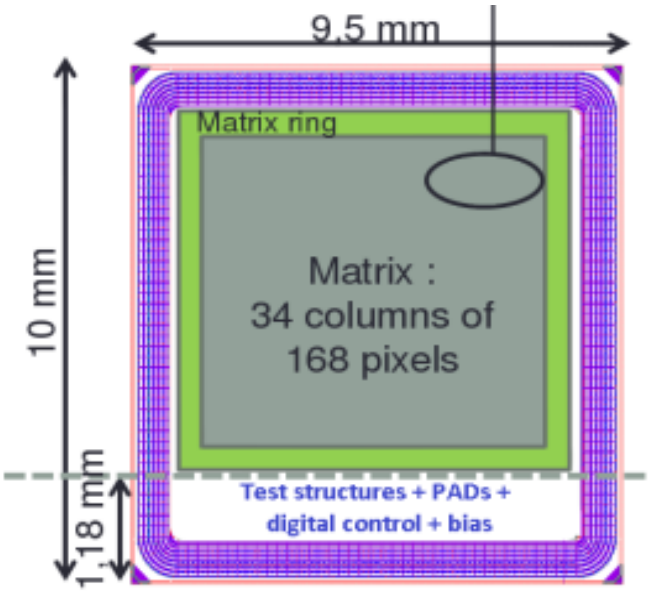
here: using LFoundry 150 nm CMOS technology

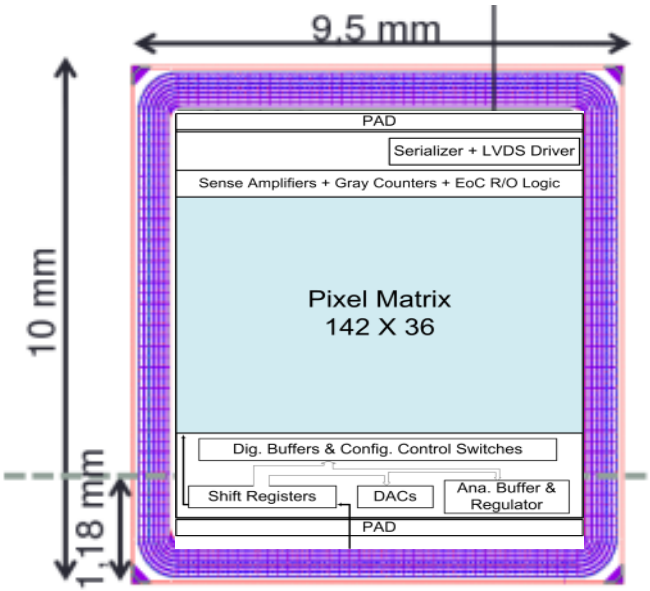
- 2kΩcm p-type bulk
- Bonn, CPPM (Marseille), IRFU (Saclay) collaboration
- also passive sensors designed in LF as a potential sensor alternative (see later)



CCPD_LF (A/B)
subm. Sep 2014
fast R/O coupled to FE-I4
also stand-alone testable
33 x 125 µm²

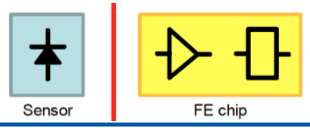


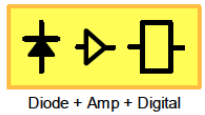
LF-CPIX Demonstrator
subm. March 2016
fast R/O coupled to FE-I4
also stand alone testable
50 x 250 µm² pixels



LF-Monopix01
subm. Aug. 2016
LF_CPIX Demo + stand-alone fast R/O
column drain type R/O variants

A comparison ...





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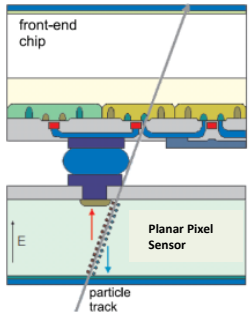
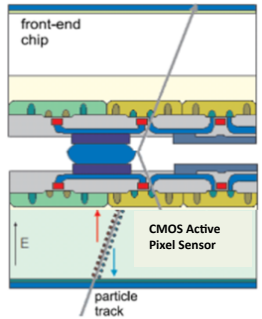
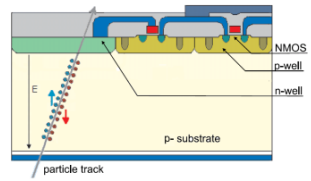
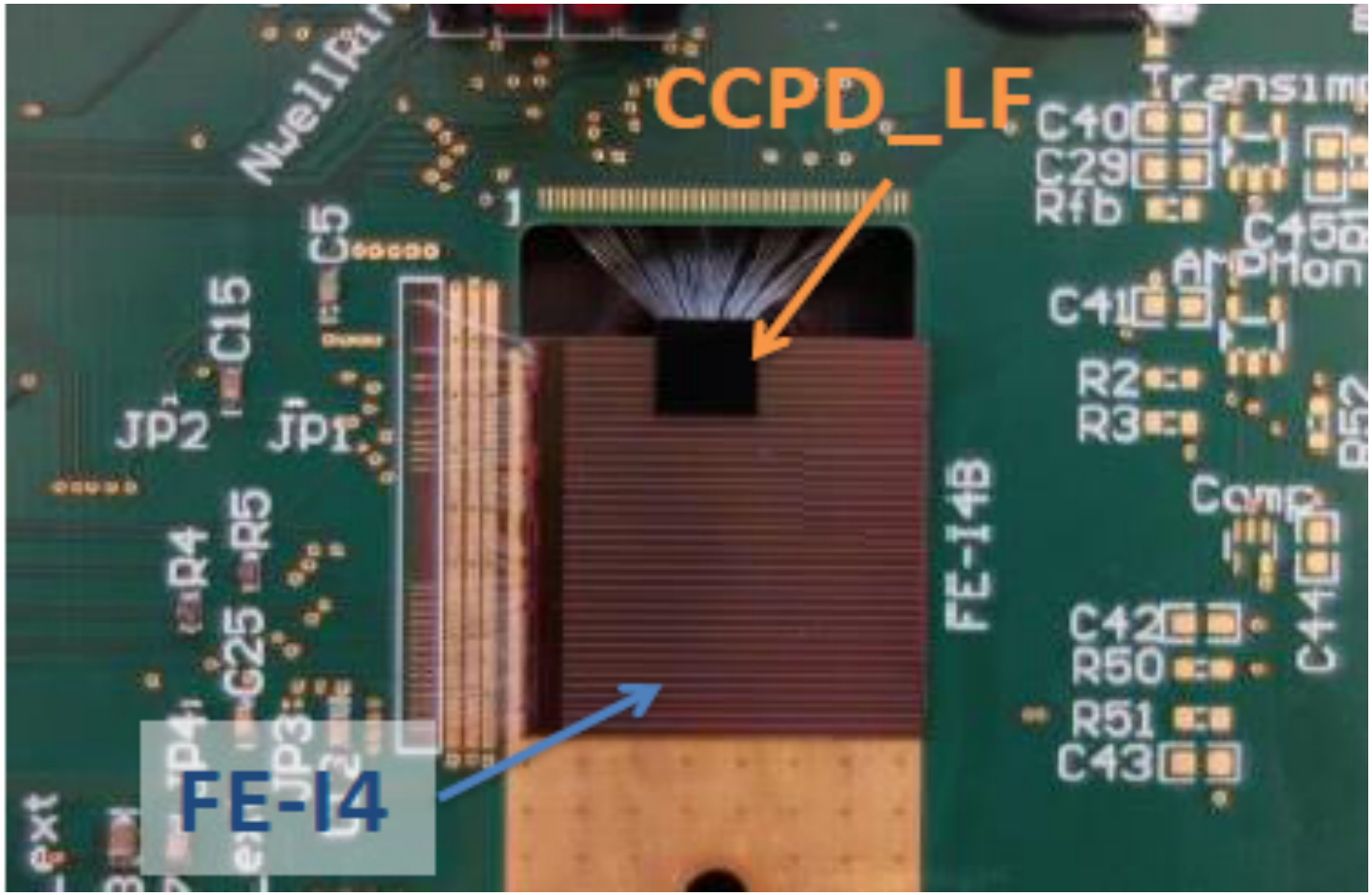






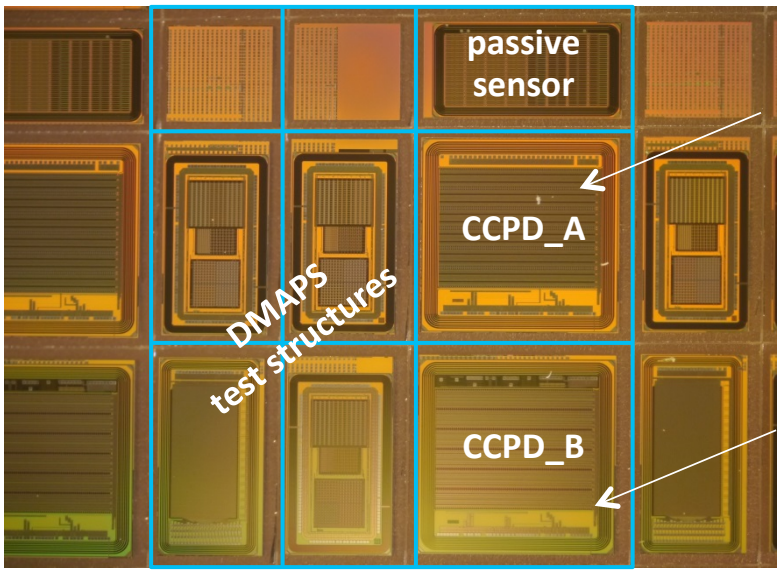
	Standard Hybrid Pixel Detector	CMOS Active Pixel Hybrid Detector	Fully Depleted Monolithic Pixel Detector
TID radiation hardness (electronics)	reference (65nm)	similar / worse (65nm R/O chip, ~150nm sensor)	similar, possibly worse (130nm -180 nm technology)
NIEL radiation hardness (sensor)	good (planar) very good (3D)	good (as planar, tbc)	good (as planar, tbc)
Power consumption	reference	worse (increased input capacitance)	worse (increased input capacitance, non std. digital logic)
Material budget (silicon only)	reference	equal	better
Assembly costs	reference (bump bonding)	equal (still needs bump bonding or glue + TSV)	**best**
Silicon costs	reference (high)	better (active CMOS sensor cheaper than planar)	**best**
Integration density (min. pixel size)	reference (50µm pixels)	possibly better	likely worse
Features/challenges		sub-pixel encoding	isolation of analog FE and digital activity

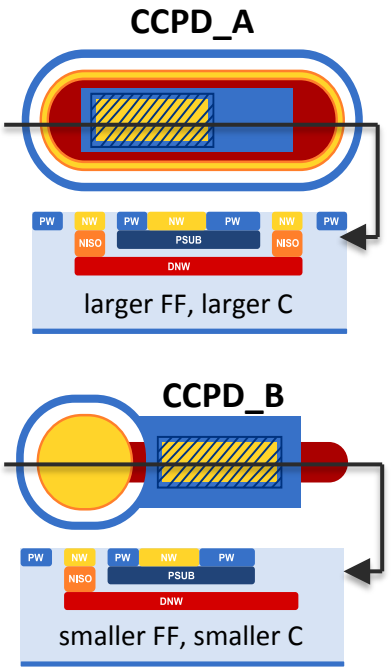
CCPD_LF bonded (w/ SnAg bumps) to FE-I4

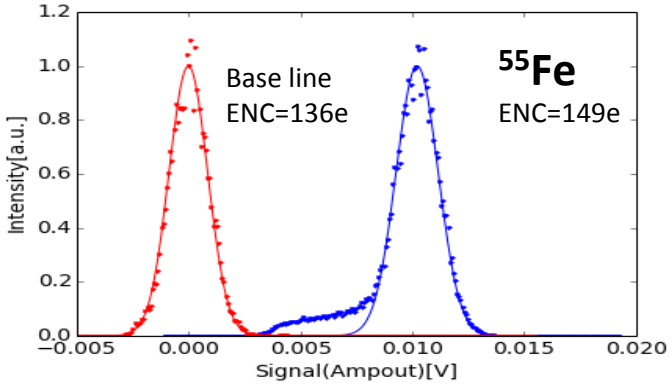


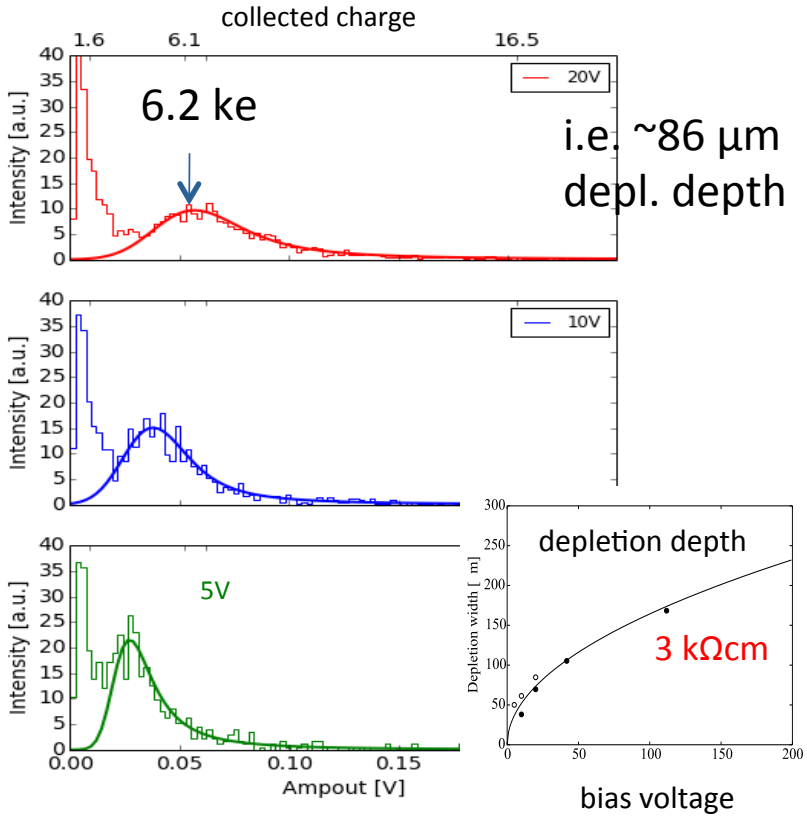
Results from CCPD_LF prototype

- **Signal spectra** (sources and 3.2 GeV e⁻ beam)
  - 160µm depletion width @ 110V bias
  - Noise ~150 (100)e⁻ for version A (B, low cap.)
- **Time walk**
  - Fraction of "in-time (25ns)" hits
    - Low threshold : 79%
    - High threshold : 91%







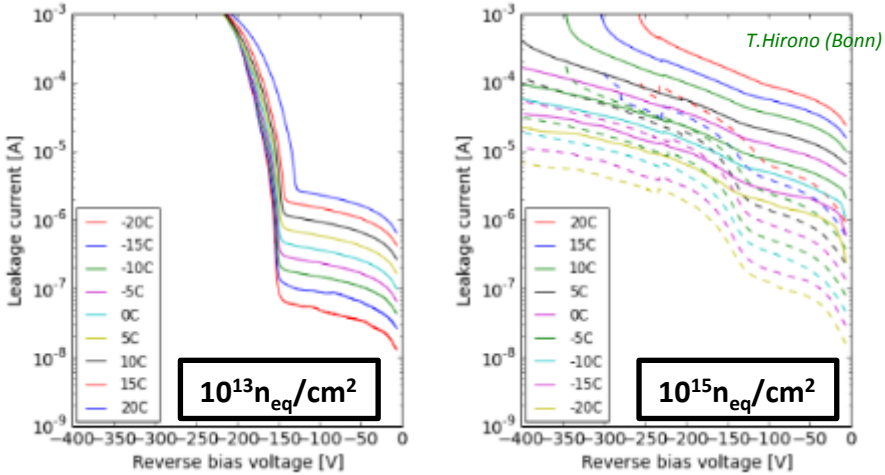


P. Rymaszewski et al., JINST 11 (2016) 02 C02045
T. Hirono et al., doi:10.1016/j.nima.2016.01.088

LFoundry 150 nm irradiation performance

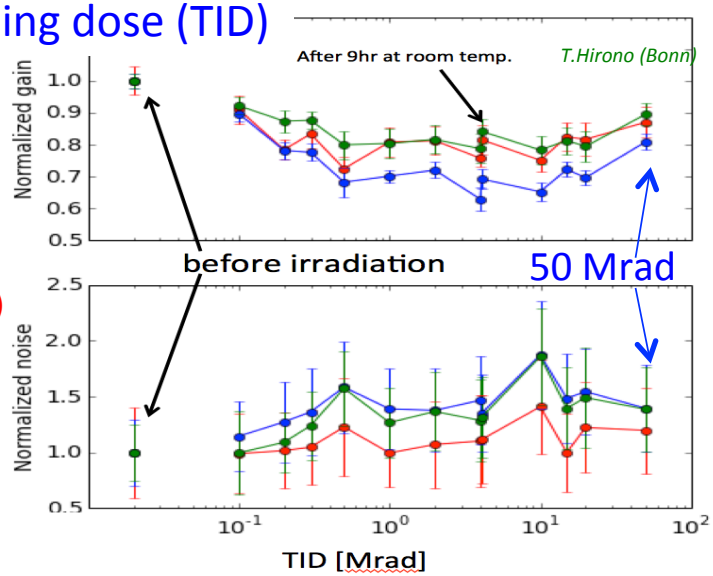
universitätbonn

Sensor reverse current

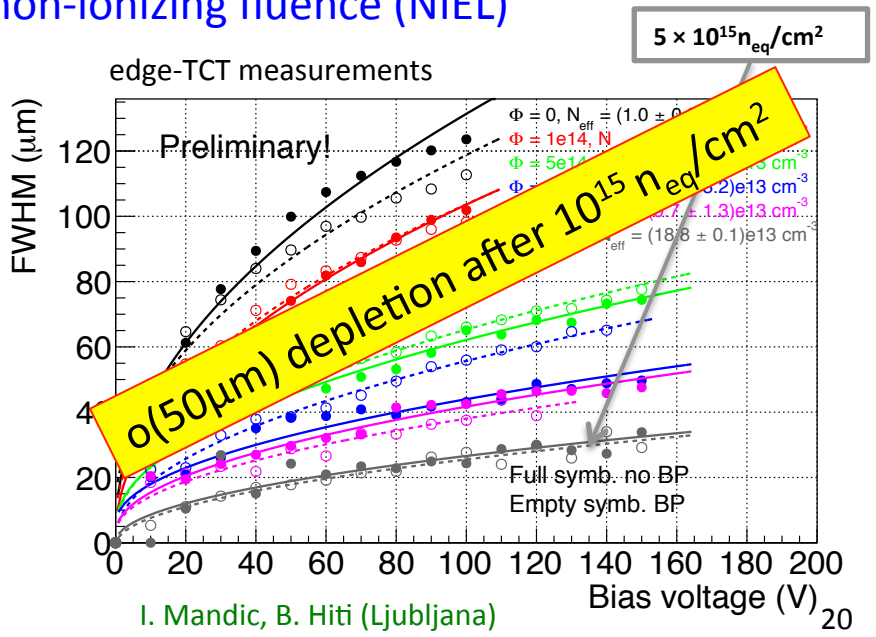


total ionizing dose (TID)

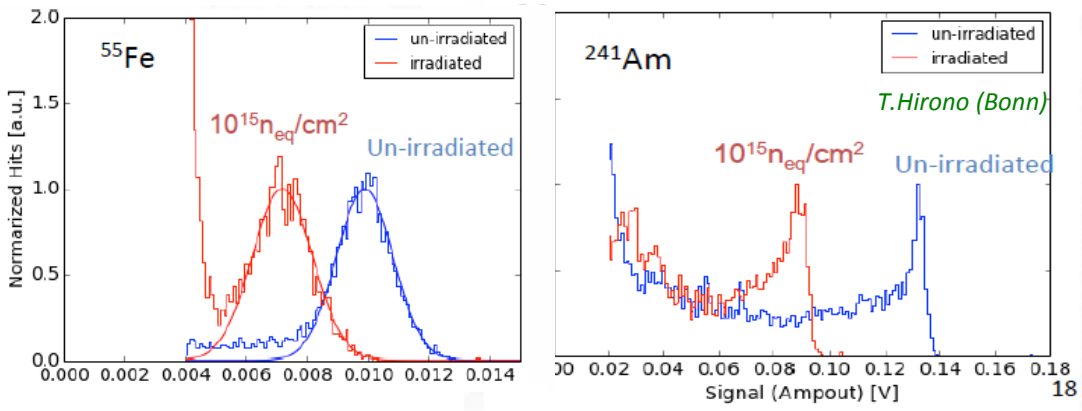
Normal (L=0.9um)
Long (L=1.5um)
Enclosed Layout (ELT)



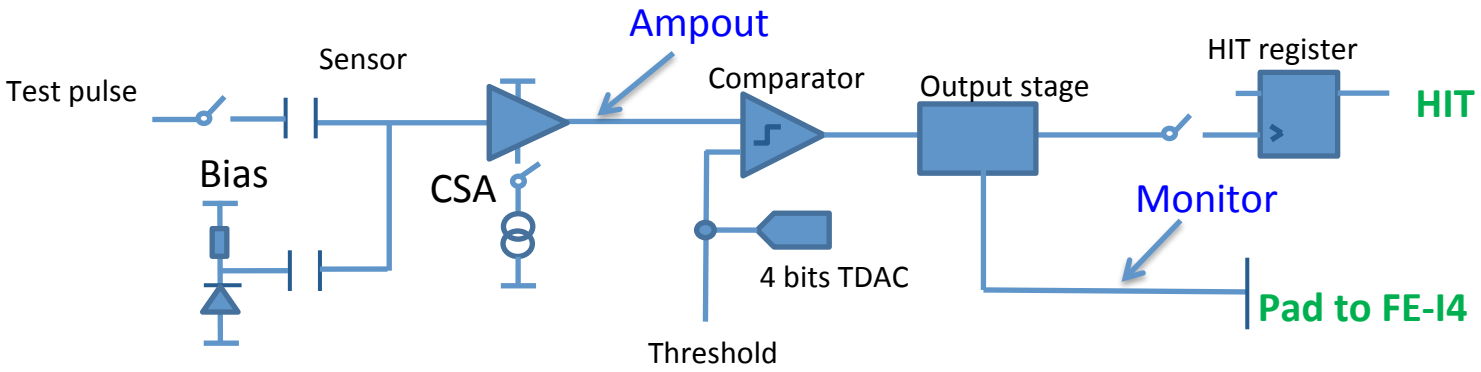
non-ionizing fluence (NIEL)



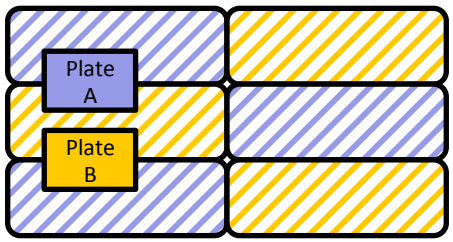
Spectra: **^{55}Fe and ^{241}Am** after **$10^{15}n_{eq}/cm^2$** (bias 100V/125 V)



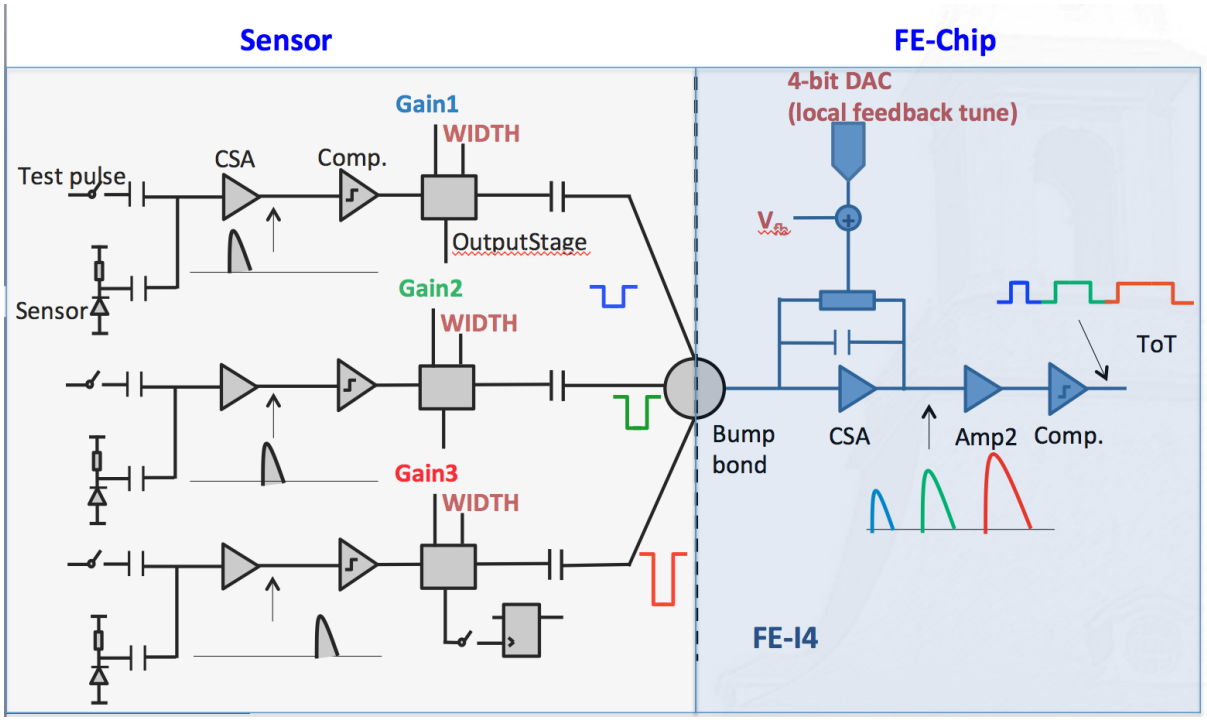
LFoundry CCPD_LF: sub-pixel decoding



33x125 µm^2



in-pixel decoding
by pulse height

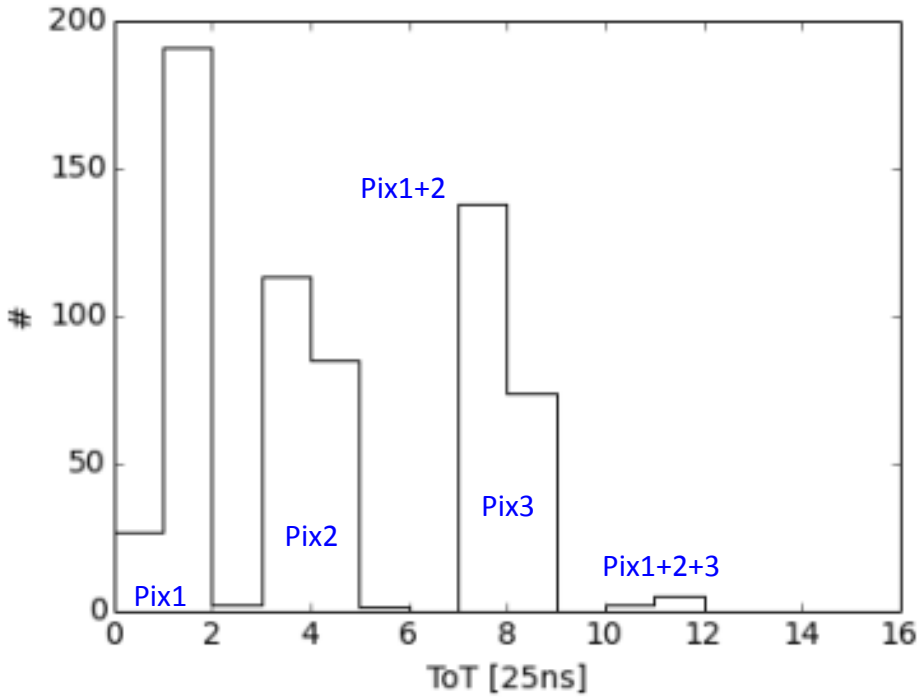


LFoundry CCPD_LF: sub-pixel decoding

universitätbonn

Test in 3.2 GeV electron beam (ELSA, Bonn)

ToT response to hits in one and the same FEI4 pixel (50 x 250 µm^2)



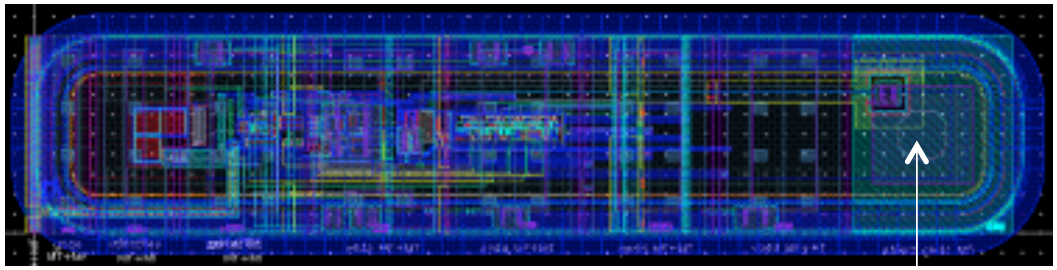
T.Hirono (Bonn)

- Sub-pixel decoding seems to work at least in principle (low rate)

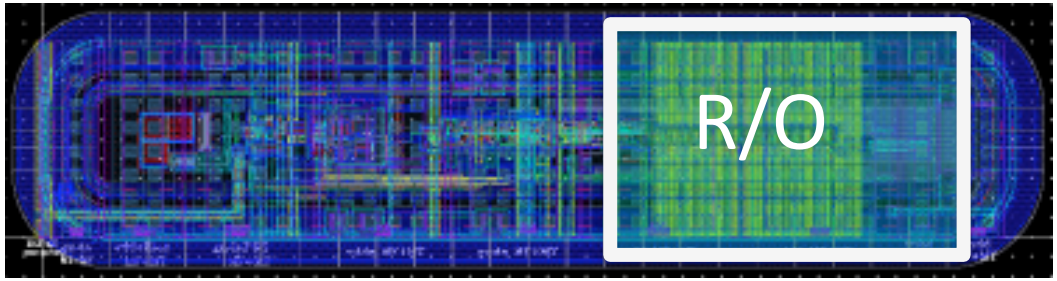
LFoundry Demonstrator and MONOPIX-01

universitätbonn

LF-CPIX Demonstrator (1x1cm^2, 158 x 36 pixels, 50 x 250 µm^2)



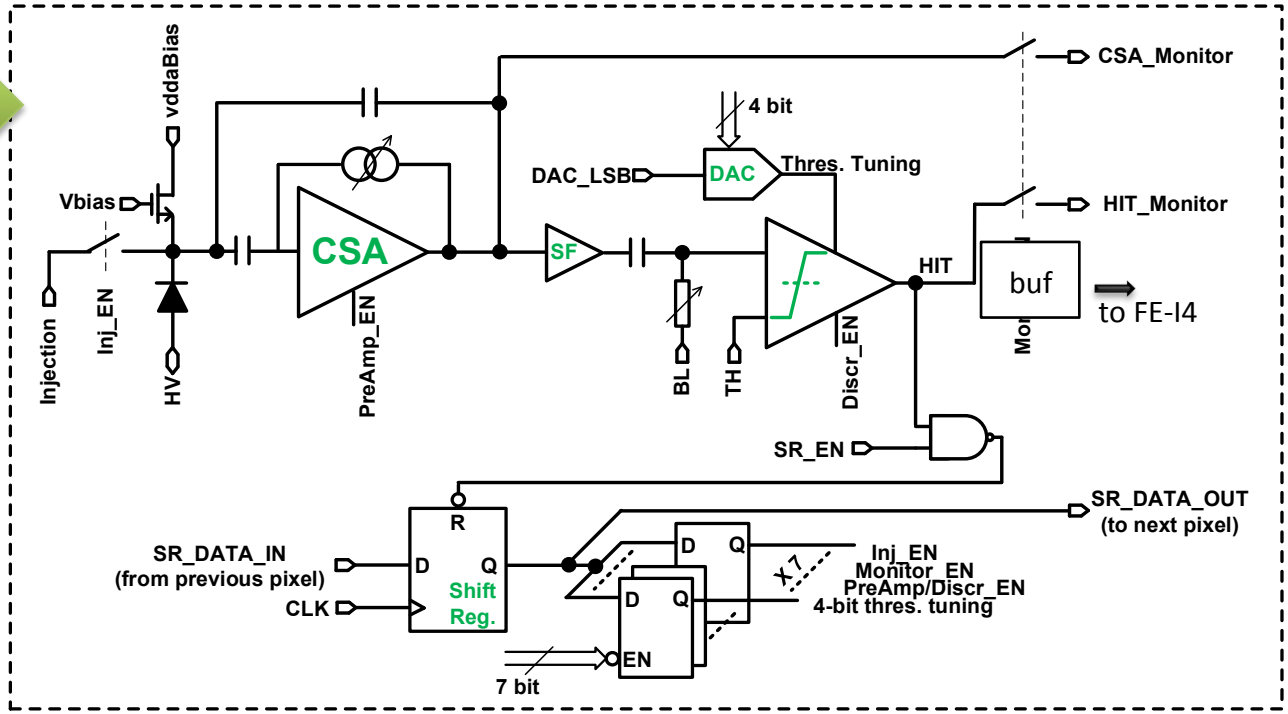
LF-Monopix 01 (1x1cm^2 142 x 36 pixels, 50 x 250 µm^2)



- Same analog parts
  9 different flavors in LF_Demo
- Full custom R/O logic to minimize the digital p-well area
  (different low coupling transmission schemes)
- Shielding of lines carrying logic signals
- Separated digital & analog substrates
- Separated digital ground and bulk connection

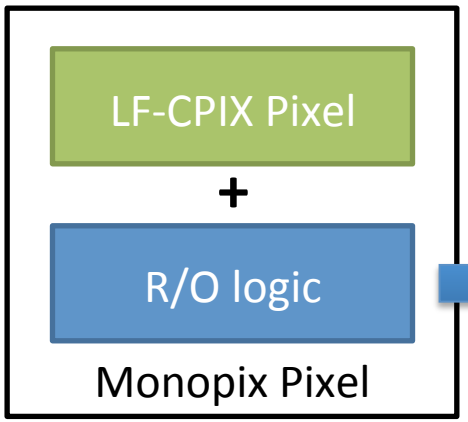
LF-CPIX Demonstrator Pixel Electronics

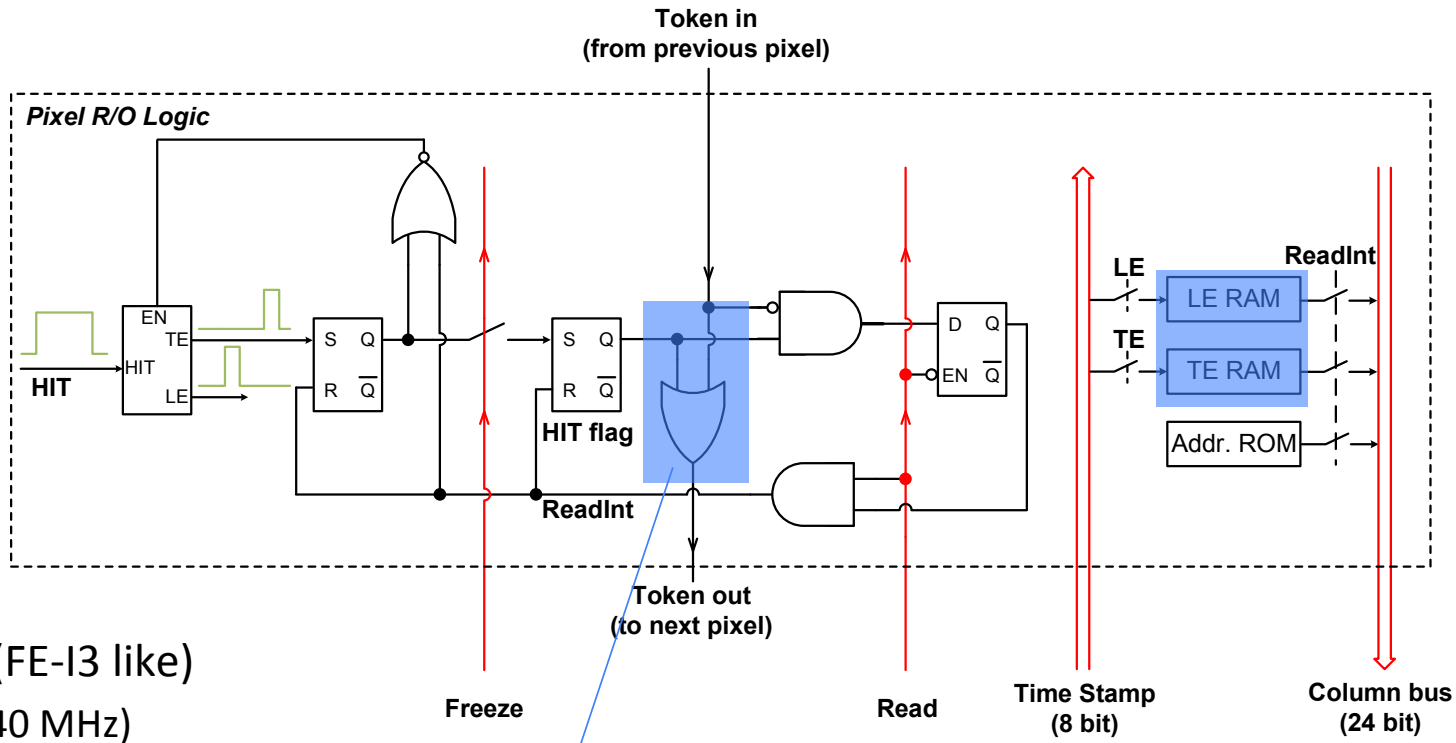
LF-CPIX Pixel



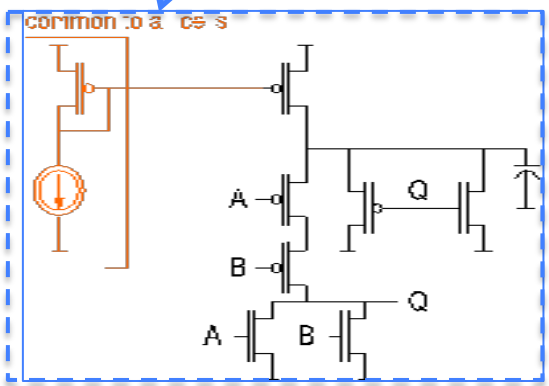
- Charge Sensitive Amplifier
  - AC coupled to sensing diode
  - Two variants: NMOS & CMOS inputs
- Discriminator
  - 4-bit threshold trim
  - Pulse width ∝ charge signal (ToT)
- 7-bit latch in every pixel
  - PreAmp/Discr. enable
  - Output monitor enable
  - Injection enable
  - threshold trimming (4 bit)
- Shift register
  - Write configuration data / Read hit data

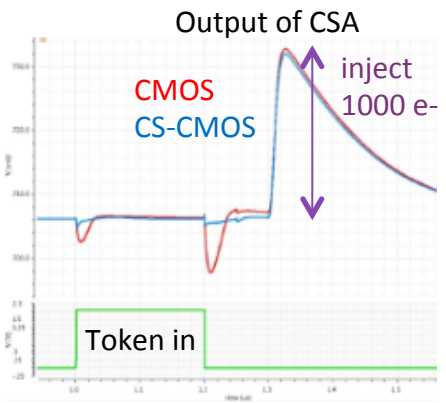
Monopix R/O Logic



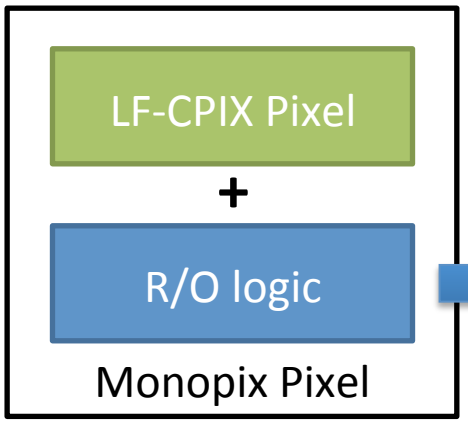


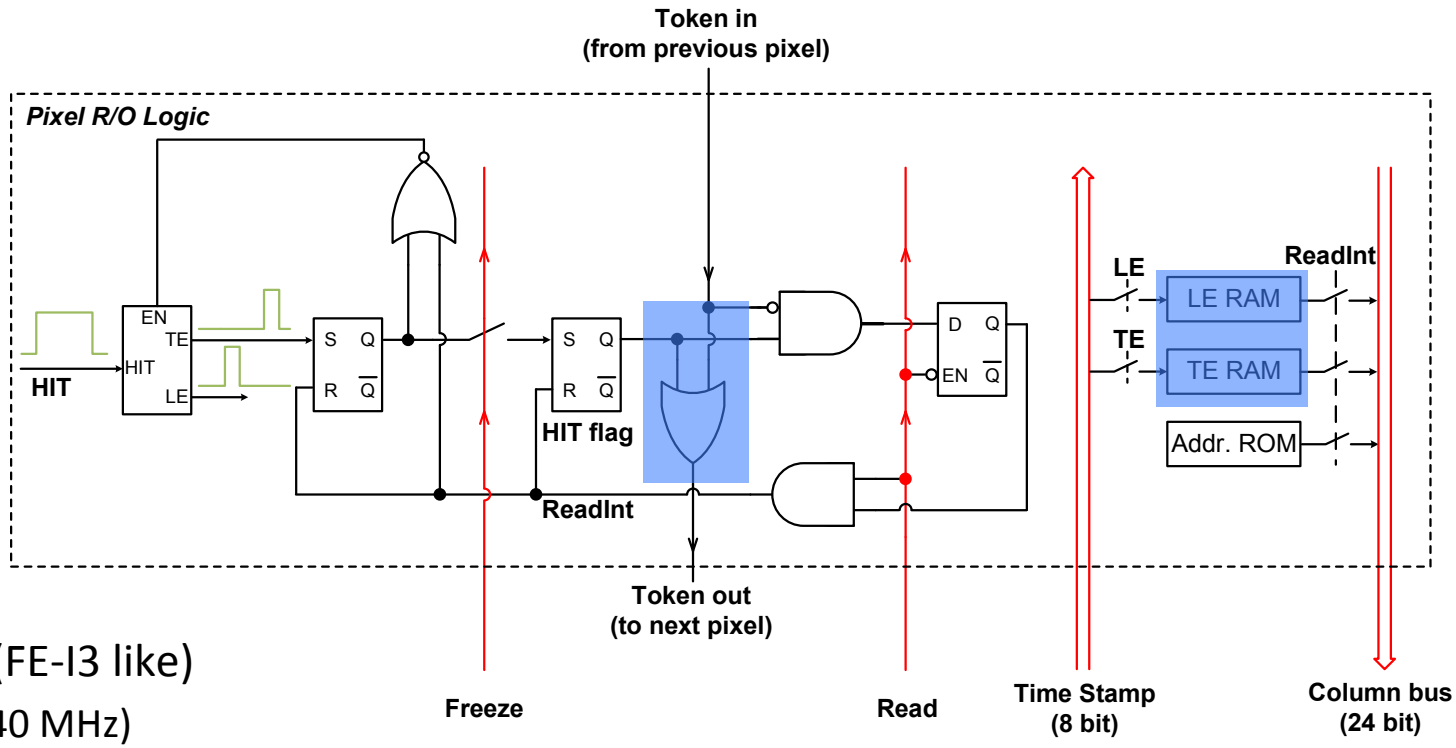
- Column-drain R/O logic (FE-I3 like)
  - 8-bit gray coded ToT (40 MHz)
  - LE RAM: leading edge time stamp
  - TE RAM: trailing edge time stamp
- Distribution of column signals (low noise)
  - Token → **current steering logic**
  - Time stamps (LE, TE) → **differential mode plus source follower**





Monopix R/O Logic





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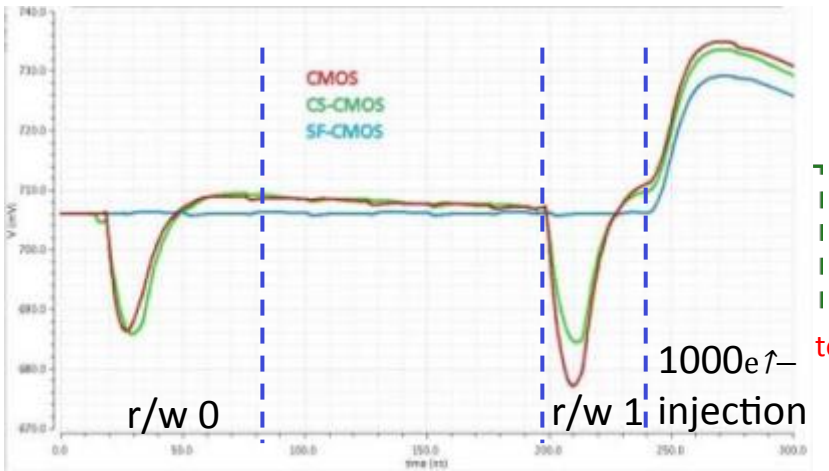

Developments in AMS 180nm and 350nm (HV-CMOS)

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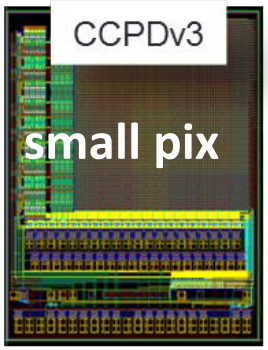
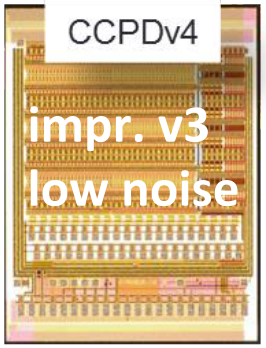
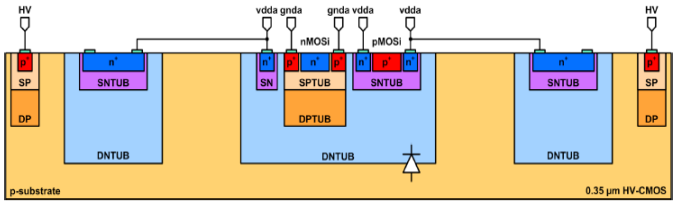
$$d \sim \sqrt{\rho \cdot V}$$

4 versions since 2011
demonstrator 12/2015





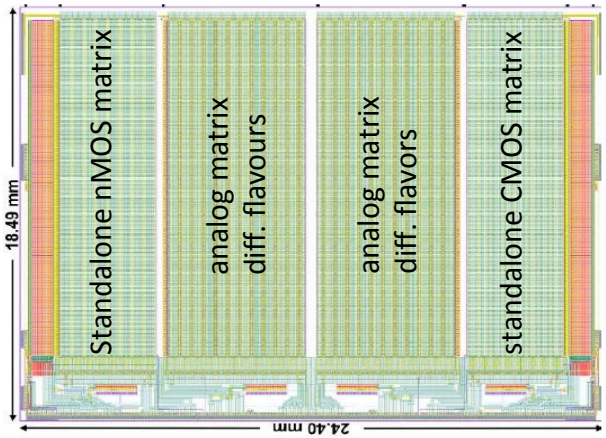
I. Peric et al. Nucl.Instrum.Meth. A582 (2007) 876-885
Nucl.Instrum.Meth. A765 (2014) 172-176



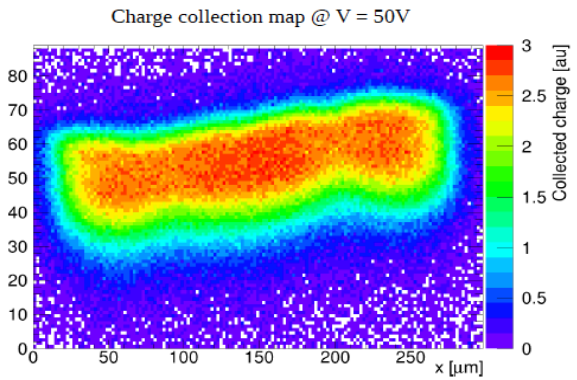
AMS specs

- ρ = 10 Ωcm – 1 kΩcm
- triple-well technology (partial CMOS)
- depletion depth >10 µm (incr. w/ irrad.)
- R/O via ATLAS pixel chip FE-I4 (CCPD)
- large monolithic chip (350 nm)

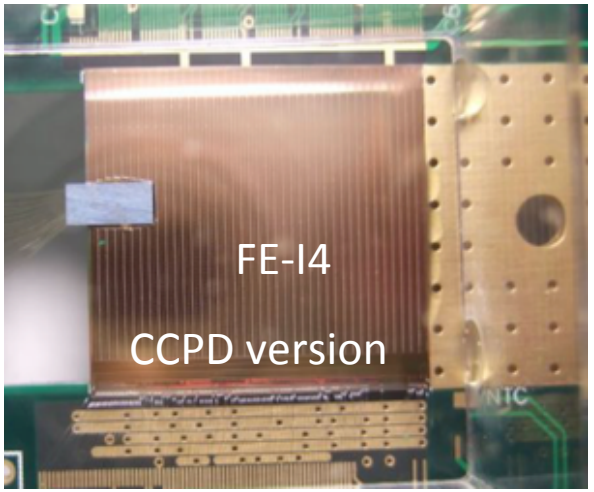
aH35 H35DEMO



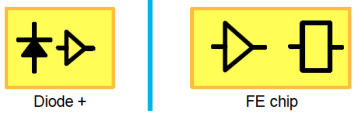
- bias up to 160 V



Edge TCT of H35DEMO Pixel 200 Ωcm
Pixel active on full length, 20-30 µm depletion



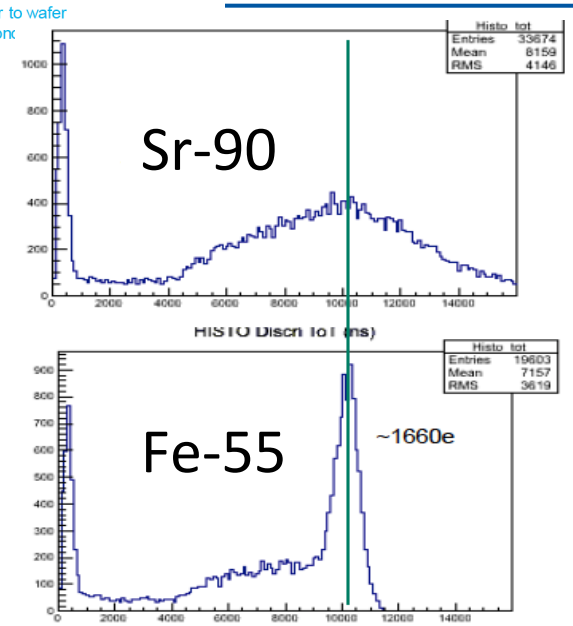
AMS 180 nm (bonded to FE-I4)



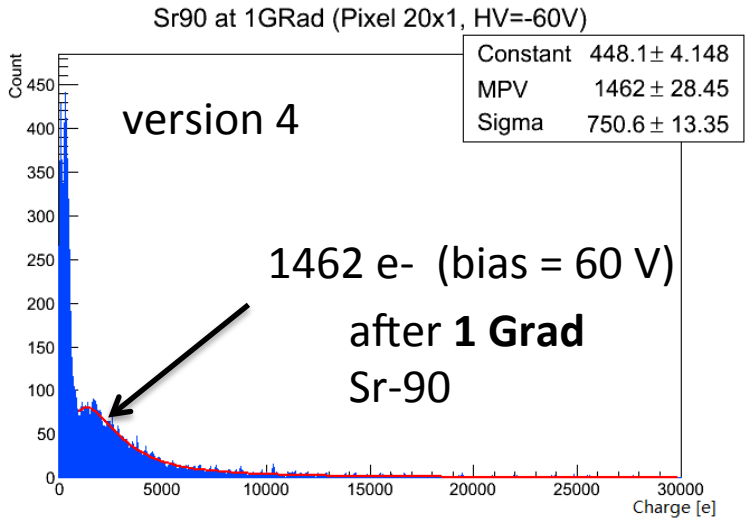
universitätbonn

- **Capacitive coupling** (glue bonding) seems to work
  whether it is competitive in terms of reliability and price is unclear; electrical contacts through TSV's? mass production?
- **TIDs** up to **1 Grad**
- **NIEL** irradiation to **> 10^{16} n_{eq}/cm^2** performed
- efficiency (time integrated): 99% -> **96%**
- signal ~1500 e ; SNR ~25
- **in-time efficiency** still to be improved
  in CCPD versions (τ_{rise}~100 ns)
  has been about met in H35DEMO

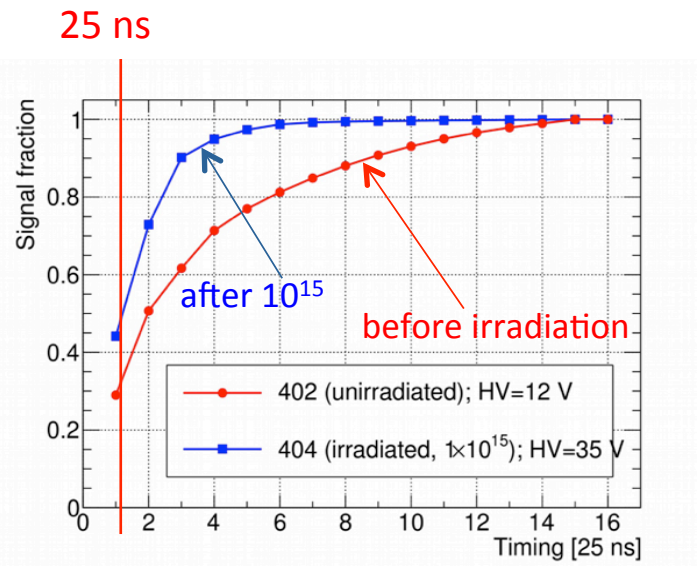
Wafer to wafer bonc



version 2
before
irradiation



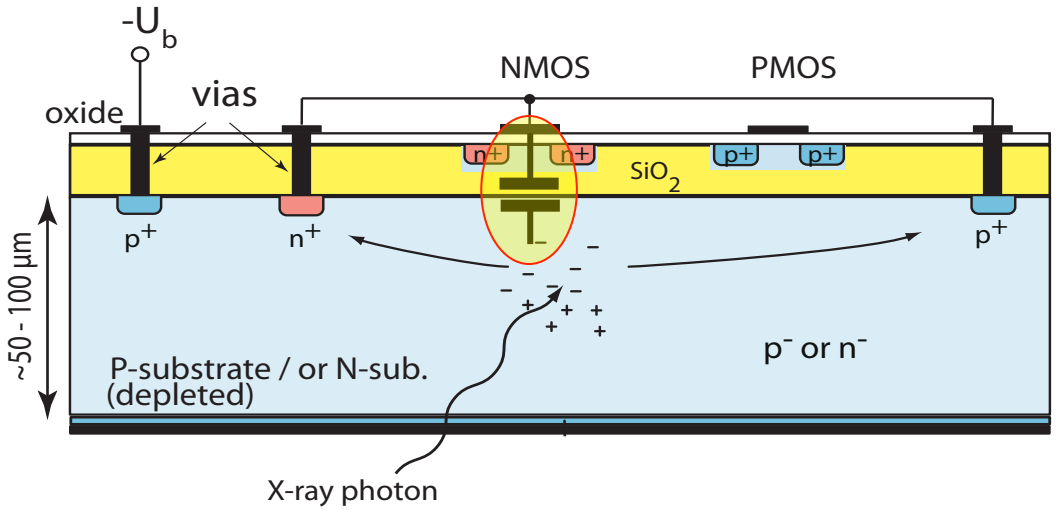
acceptor removal effect



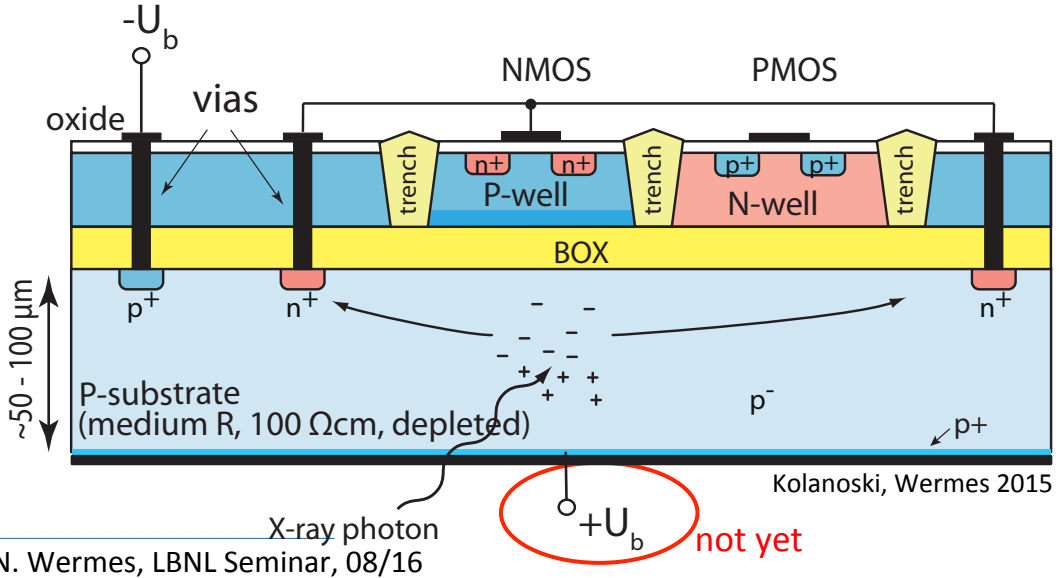
CMOS on SOI

CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$



- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al.
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- not suited for LHC - pp



- **HV-SOI (thick film)**
- Hemperek, Kishishita, Krüger, NW
  Nucl.Instrum.Meth. A796 (2015) 8-12
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

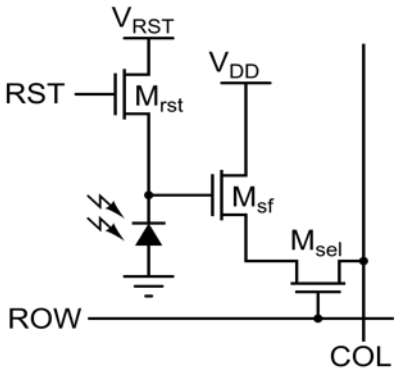
HV-SOI: test chips XTB01 and XTB02

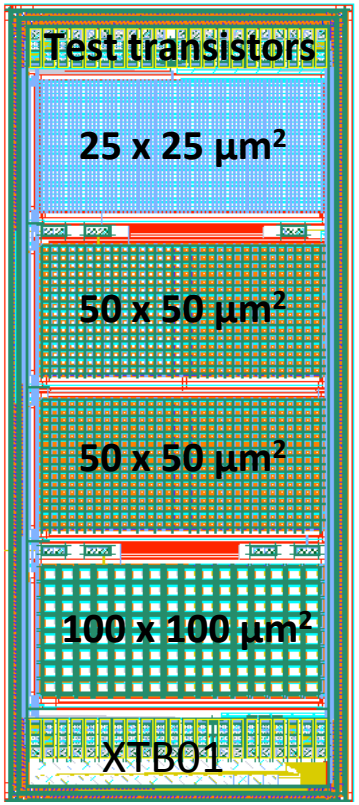
universitätbonn

XFAB 180 nm: Electronics outside collection well

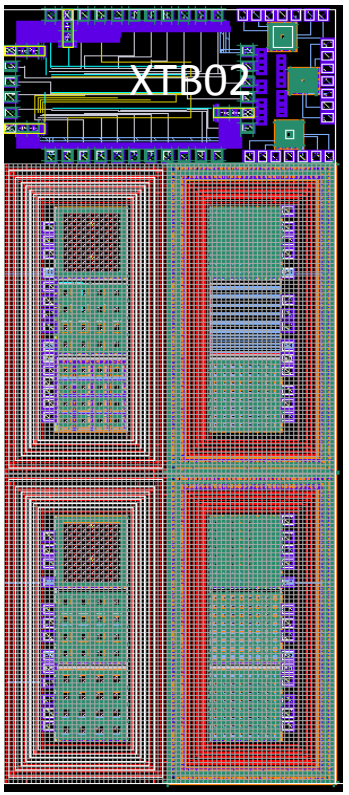
- Small charge collection well
- Full CMOS, no backgate effect
  due to isolation via deep p-well (non-depleted)
  between CMOS layer and BOX
- HV technology + med-R substrate (100 Ωcm), p bulk

- simple 3 T readout
  => no CSA
  => no in-time measm'ts





Design: Bonn
Testing: Bonn, CERN



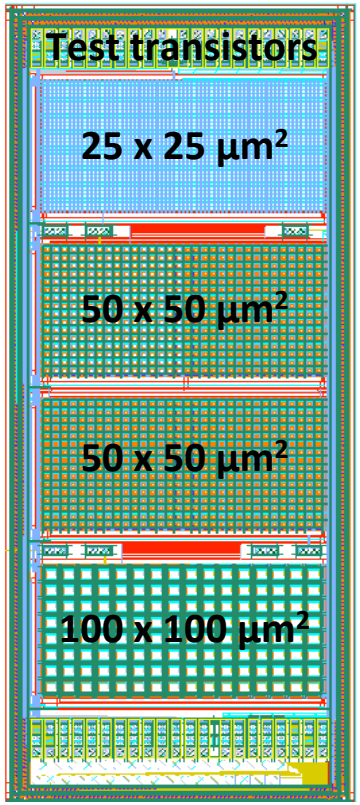
dedicated structures to test the technology further (leakage, break down voltage, etc.)

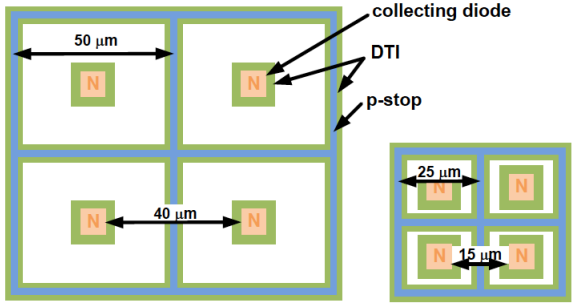
irradiations so far:

TID: 700 Mrad

Fluence: up to $5x10^{13}$ n_{eq}/cm^2 and $5x10^{14}$ n_{eq}/cm^2

XFAB SOI XTB01 prototype chip: irradiation tests

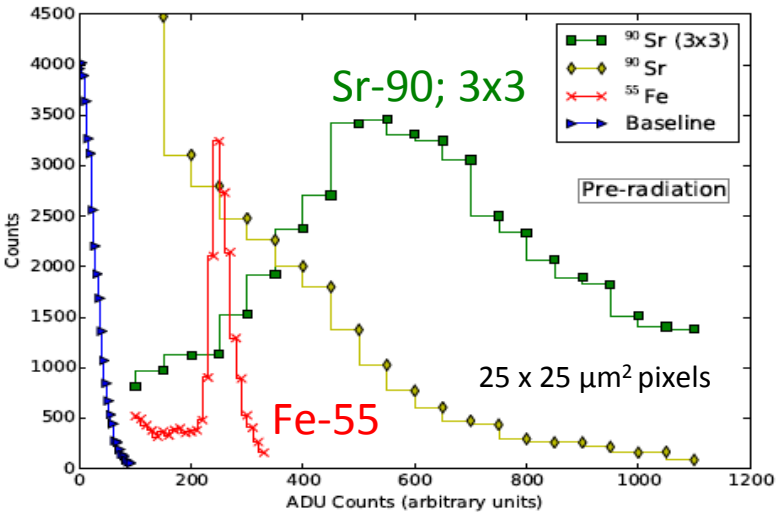




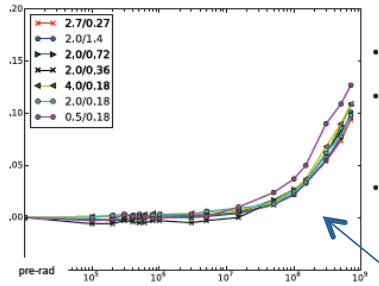
NIEL

TID

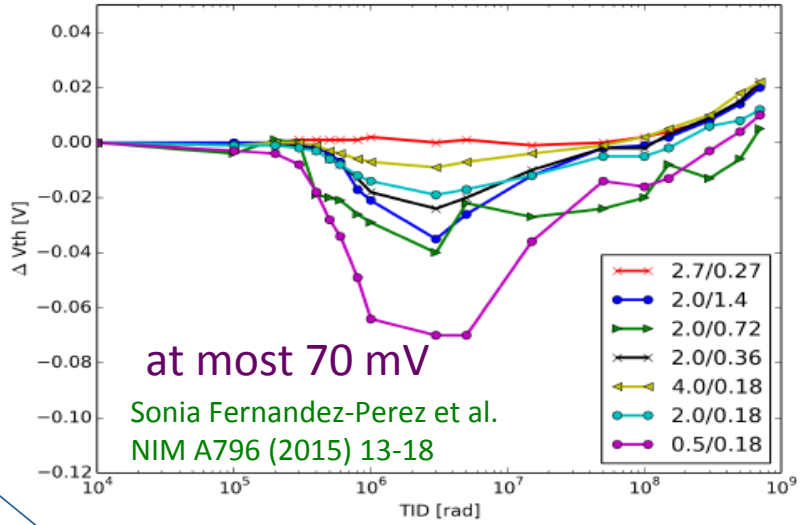
before irradiation



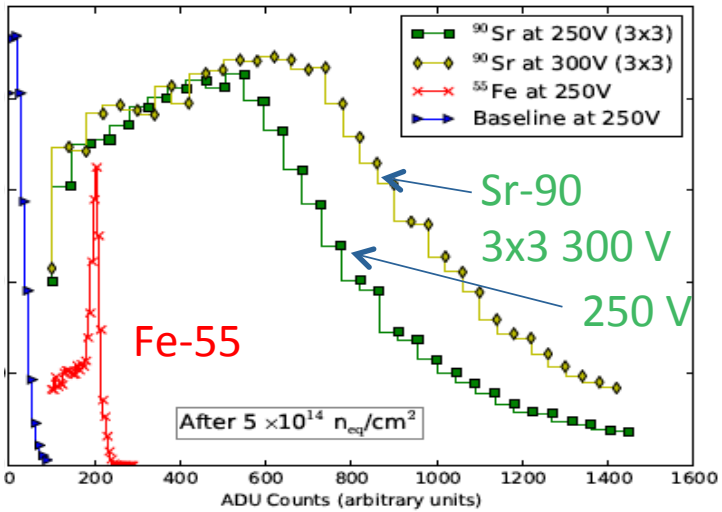
PMOS



NMOS threshold shift after **700 Mrad**



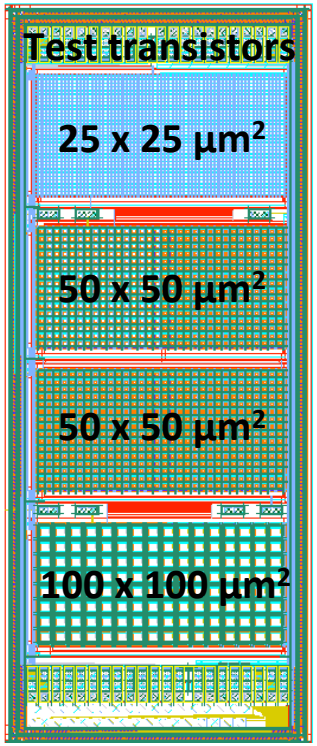
after irradiation: **5 x 10^{14}** n_{eq}/cm^2



PMOS shift ~100 mV after 1 Grad

Hemperek, Kishishita, Krüger, NW
JINST 10 (2015) no.03, C03047

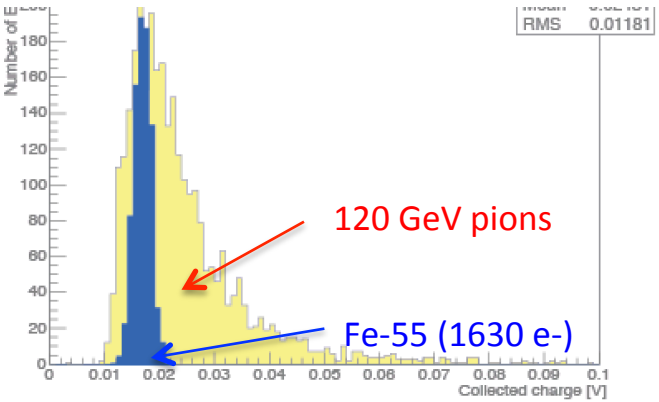
SOI - CMOS



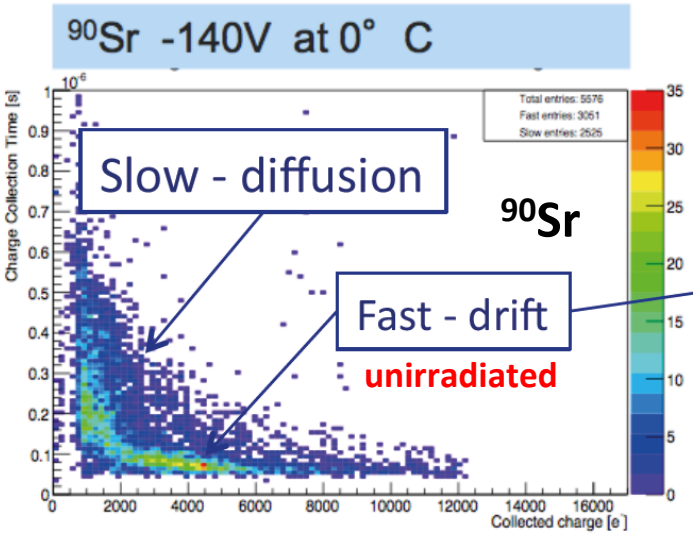
XFAB 180 nm: CMOS electronics outside well collection

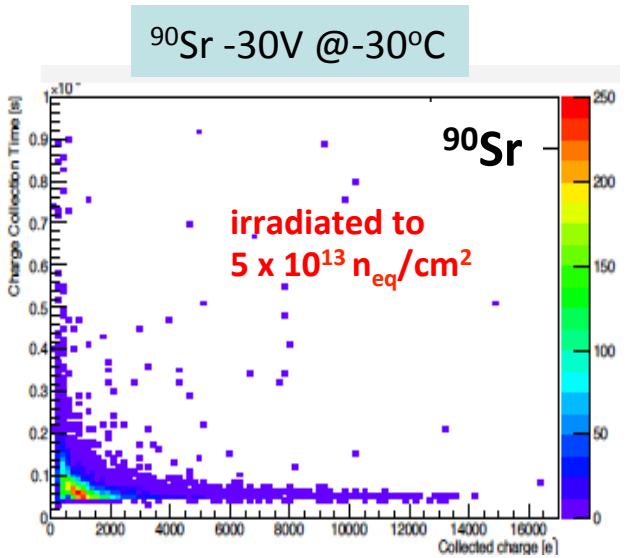
- Small charge collection well -> small C
- HV + medium-R (100 Ωcm), p bulk
- simple 3 T readout

TID: 700 Mrad
up to 5x10^{14} n_{eq}/cm^2



S. Fernandez-Perez et al., NIM A796 (2015) 13-18





observation:
charge collected from high-field (fast drift) and low field (slow diffusion) regions

acceptor removal (likely) sets in => resistivity increases
=> larger "drift" - volume

Tower Jazz 180nm Investigator

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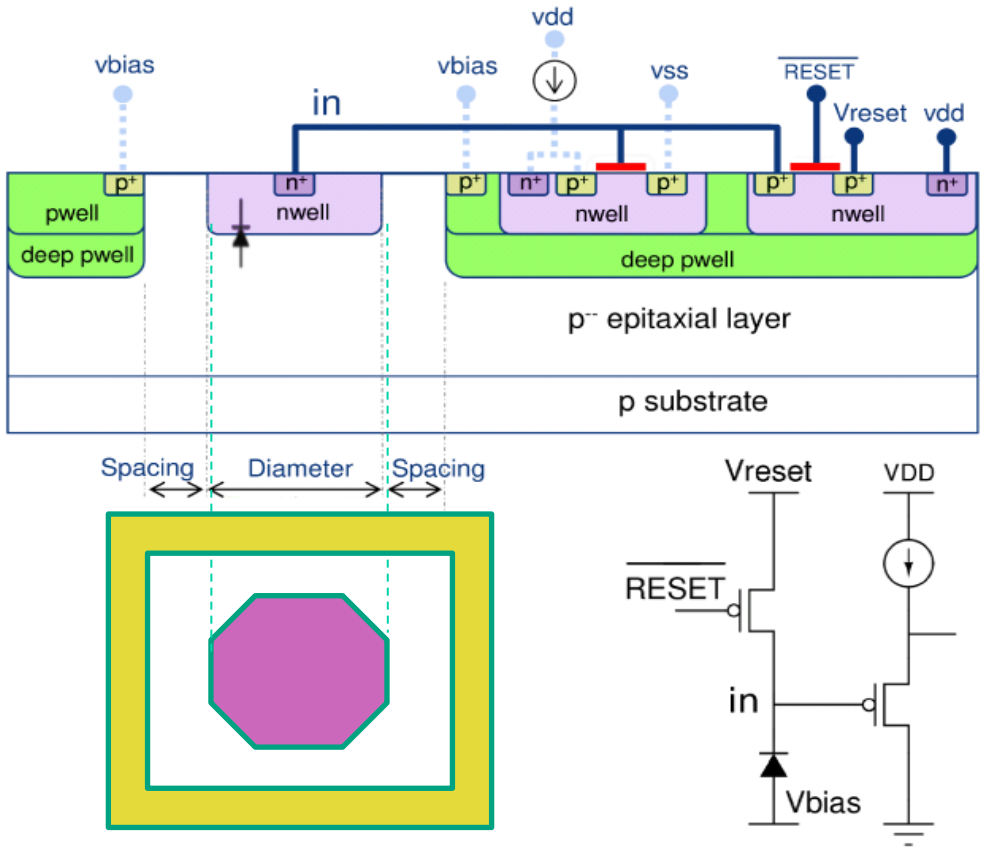
Technology

TowerJazz 180 nm CMOS imaging process

- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Epitaxial layer
  - Thickness: 18 – 40 µm
  - High resistivity: 1 – 8 kΩ·cm
- Reverse substrate bias



These measurements all on 25um EPI:

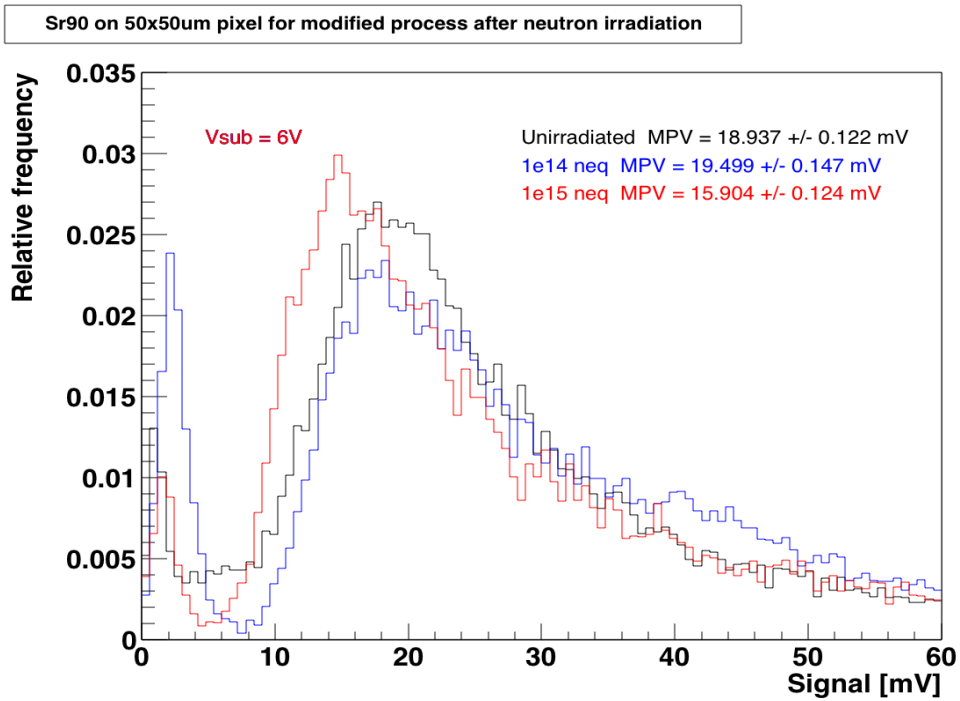
•50x50um pixel size

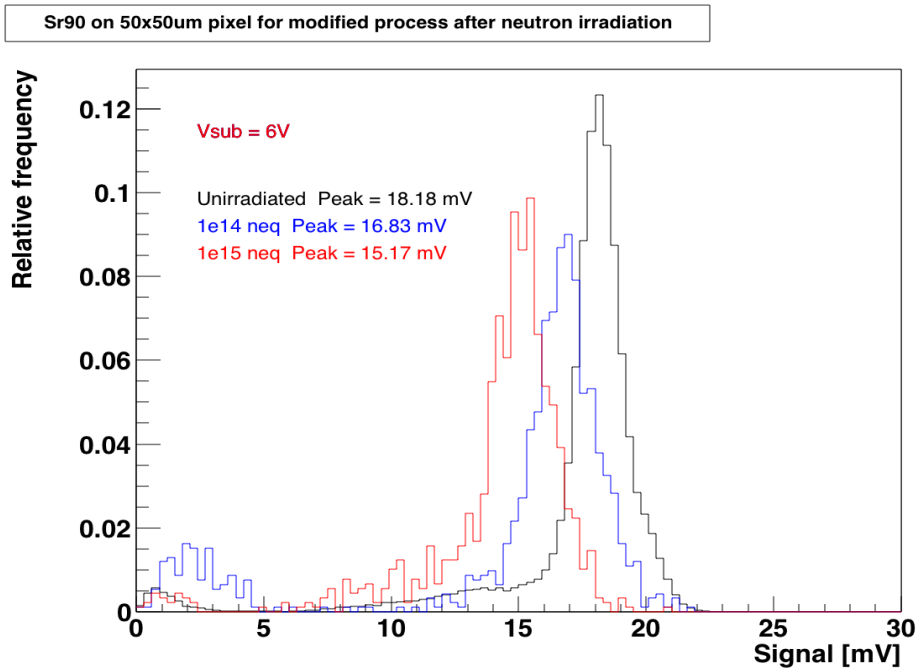
•20x20um pixel size

Small collection NW in p-type epi to minimize capacitance (2-5fF)
Modified process to improve lateral depletion and in particular charge collection after irradiation - new chips with 25um epi now irradiated

TJ results on Investigator

- Structures irradiated up to 10^{15} neutrons/cm2
- Measure signal before / after with Sr and Fe sources

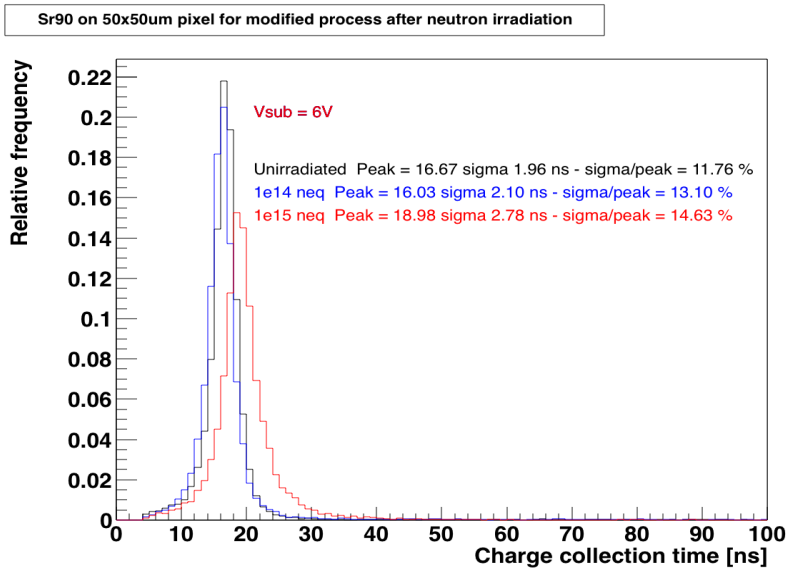


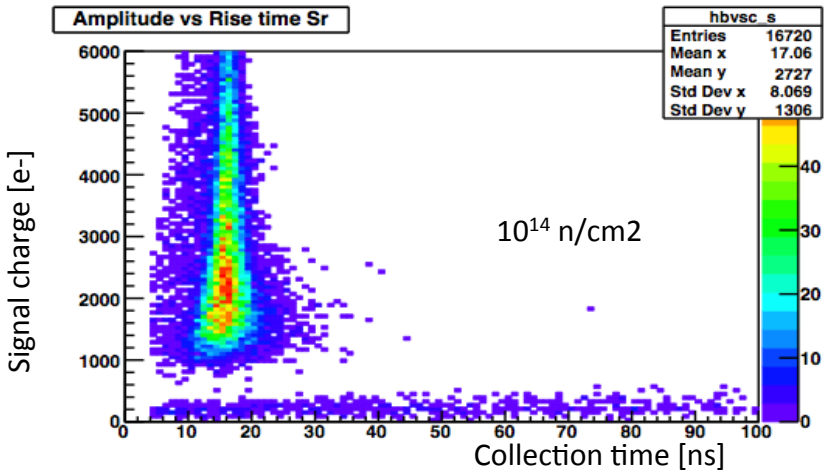


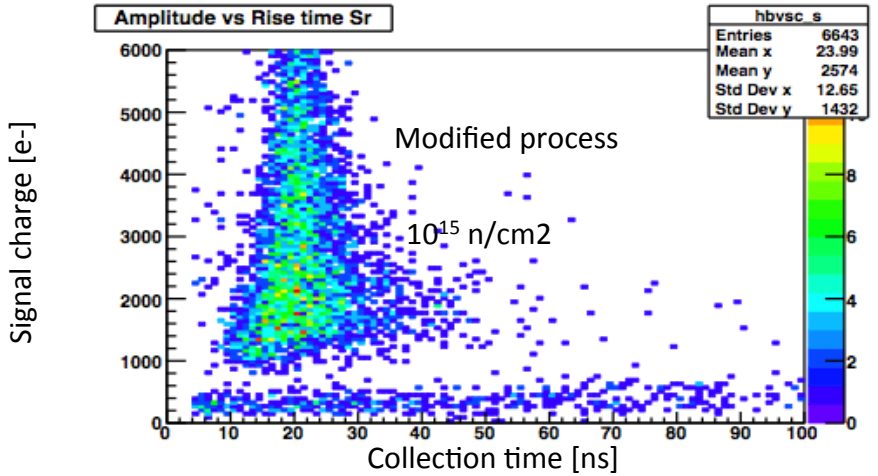
Christian Riegel, Doug Schaefer (CERN)

TJ Investigator after irradiation

- First indications are full charge collection, good noise separation and collection times <25ns
- Currently measuring efficiency and uniformity in testbeams and DIAMOND X-ray beam







Christian Riegel, Doug Schaefer (CERN)

Not sexy ... but cheap and easy

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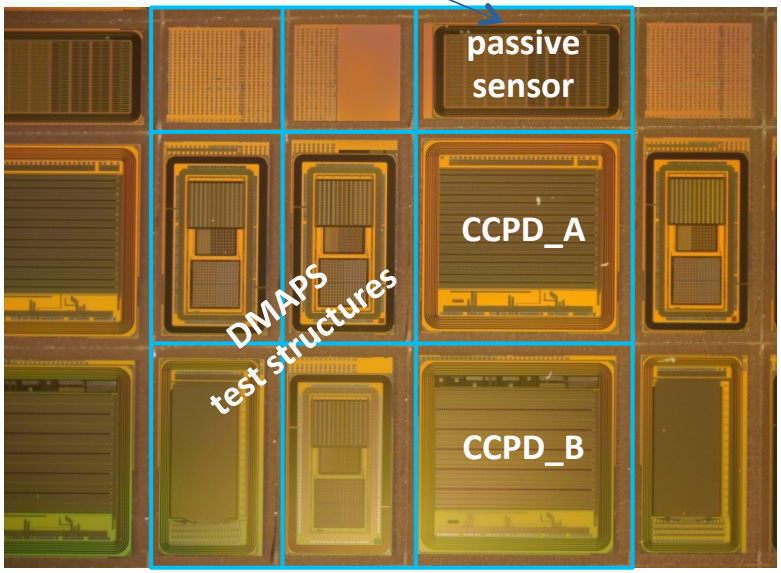
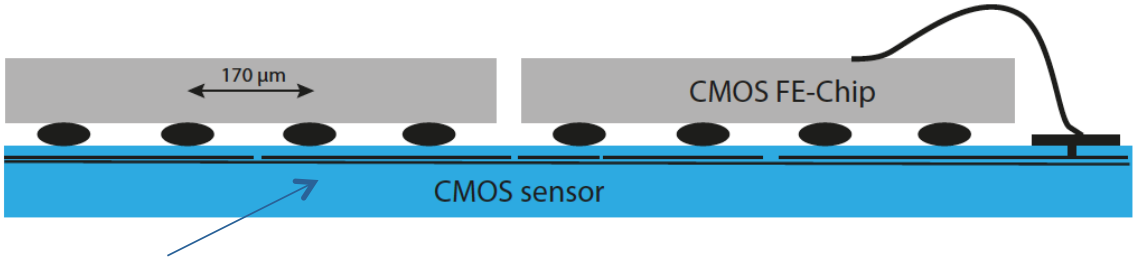
Passive CMOS technology sensors

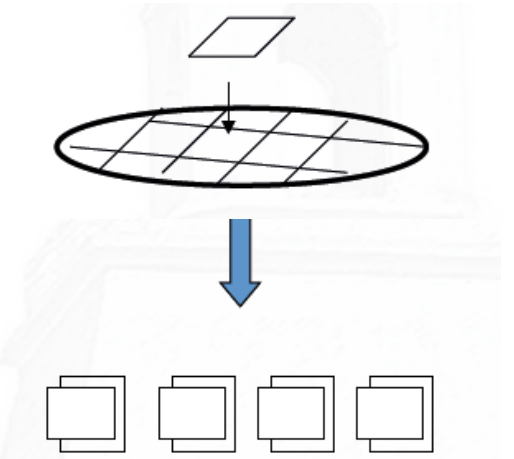
large pitch bumps

stripped down R/O chip



Not sexy ... but cheap and e area .... passive CMOS pixels

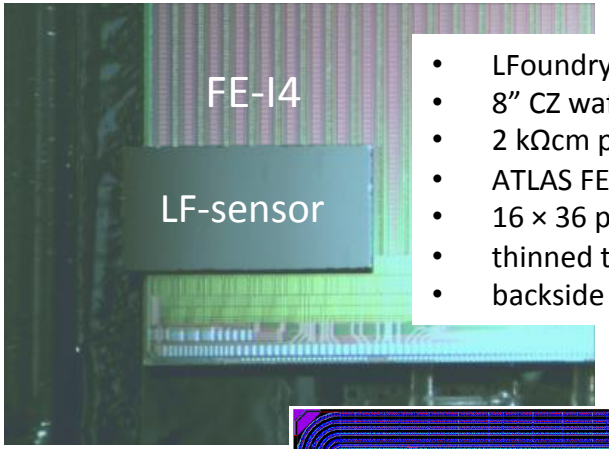




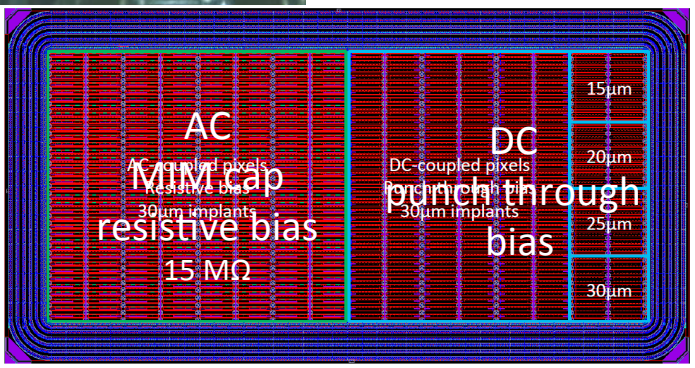
C4 bumps: come with chip fabrication at low cost

- no extra bumping process
- large sensors (8” or 12” w/ reticle stitching)
- in-house (wafer based) flip-chipping (large pitch)
- cheap large feature size (e.g. 1.2 µm) technology
- can have in-pixel AC coupling
- RDL possibilities via metal layers

- MIM capacitors, shielding possibilities
- could use dedicated FE-chip
  - lower rates => lower power => low material

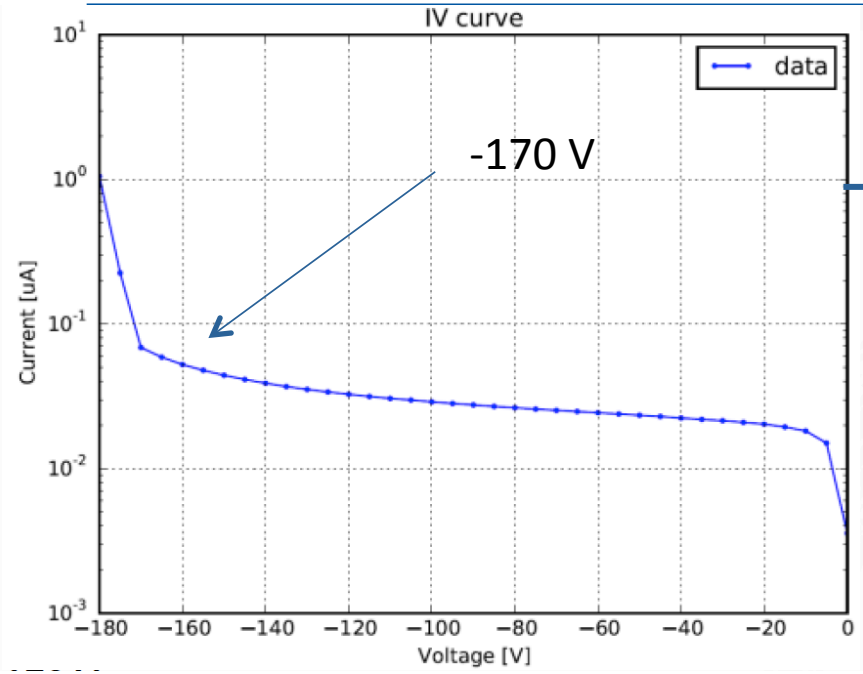


- LFoundry 150 nm CMOS
- 8” CZ wafers
- 2 kΩcm p-type bulk
- ATLAS FE-I4 pixel size (50 x 250 µm^2)
- 16 × 36 pixels (1.8 x 4 mm^2)
- thinned to 300 µm (and 100 µm)
- backside processed (HV contact)



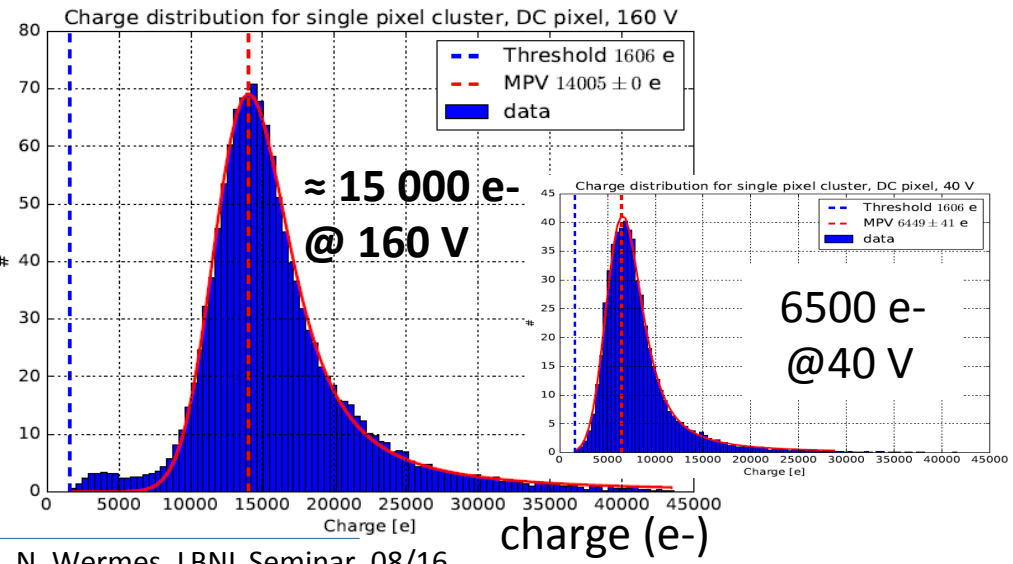
T. Hemperek, F. Hügging, H. Krüger, L. Gonella, J. Janssen, D. Pohl, NW (UBonn)
A. Macchiolo (MPI M) , L. Vigani (Oxford)

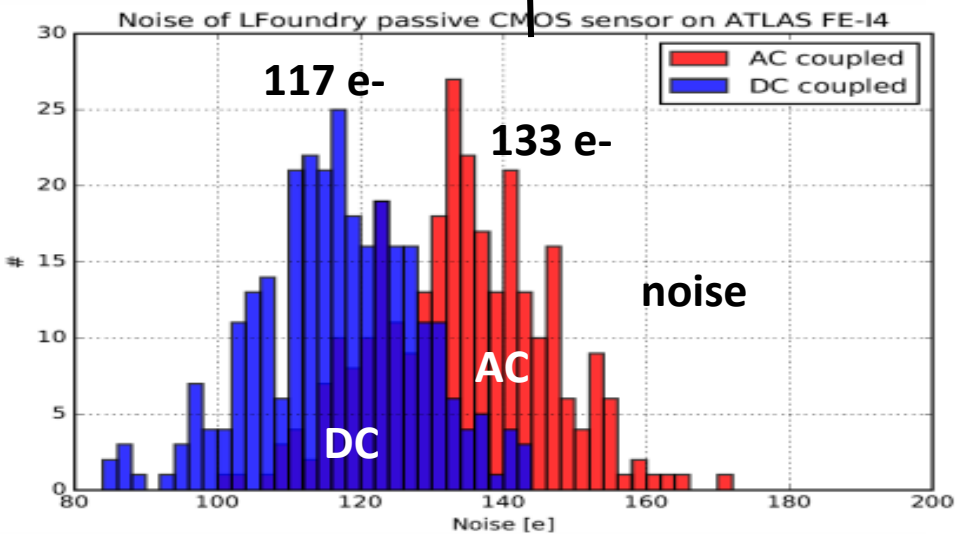
Performance of sensor (CMOS technology)



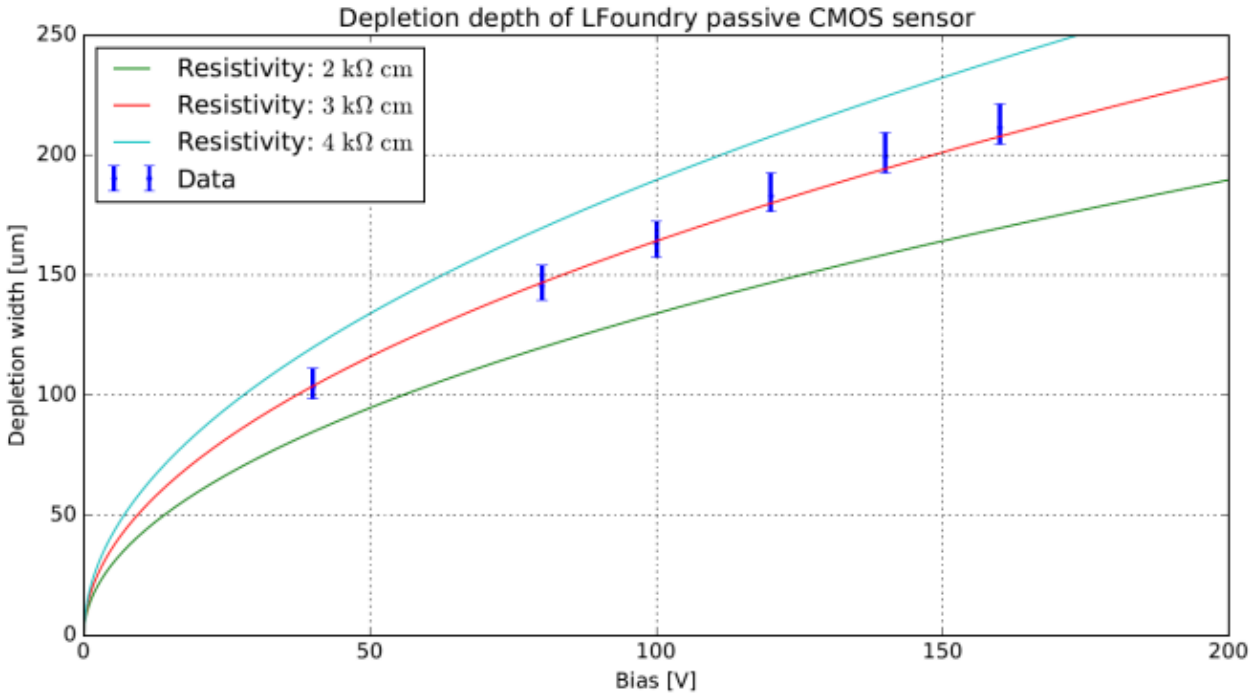
- break down at 170 V
- leakage 20 µA / cm^3 (assuming 220 µm depletion, estimated from simulation and indep. measurements)
- <u>compare:</u> planar sensor ATLAS IBL: 15 µA/cm^3 (assuming 200 µm depletion depth)

<u>compare</u> IBL
- planar sensors (C_D = 117 fF): ENC = 120 e-
- 3D-Si sensors (C_D = 180 fF): ENC = 140 e-

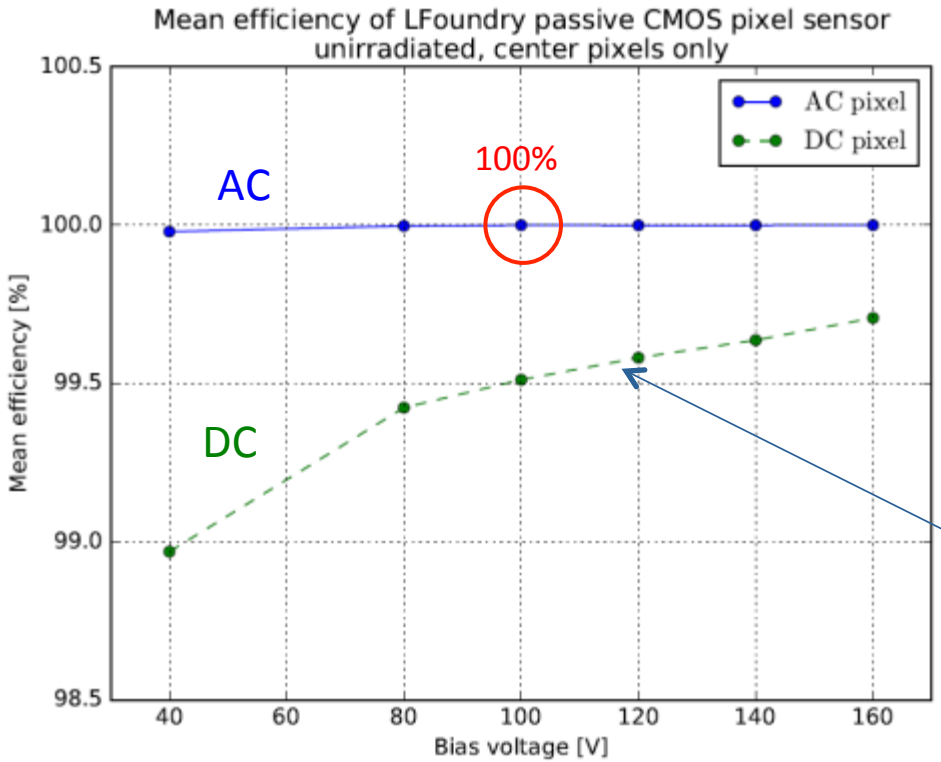




Performance of sensor



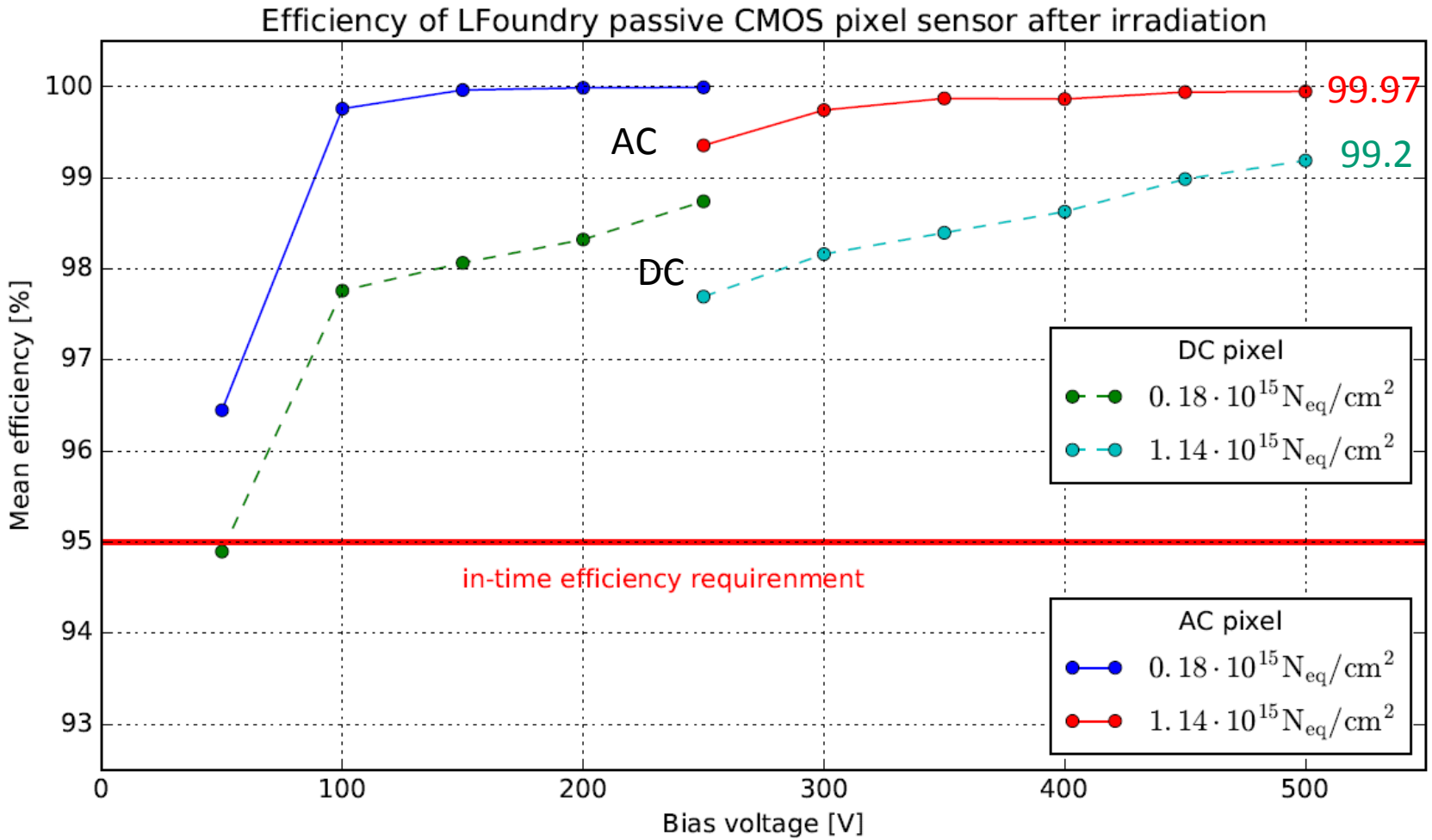
Performance



Setup
- 2.5 GeV electron beam (ELSA)
- threshold: 1500 e- (tuned)
- FE-I4 based telescope

DC: efficiency lost
in punch-through bias dot

Performance after irradiation: 1.14 10^{15} n_{eq}/cm^2



Cost comparisons

Layer 5 & 6 total	112 CHF/cm^2
Sensor	33 CHF/cm^2
Front End	15 CHF/cm^2
Hybridization	64 CHF/cm^{2*}

cost drivers

*reduced to 54 CHF/cm2 for thicker FE ICs (250 µm -> 450 µm)

Reference: T. Hemperek, F. Hügging ITk week @ CERN, 14 – 18 Sept 2015

assume:

- 8" sensors (CMOS fab)
- > 2kΩ cm
- 300 µm thin
  - backside processing
  - 50 x 450 µm^2 pixels
  - 2-3 metal layers
- C4 bumps (150 µm pitch)
- chip to wafer flip-chipping (in-house)

CMOS based Hybrid	35 CHF/cm^2
Sensor	5 CHF/cm^2
Front End	15 CHF/cm^2
Hybridization	10 CHF/cm^{2*}

reduction by factor ~3

Conclusions

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- There is a large momentum in R&D for CMOS active (monolithic) as well as passive (hybrid) pixels as an attractive direction for LHC experiments, even for LHC-pp experiments.

- … outer layers … cost savings … less radiation, (less power?)
- … inner layers … small pixel sizes … position decoding

- R&D profits from micro electronics processing and technology variants and their rapid progress

- Next on the agenda:
  - full **monolithic** devices with radiation tolerance to > 5 x 10^{14} cm^{-2} and in-time (<25 ns) efficiency > 95%
  - full hybrid module w/ **CMOS technology sensors**, low X_0

CMOS Pixel Collaboration

- ~20 ATLAS ITK institutions