PicoTDC Overview

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picoTDC Architecture

- 64 channels
- LSB: 3.05 ps
- Large dynamic range: ~200 us
- Fires on rising and falling edge and has a TOT mode
- Triggerable
- Optional timing channel

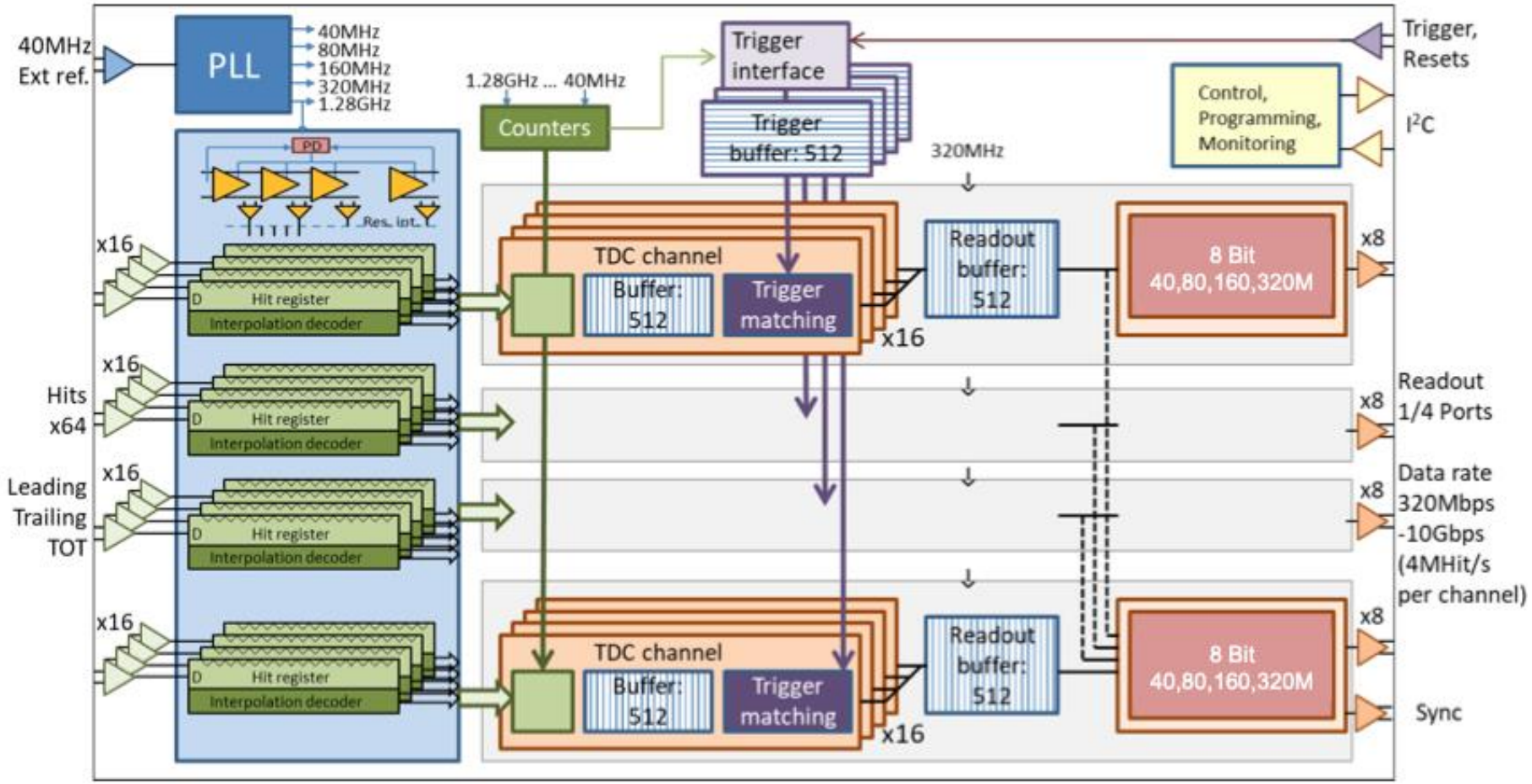


Figure from picoTDC Manual

picoTDC Architecture

- **Critical Requirement:** 40 MHz Ext. Ref. Clock must be very low jitter to get high time resolution.
- 40 MHz Ext. Ref. clock is divided with Phase Locked Loop (PLL) to 1.28 GHz.

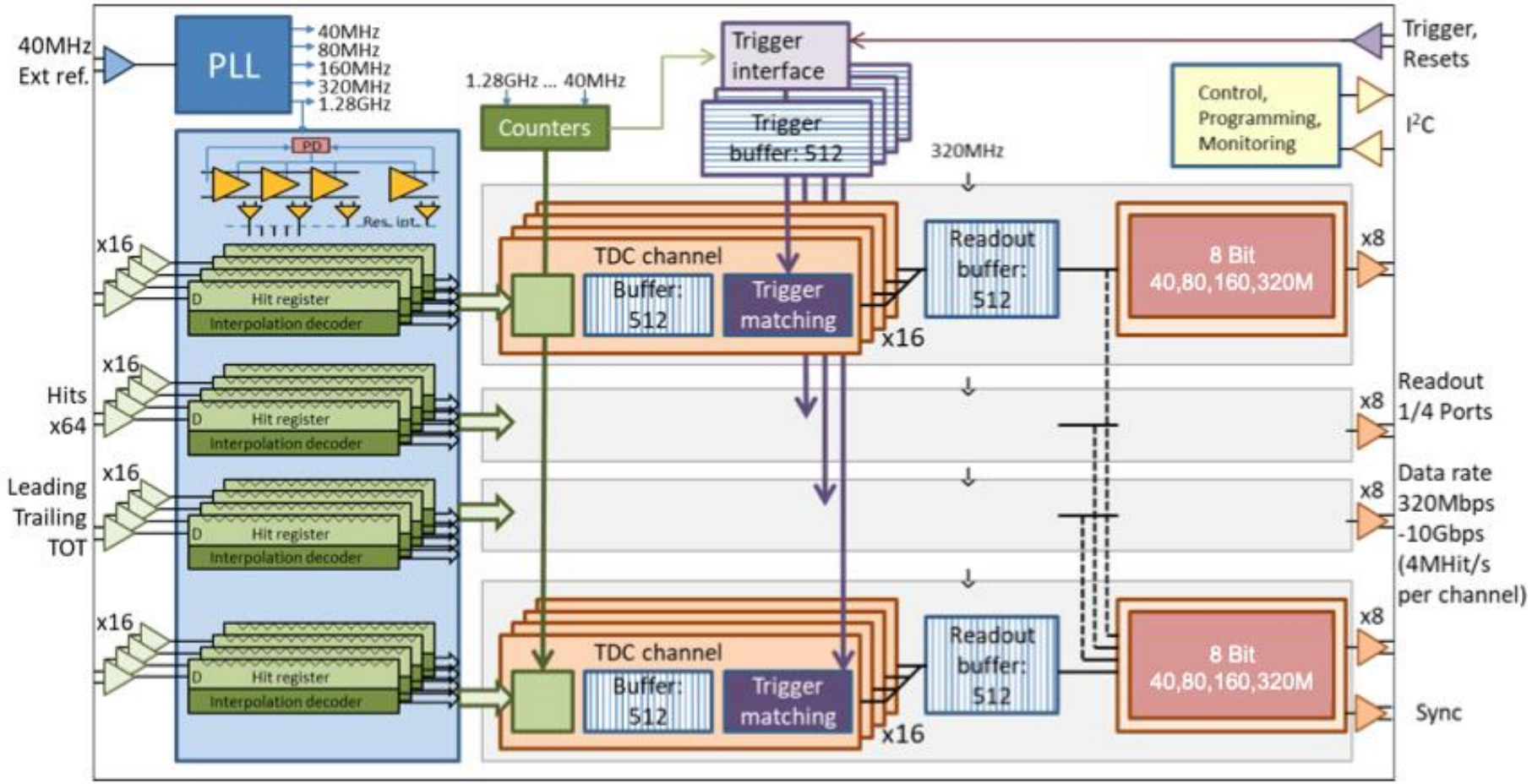


Figure from picoTDC Manual

How to get 3 ps LSB

- 1.28 GHz clock is divided with a 64 tap Delay Locked Loop (DLL) to get a **12.2 ps** delay
  - Coarse mode resolution
- Then divided with resistors to get **3.05 ps** delay
  - Fine mode resolution

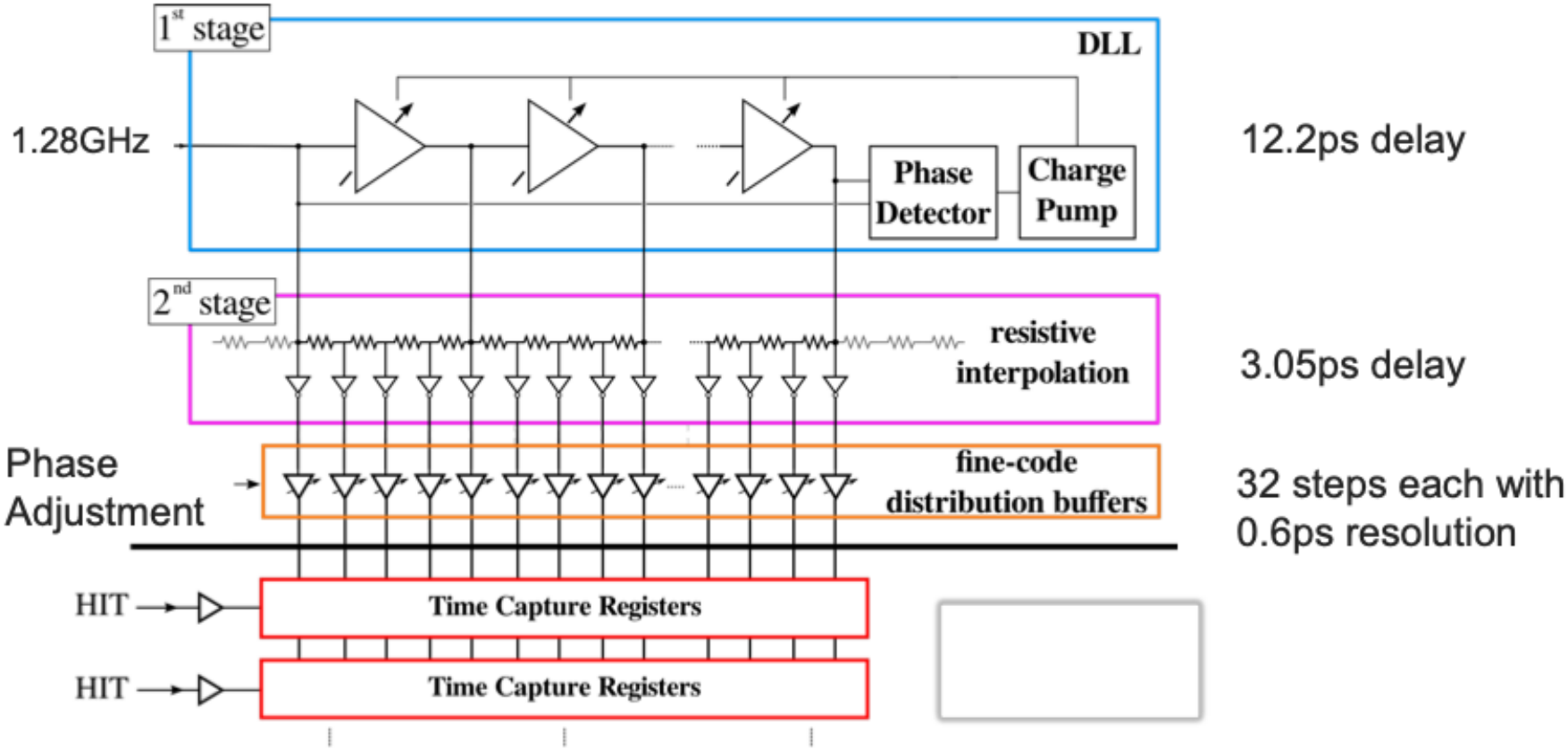


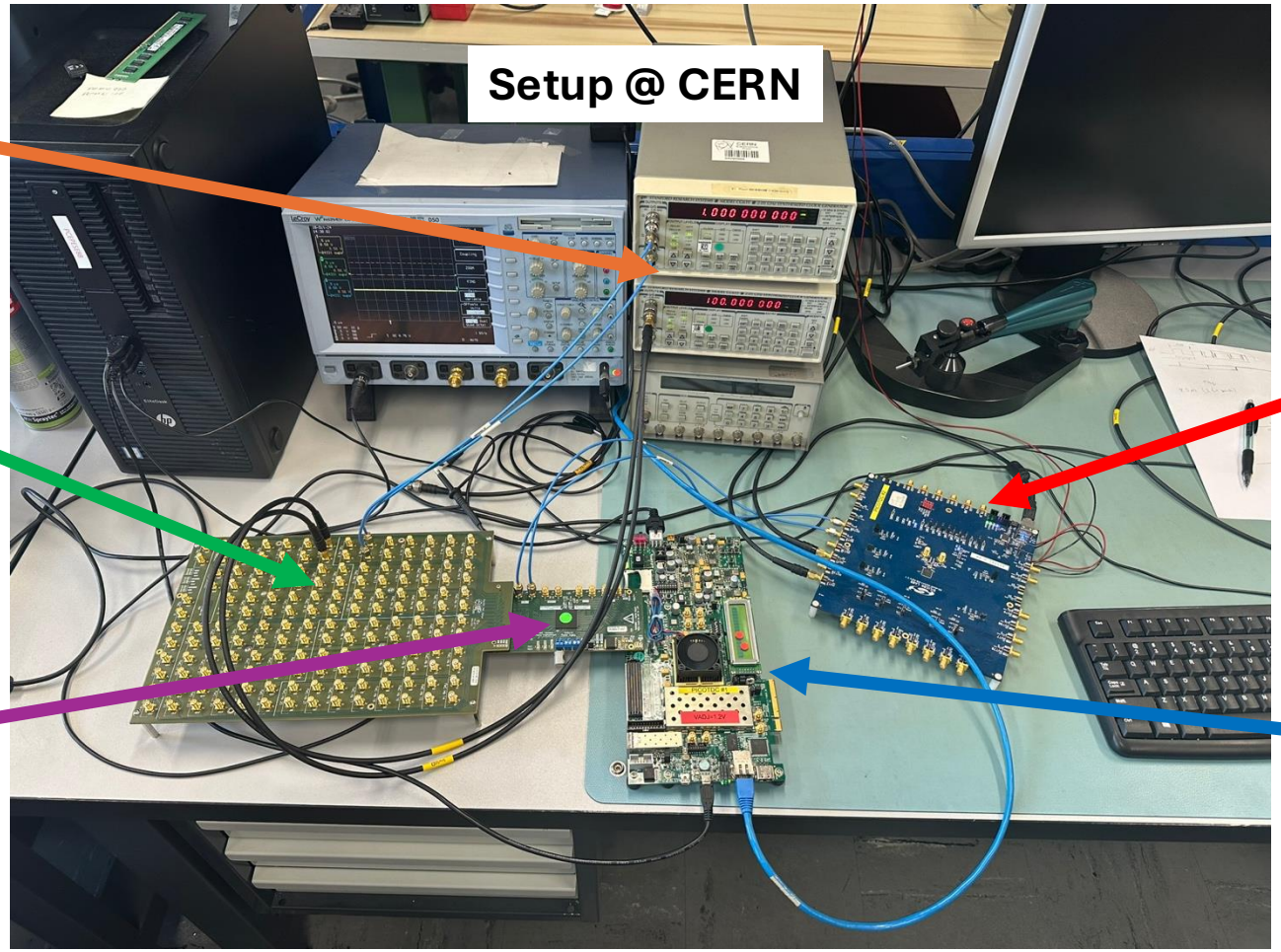
Figure from TWEPP presentation on picoTDC: M. Horstmann TWEPP2019

Lab Setup

your signal + trigger setup

Fanout Board

PicoTDC



40 MHz External Clock

FPGA

How we want to use the picoTDC

- MetaRock has a low power TDC fabricated in 28 nm CMOS.

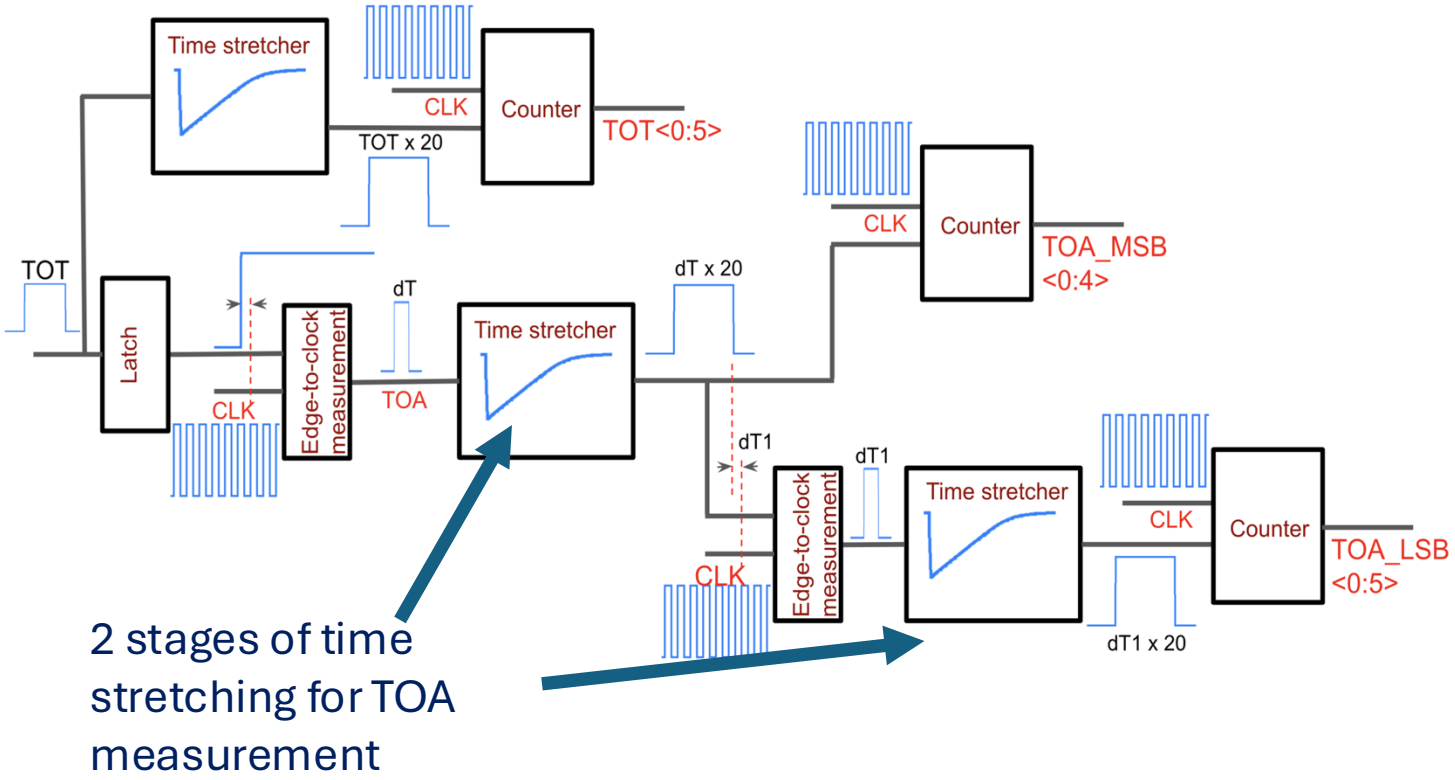
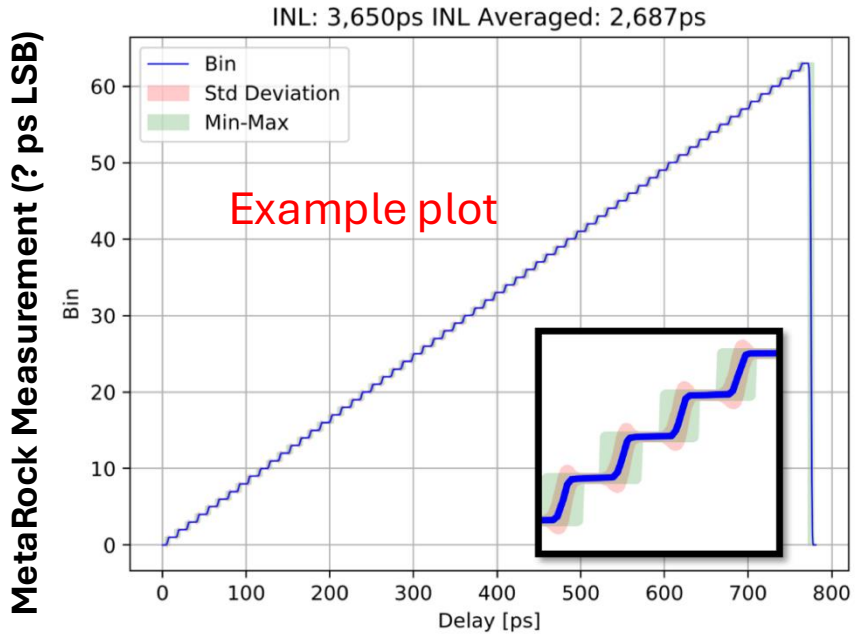


Figure from TDC design from Zhicai Talk

- We want to measure against something more precise.
- There is a built in high-power 20 ps LSB TDC built into MetaRock, but 3 ps is better.



picoTDC Measurement (3 ps LSB)

Figure from TWEPP presentation on picoTDC: M. Horstmann TWEPP2019

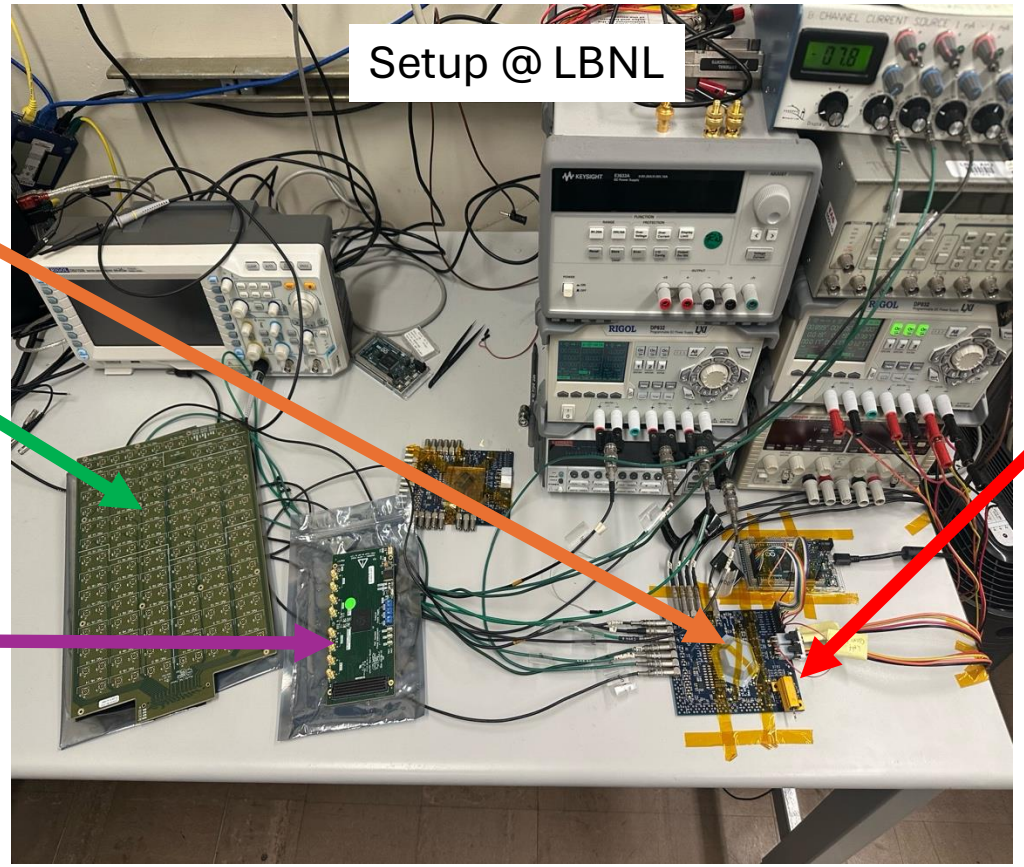
How we want to use the picoTDC

- We'd like to measure output from MetaRock using the picoTDC.
- We already have a picoTDC, fanout board, and an FPGA. The biggest setup challenge will be setting up the FPGA.

MetaRock

Fanout Board

PicoTDC

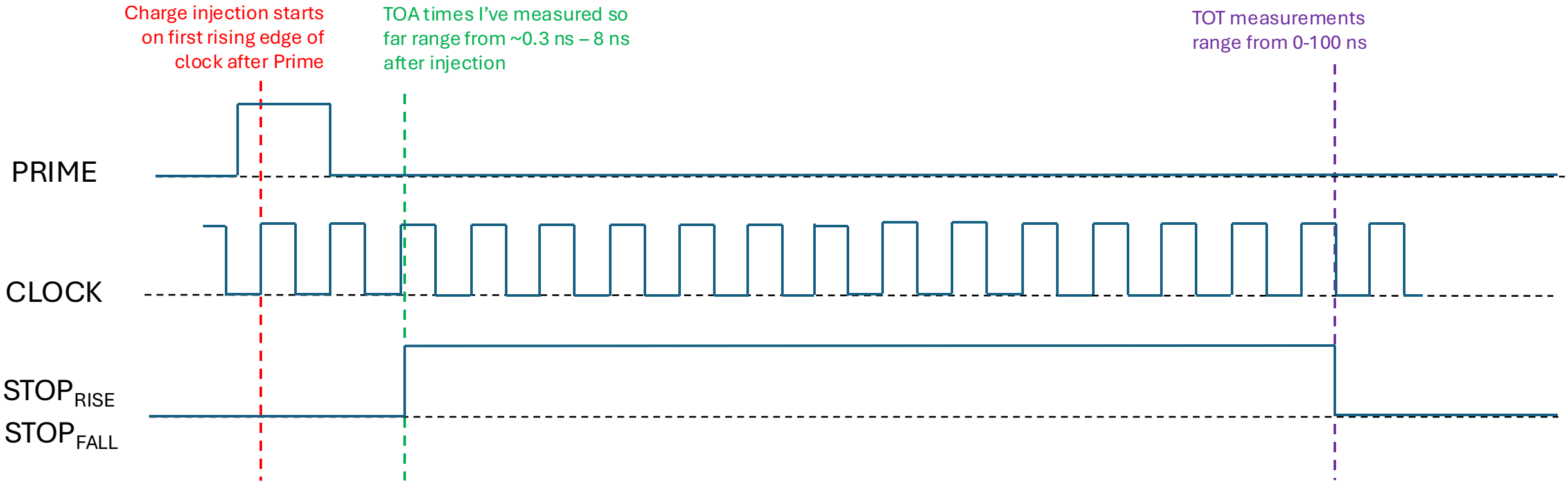


40 MHz External Clock

FPGA ?

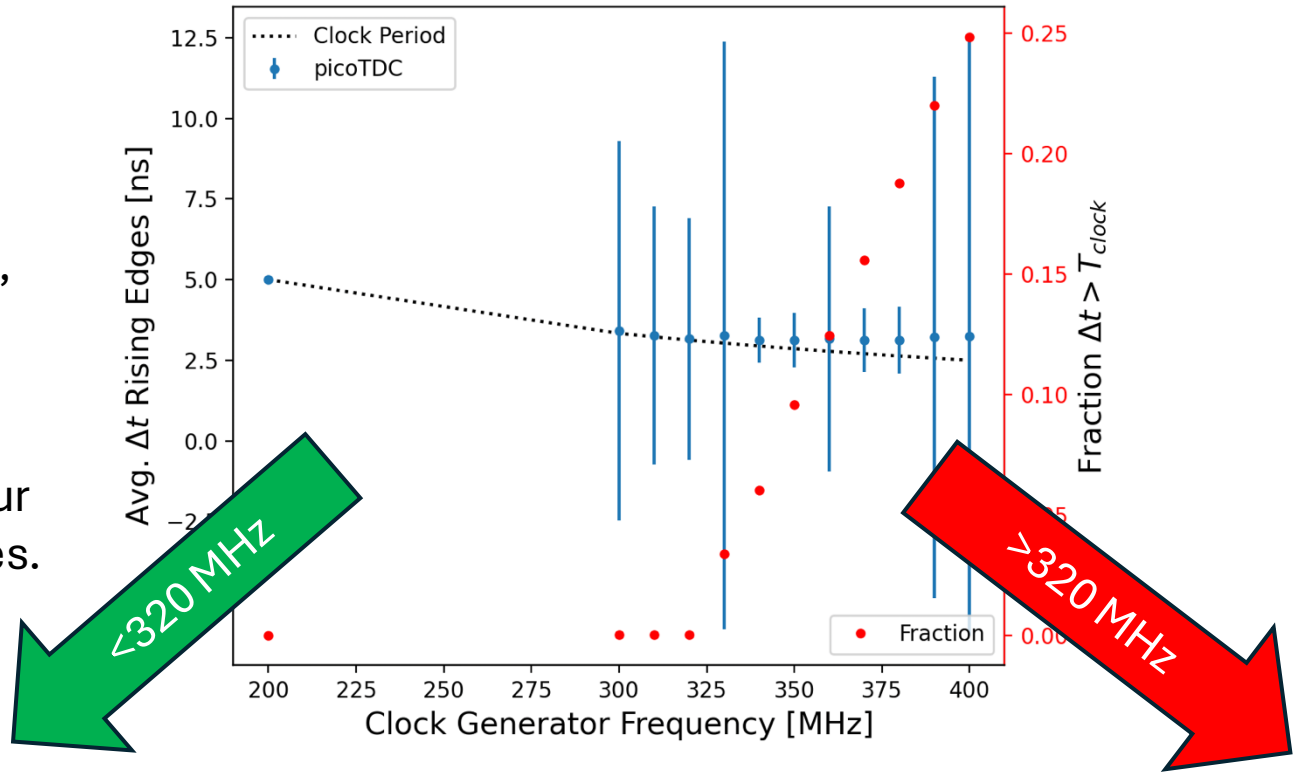
Challenges

- We need three signals from MetaRock for a parallel measurement of the TDCs performance: PRIME, CLOCK, and STOP.
- The biggest constraint is the minimum clock frequency for MetaRock's high power TDC is 390 MHz, however this exceeds the maximum hit rate of the picoTDC, which is 320 MHz.



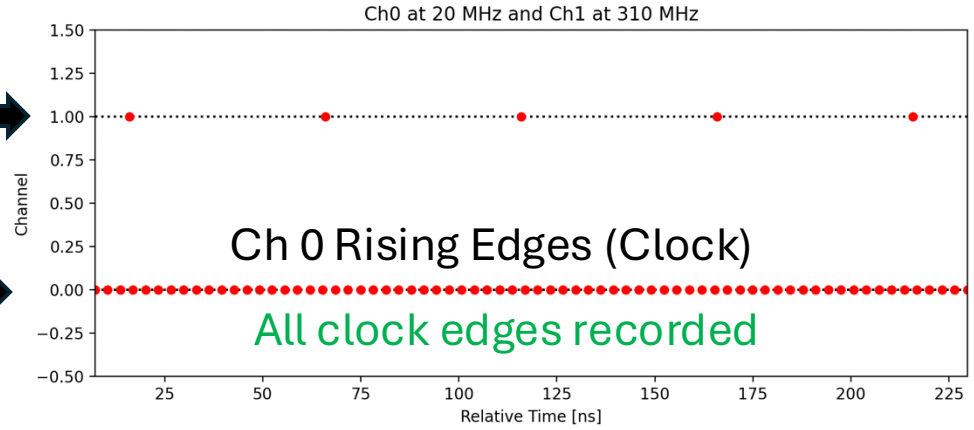
Challenges

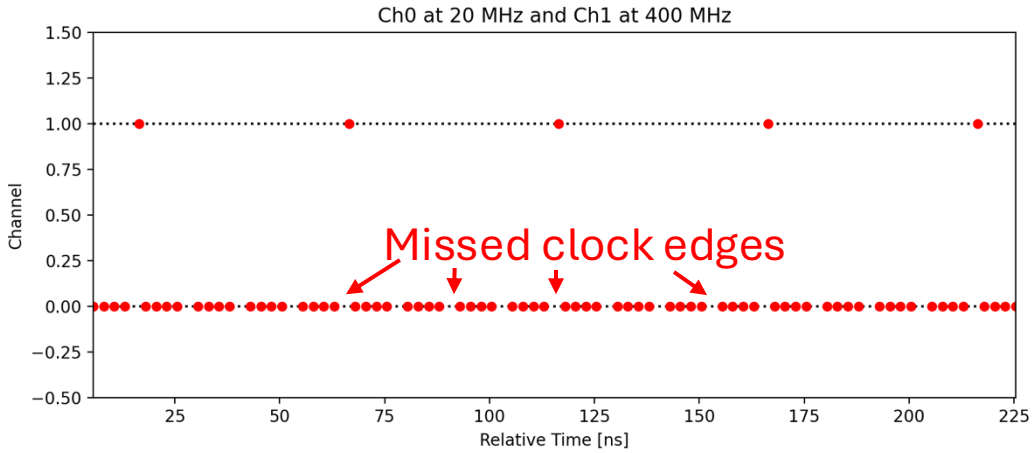
- This plot shows that above 320 MHz, the picoTDC will start missing rising edges.
- However, the edges missed are periodic. We can play games with our setup to overcome the missing edges.



Ch 1 Rising Edges (PRIME, STOP edges)

Ch 0 Rising Edges (Clock)





Recap

- picoTDC provides a 64 channel, 3 ps LSB, readout with a 200 us dynamic range.
  - Performance driven by external clock jitter, not that hard to use.
- We will use picoTDC to measure the performance of MetaRocks two built in TDCs.
  - Pending some challenges with the chip… possible not working…