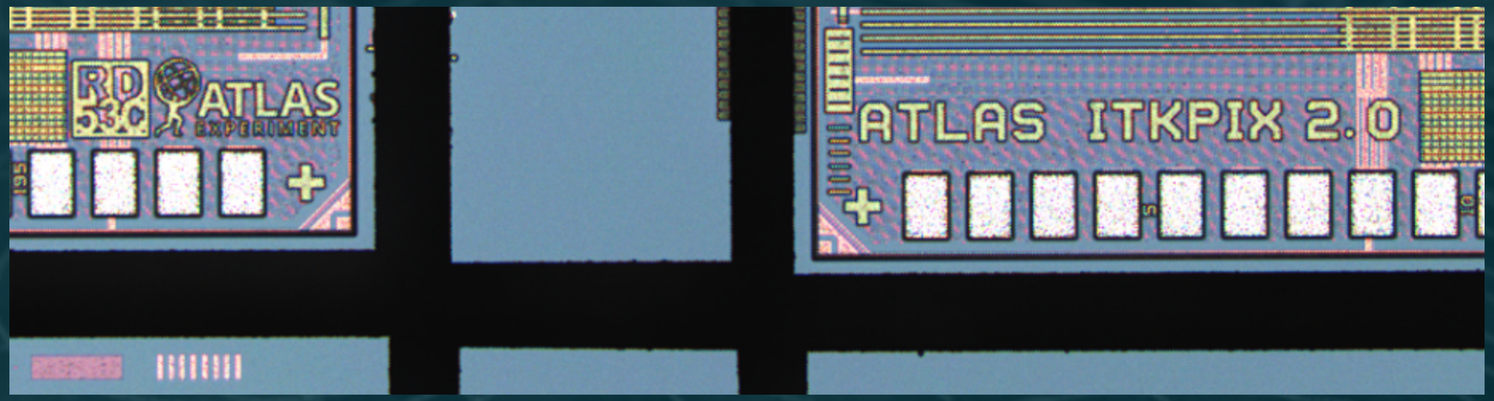


ITkPix 101

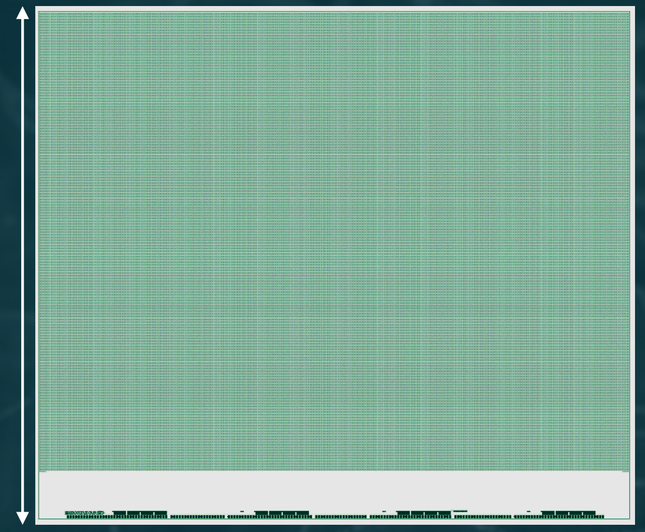
ITk Pixel Module QC Workshop
Not a lecture - 13.01.25

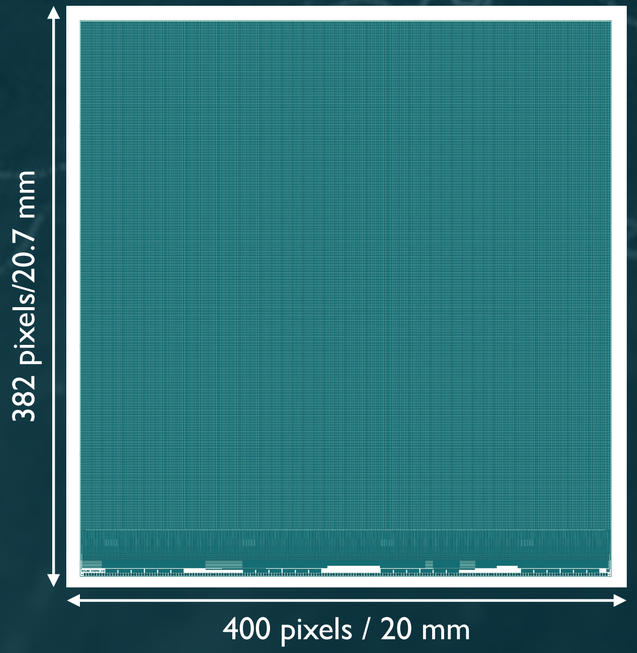
Timon Heim - LBNL

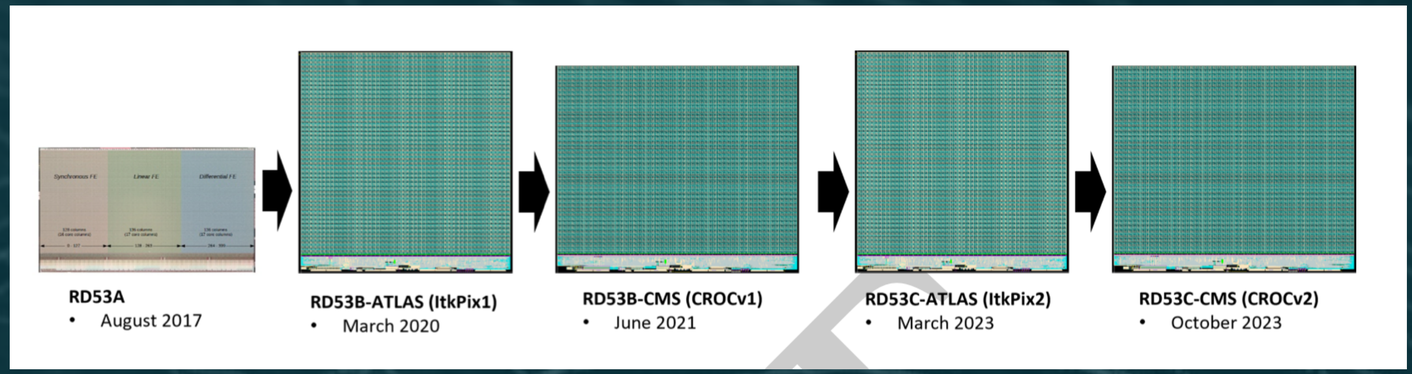
Disclaimer

- I will/can not be exhaustive, happy to go into more detail if questions come up
  - Here I compiled information I would consider useful at the user-level
- I will make generalizations that are not fully correct but are communicating the right understanding
- The slides are “incomplete” if viewed offline as I will make use of the white board
  - I explain better when I can see what is unclear
- Most of the information is leveraged from the manual and paper:
  - Manual: https://cds.cern.ch/record/2890222
  - Paper: https://cds.cern.ch/record/2898416

Nomenclature



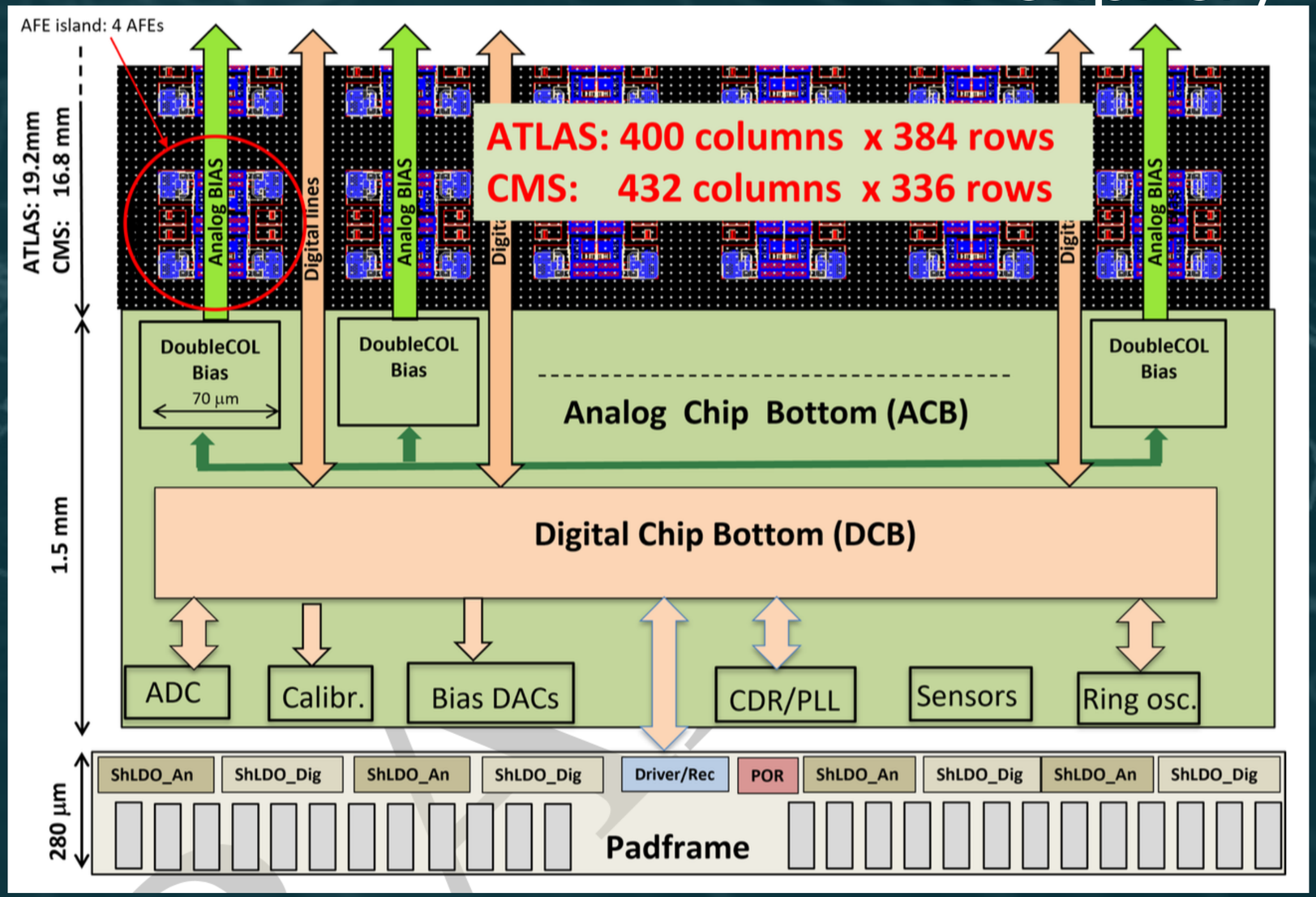




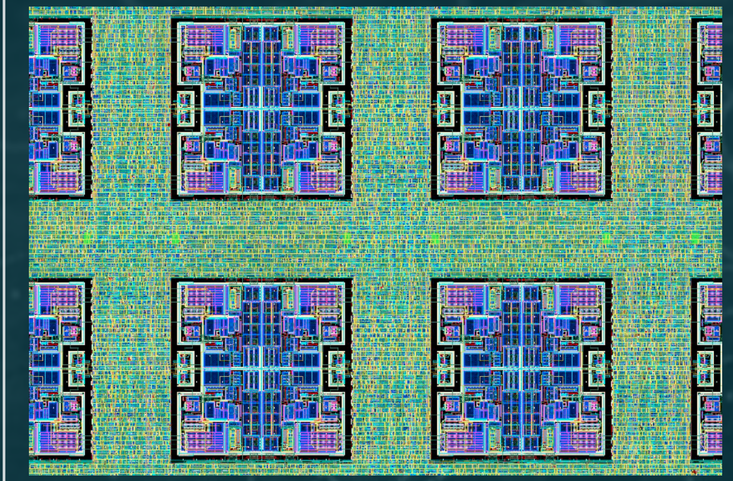
RD53B/C:

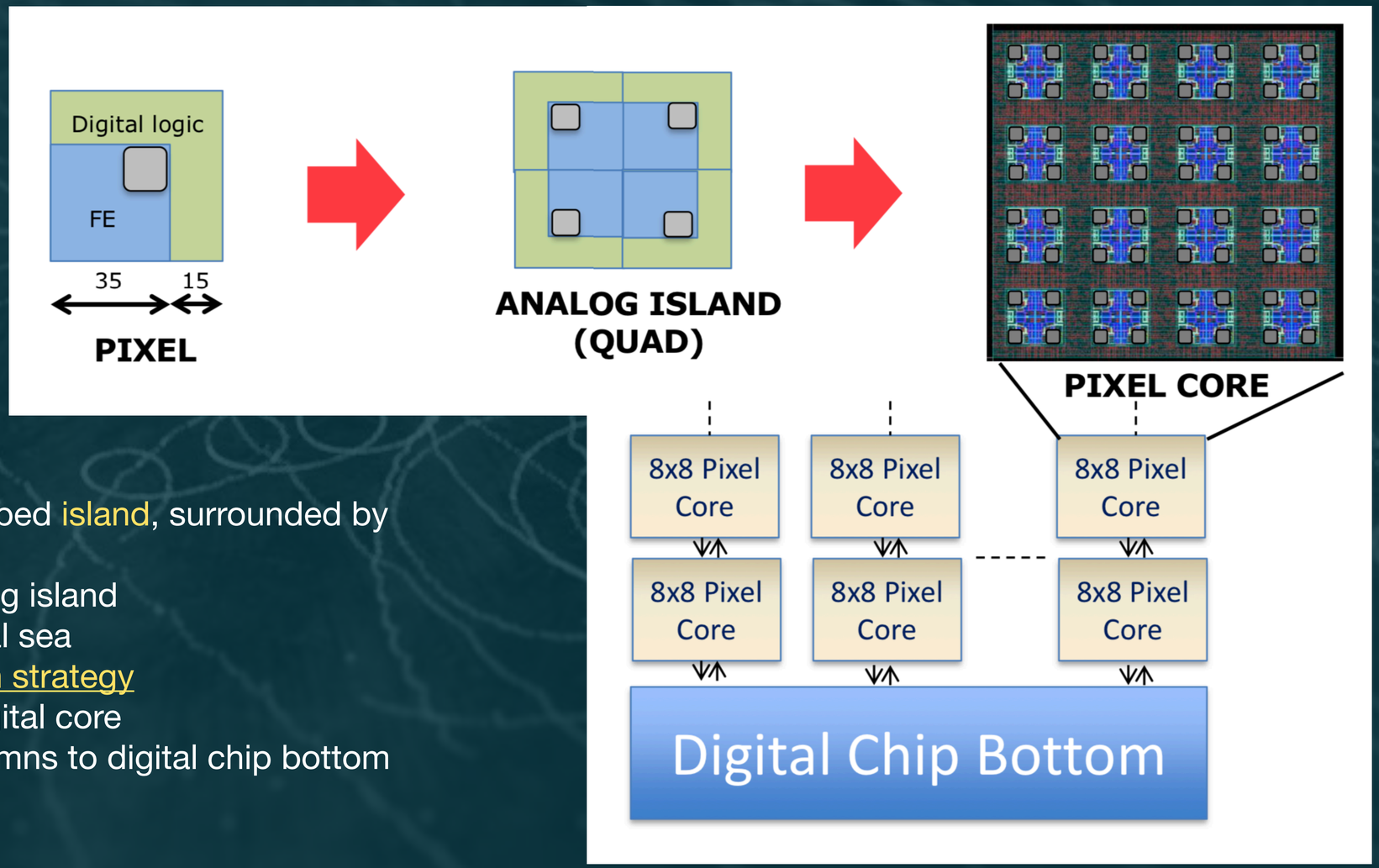
- Virtual chip library
- “Compiled” in two versions:
  - CMS CROC V1/2 (432x332 pixels)
    - lin FE
  - ATLAS ITkPixV1/2 (400x384 pixels)
    - diff FE
- Digital RTL shared between both chips
- Same End-Of-Chip (analog and digital) for both chips
  - Same pad ring
- Within ATLAS usually:
  - RD53B = ITkPixV1 = ITkPixV1.1 != ITkPixV1.0
  - RD53C = ITkPixV2

Periphery


AFE island: 4 AFEs
ATLAS: 19.2mm
CMS: 16.8 mm
1.5 mm
280 µm
ATLAS: 400 columns x 384 rows
CMS: 432 columns x 336 rows
Analog BIAS
Digital lines
Analog BIAS
Digit
Digit
Analog BIAS
DoubleCOL Bias
70 µm
DoubleCOL Bias
DoubleCOL Bias
Analog Chip Bottom (ACB)
Digital Chip Bottom (DCB)
ADC
Calibr.
Bias DACs
CDR/PLL
Sensors
Ring osc.
ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig
Driver/Rec
POR
ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig
Padframe

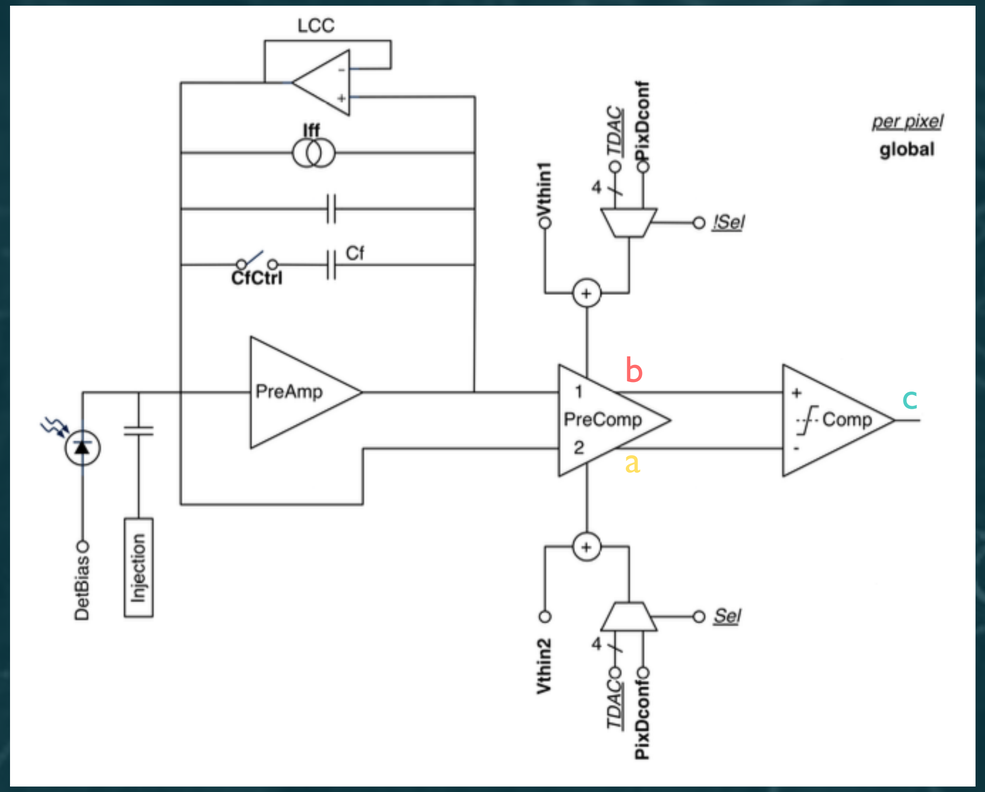
Pixel Matrix

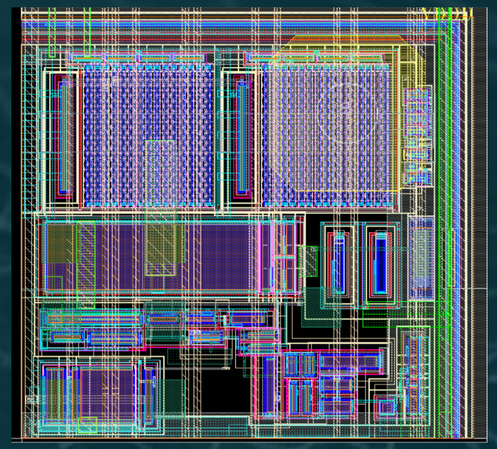


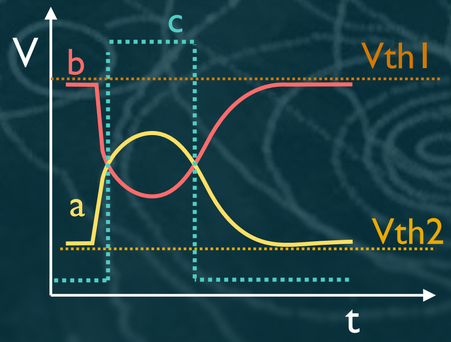


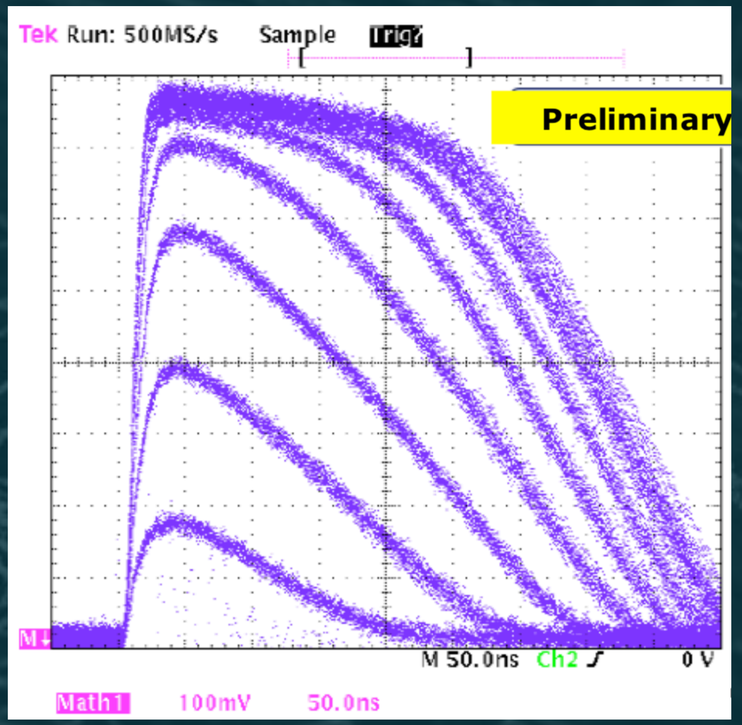
- 2x2 pixel analog region, dubbed island, surrounded by digital, dubbed sea
  - Deep-n-well isolated analog island
  - Deep-n-well isolated digital sea
  - See new study on isolation strategy
- Assembled into 8x8 pixel digital core
- Core connected in core columns to digital chip bottom

Differential Front-End







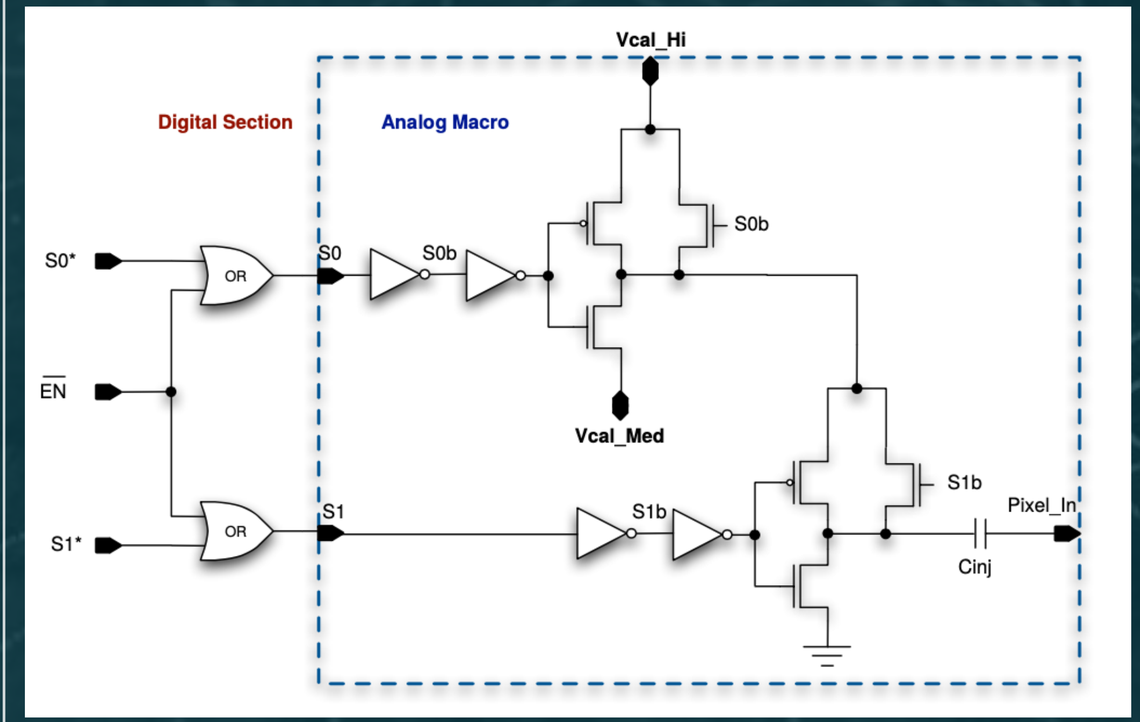


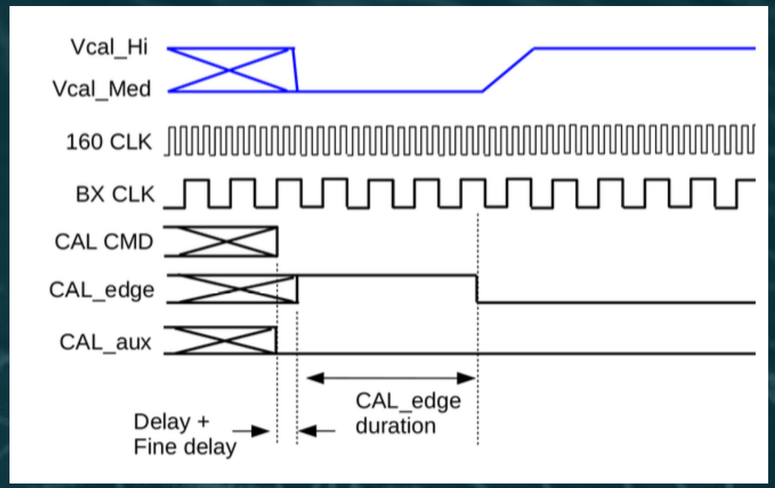
Charge Sensitive Amplifier:
- Straight cascode design
- Global settings for I_f (8-bit DAC)
- Selectable gain

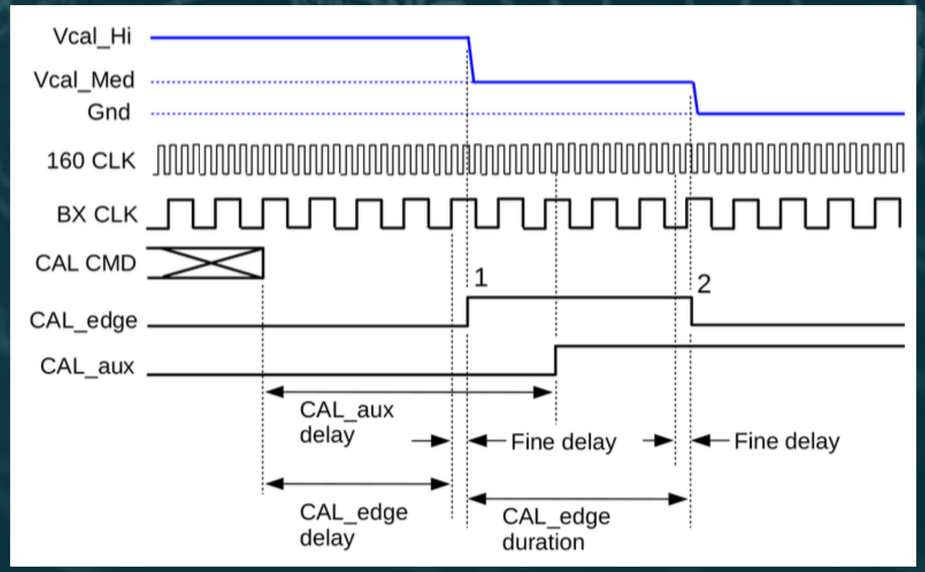
Two Stage Comparator:
- Differential design
- Global 8-bit threshold DAC
- Two per pixel 4-bit threshold DACs
- Optimised for low threshold operation

Injection

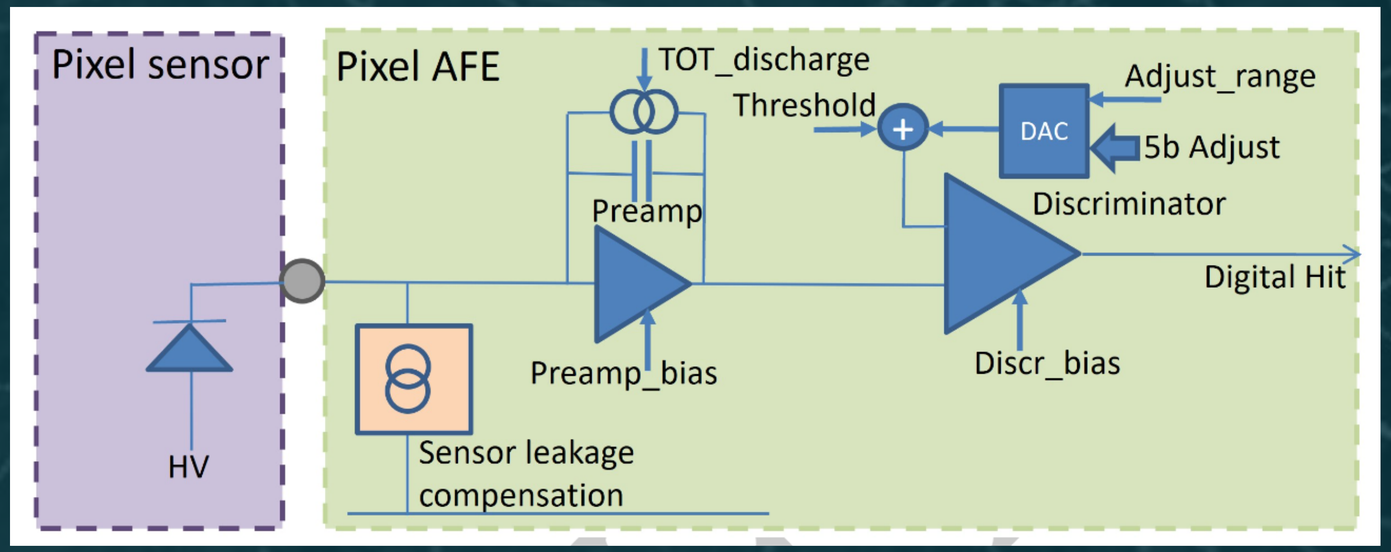
$$S0 = \text{CAL\_edge } \textit{OR } \text{CAL\_aux}$$
$$S1 = \overline{\text{CAL\_edge}} \textit{ AND } \text{CAL\_aux}$$

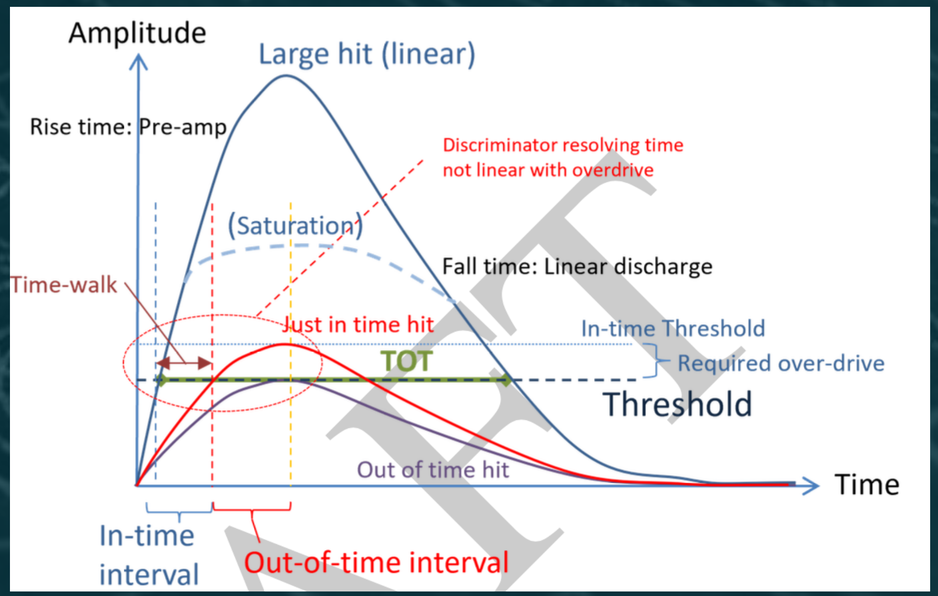




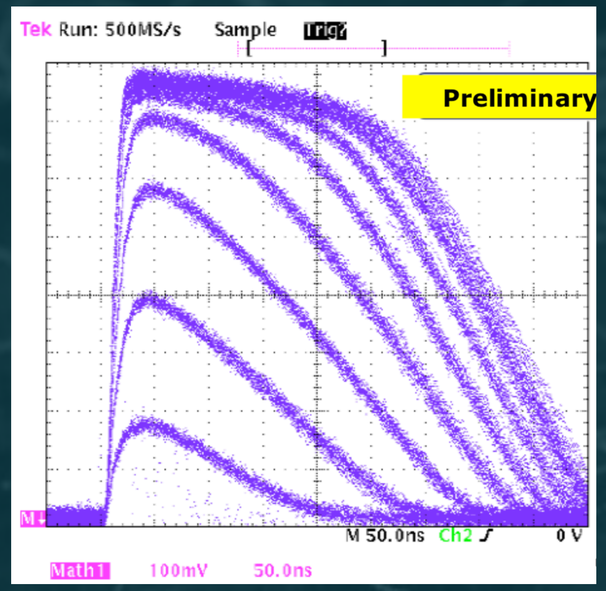


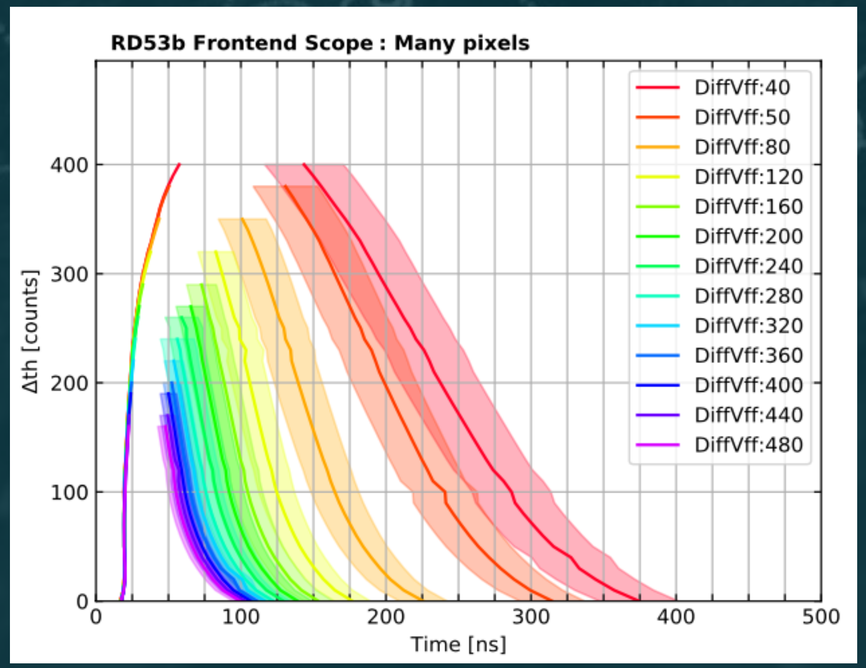
Generic AFE

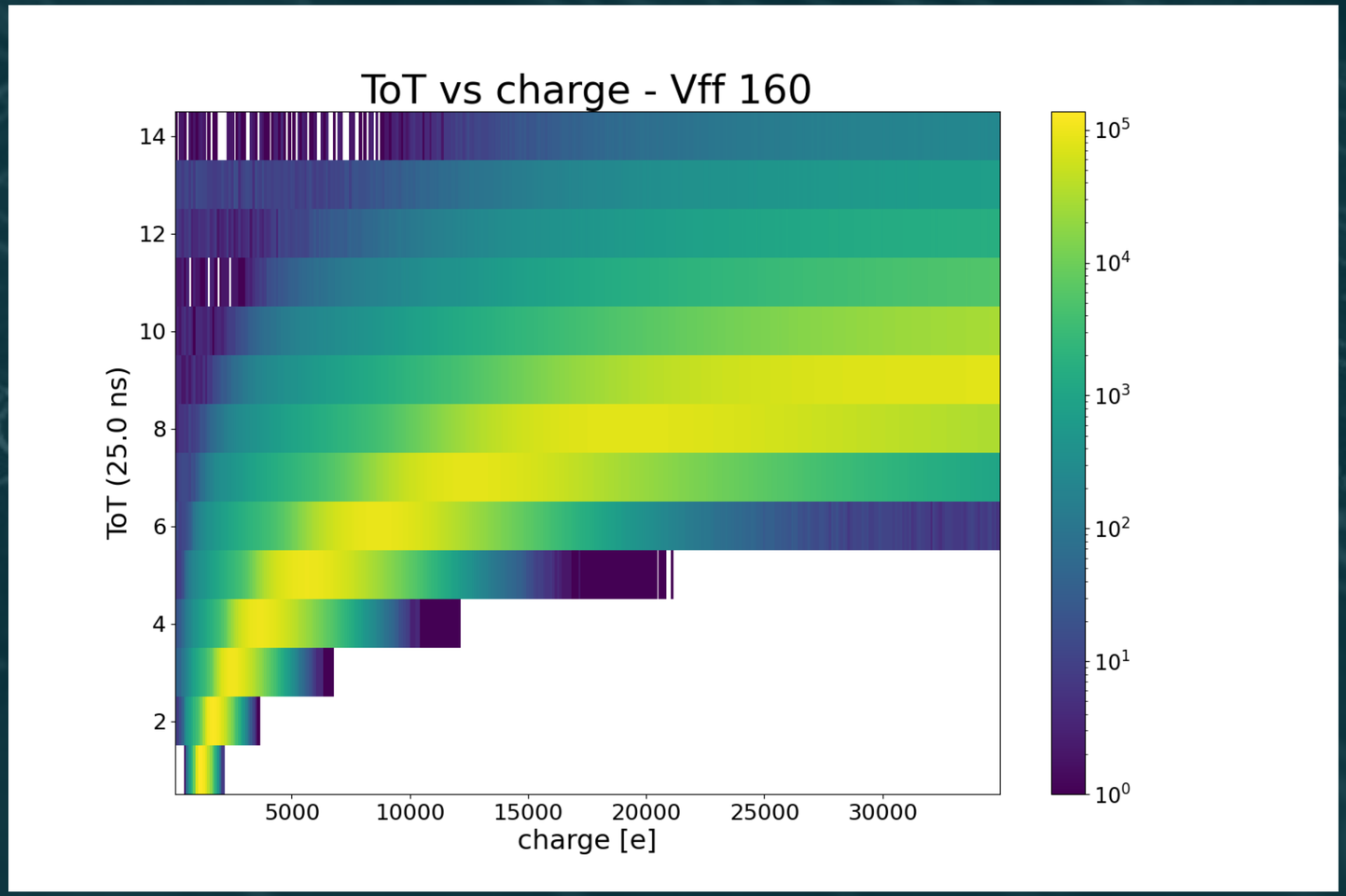

Pixel sensor
Pixel AFE
TOT_discharge
Threshold
Adjust_range
DAC
5b Adjust
Preamp
Discriminator
Digital Hit
HV
Preamp_bias
Discr_bias
Sensor leakage
compensation


Amplitude
Large hit (linear)
Rise time: Pre-amp
Discriminator resolving time
not linear with overdrive
(Saturation)
Fall time: Linear discharge
Time-walk
Just in time hit
In-time Threshold
TOT
Required over-drive
Threshold
Out of time hit
Time
In-time
interval
Out-of-time interval

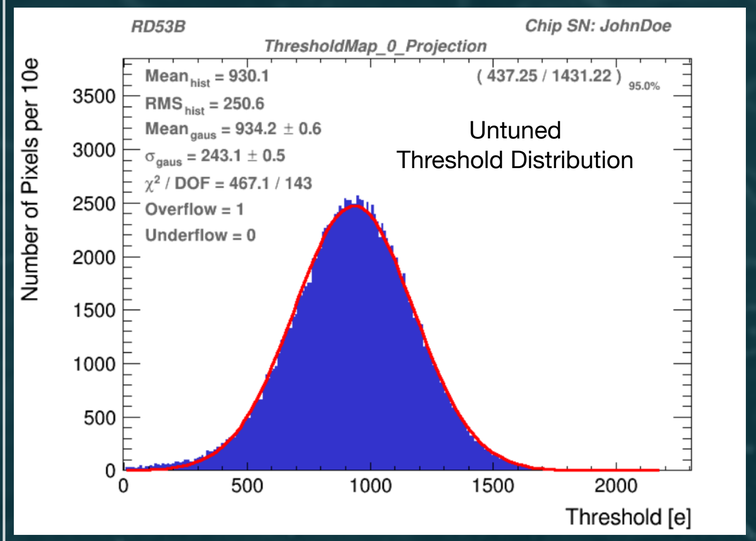
Diff FE ToT Response

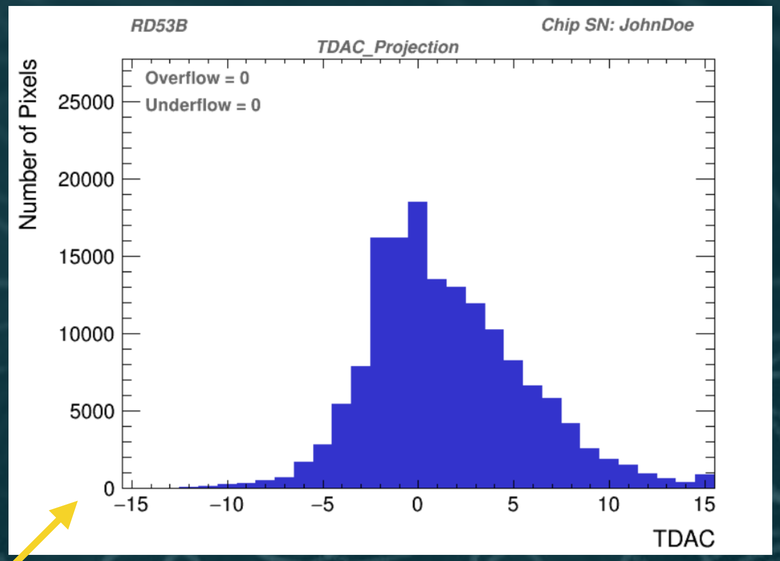


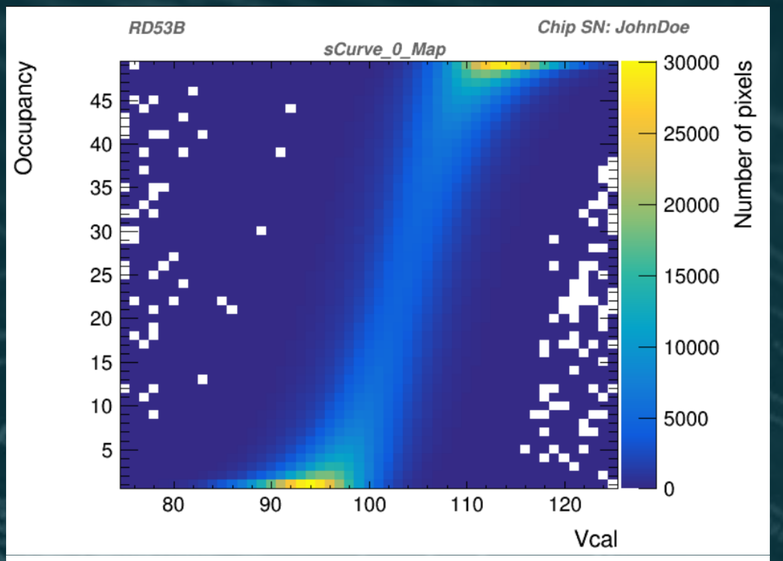


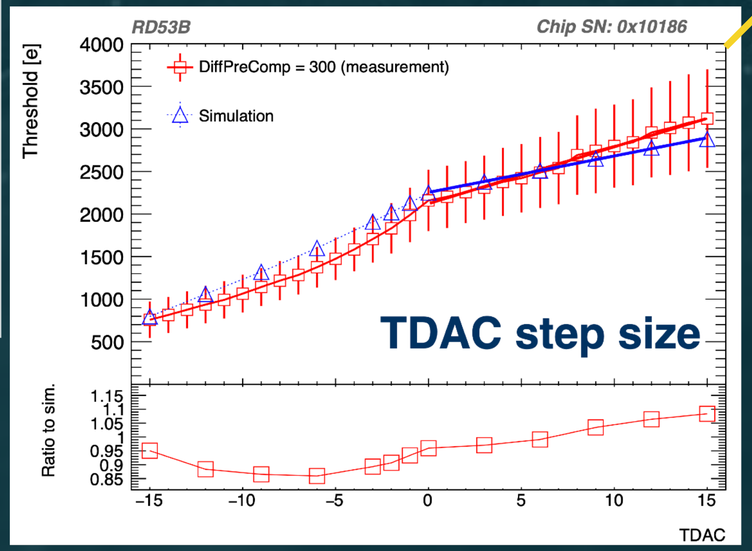


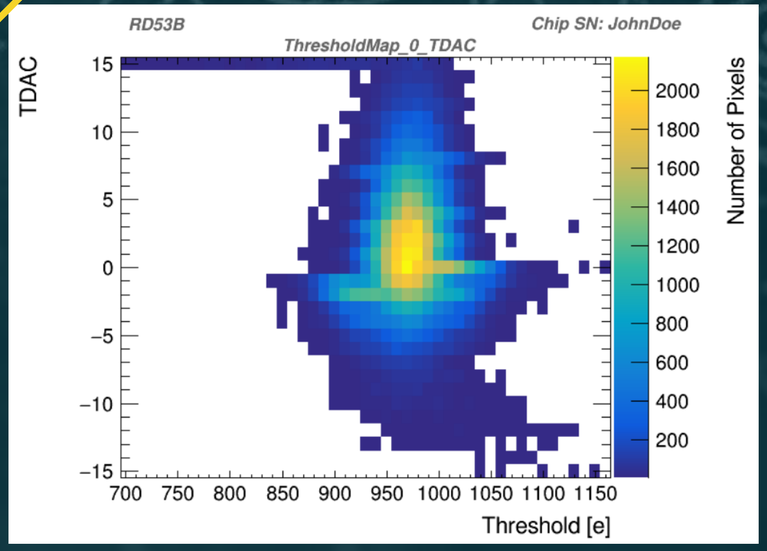
Threshold

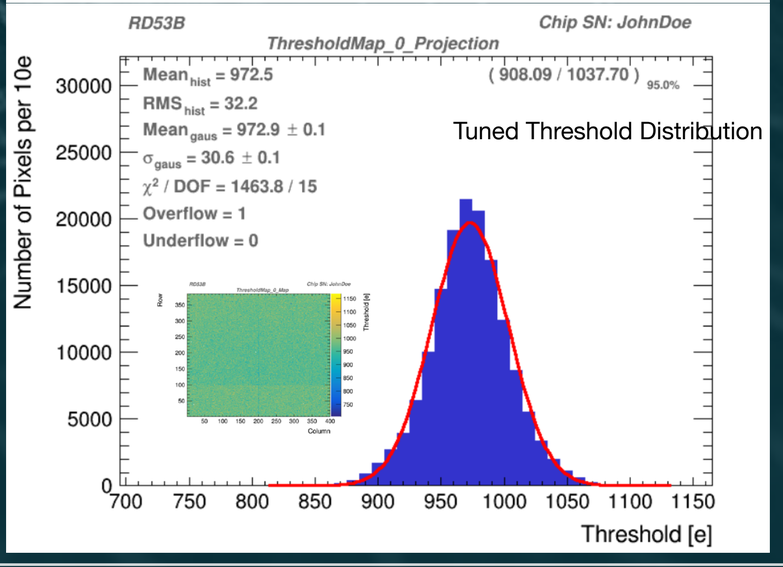

RD53B
Chip SN: JohnDoe
ThresholdMap_0_Projection
Mean$_{hist}$ = 930.1
(437.25 / 1431.22) 95.0%
RMS$_{hist}$ = 250.6
Mean$_{gaus}$ = 934.2 ± 0.6
σ_{gaus} = 243.1 ± 0.5
χ^2 / DOF = 467.1 / 143
Overflow = 1
Underflow = 0
Untuned
Threshold Distribution
Number of Pixels per 10e
Threshold [e]


RD53B
Chip SN: JohnDoe
TDAC_Projection
Overflow = 0
Underflow = 0
Number of Pixels
TDAC

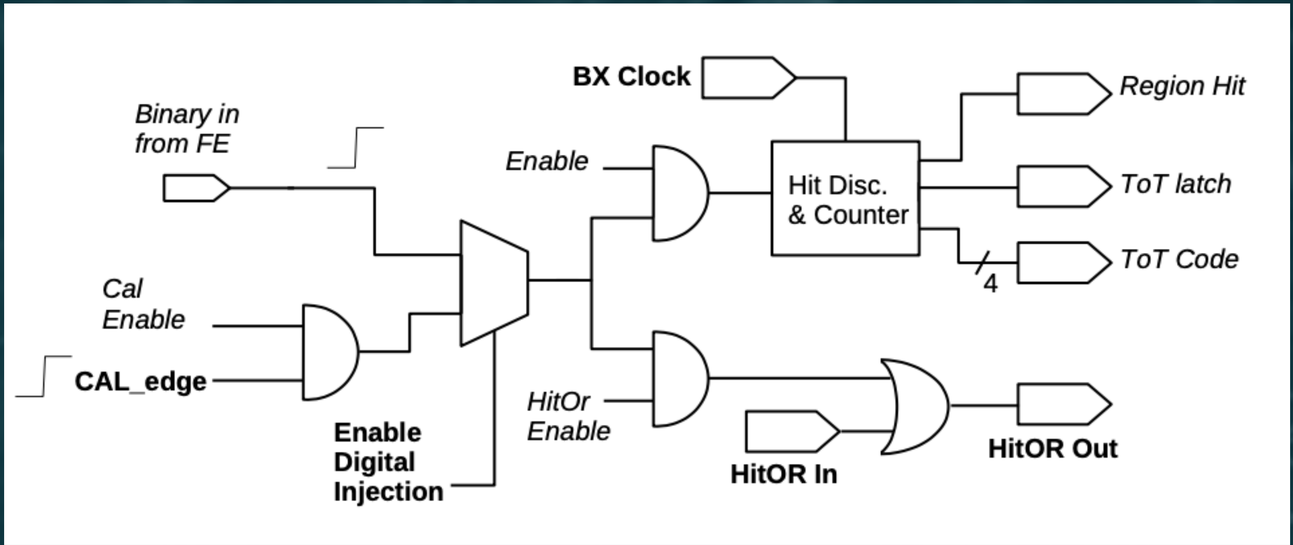

RD53B
Chip SN: JohnDoe
sCurve_0_Map
Occupancy
Number of pixels
Vcal


RD53B
Chip SN: 0x10186
DiffPreComp = 300 (measurement)
Simulation
TDAC step size
Threshold [e]
Ratio to sim.
TDAC


RD53B
Chip SN: JohnDoe
ThresholdMap_0_TDAC
TDAC
Number of Pixels
Threshold [e]

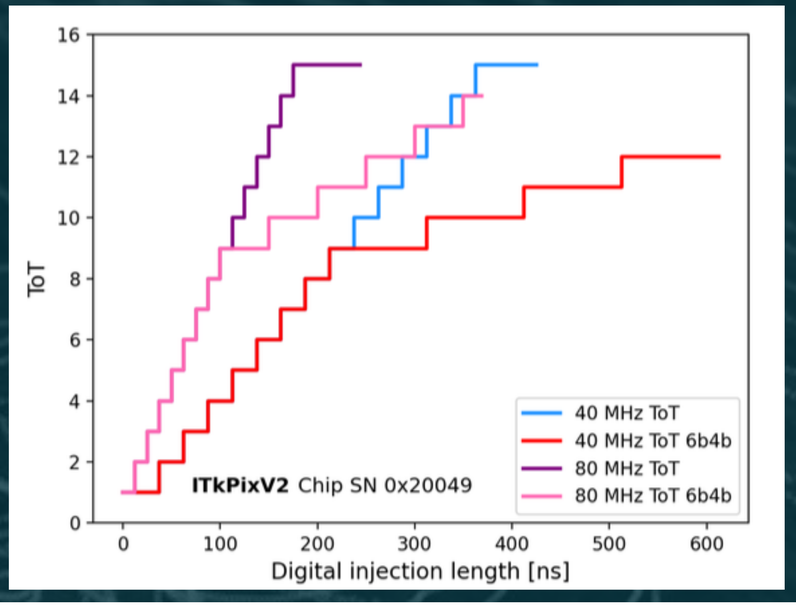

RD53B
Chip SN: JohnDoe
ThresholdMap_0_Projection
Mean$_{hist}$ = 972.5
(908.09 / 1037.70) 95.0%
RMS$_{hist}$ = 32.2
Mean$_{gaus}$ = 972.9 ± 0.1
σ_{gaus} = 30.6 ± 0.1
χ^2 / DOF = 1463.8 / 15
Overflow = 1
Underflow = 0
Tuned Threshold Distribution
Number of Pixels per 10e
Threshold [e]

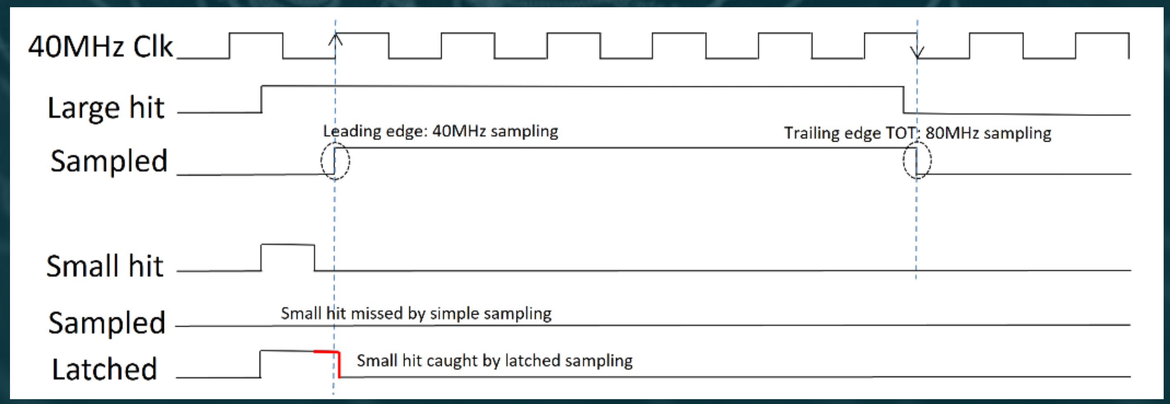
Digitization



Output 4-bit code	True ToT bin (low edge) [BX]			
	40 MHz speed		80 MHz speed	
	4-bit (DEF)	6-to-4 bit	4-bit	6-to-4 bit
0	0	0	0	0
1	1	1	0.5	0.5
2	2	2	1	1
3	3	3	1.5	1.5
4	4	4	2	2
5	5	5	2.5	2.5
6	6	6	3	3
7	7	7	3.5	3.5
8	8	8	4	4
9	9	12	4.5	6
10	10	16	5	8
11	11	20	5.5	10
12	12	24	6	12
13	13	28	6.5	14
14	≥14	≥32	≥7	≥16

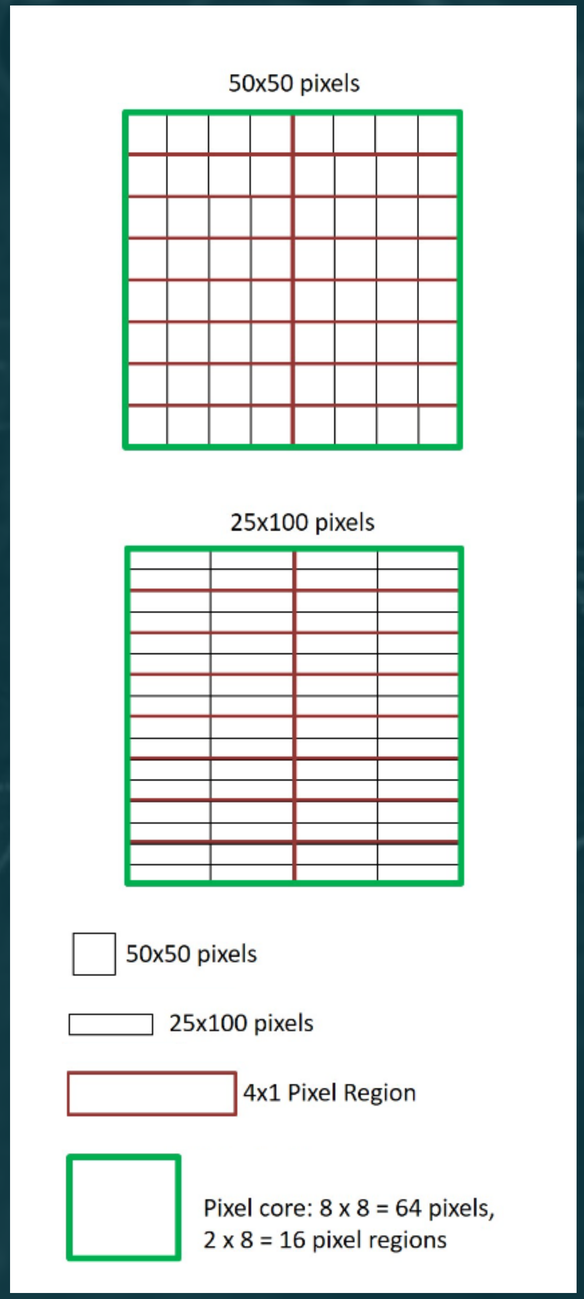
YARR_ToT = Chip_ToT + 1

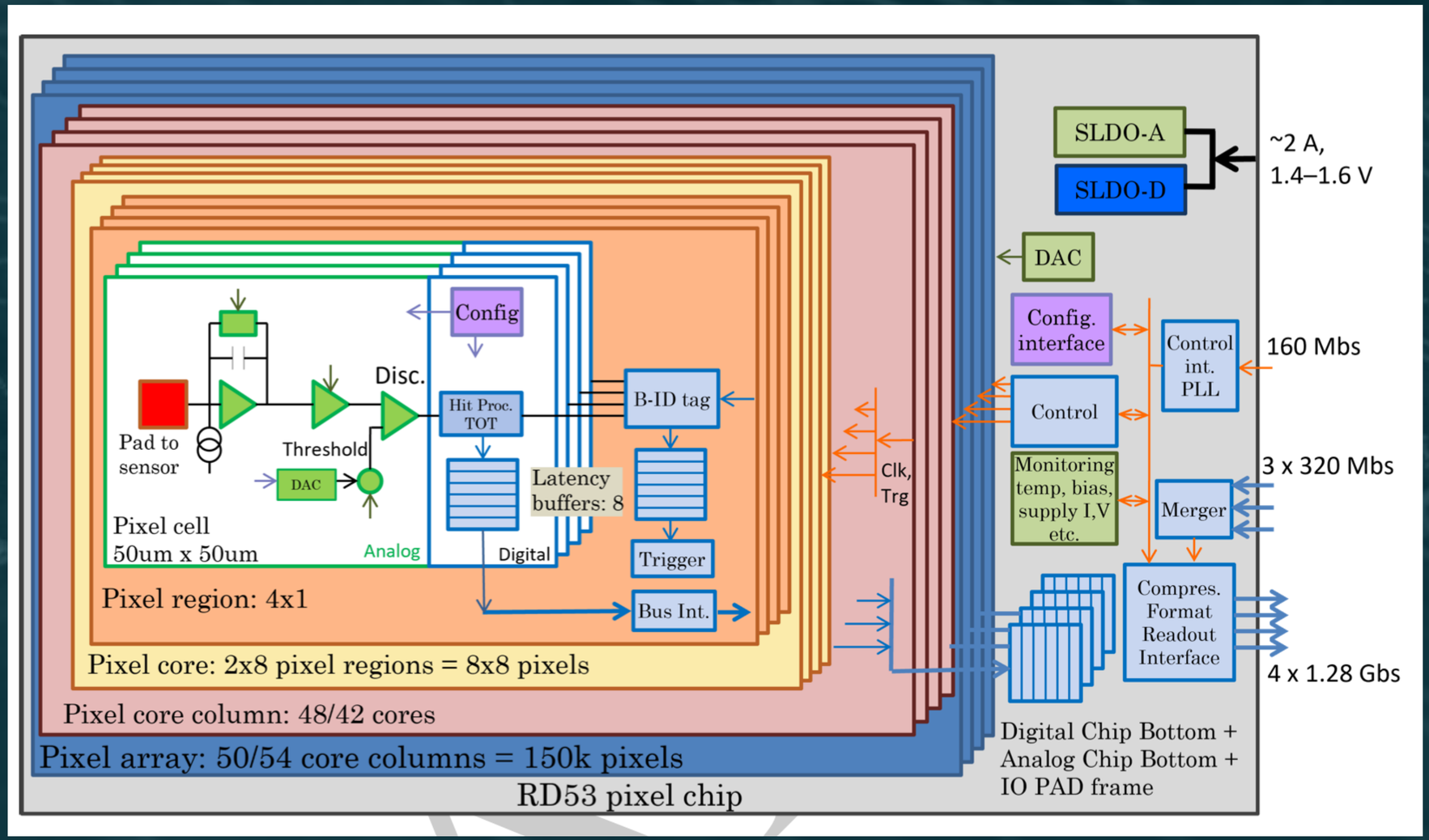




ITkPix only has sync hit sampling

Dataflow


50x50 pixels
25x100 pixels
50x50 pixels
25x100 pixels
4x1 Pixel Region
Pixel core: 8 x 8 = 64 pixels,
2 x 8 = 16 pixel regions


SLDO-A
SLDO-D
~2 A,
1.4–1.6 V
DAC
Config.
interface
Control
int.
PLL
160 Mbs
Control
Monitoring
temp, bias,
supply I,V
etc.
Merger
3 x 320 Mbs
Compres.
Format
Readout
Interface
4 x 1.28 Gbs
Clk,
Trg
Config
Disc.
Hit Proc.
TOT
B-ID tag
Pad to
sensor
Threshold
DAC
Latency
buffers: 8
Trigger
Bus Int.
Pixel cell
50um x 50um
Analog
Digital
Pixel region: 4x1
Pixel core: 2x8 pixel regions = 8x8 pixels
Pixel core column: 48/42 cores
Pixel array: 50/54 core columns = 150k pixels
RD53 pixel chip
Digital Chip Bottom +
Analog Chip Bottom +
IO PAD frame

Trigger Timing

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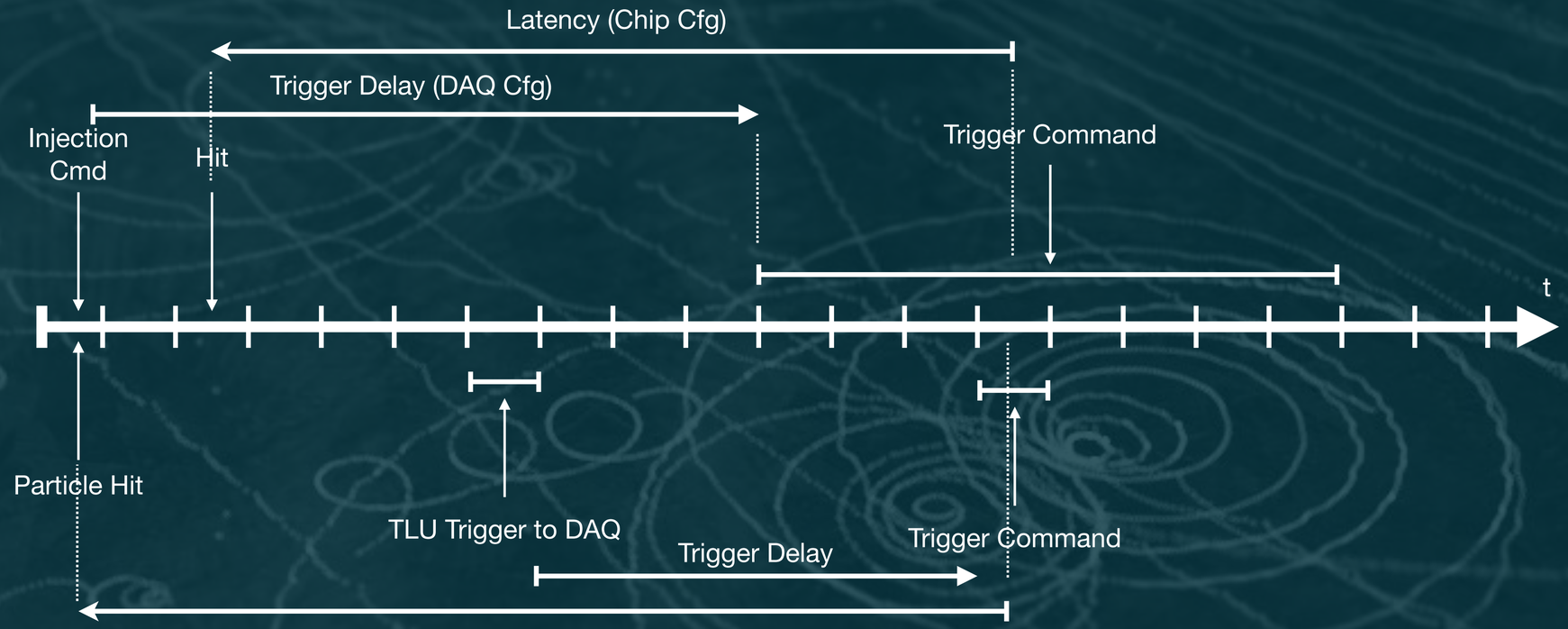
Calibration Scenario

Data taking Scenario

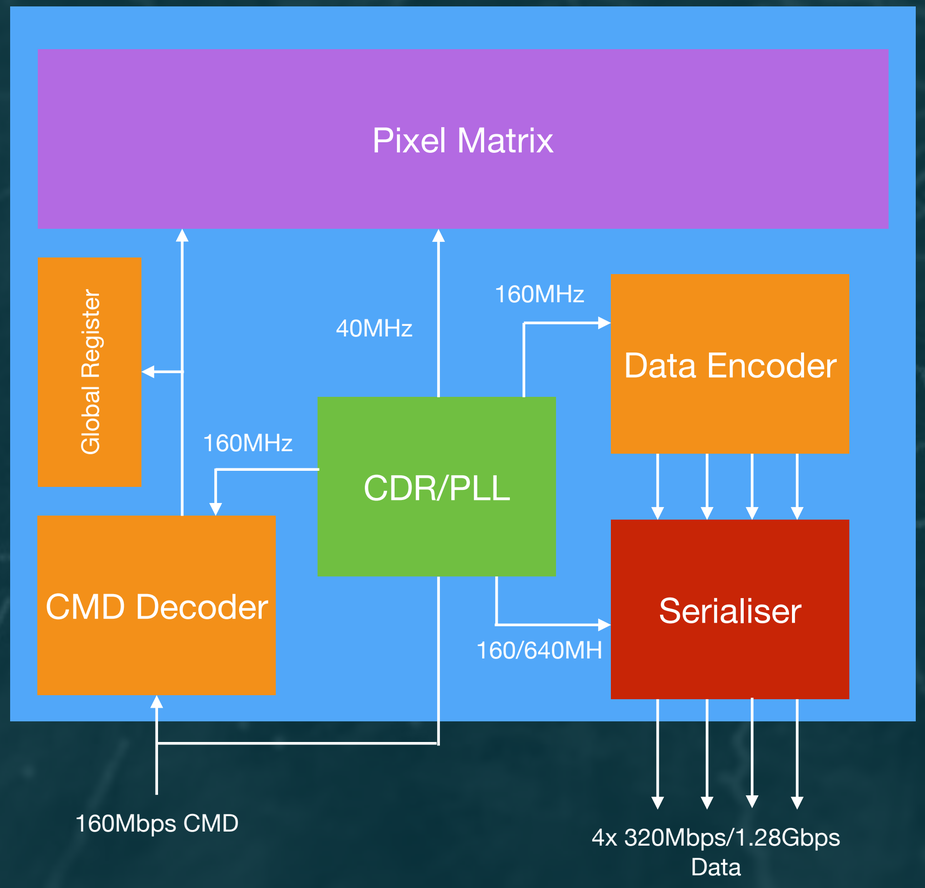


Trigger Delay: defined in scan config as part of trigger loop
Latency: part of chip config

$t_{hit} = t_{trigger}$ - latency

Trigger Commands: 16bit frame stretches over 4 bunch crossings => 15 different trigger commands for all possible combinations

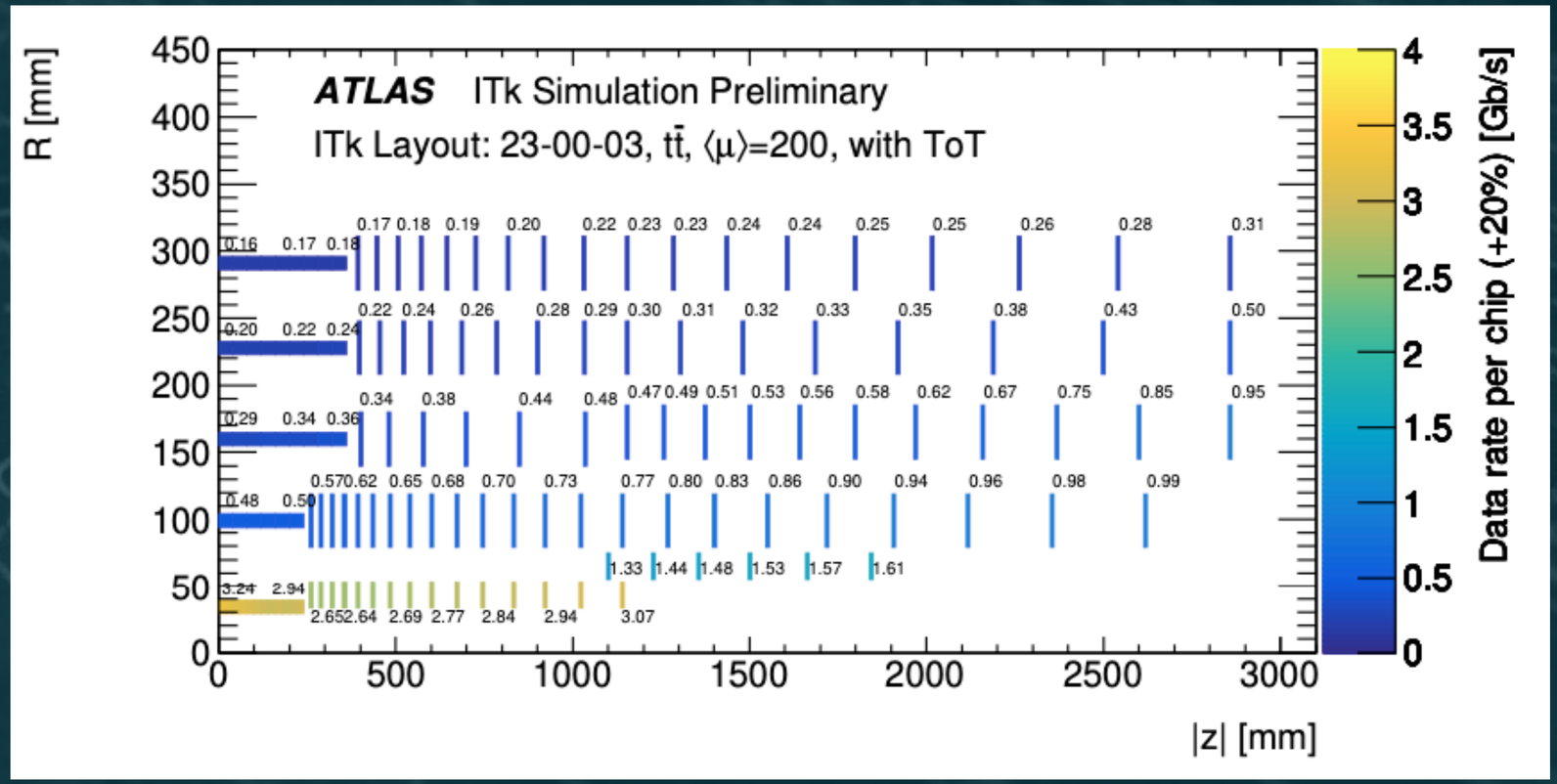
Digital I/O



- Sending only single CMD signal to chip (custom DC balanced encoding)
- CDR/PLL recovers 160MHz clock and generates clocks for different domains (LHC runs with 40MHz bunch crossing frequency)
- High output speed requires 8x multiplication of recovered clock
- Total of four 1.28Gbps output lanes which can be bonded into one Aurora 64b/66b channel (320Mbps in case of data merging)

Data Rates

- Data rates vary drastically over whole detector
- Chip designed for central barrel innermost layer
  - 4x 1.28Gbps links
- Can use single link @ 1.28Gbps
- Majority of detector needs less than half of 1.28Gbps
  - Introduced capability into chip to merge multiple links into one



Link Configuration

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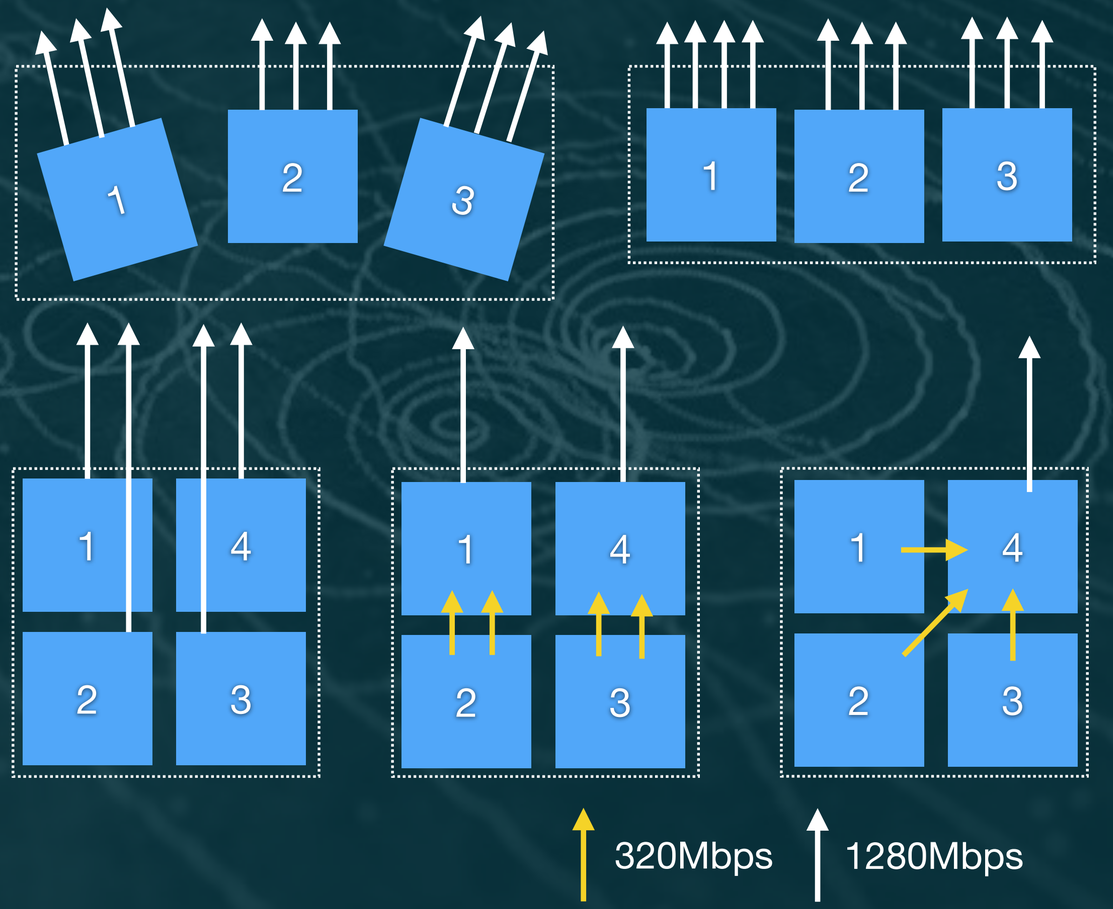
Common Quad Module:
- Three possible modes, chosen via chip configuration
  - 1 link per chip
  - 0.5 links per chip (1 primary, 1 secondary)
  - 0.25 links per chip (1primary, 3 secondary)

Triplet

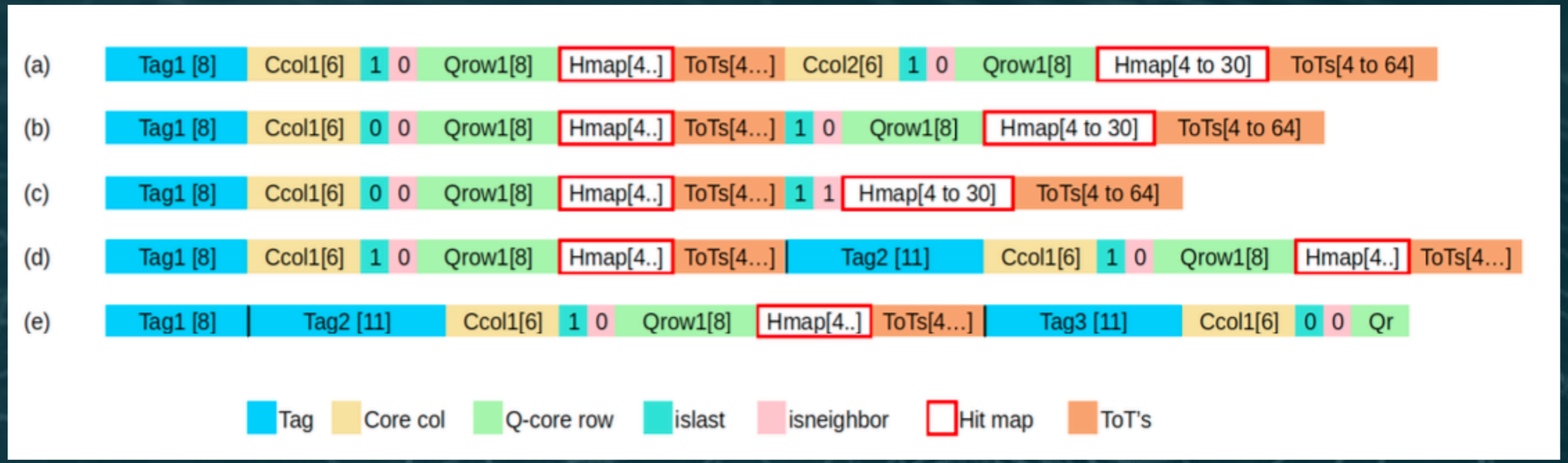
Common Quad

Layer	Section	Number of Links/FE
0	Flat barrel	4
	Barrel rings	3
	End-cap rings	2
1	Flat barrel	0.5
	Barrel rings	1
	End-cap rings	1
2	Flat barrel	0.5
	Barrel rings	0.5
	End-cap rings (1-5)	0.5
	End-cap rings (6-11)	1
3	Flat barrel	0.25
	Barrel rings	0.25
	End-cap rings	0.5
4	Flat barrel	0.25
	Barrel rings	0.25
	End-cap rings (1-7)	0.25
	End-cap rings (8-9)	0.5

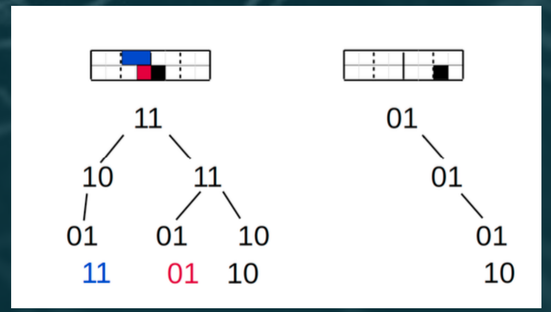
Triplet Module:
- Linear Triplet: 4 links per chip
- Ring Triplet: 3 links per chip



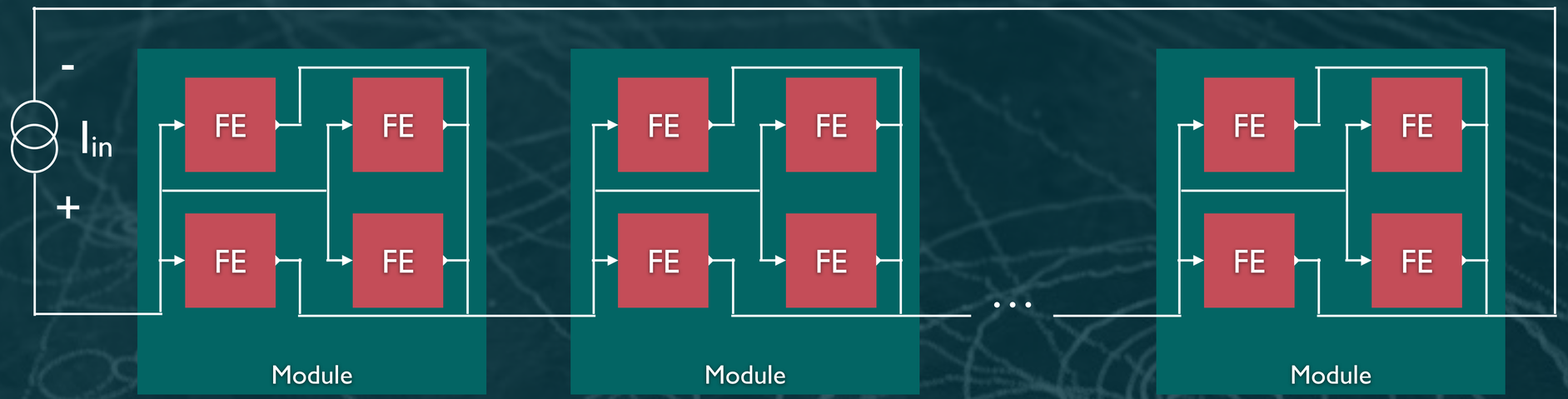
Data Output Protocol



- Link layer protocol: Aurora 66b/66b:
  - Only 3% overhead, DC balanced through scrambling, support of K-words for non-hit-data transfer (register reads)
- Custom data encoding (compression):
  - Had to serve wide range data sparsity, from dense small cluster hits in the inner layer, to sparse large clusters in out layer
- Hit data organized in “streams”, each stream can contain more than one event to effectively use 64bit aurora frame (though ATLAS choose not to use this feature)
- Streams are not-byte aligned, hit addresses can be relative to previous address
- Hit maps combine 4 1x4 pixel regions (16 pixel), hit maps are encoded as binary trees, length can vary

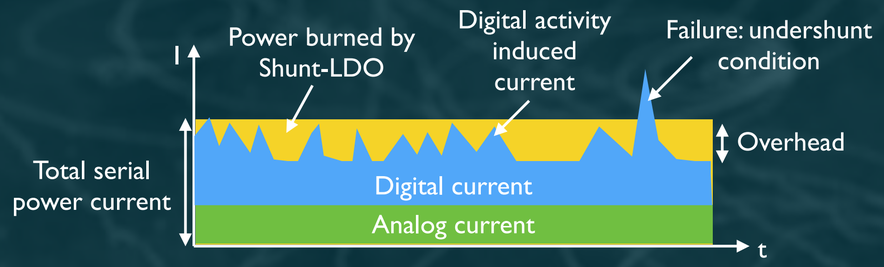


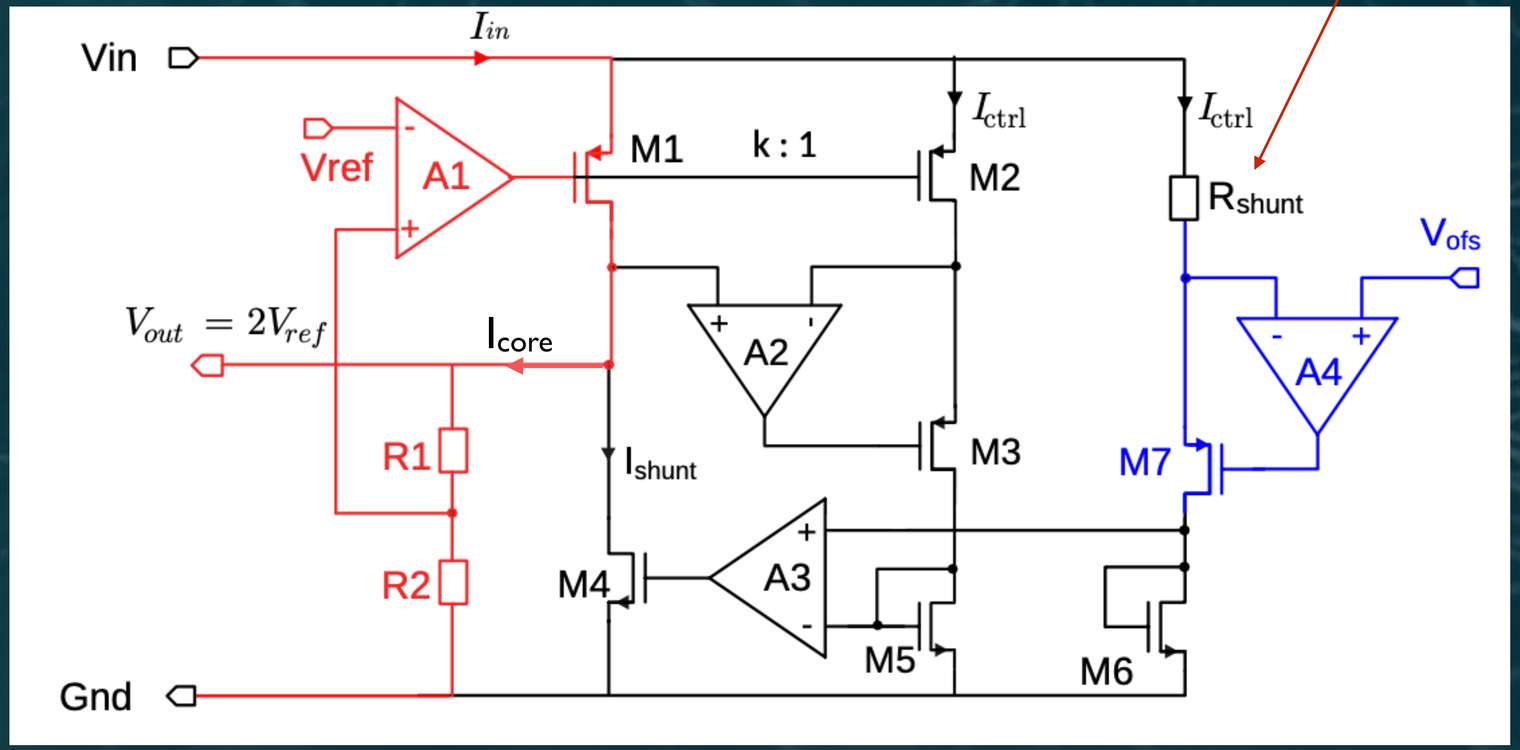
Serial Powering

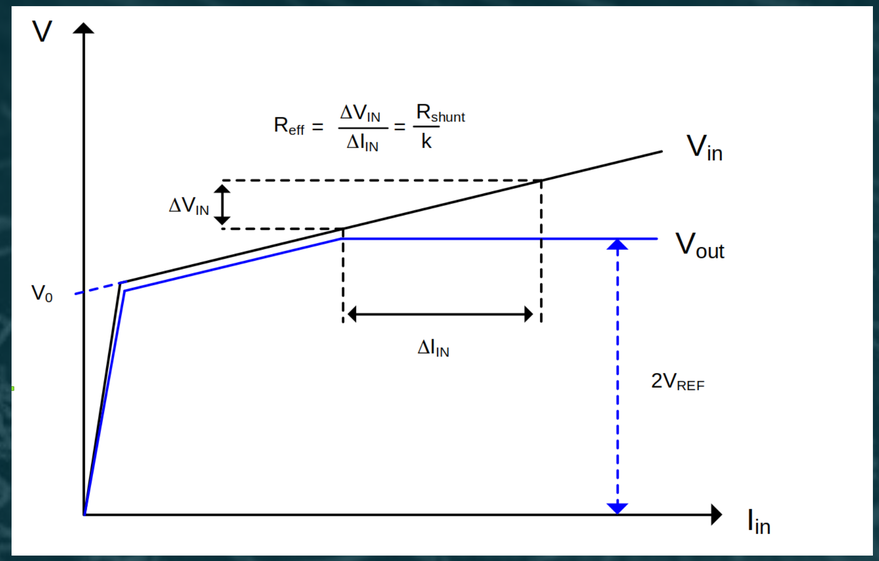


- Advantage of serial powering:
  - Power loss in cable: $P_{heat} = R_{cable} * I^2$ => Less current => Less mass (Higher resistance)
  - Parallel powering: current scales with modules
  - Serial powering: voltage scales with modules
- But serial powering requires module impedance to be constant
  - If impedance is not constant over time, power supply will have to react
  - PSU reaction is delayed due to cable inductance
  - => Impedance changes result in voltage transients in chain
- Chip impedance inherently not constant but depends on activity
  - Shunt LDO circuit stabilizes chip impedance to the outside world

Powering







k ≈ 1000

$$I_{in} = I_{core} + I_{shunt} = k * I_{ctrl}$$

$$I_{ctrl} = (V_{in}-V_{ofs}) / R_{shunt}$$

$$V_{in} = V_{ofs} + I_{in} * R_{shunt} / k$$

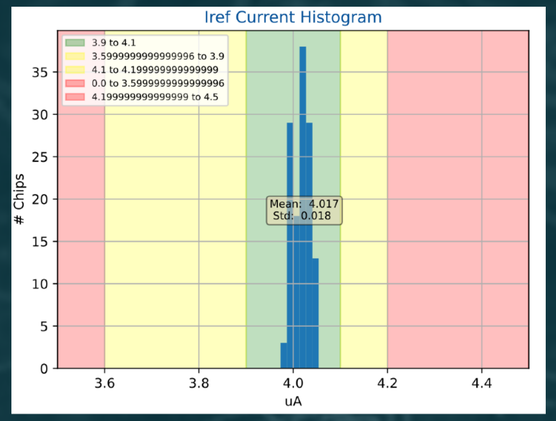
An Example

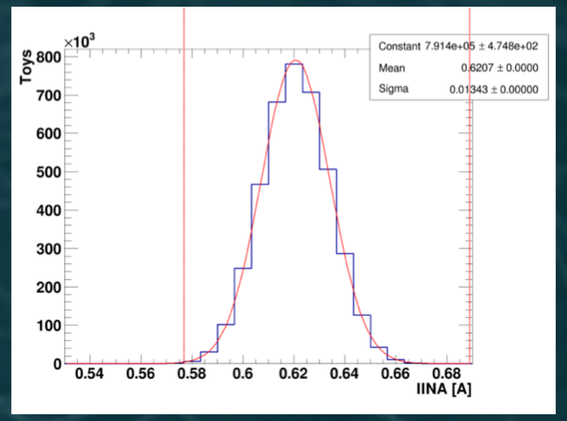
	Analog	Digital	Total Chip	Total Module
Analog Periphery [A]	0.120			
Analog Matrix [A]	0.440			
Digital Periphery [A]		0.250		
Digital Periphery Activity [A]		0.010		
Digital Matrix [A]		0.450		
Digital Matrix Activity [A]		0.040		
Icore[A]	0.560	0.750		
I_{core}+ overhead (10/20%) [A]	0.616	0.900		
I_{shunt}	0.056	0.150		
I_{in}current per chip [A]			1.516	6.064
k	1000	1000		
Offset [V]			1.000	
Target V_{in} [V]			1.500	
R_{ext} [Ohm]	812	556		
R_{eff} [Ohm]			330	82

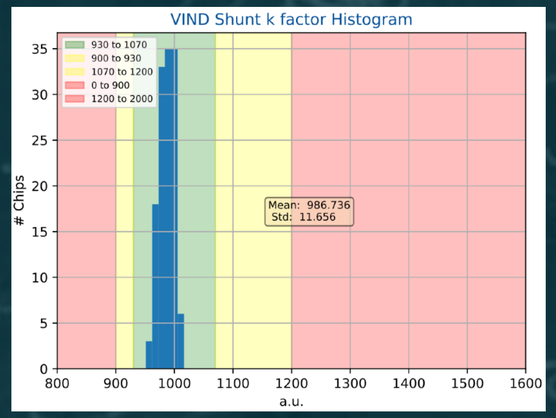
$$R_{shunt} = (V_{in}-V_{ofs}) / I_{ctrl}$$
$$= (V_{in}-V_{ofs}) / (I_{in} / k)$$
$$V_{in} = V_{ofs} + (R_{eff} * I_{in})$$

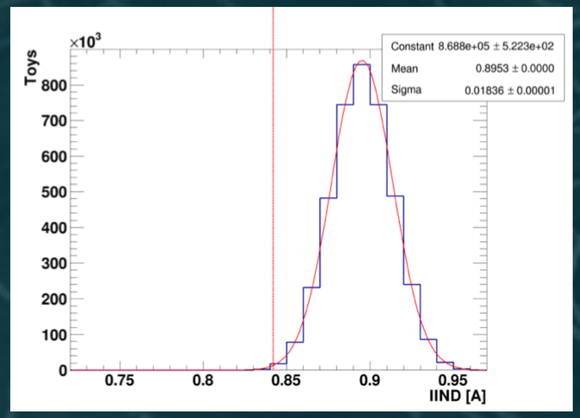
Impedance of chip/module will be equal to R_{eff} unless I_{shunt} goes to 0A!

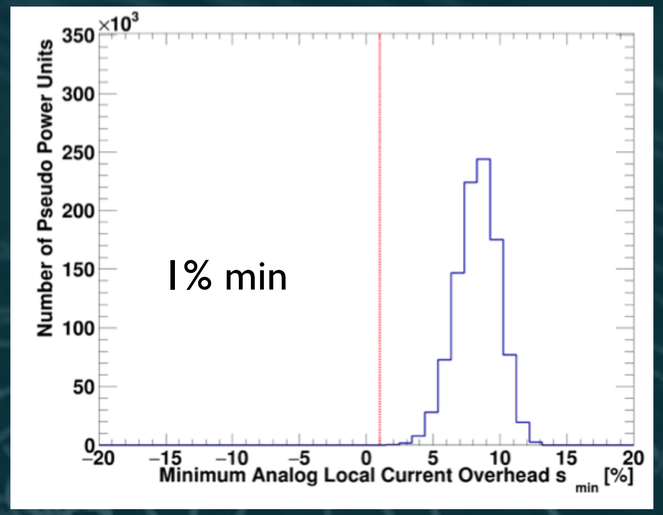
The Culprit

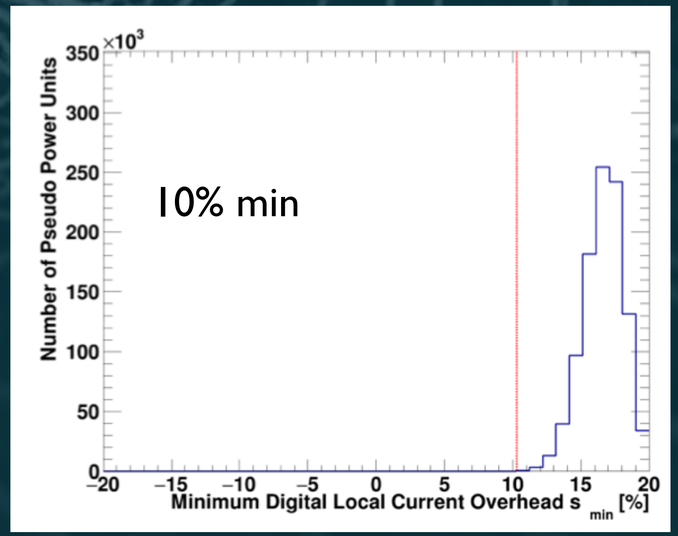












- Variations in k-factor, resistance, Vin, and Vofs will lead to change in impedance
  - k-factor measured on cut on during wafer probing
  - 0.1% tolerance resistors
  - $V_{ofs} = 2*(R_{ofs}*I_{ref})$ => Ref measured and cut on during wafer probing
- Variation in impedance will lead to unequal current splitting in module
  - Lower impedance chips will take away current from higher impedance chips
- Variation in I_{core} will lead to reduced overhead

Backup

25um x 100um Pixels

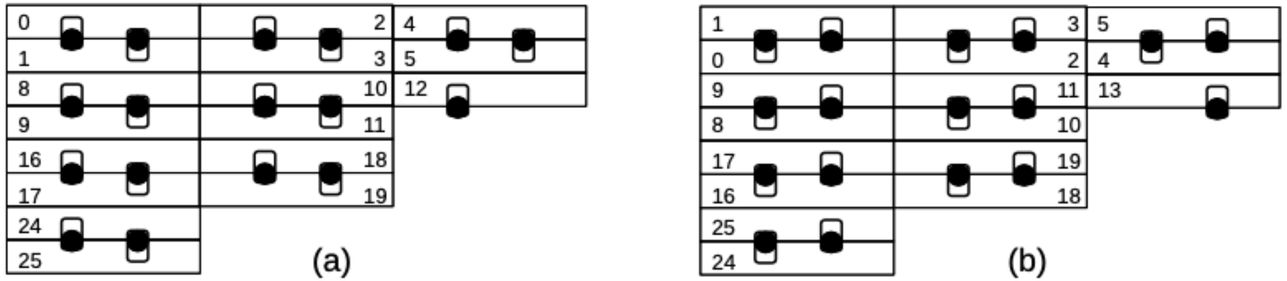
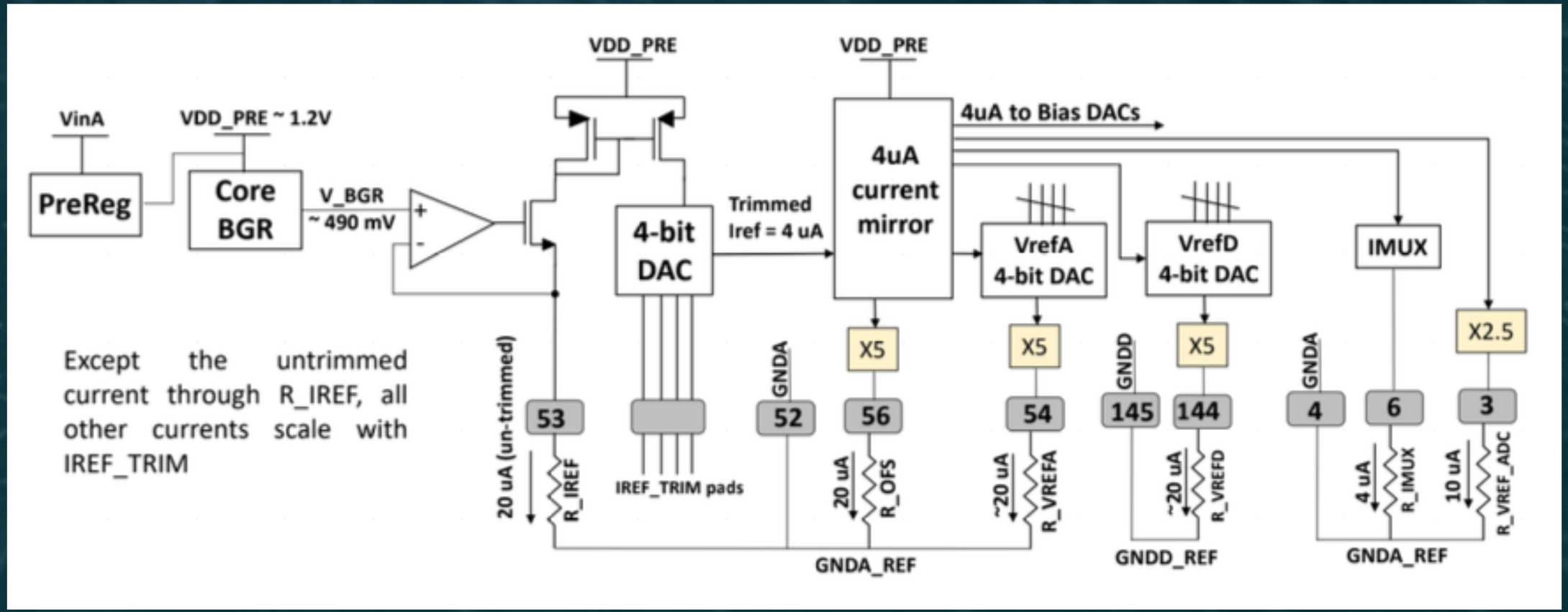
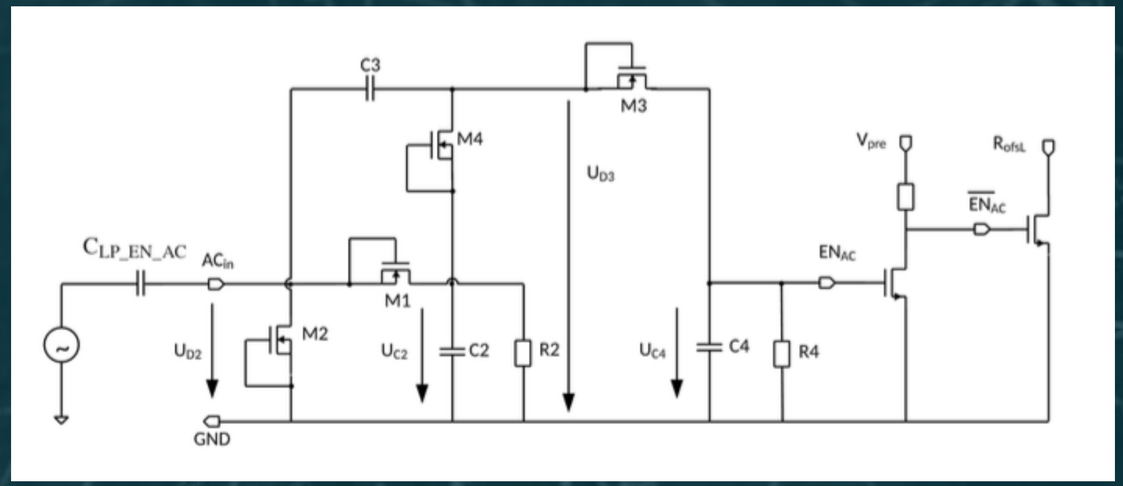


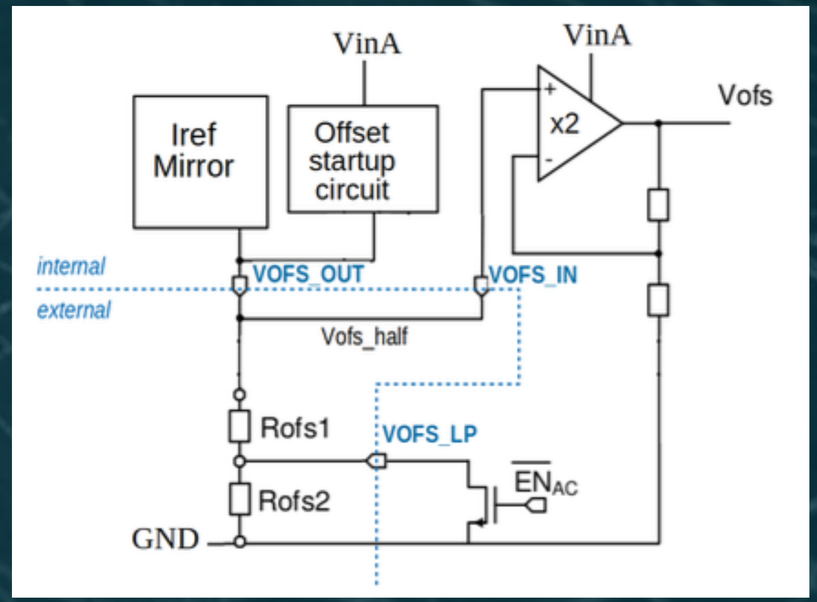
Figure 48: Two options (a and b) for mapping of 25 μm $\times$ 100 μm pixel sensors to the core pixel address. Which option is correct is determined by the sensor metalization. The filled circles represent the bump bond locations while the open rounded rectangles extend from each bump to the center line of the sensor pixel served. The top left corner of an 8 by 8 pixel core is shown.

References

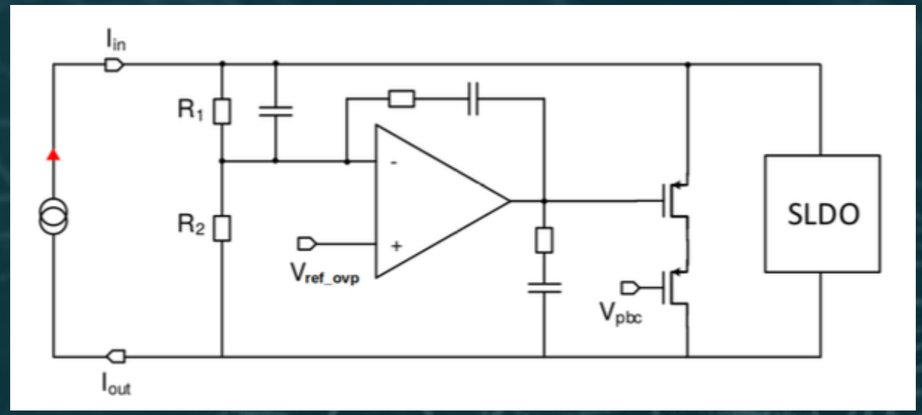

VinA
VDD_PRE ~ 1.2V
PreReg
Core BGR
V_BGR ~ 490 mV
VDD_PRE
VDD_PRE
4-bit DAC
Trimmed Iref = 4 uA
4uA current mirror
4uA to Bias DACs
VrefA 4-bit DAC
VrefD 4-bit DAC
IMUX
X2.5
X5
X5
X5
Except the untrimmed current through R_IREF, all other currents scale with IREF_TRIM
20 uA (un-trimmed)
53
R_IREF
IREF_TRIM pads
GNDA
52
20 uA
56
R_OFS
~20 uA
54
R_VREFA
GNDD
145
~20 uA
144
R_VREFD
GNDA
4
4 uA
6
R_IMUX
10 uA
3
R_VREF_ADC
GNDA_REF
GNDD_REF
GNDA_REF

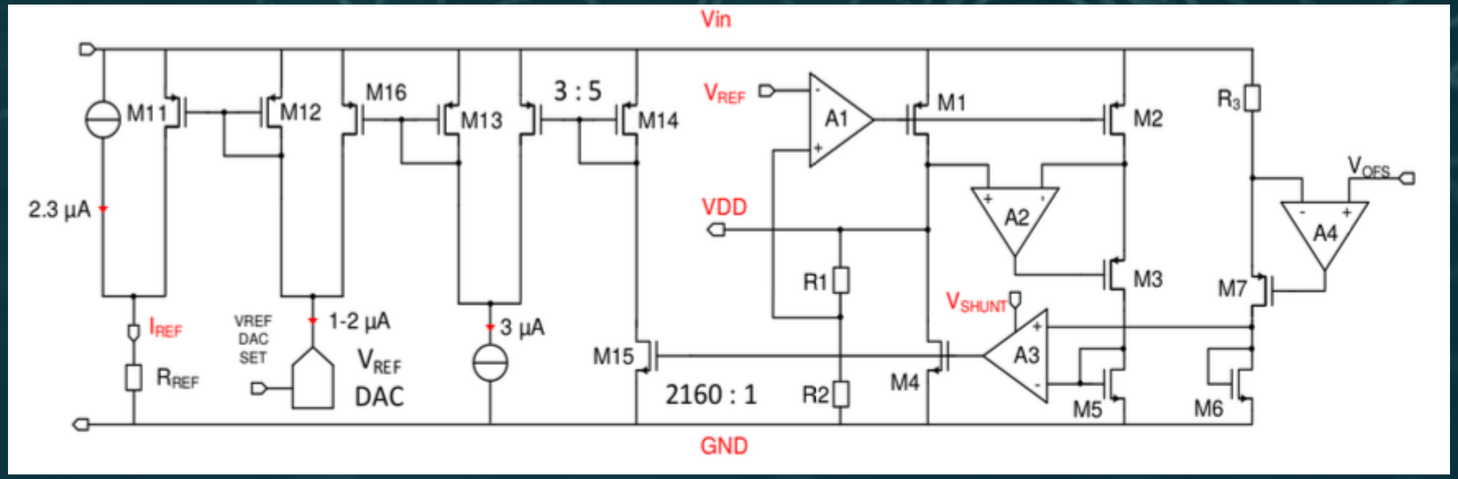
Low Power Mode



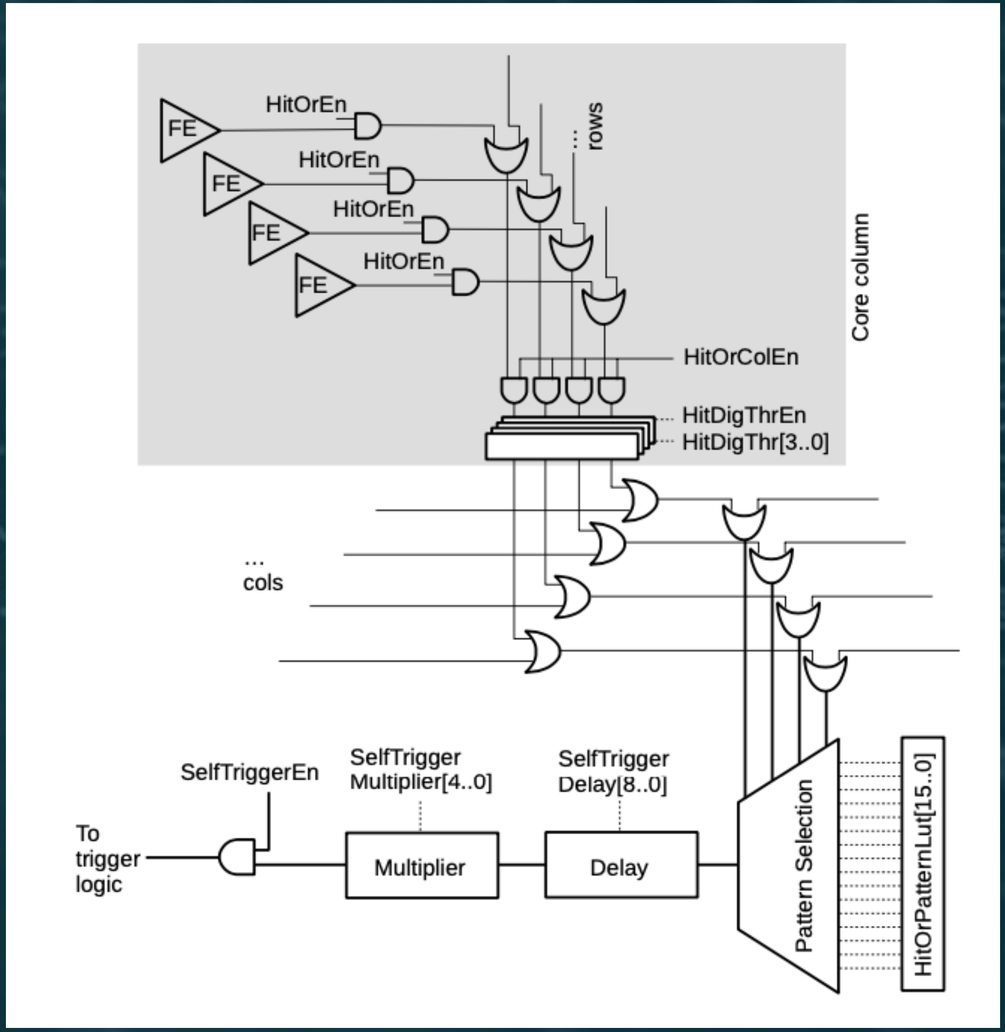


Overvoltage & Undershunt Protection

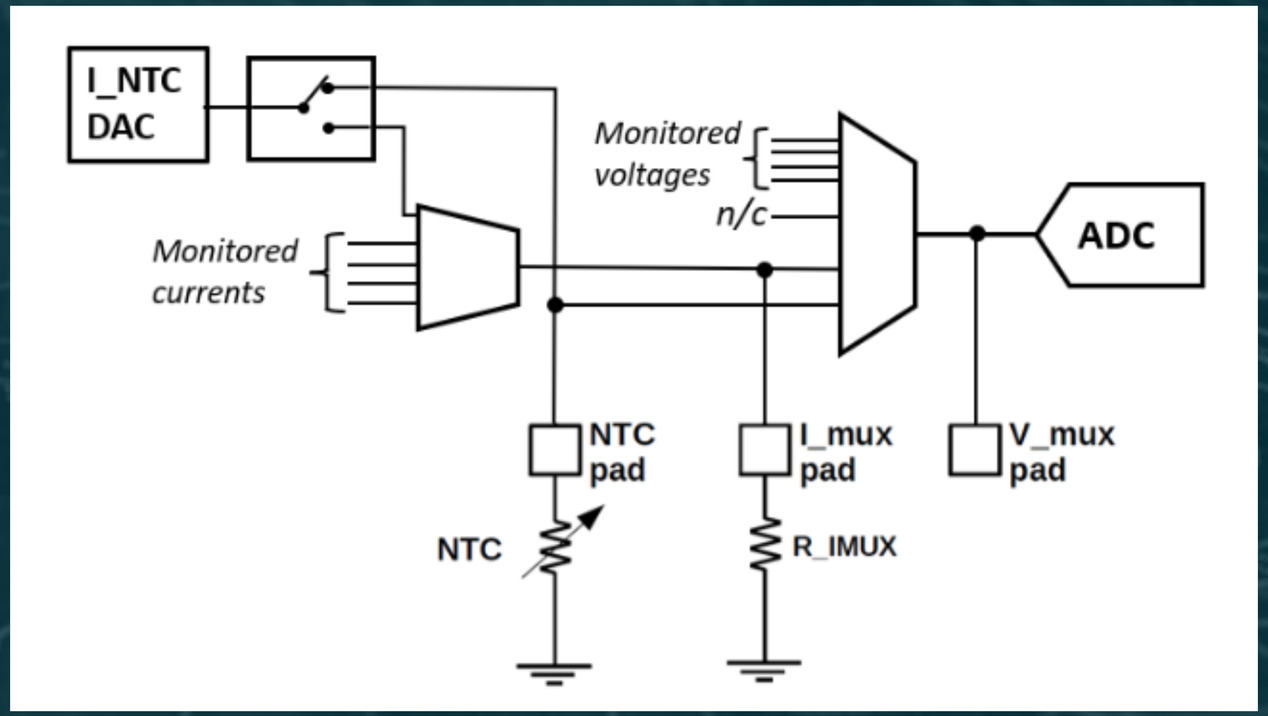




Selftrigger



Vmux/Imux


I_NTC
DAC
Monitored
voltages
n/c
ADC
Monitored
currents
NTC
pad
I_mux
pad
V_mux
pad
NTC
R_IMUX