Radiation Effects in CMOS Technologies for LHC Detector Upgrades

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Total Ionising Dose

This is the ‘classical’ problem for CMOS technologies and has to be addressed

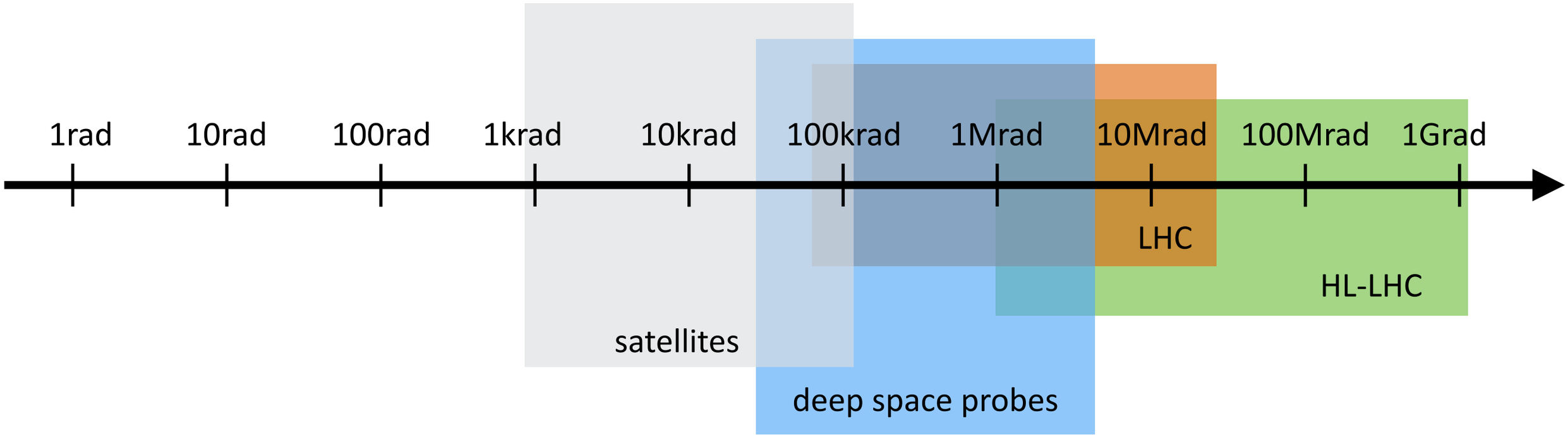
Displacement Damage

It is very difficult to design a Reference voltage generator (bandgap) very stable with displacement damage and TID

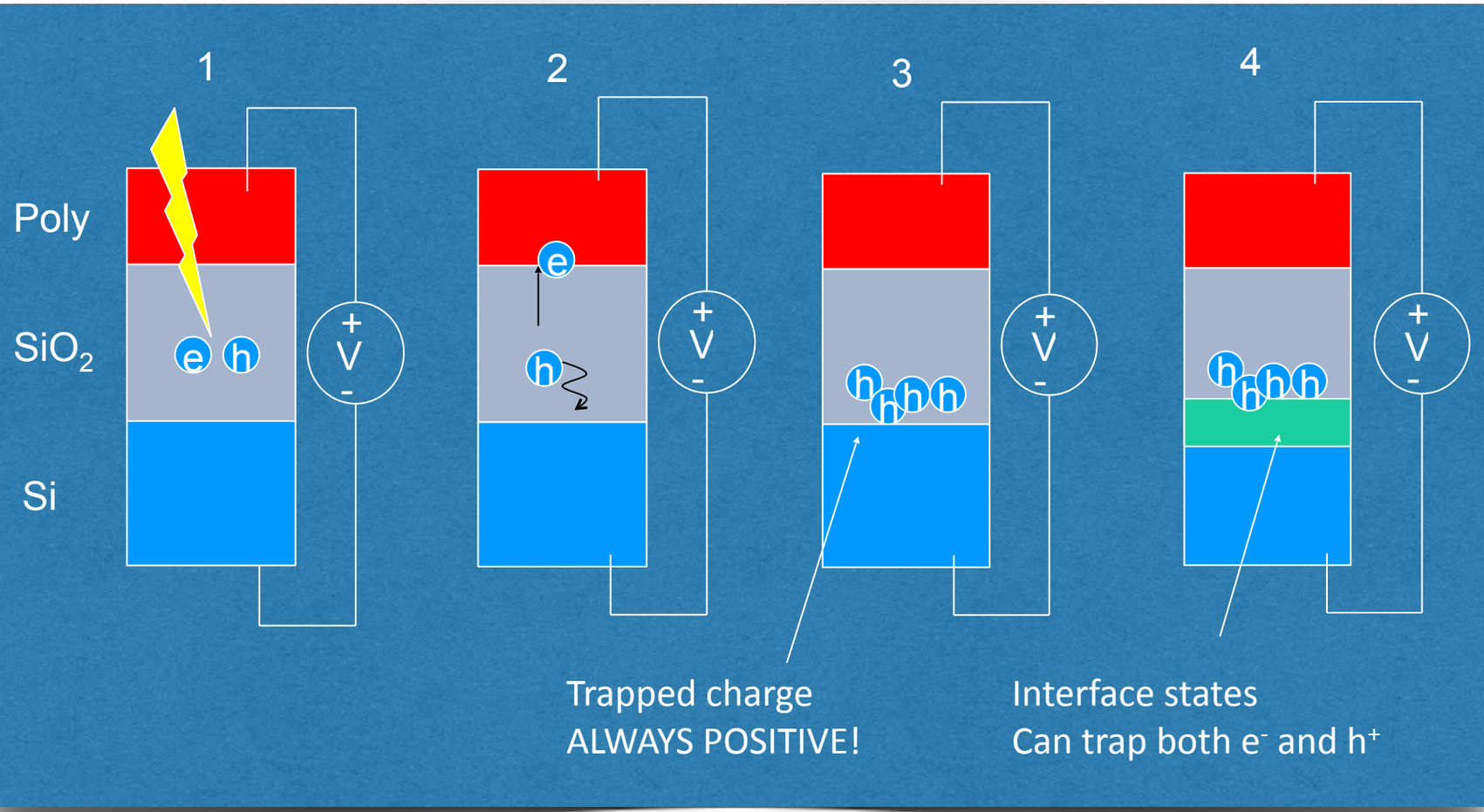
Single Event Effects

‘Usual’ strategies are needed, but multiple bit errors are more likely - separation between redundant storing cells is required

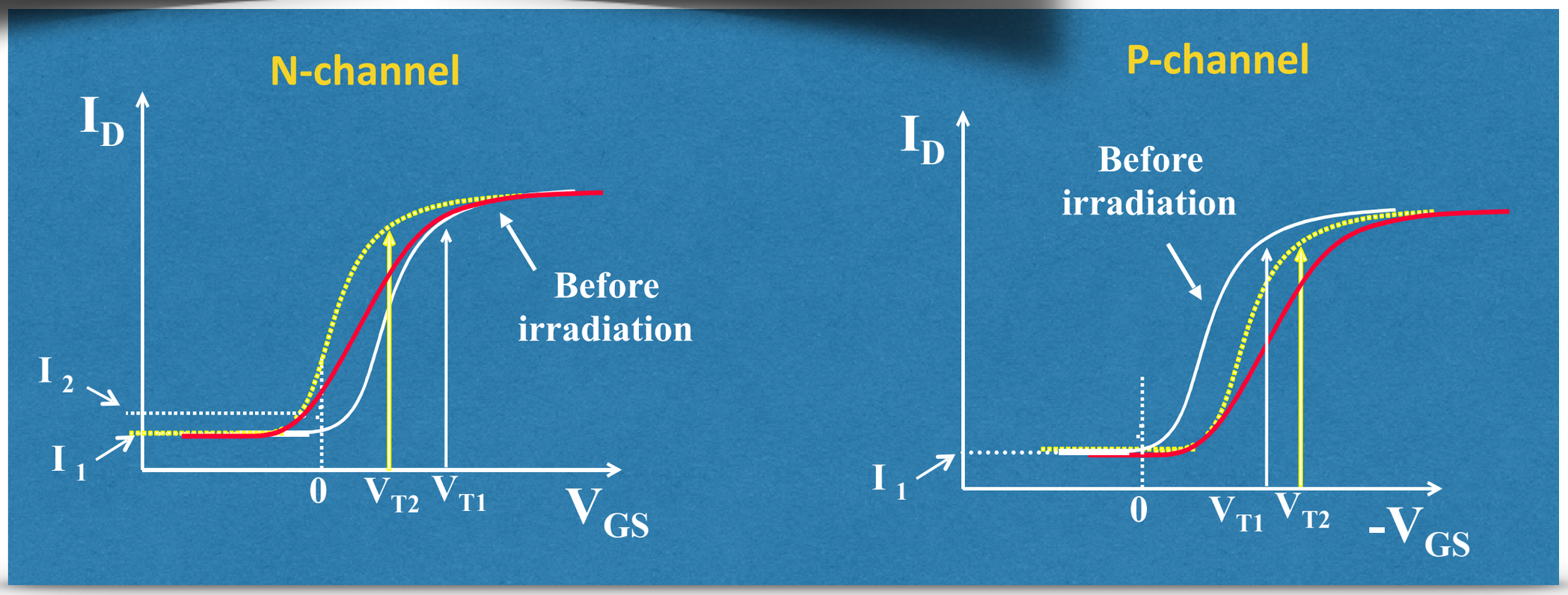
TID levels in different applications



The basis of TID effects in CMOS structures

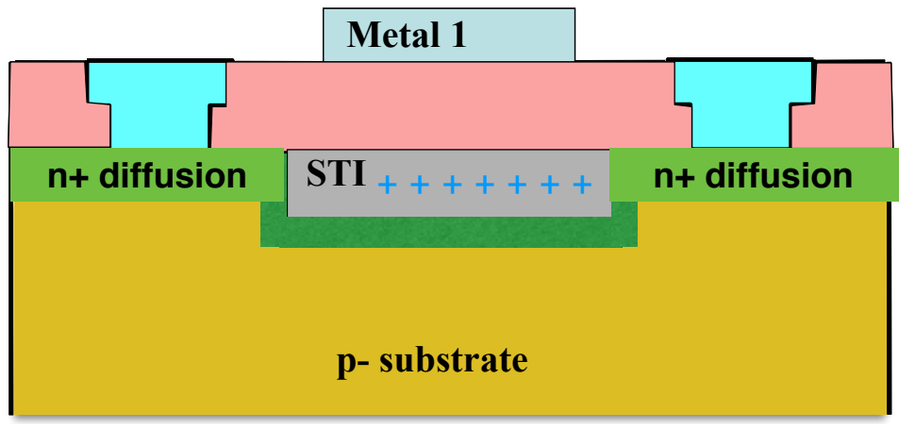


	n-channel	p-channel
Oxide charges	+	+
Interface states	–	+

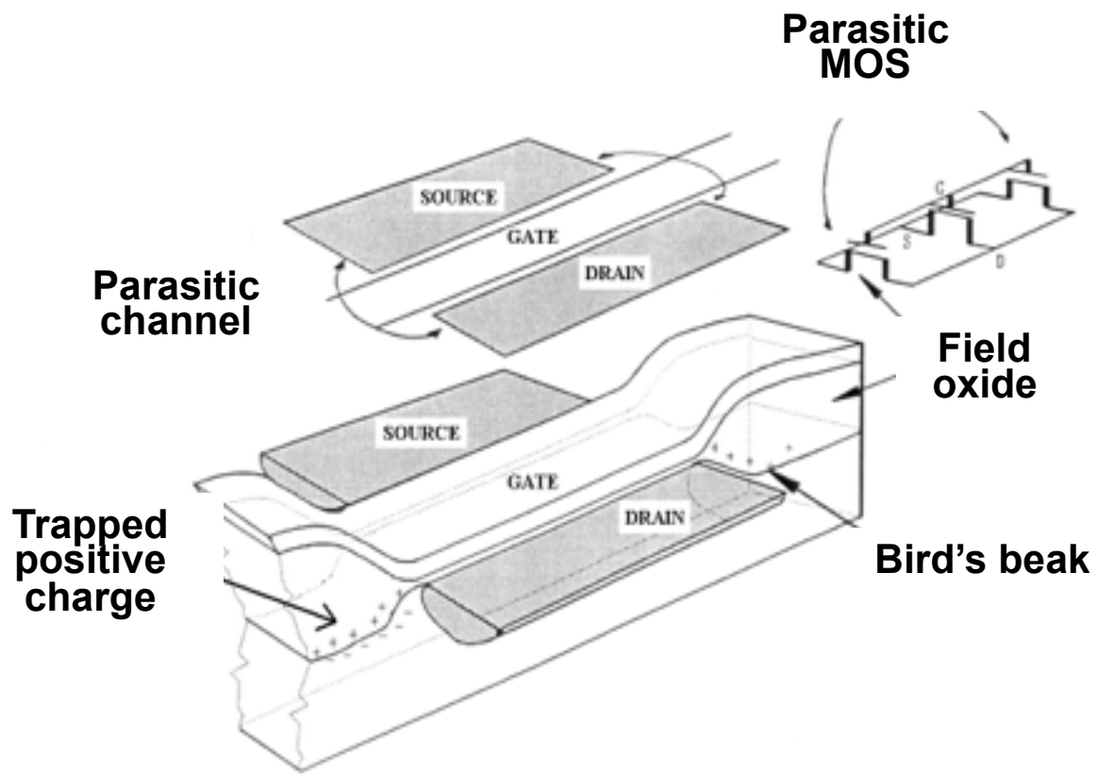


Charge buildup in the oxides and at their interface influences the electrical parameters of transistors (for the gate oxide) and of parasitic structures unavoidable in CMOS

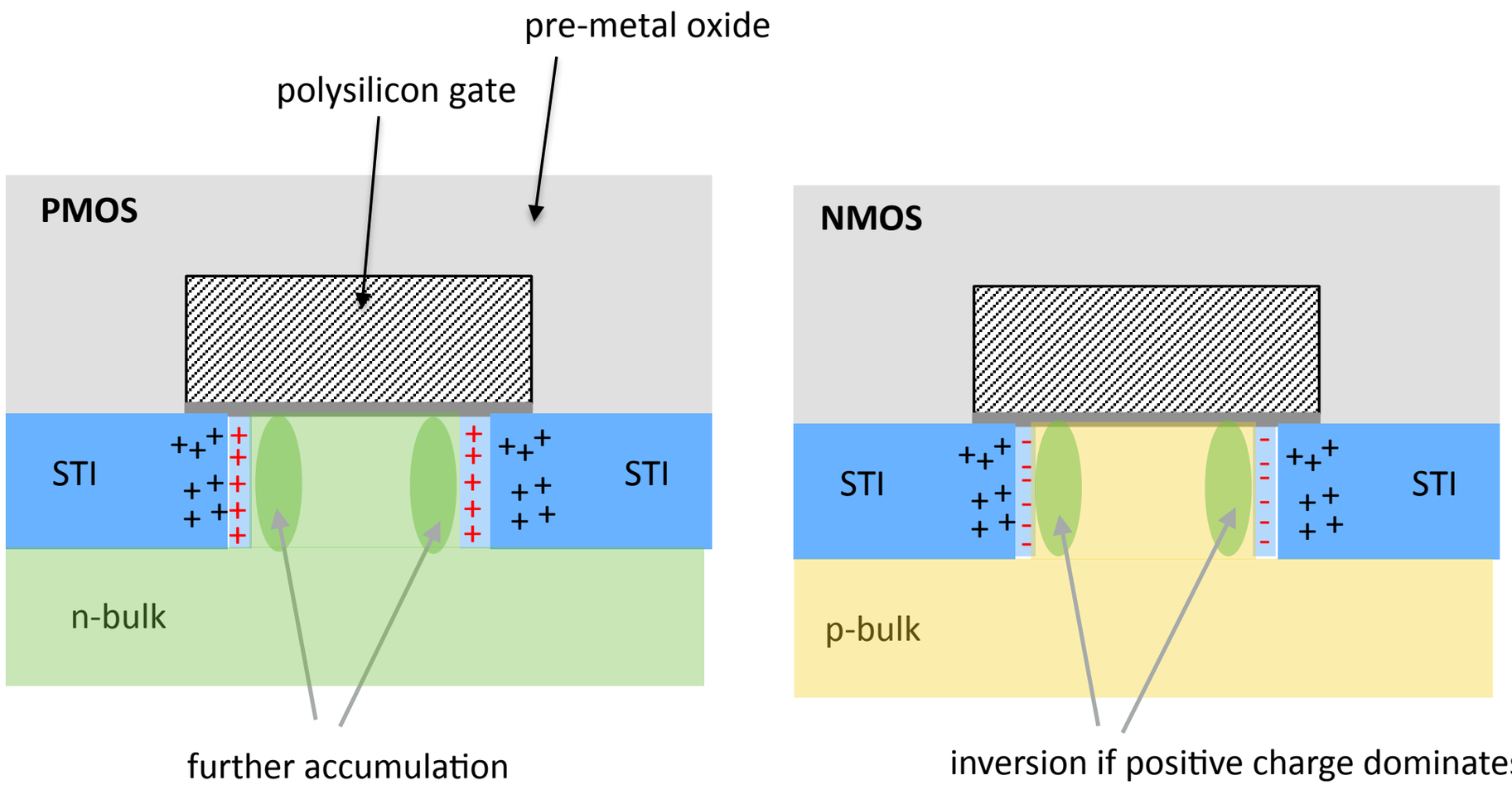
Leakage between adjacent n-diffusions



Source-Drain leakage in NMOS

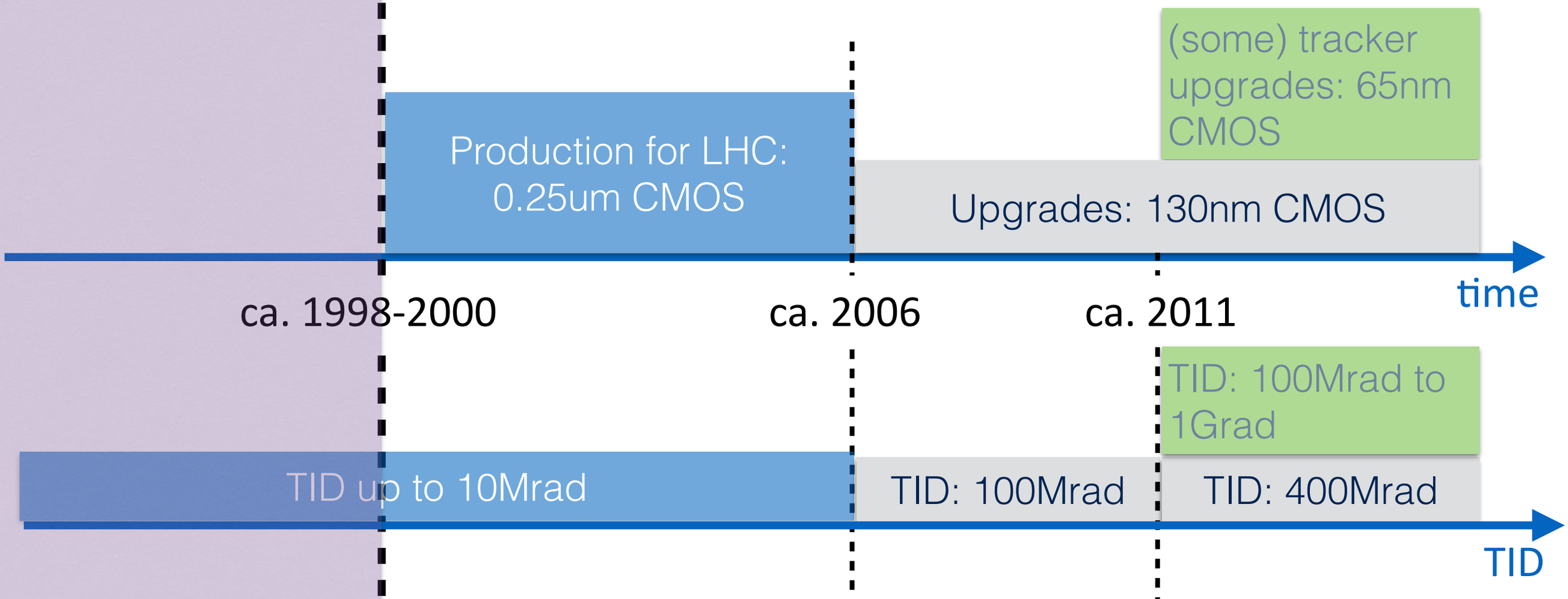


Source-Drain leakage in NMOS is due to positive charge trapped in the bulk of the STI oxide



Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes



Main transistor

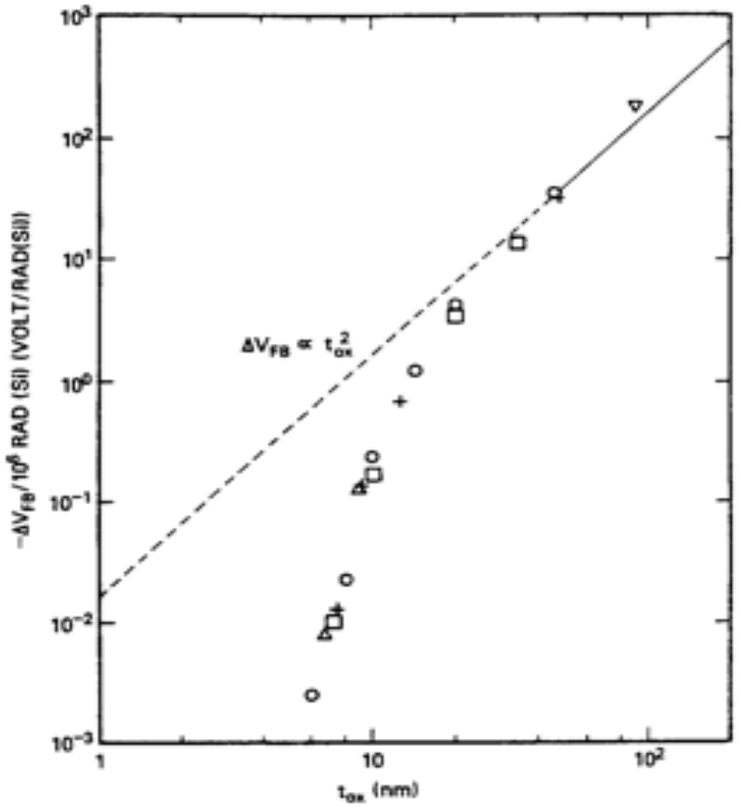
V_{th}, g_m, …

Leakage in parasitics

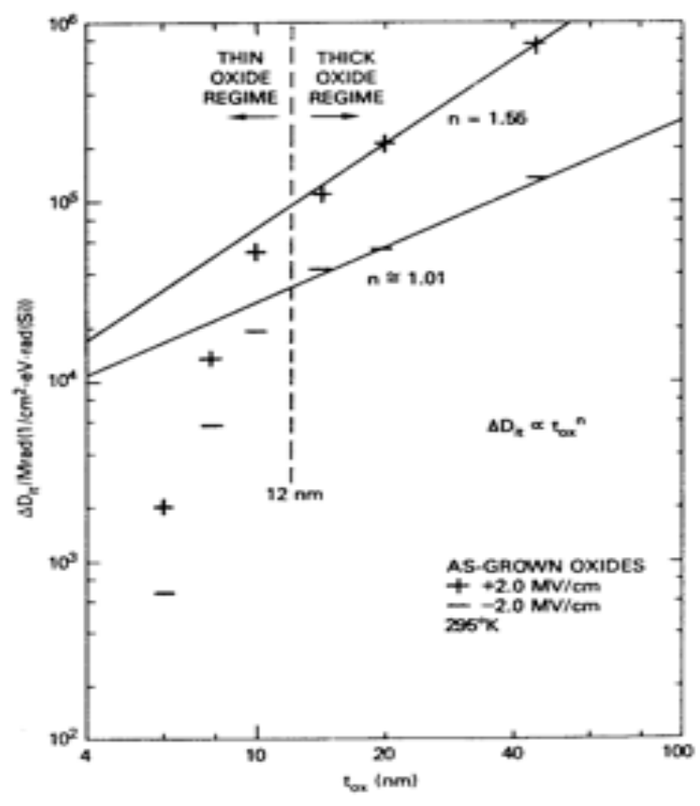
Leakage in parasitics

The accumulation of TID-inducd ‘defects’ in an oxide decreases with the thickness of the oxide

Oxide trapped charge



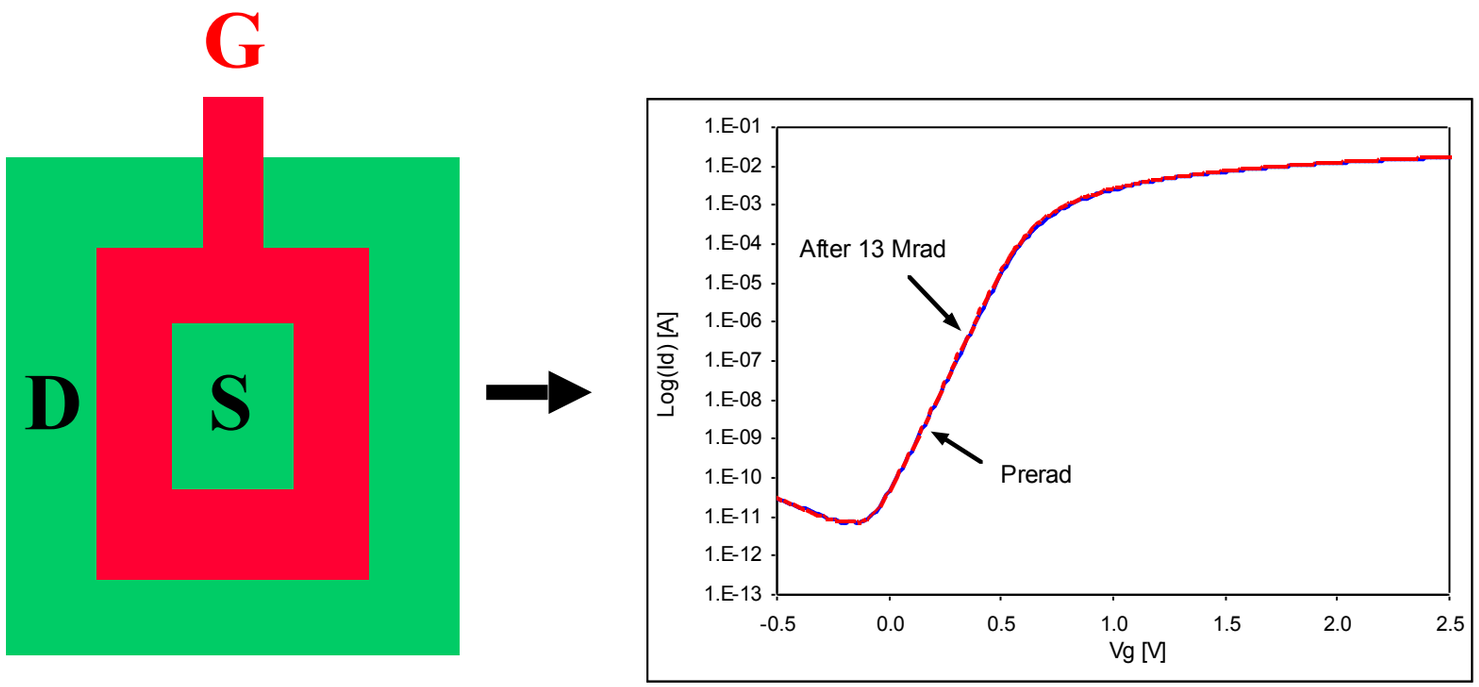
Interface states



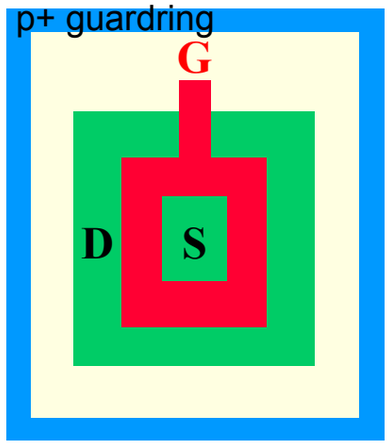
N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

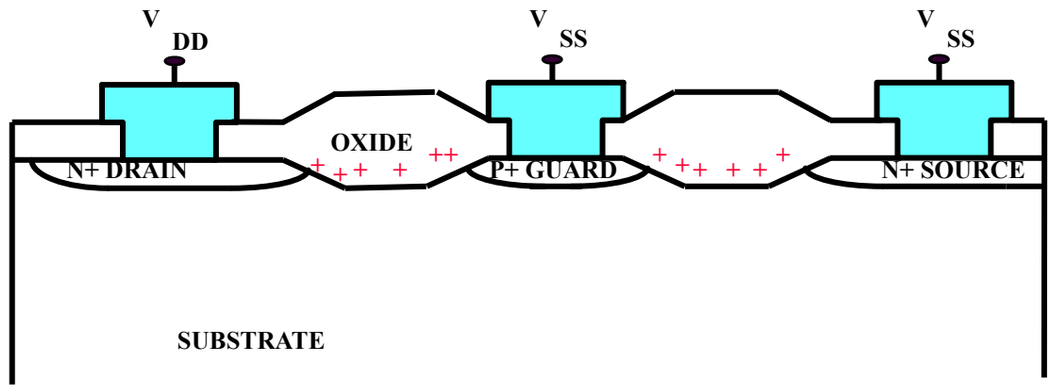
If the gate oxide is sufficiently thin, problems arise in the parasitic structures where the oxide thickness does not follow any scaling rule

Source-Drain leakage is eliminated by the Enclosed Layout Transistor (ELT)…



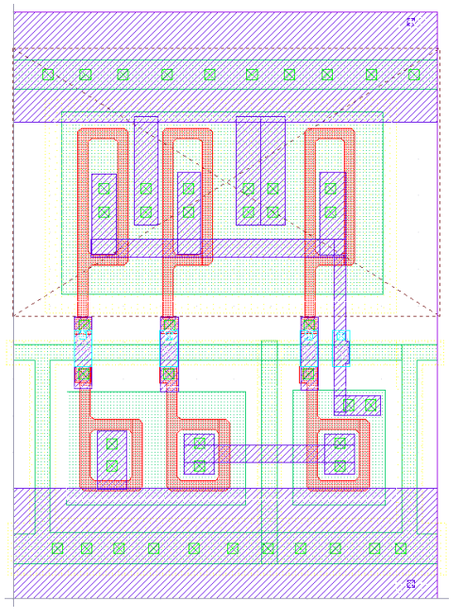
Inter-diffusion leakage is eliminated by p+ guard rings…

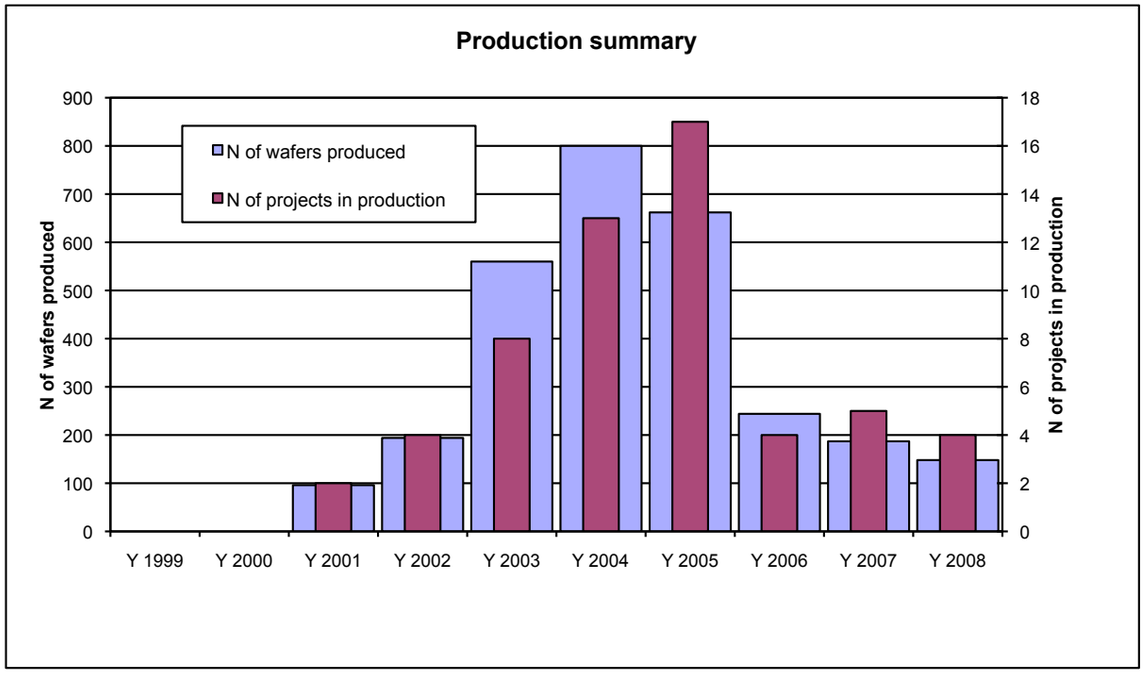




The equation used for the design of ASICs used in today's LHC experiments and manufactured in an (affordable) commercial-grade 0.25um process is:

Thin gate oxide + HBD techniques = Radiation tolerance





Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes

(some) tracker upgrades: 65nm CMOS

Production for LHC: 0.25um C

Upgrades: 130nm CMOS

Valid HERE

Still valid?

time

ca. 1998-2000

ca. 2006

ca

D: 100Mrad to 1Grad

TID up to 10Mrad

TID: 100Mrad

TID: 400Mrad

TID

Main transistor

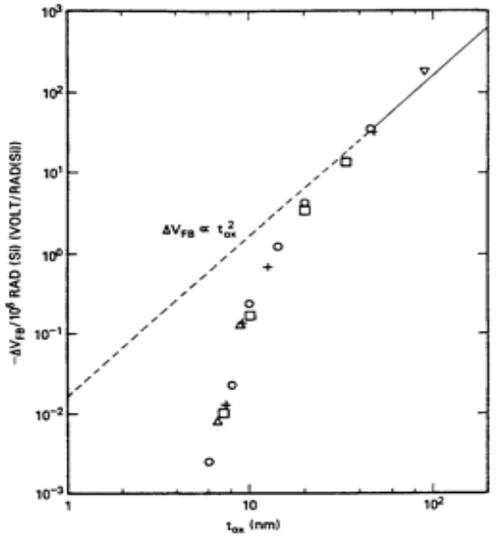
V_{th}, g_m, …

Leakage in parasitics

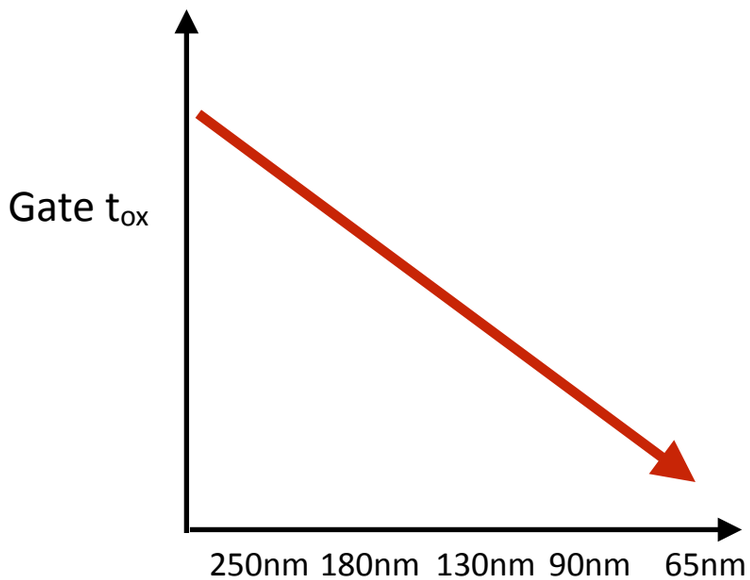
Leakage in parasitics

Is this extrapolation correct?

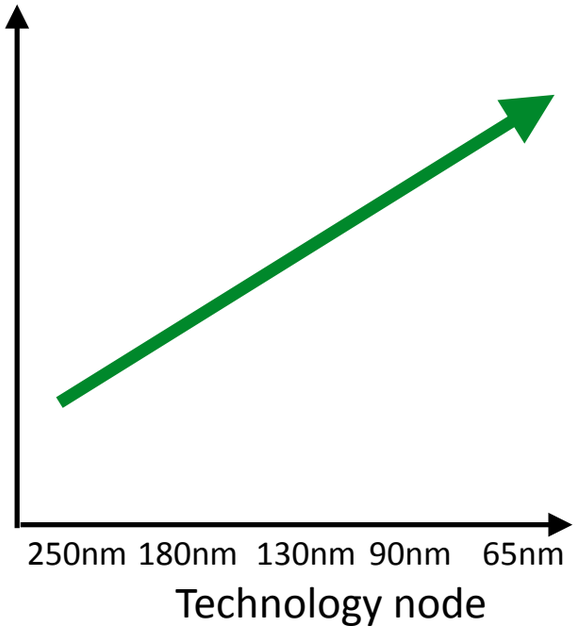
TID damage



Gate t_{ox}



TID tolerance



In 2003-2005 we started to look at the 130nm node in view of application in LHC upgrades

Samples from 3 different vendors were irradiated and measured

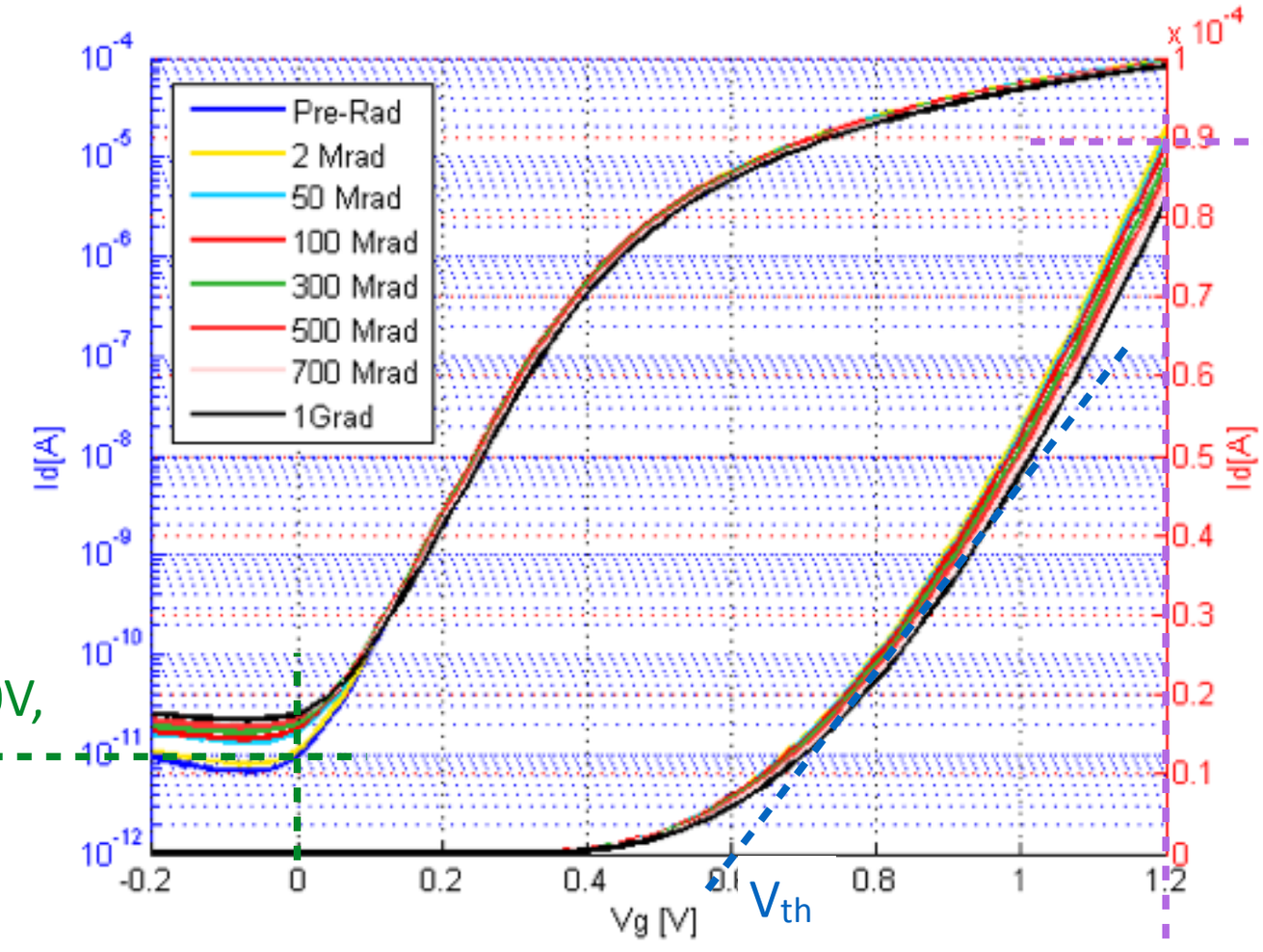
Need for a commercial framework

Is gate oxide tolerance confirmed?

Is there still the need for ELTs and guard rings?

The main parameters extracted from the measurements are:

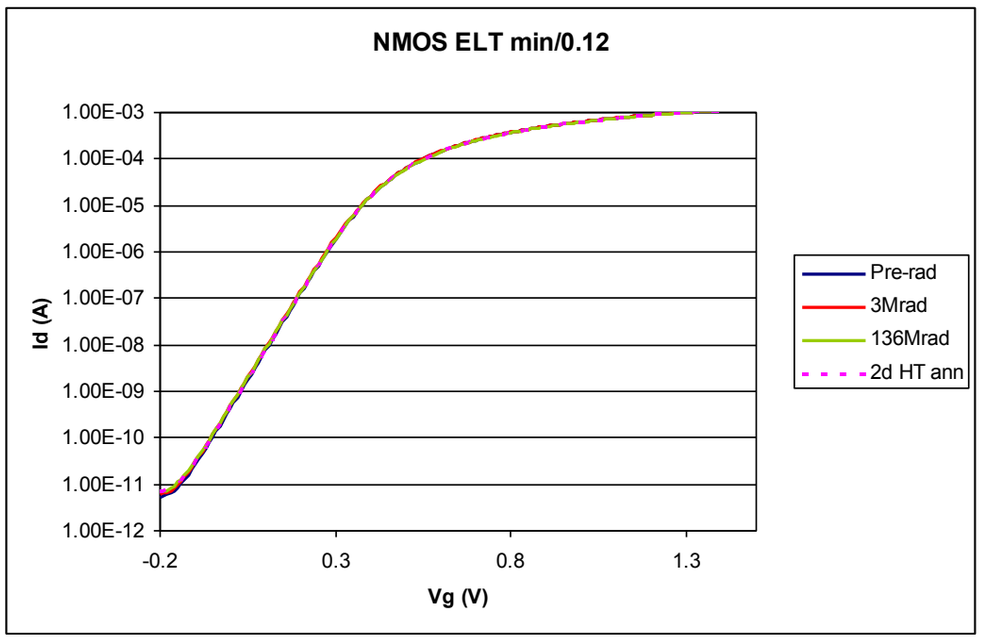
- **Drive current (I_{on})**
- **Threshold voltage (V_{th})**
- **Transconductance (G_m)**
- **Leakage current**

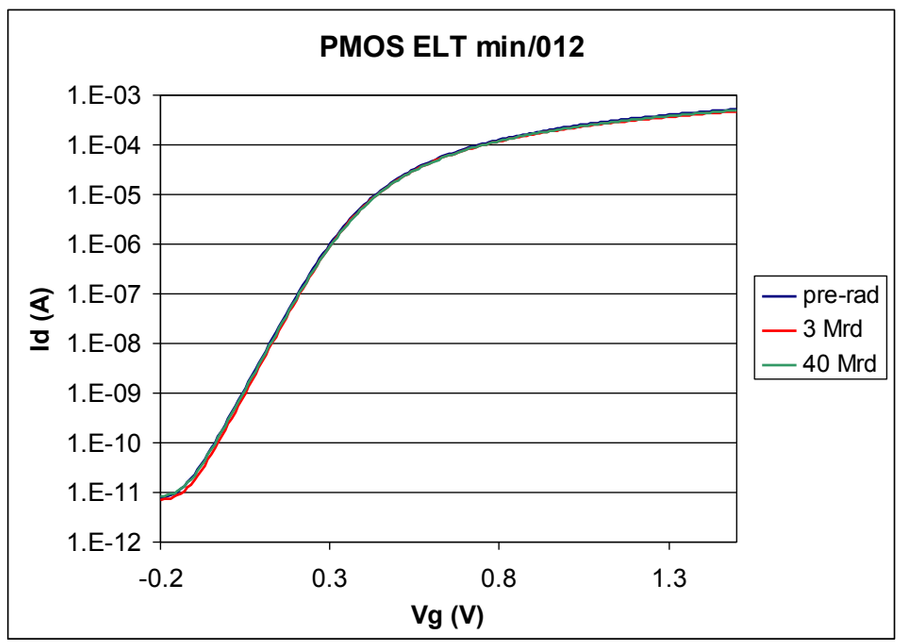


The gate oxide in the three 130nm technologies studied appeared to be hard to the explored levels (30-140Mrad)

This was directly measured on ELT transistors in 2 of the 3 technologies

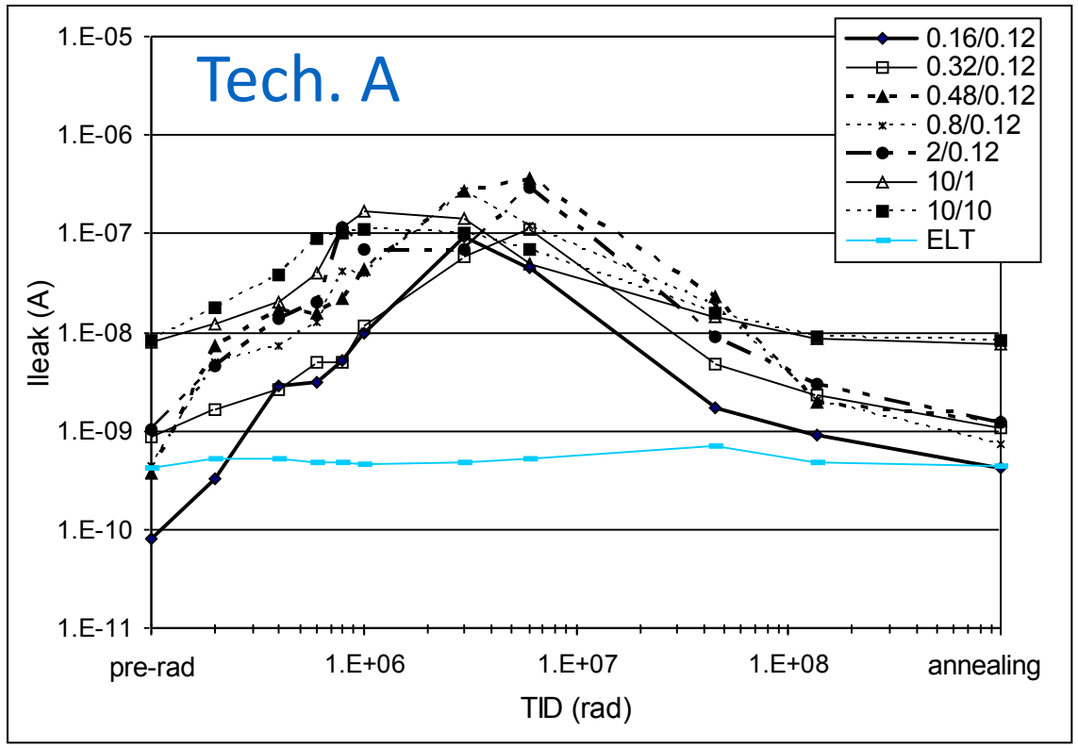
Example for ELTs in tech.A

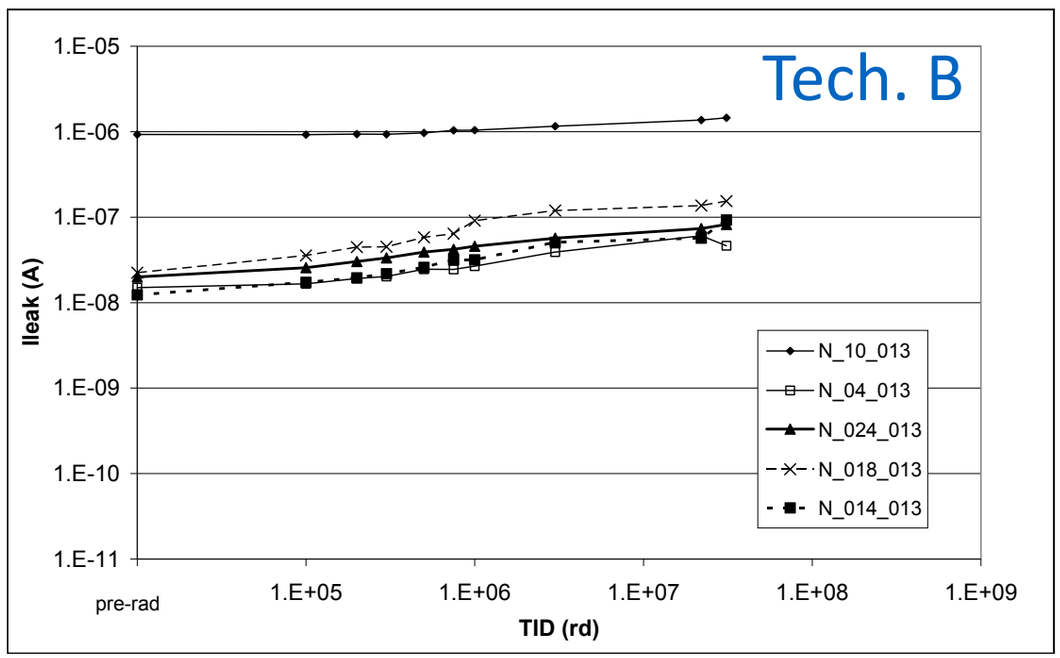


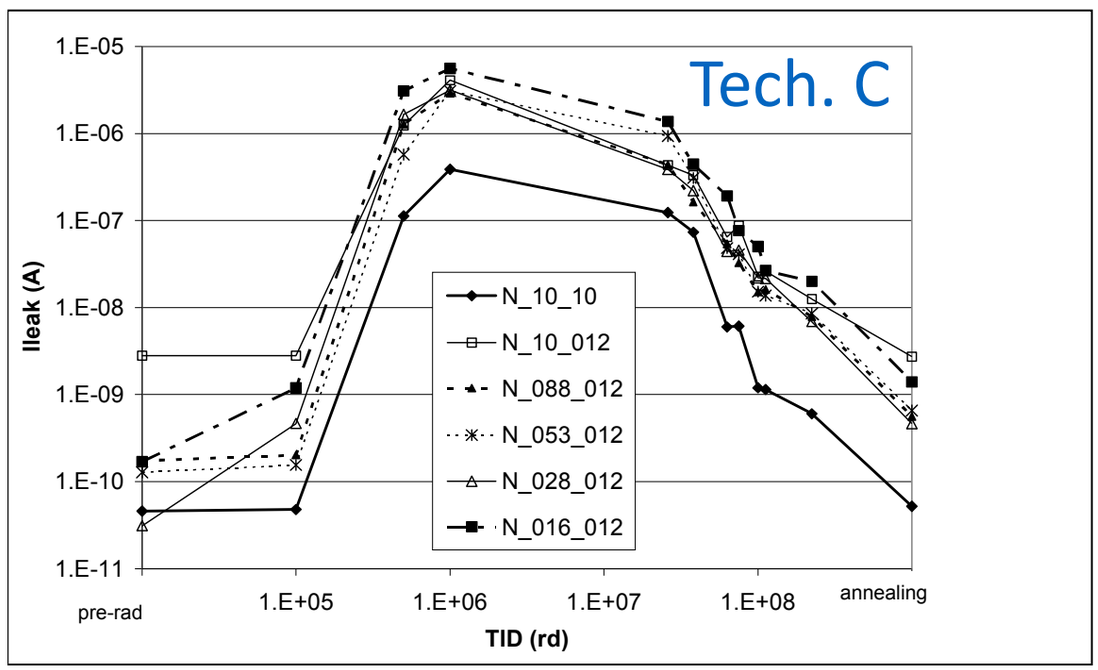


The leakage paths are technology dependent

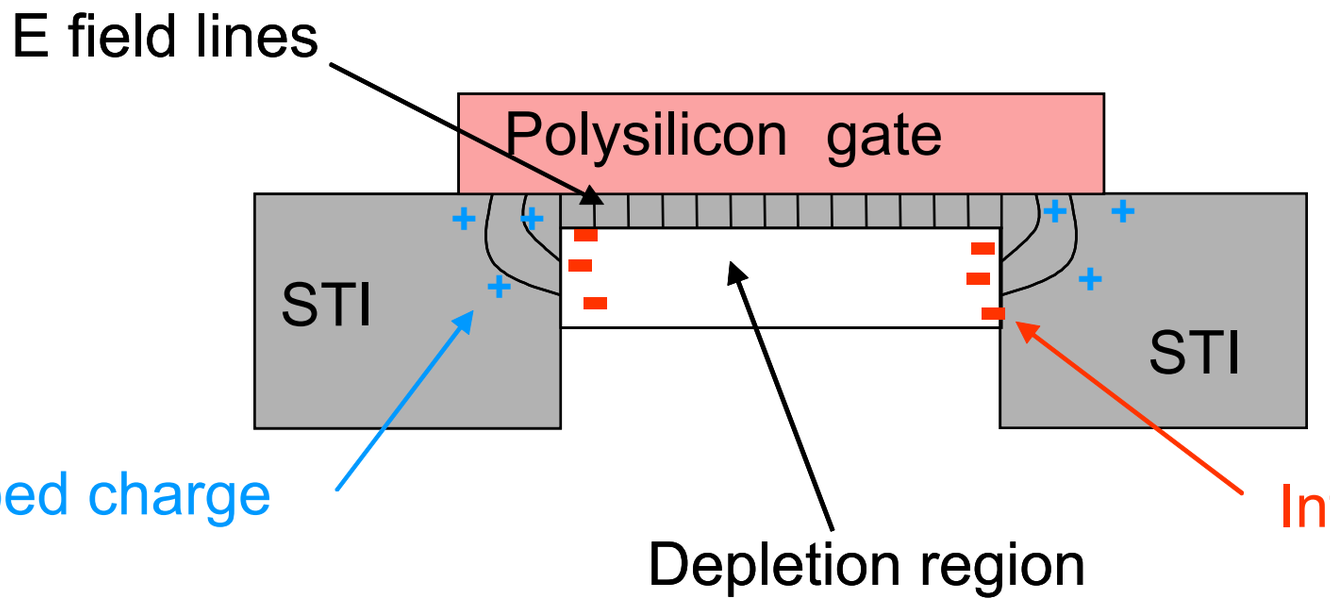
(here this is shown for source-drain leakage currents in NMOS)

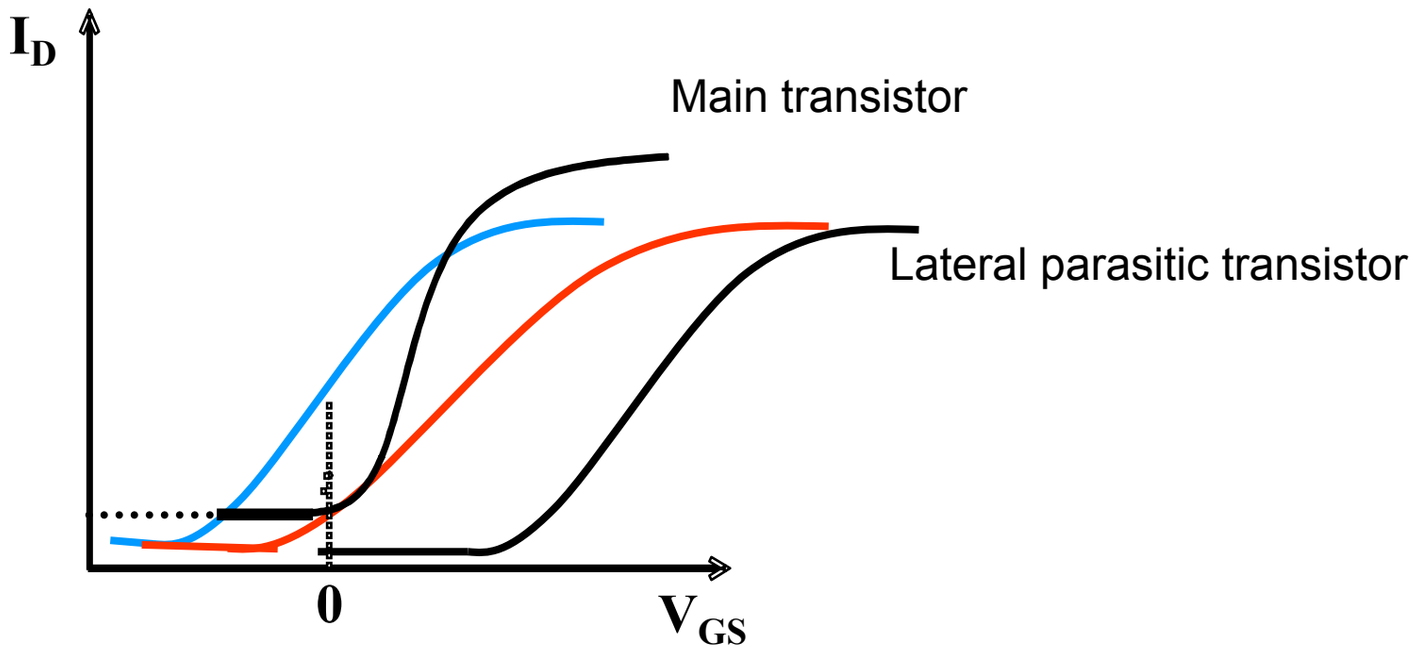






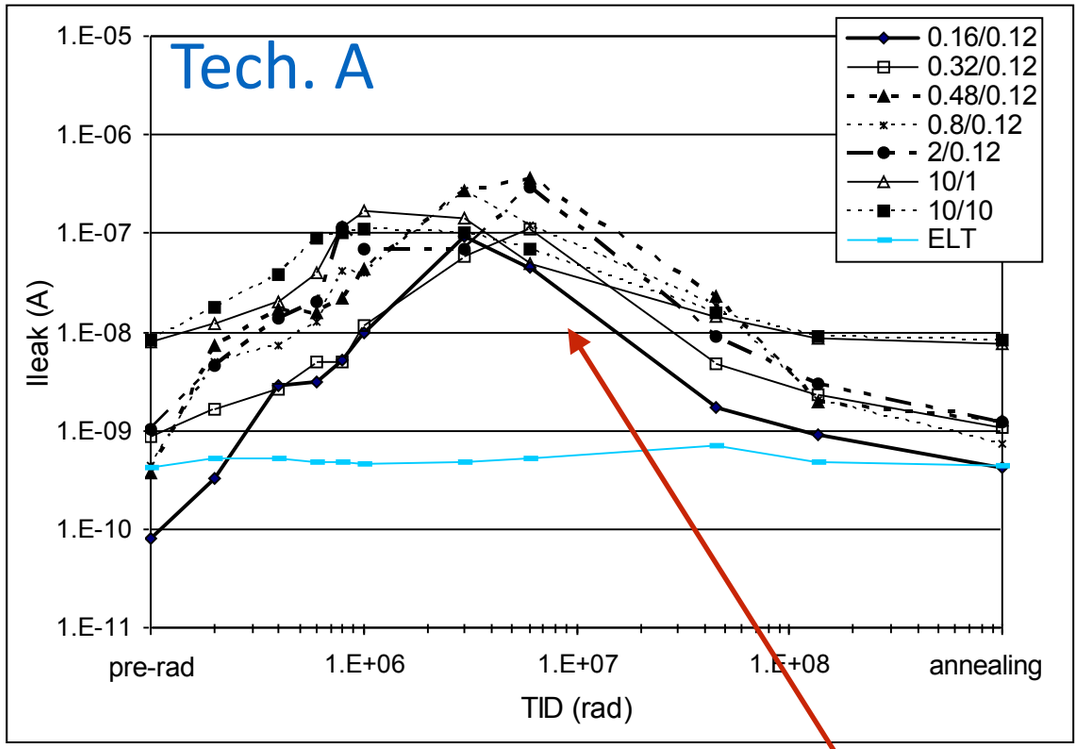
The leakage current in NMOS is due to the accumulation of defects in the lateral Shallow Trench Isolation (STI) oxide





The selection of the manufacturer (Tech. A) was based on a number of criteria: long-term availability, cost, radiation tolerance, support offering, …

A large effort was dedicated to the characterisation of the selected technology



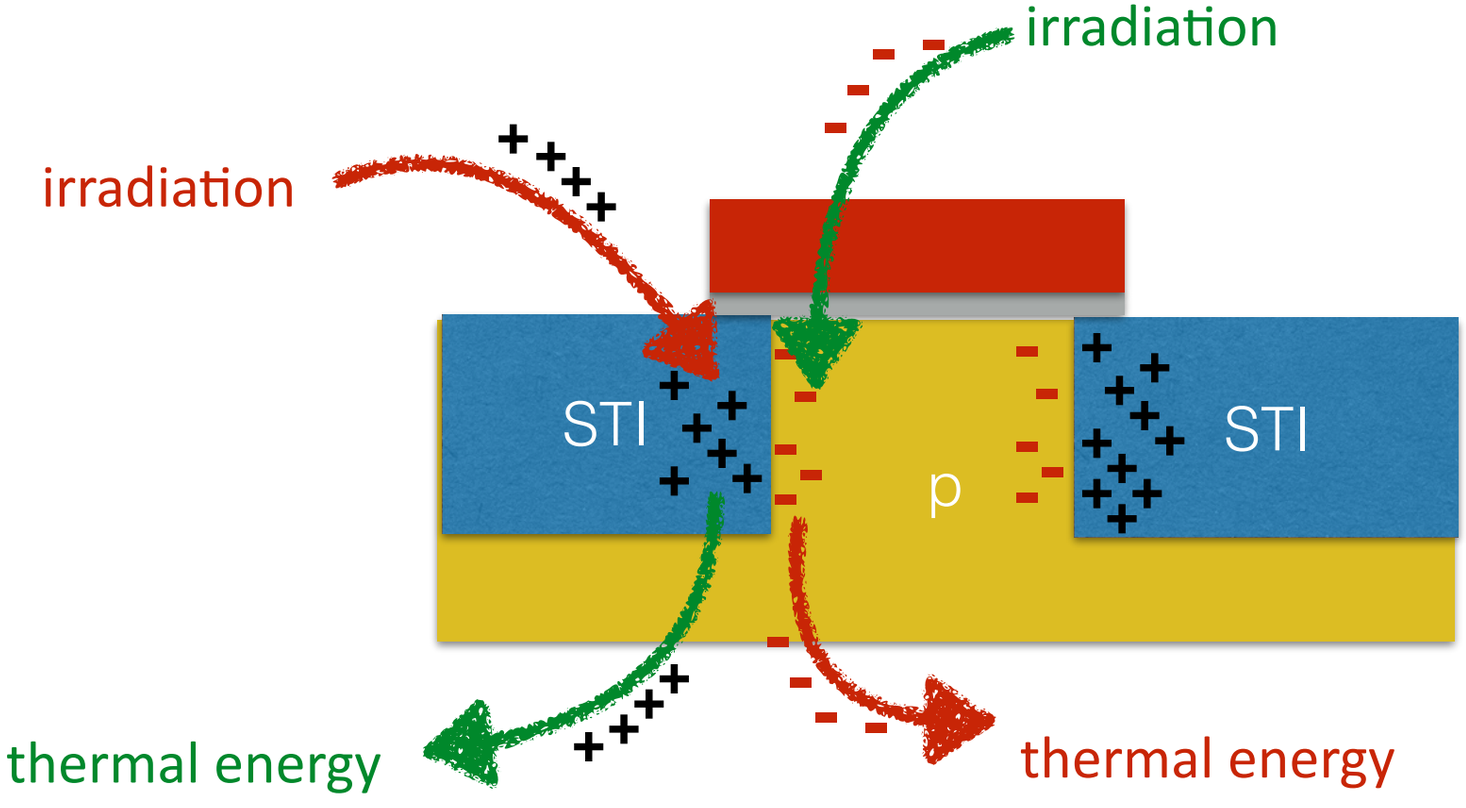
Is there still the need for ELTs and guard rings?

Is there still the need for ELTs and guard rings?

The leakage current is the sum of different mechanisms involving:

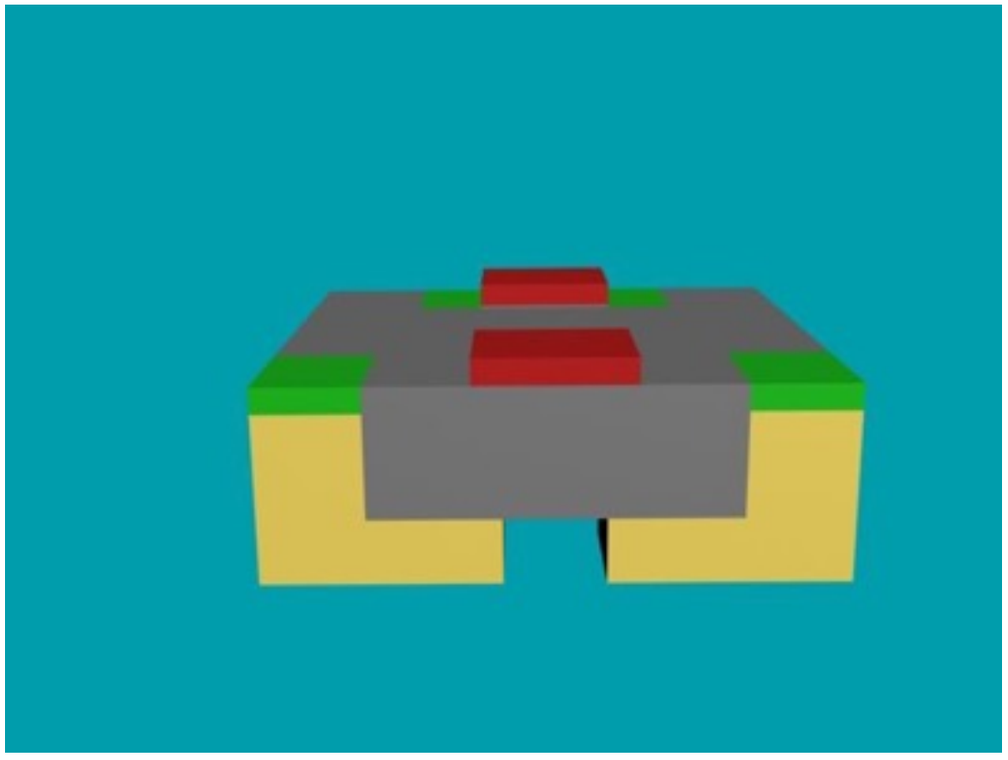
- the creation/trapping of charge (by radiation)
- its passivation/de-trapping (by thermal excitation)

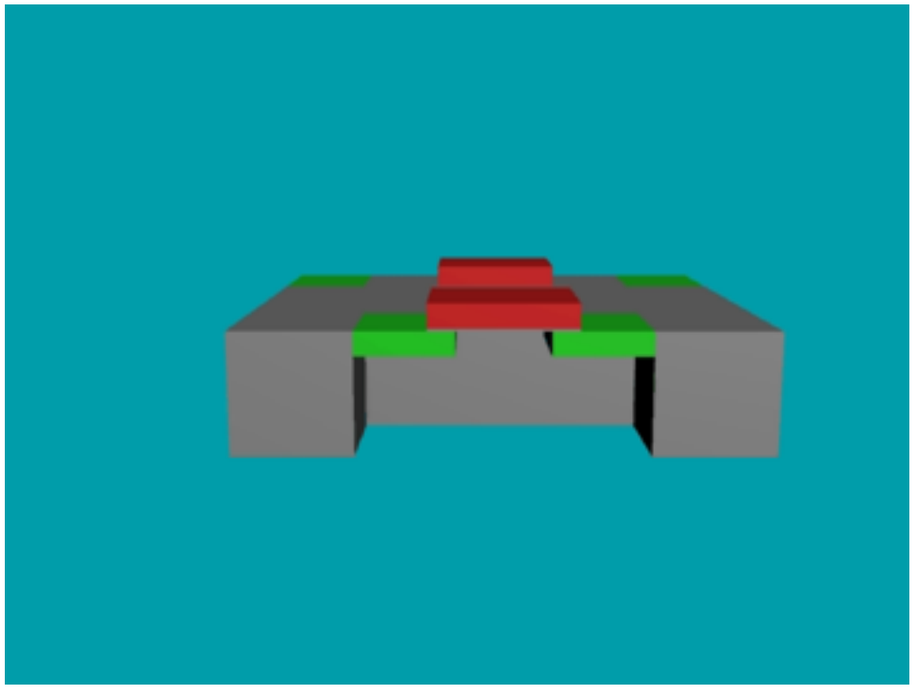
These phenomena are Dose Rate and Temperature dependent!



The properties of the defects (hole traps, interface states) have been studied in these two publications:

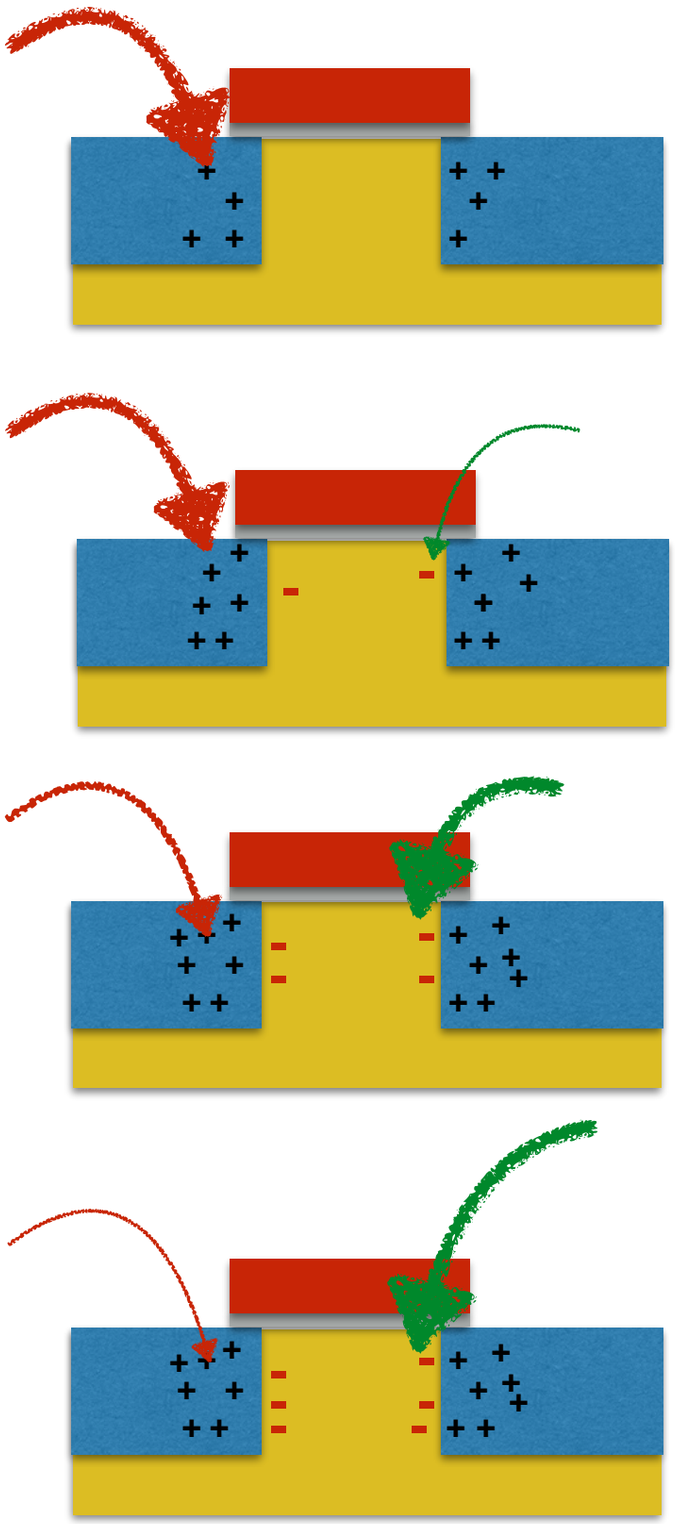
- F.Faccio, G.Cervelli, “Radiation-induced edge effects in deep submicron CMOS transistors”, IEEE Trans. Nucl. Science, Vol.52, No.6, December 2005, pp.2413-2420
- F.Faccio et al., “Total ionizing dose effects in shallow trench isolation oxides”, Microelectronics Reliability 48 (2008) 1000-1007

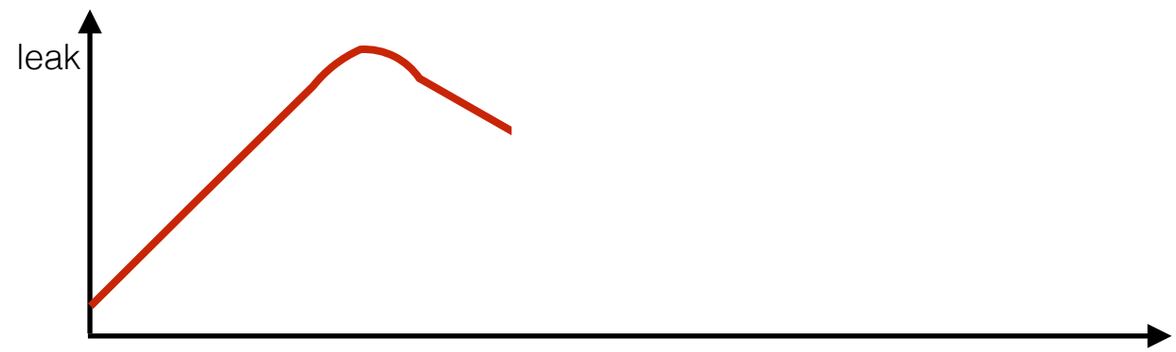




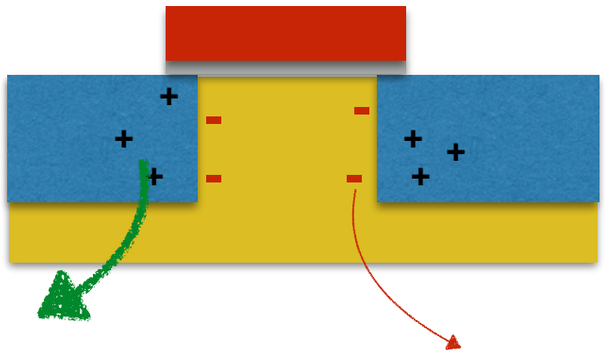
On the basis of our understanding of the mechanisms leading to the leakage current, the following scenario is plausible for discontinuous irradiation tests

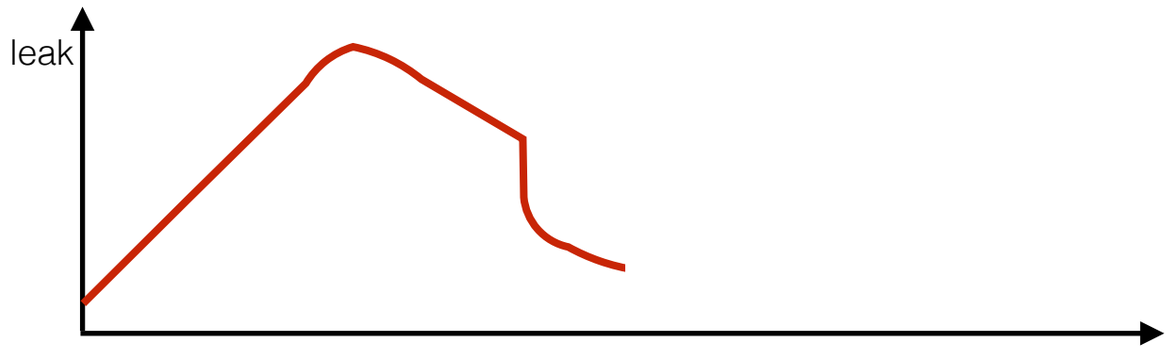
Irradiation



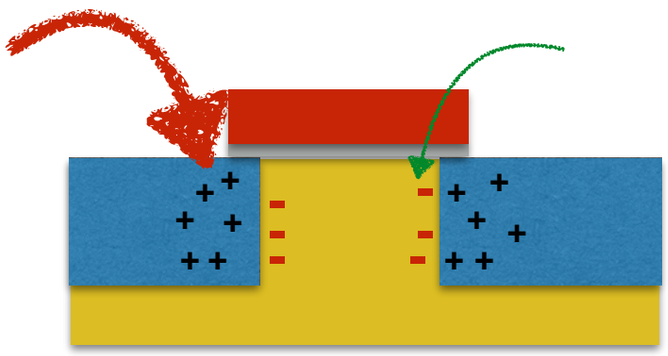


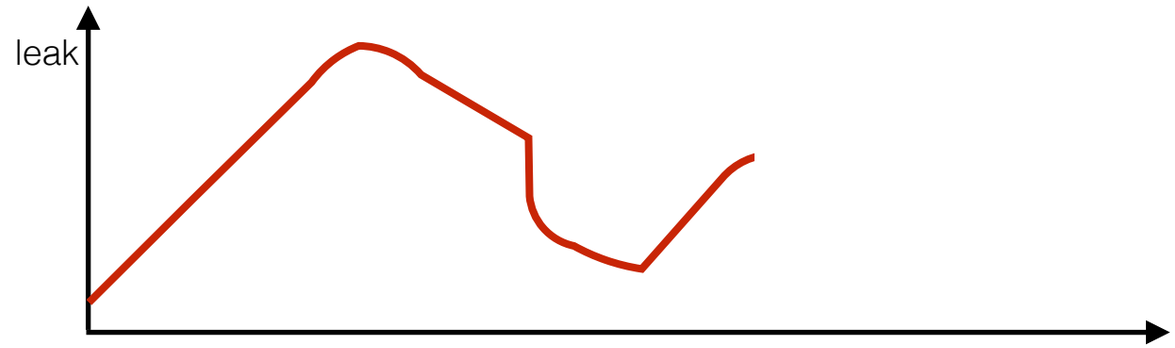
Annealing

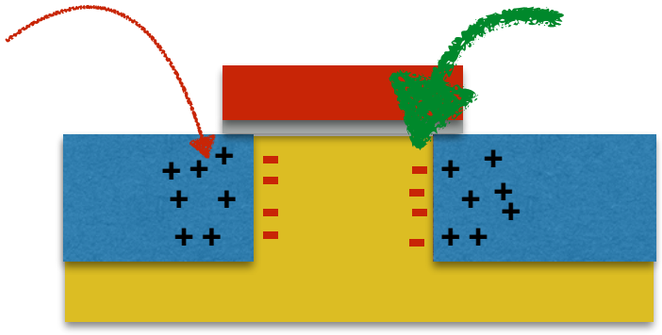


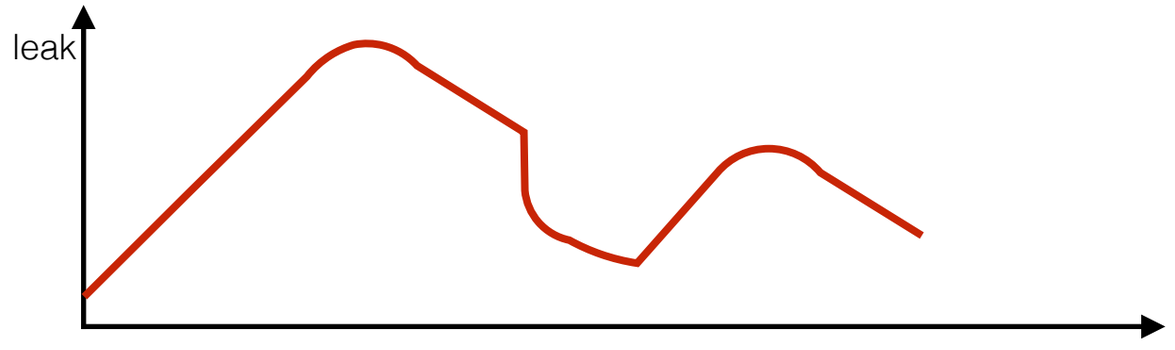


Irradiation









No digital library with ELTs and guardrings was developed. The standard cells library from a commercial supplier was considered usable

Designers have to evaluate if the leakage could threaten the circuit/system functionality in the application

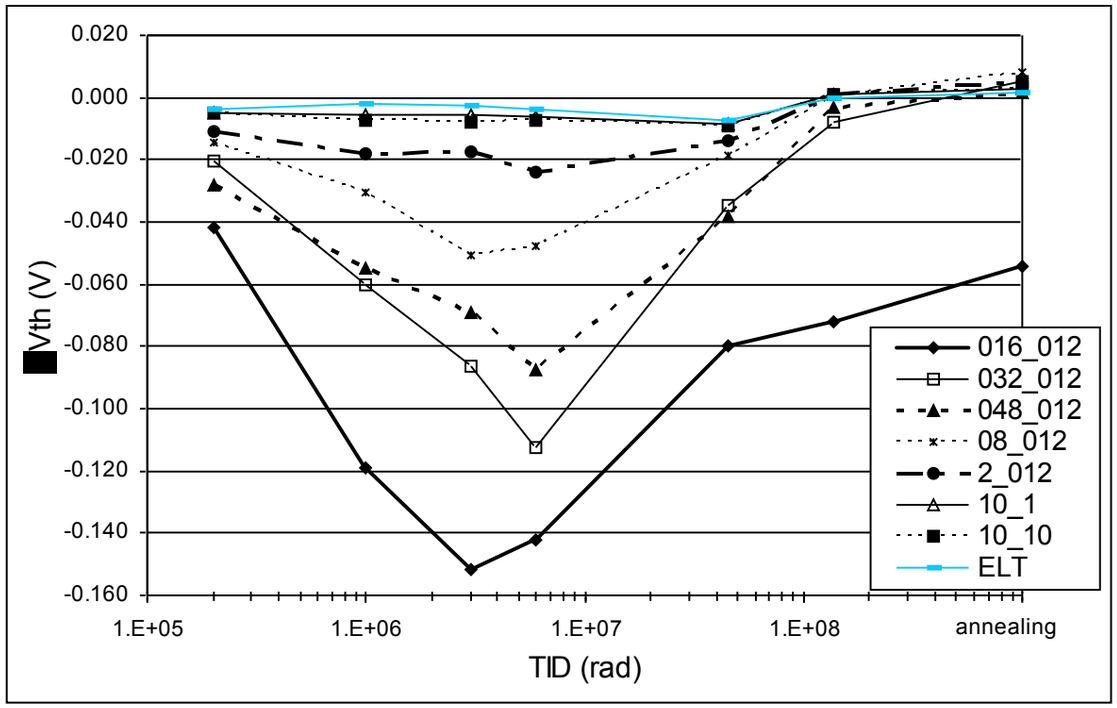
The charge trapped in the lateral STI can also influence the characteristics of the main transistor - more evidently if it is narrow.

This has been called Radiation Induced Narrow Channel Effect (RINCE)

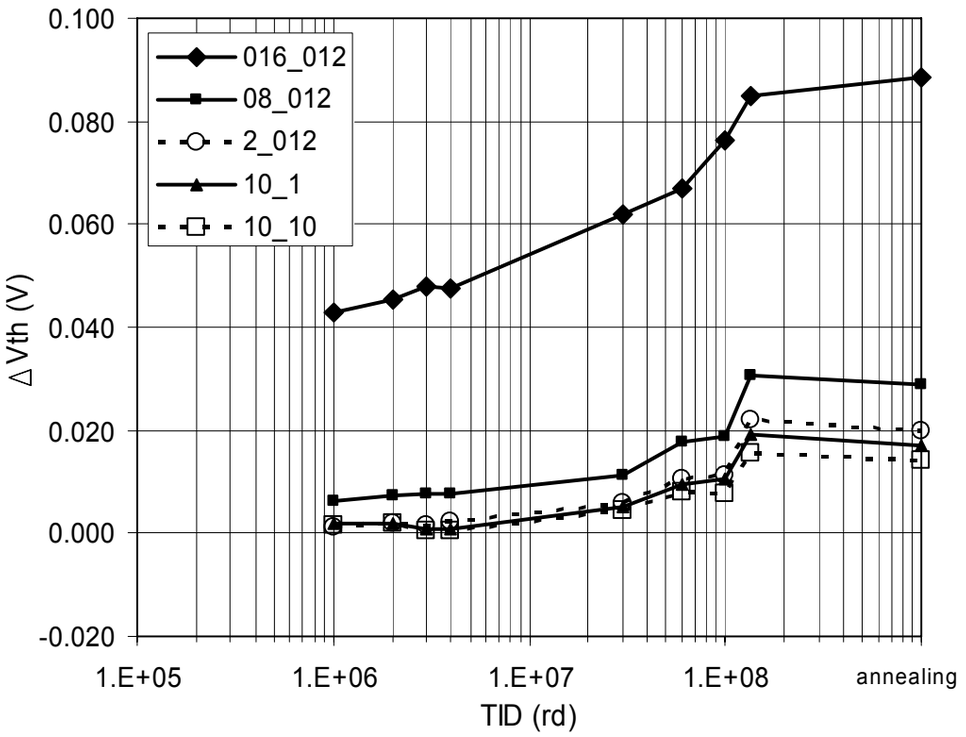
"RINCE" introduced at NSREC 2005 (F.Faccio and G.Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors", IEEE Trans Nucl Science, Vol.52, N.6, Dec2005, pp.2413-2420)

Example: apparent Vth shift in NMOS and PMOS transistors of different W, Tech. A

NMOS

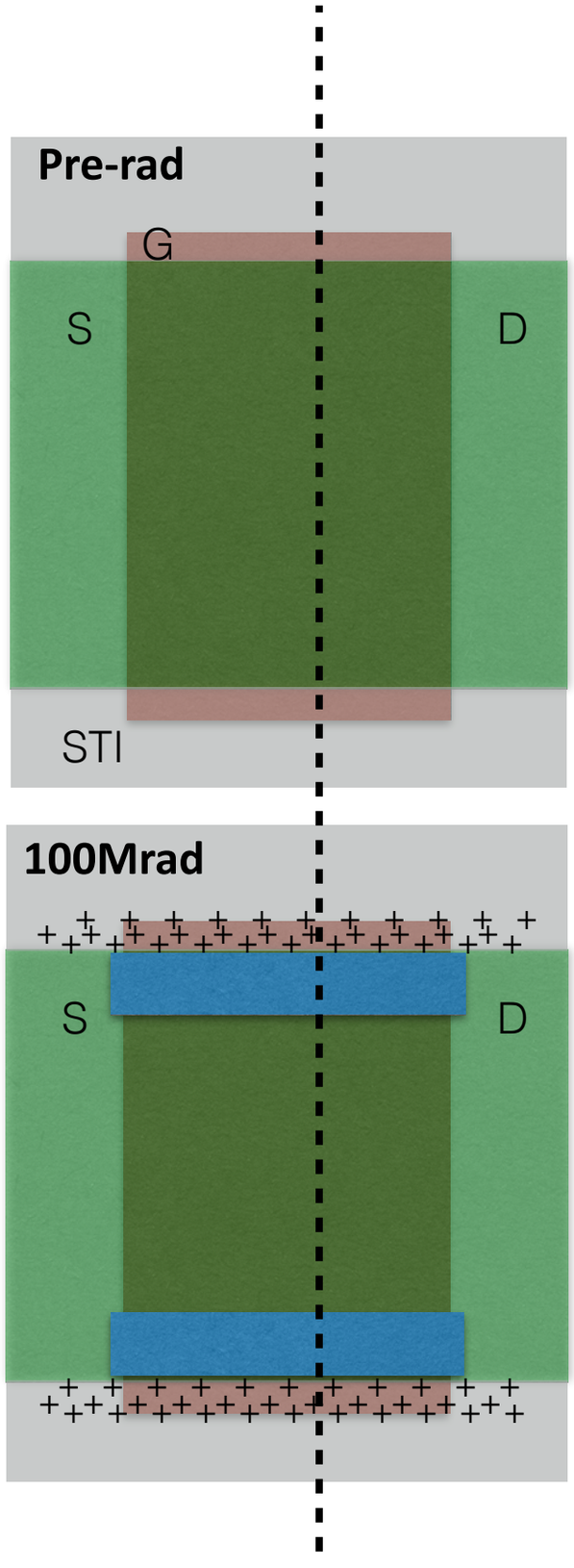


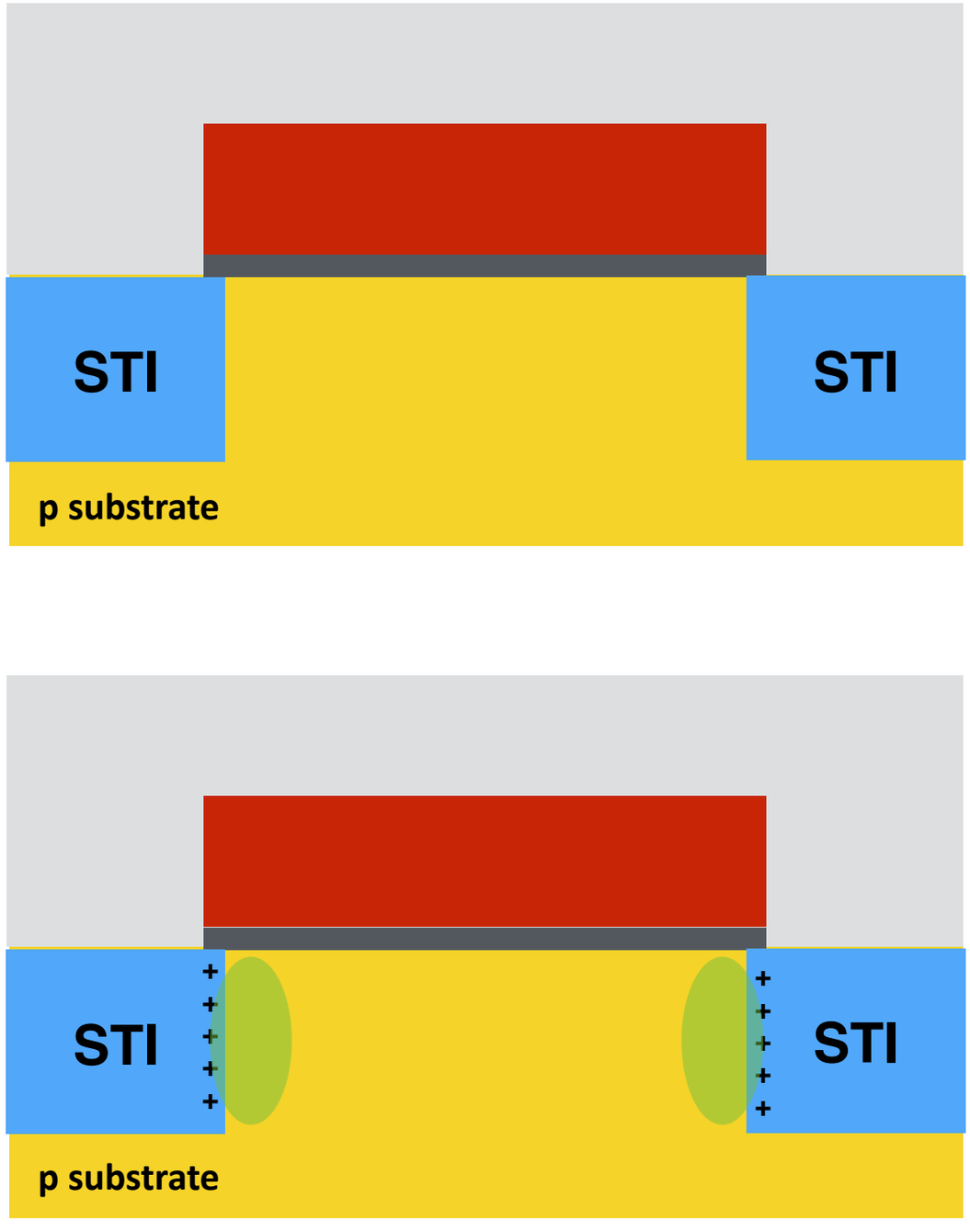
PMOS



RINCE can be conceptually represented by this cartoon

W = large size

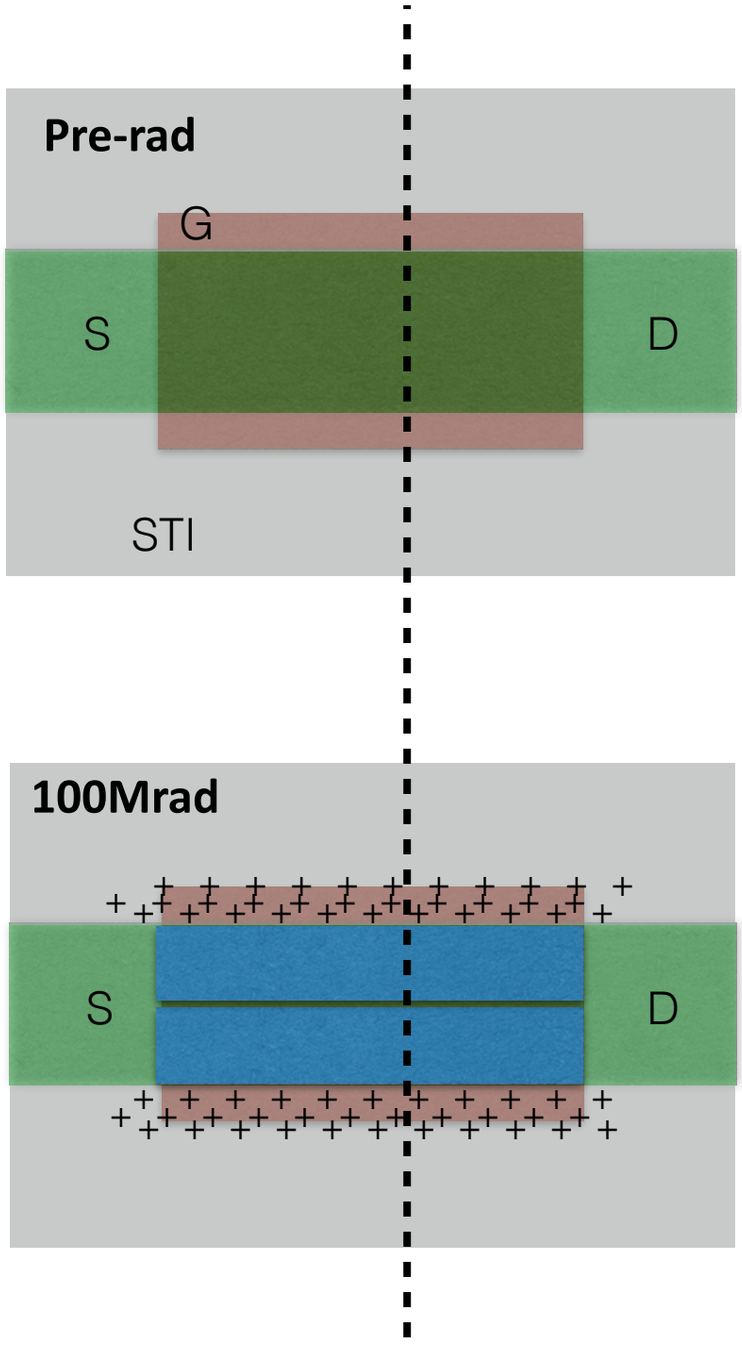


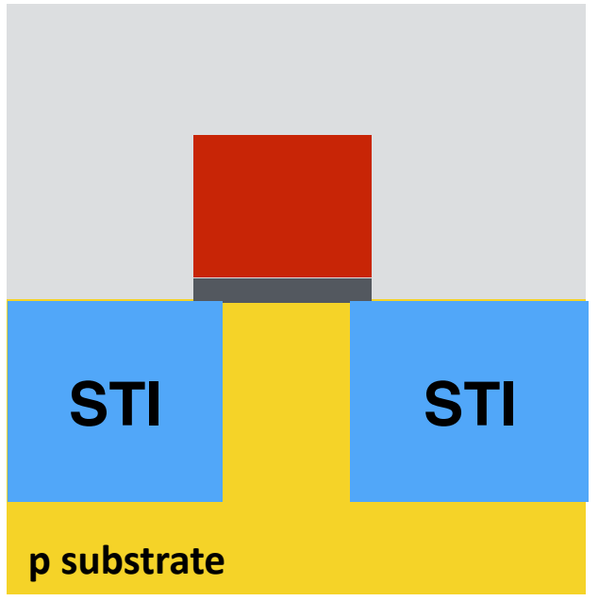


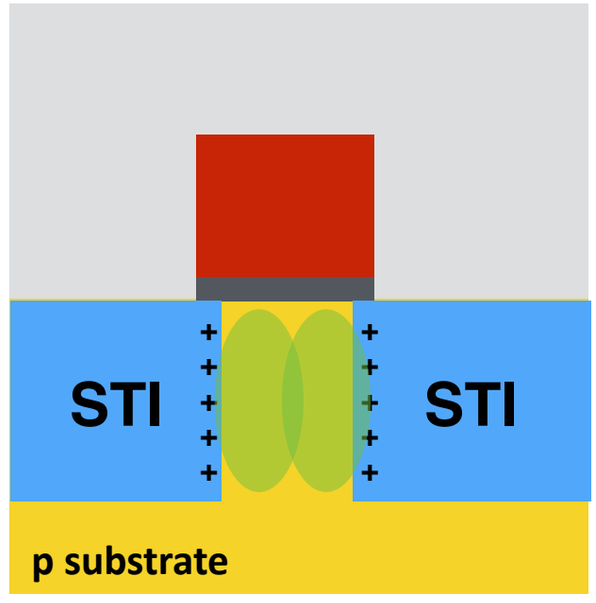
NOTE: In this cartoon, there is no distinction between the positive charge trapped in the oxide or in interface traps

RINCE can be conceptually represented by this cartoon

W = minimum size







NOTE: In this cartoon, there is no distinction between the positive charge trapped in the oxide or in interface traps

A report containing all irradiation results and guidelines for designers has been written in 2006 and distributed since

The report and links to the papers are available at the ASIC Support service Web site:
http://support-ictech-mpws.web.cern.ch/support-ICtech-MPWs/
The documents can be found under the page:
https://support-ictech-mpws.web.cern.ch/support-ICtech-MPWs/IBM-CMOS8RF/RadTol.htm

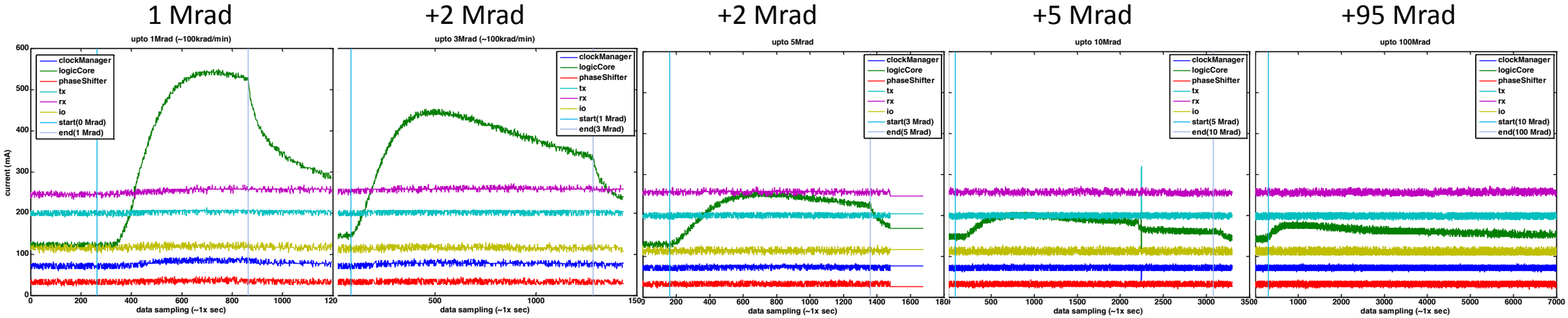
Excerpt from the report

In reading and applying the recommendations, one should remember that, while small analog circuits have been integrated by the HEP community in this technology and have given radiation results in line with the expectations, no real demonstrator of a medium-large digital circuit has been implemented and tested for radiation so far. It is also important to point out that, although the radiation response of the technology has been measured as unchanged over time (see section 2), exploiting its natural radiation tolerance presents some risks and requires constant monitoring over the full prototype and production cycle.

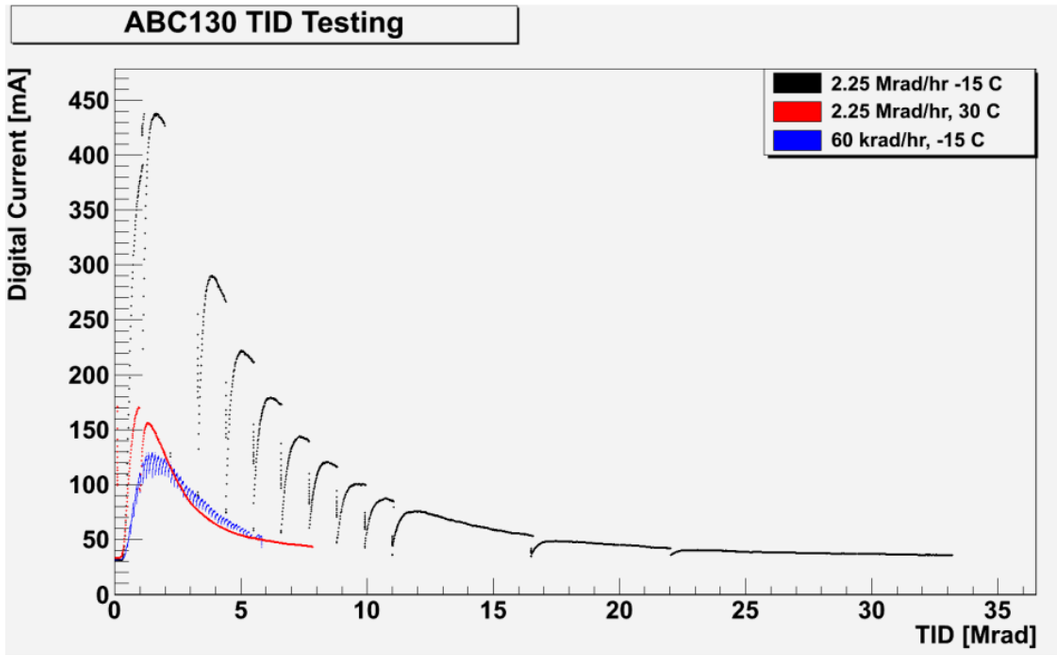
Also, measurements at low T could not be made at the time…

The leakage increase is visible in complex logic ASICs developed in this technology

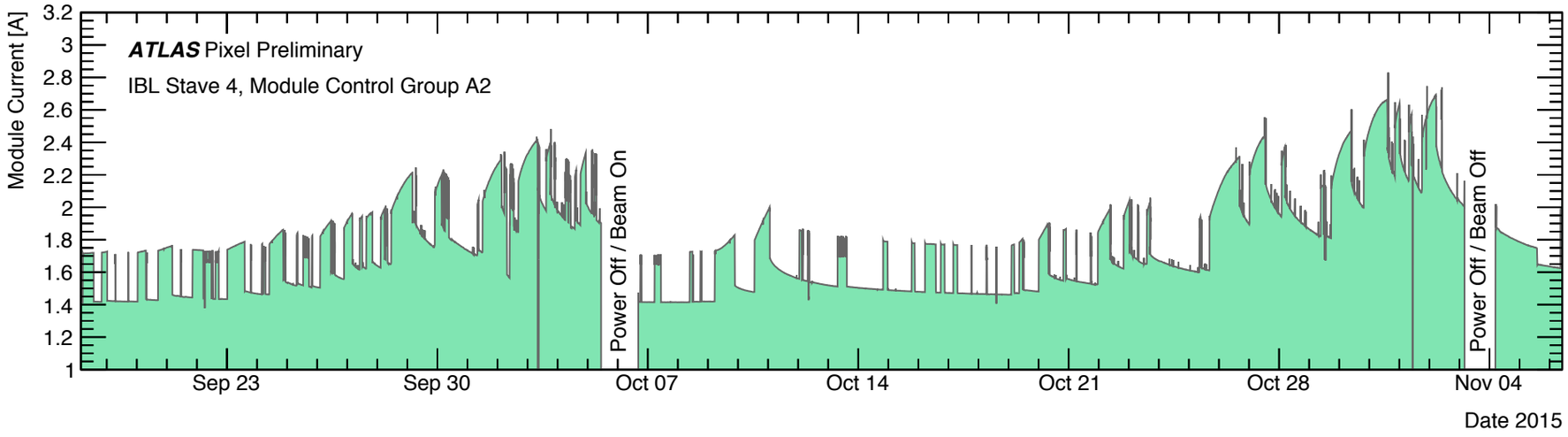
Logic core current consumption in the GBTx at room T: green curve (courtesy P.Moreira and GBT Team)



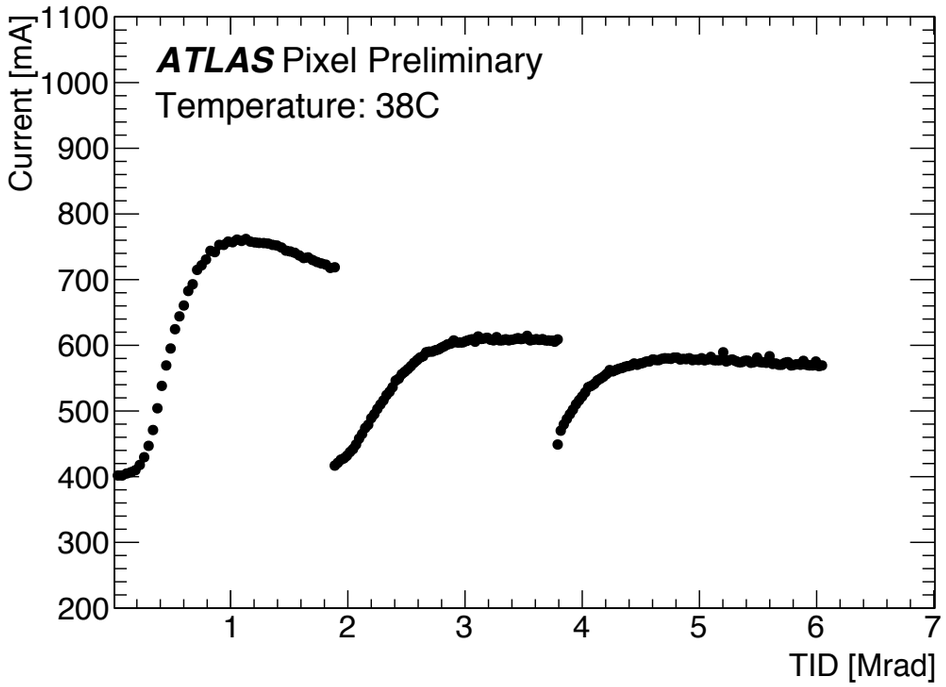
Logic core current consumption of the ABC130 at different T and dose rates (courtesy F.Anghinolfi and ABC130 Team)

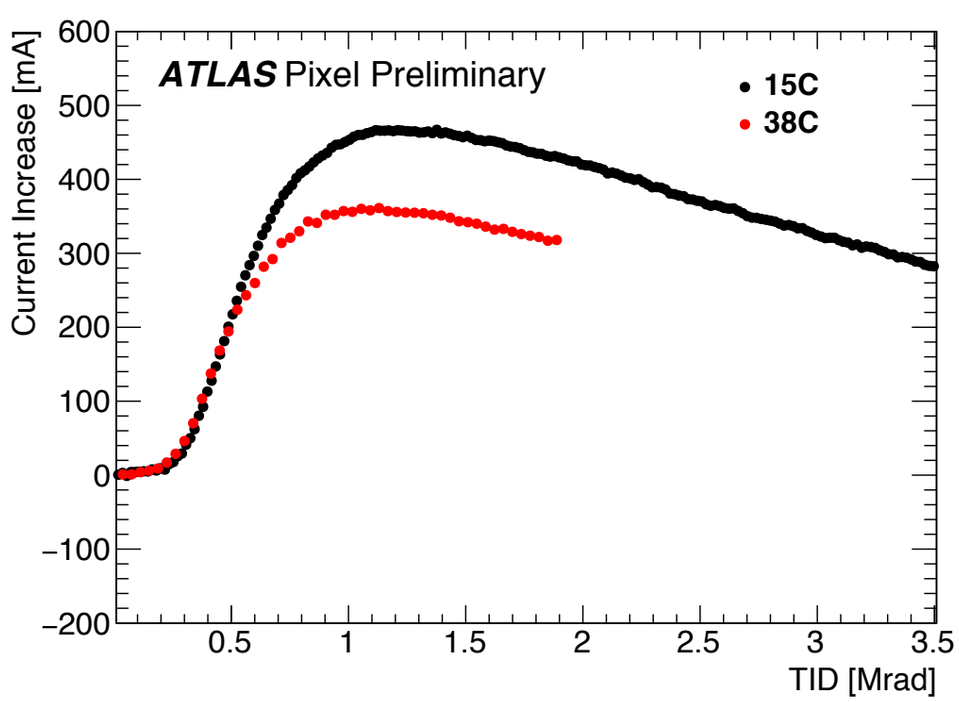


… and current consumption in the ATLAS IBL in the experiment during data acquisition



… due to radiation-induced leakage current in the FEI4 ASIC





References to publications for radiation studies in this 130nm technology

Leakage current properties

F.Faccio and G.Cervelli, “Radiation induced edge effects in deep submicron CMOS transistors”, IEEE Trans Nucl Science, Vol.52, N.6, Dec2005, pp.2413-2420

F.Faccio et al., “Total Ionizing dose effects in shallow trench isolation oxides”, Microelectronics Rliability 48 (2008) 1000-1007

Noise properties

- M.Manghisoni et al., “Noise Characterization of 130 nm and 90 nm CMOS Technologies for Analog Front-end Electronics”, IEEE TNS Vol.55, n4, August 2006, p.2456
- V.Re et al., “Total Ionizing Dose Effects on the Noise Performances of a 0.13 μm CMOS Technology”, IEEE TNS Vol.55, n3, June 2006, p.1599
- V.Re et al., “Review of radiation effects leading to noise performance degradation in 100 - nm scale microelectronic technologies”, in 2008 IEEE NSS conference record, p.3086

Reliability

M.Silvestri et al., “Channel Hot carrier Stress on Irradiated 130-nm MOSFETs”, IEEE TNS 55, n4, Aug. 2008, p.1960

M.Silvestri et al., “Degradation induced by X-ray irradiation and Channel Hot Carrier stresses in 130-nm NMOSFETs with enclosed layout”, IEEE TNS 55, n6, Dec.2008, p.3216

M.Silvestri et al., “The role of irradiation bias on the Time-Dependent Dielectric Breakdown of 130-nm MOSFETs exposed to X-rays”, IEEE TNS 56, n6, Dec. 2009, p.3244

M.Silvestri et al., “Single Event Gate Rupture in 130-nm CMOS Transistor Arrays Subjected to X-ray Irradiation”, Presented at RADECs 2009, accepted for publication in IEEE TNS

The TID characterisation of transistors from the selected ‘backup’ 130nm technology has been made in 2014-15. The backup has meanwhile become the mainstream for all new developments.

The study was targeted at a TID of up to 400Mrad.

All the following figures have been provided by S.Michelis (CERN/EP/ESE)

Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes

Entering HERE

Production for LHC: 0.25um CMOS

(some) tracker upgrades: 65nm CMOS

Upgrades: 130nm CMOS

ca. 1998-2000

ca. 2006

ca. 2011

time

TID up to 10Mrad

TID: 100Mrad

TID: 100Mrad to 1Grad

TID: 400Mrad

TID

Main transistor

V_{th}, g_m, …

Leakage in parasitics

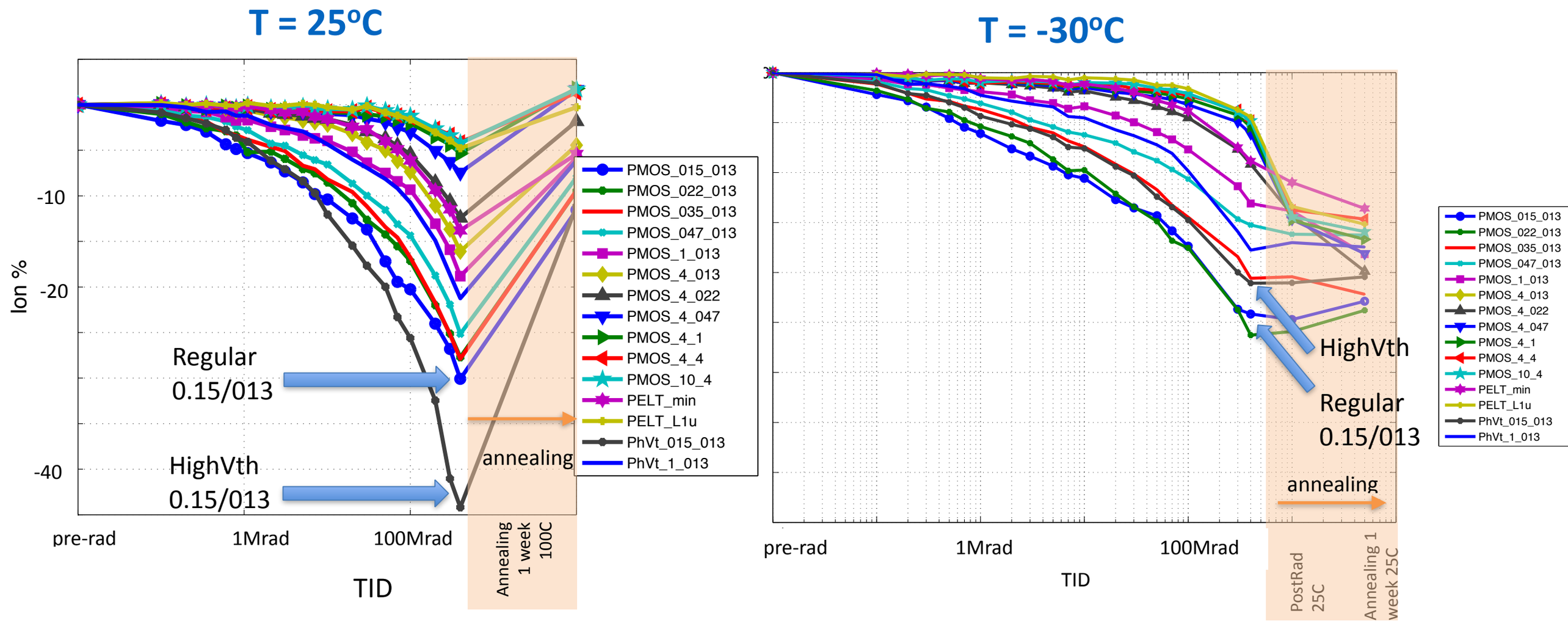
Leakage in parasitics

Leakage in parasitics

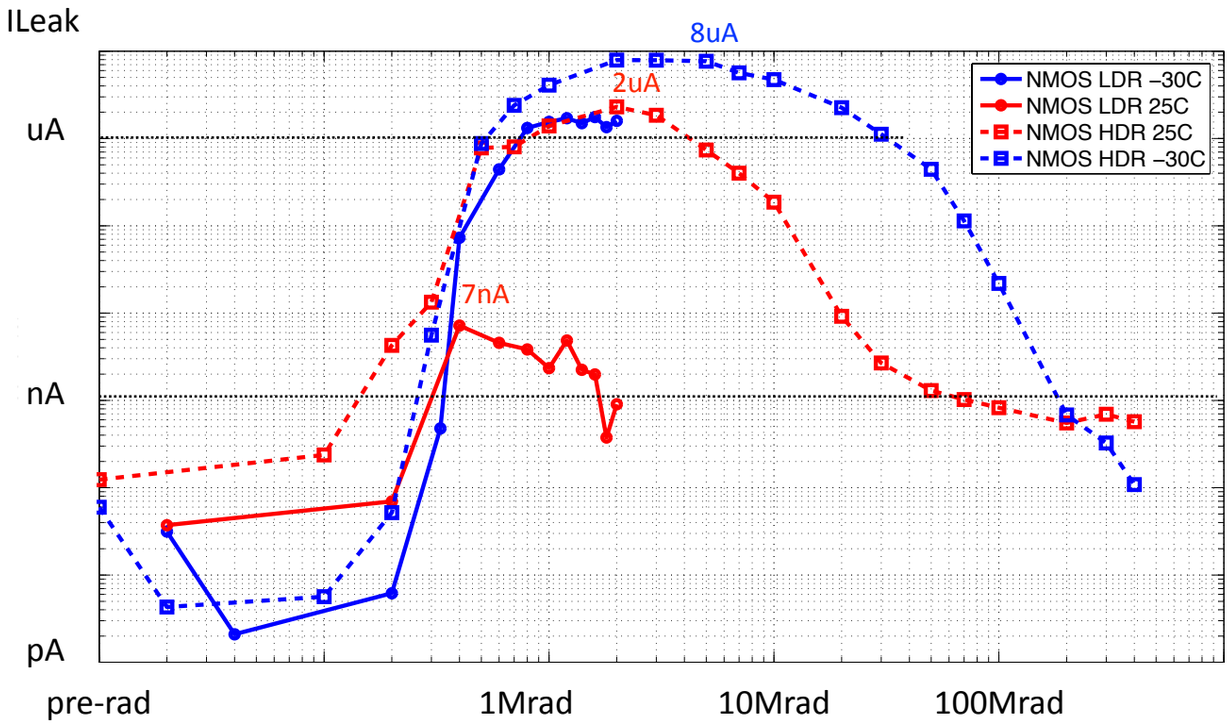
RINCE

The electrical performance of the NMOS transistors in practically unaffected, while PMOS loose drive current (I_{on}) by an amount dependent on their size: the smaller the transistor, the larger the degradation. The degradation is reduced during irradiation at lower temperature.

The study was targeted at a TID of up to 400Mrad



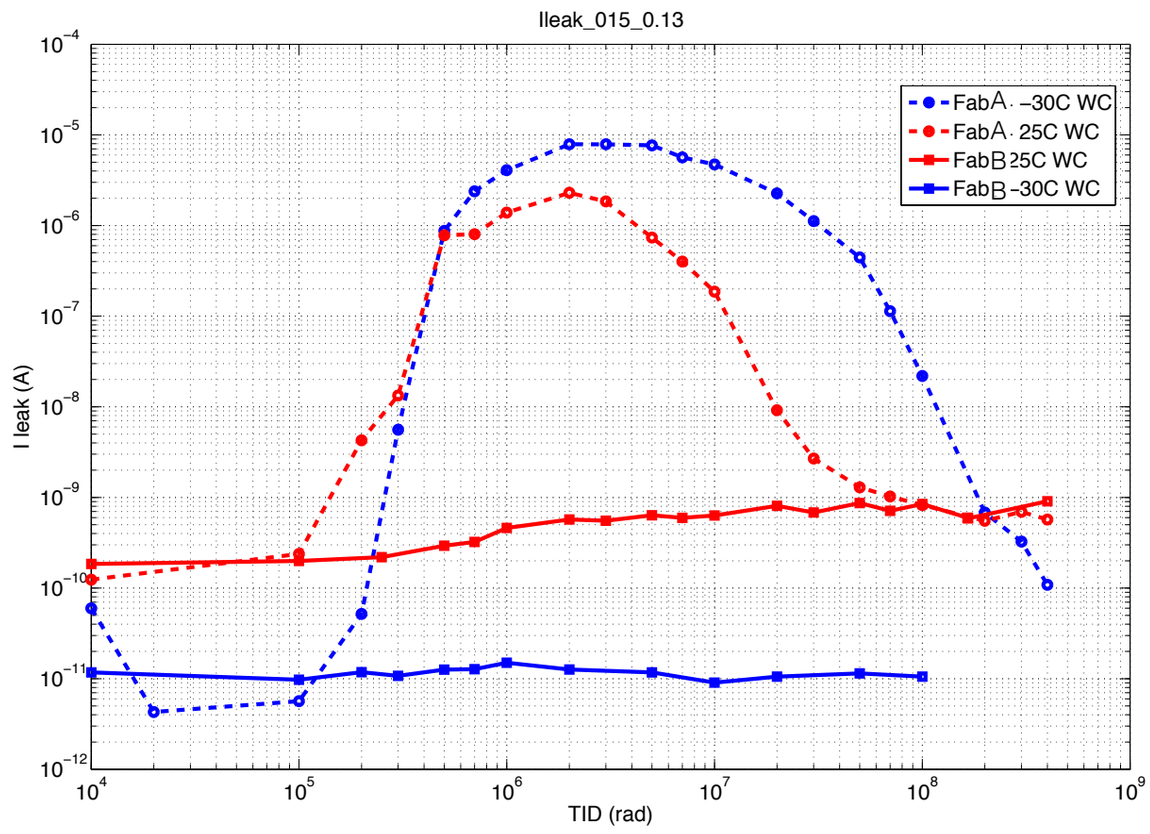
As already observed for Tech.A, the evolution of the NMOS leakage current is a function of the temperature and dose rate: it is the same physics!



HDR = 9Mrad/hour
LDR = 90krad/hour

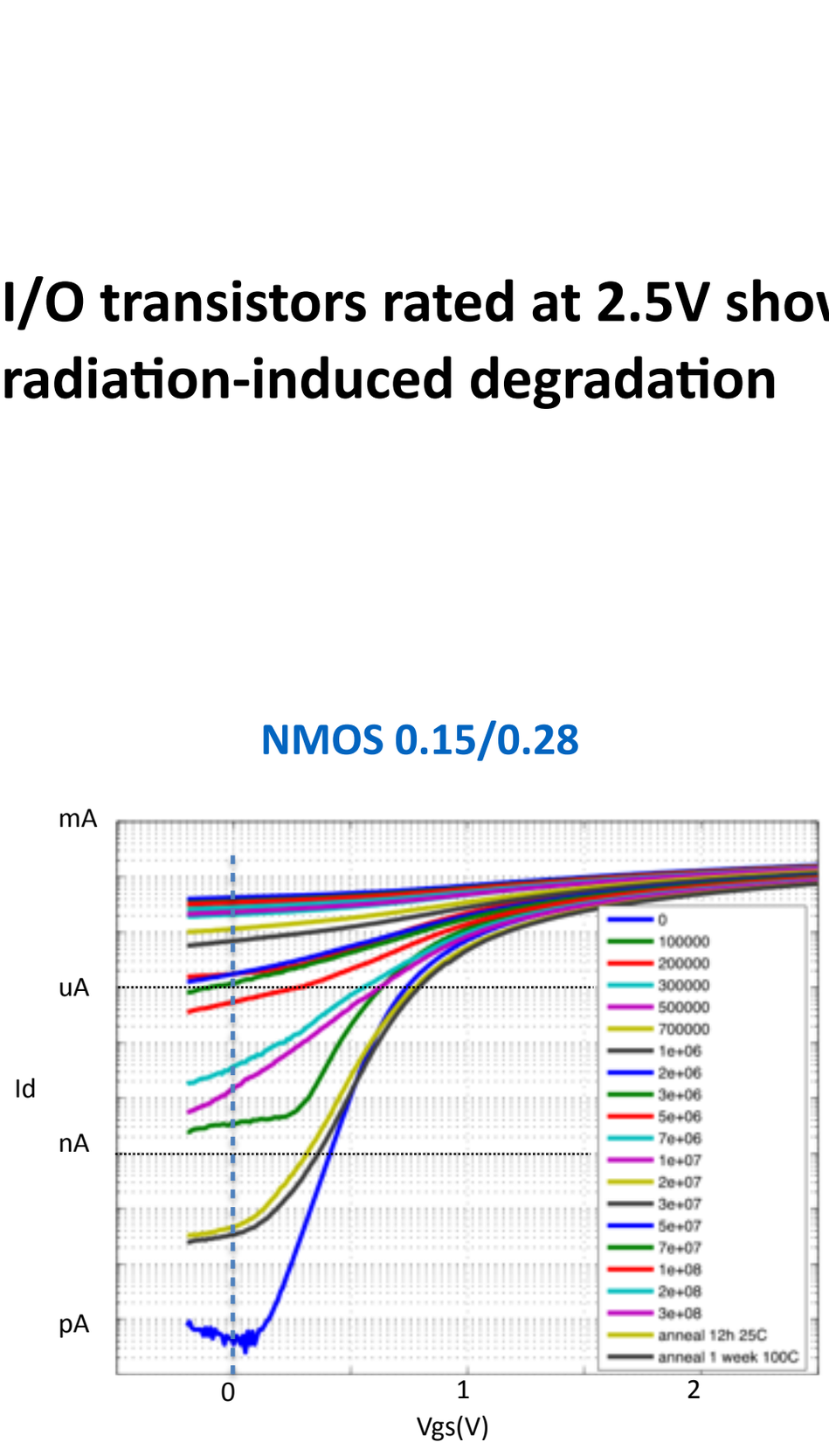
The source-drain leakage current in NMOS is very different in samples produced in 2 different Fabs

Regular 0.15/0.12 Vth transistors from Fab14 and Fab6

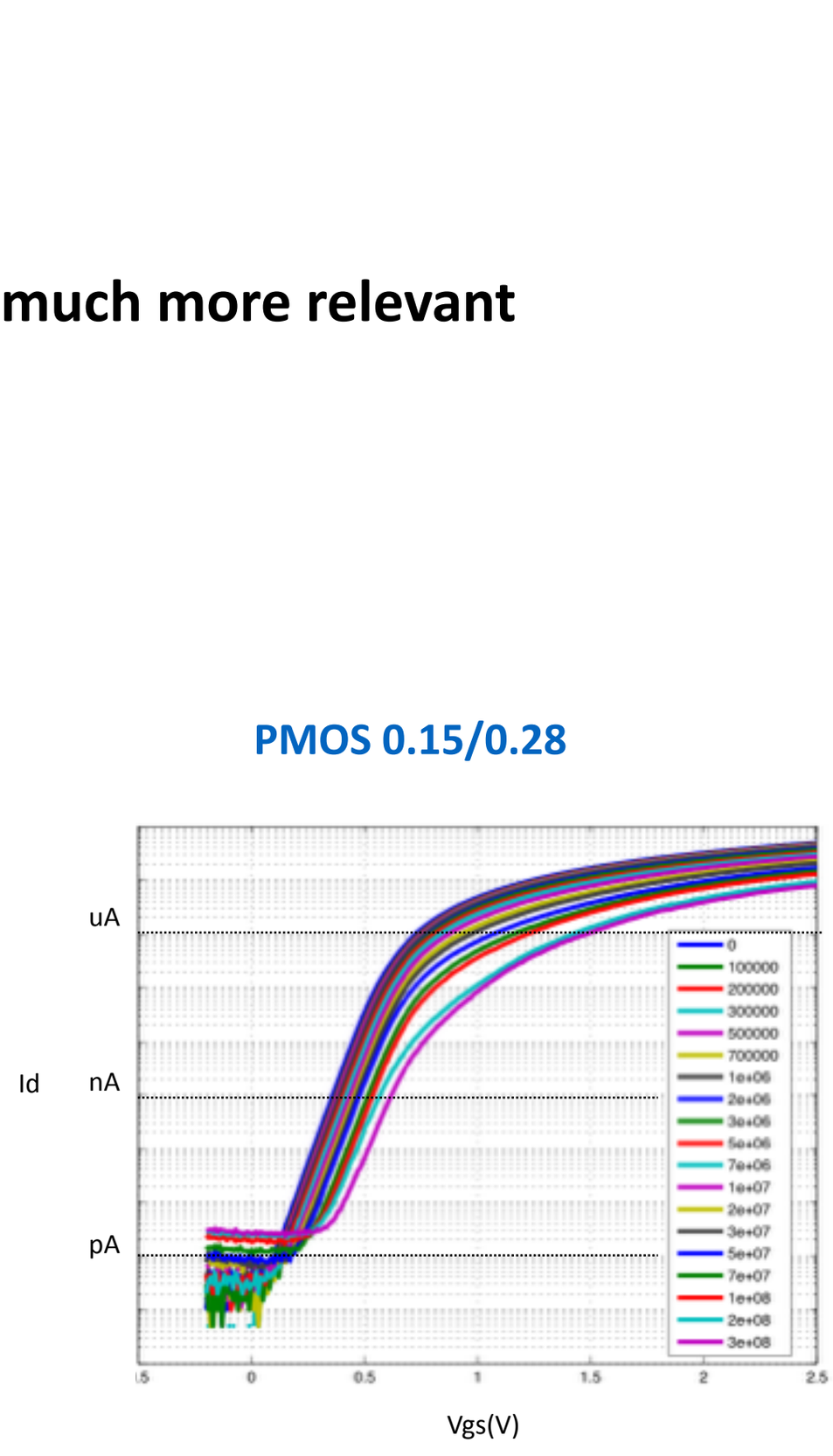


I/O transistors rated at 2.5V show a much more relevant radiation-induced degradation

NMOS 0.15/0.28



PMOS 0.15/0.28



The radiation tolerance of the ‘backup’ 130nm technology (now streamline) is at least as good as for Tech. A - for “core” transistors

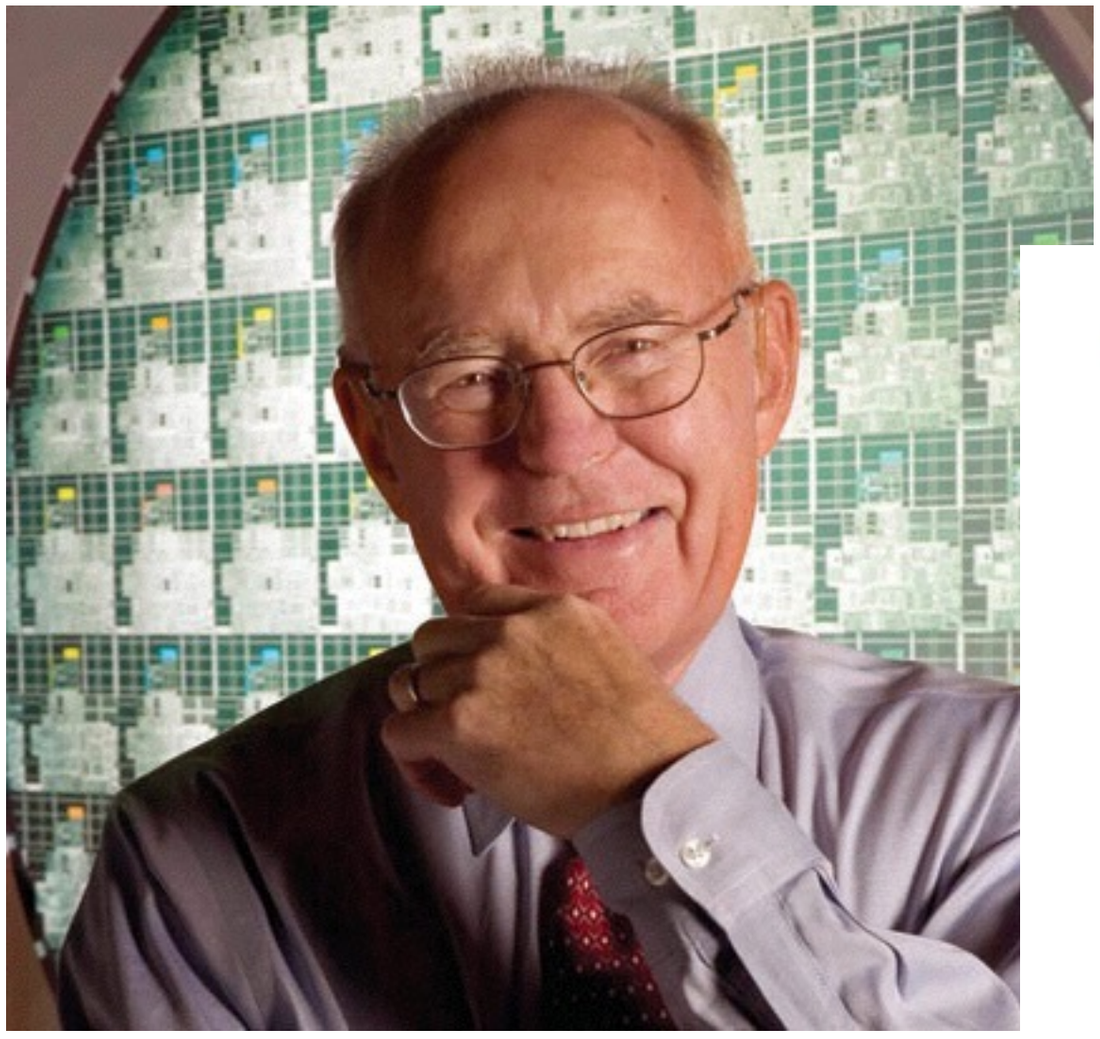
Samples from one of the Fabs do not show any significant leakage current

The difference in the leakage current between the two Fabs highlights the sensitivity of the radiation tolerance to processing

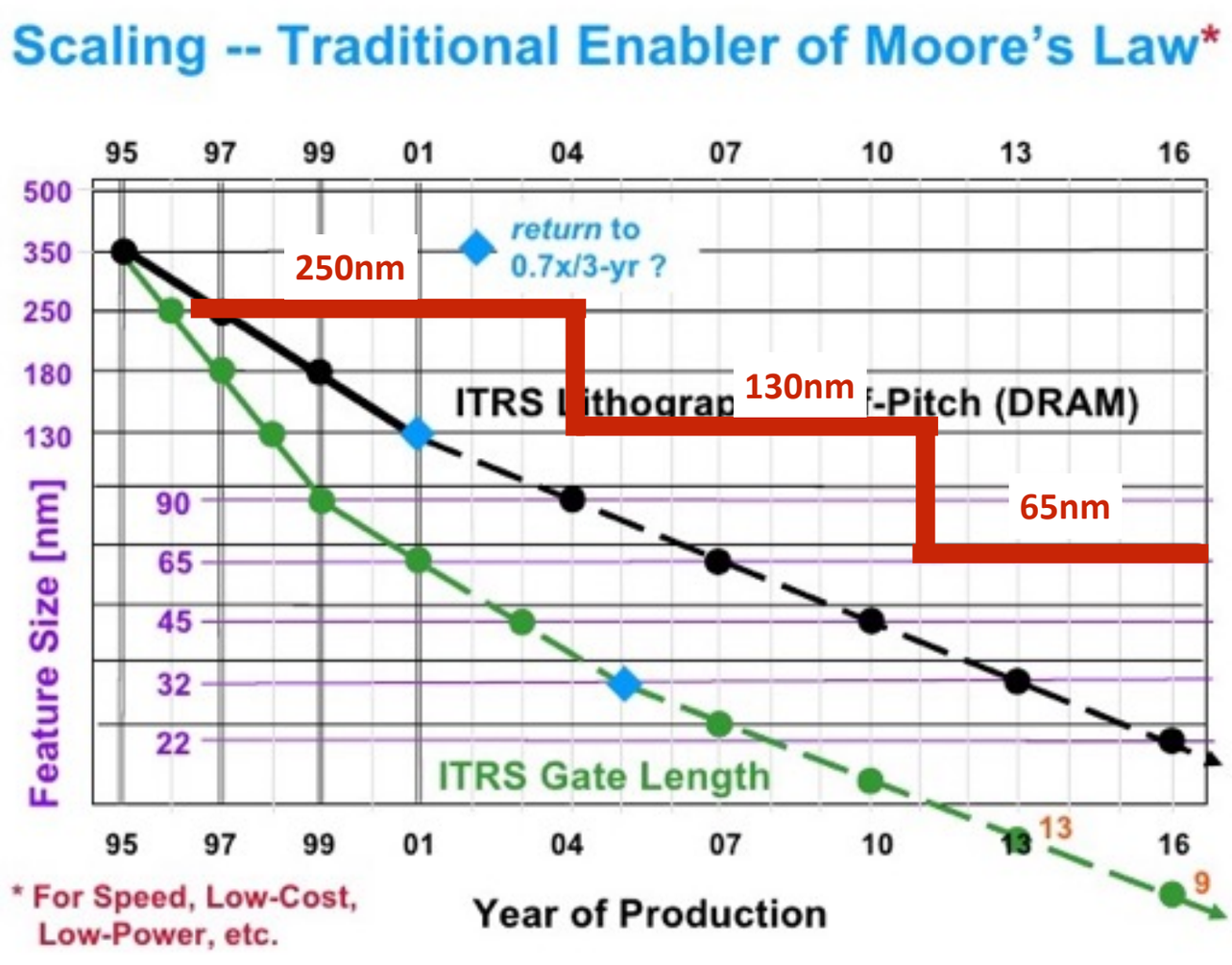
Only one Fab has to be qualified and used for all runs (prototyping, production)
The natural radiation tolerance of the process should be regularly monitored
Qualification of every lot has to be performed

A report summarising all the available radiation results and containing guidelines will be soon published

Scaling…



Year of first Radiation Tests in a technology for HEP on top of ITRS roadmap



65nm needs mainly for pixel FE ASICs and very high speed data communication (GBT-like)

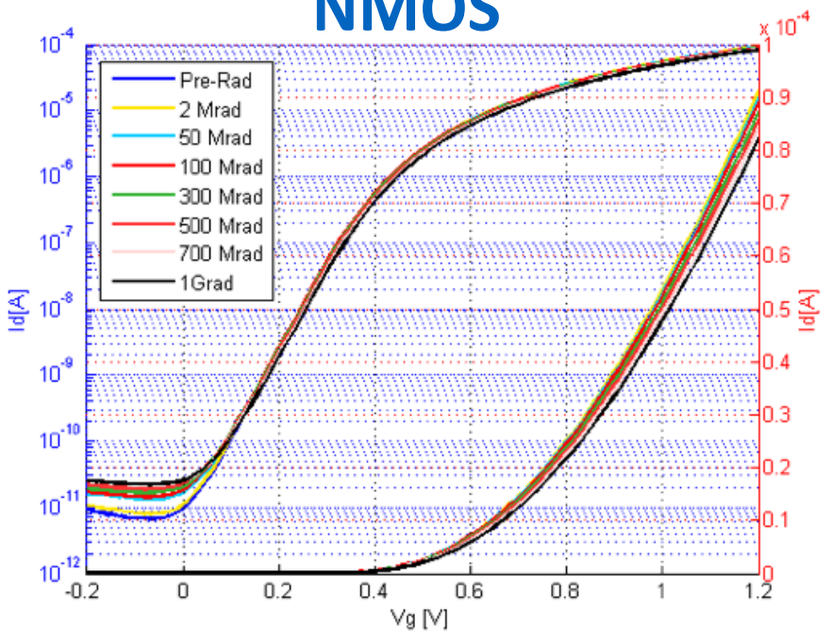
The TID characterisation of transistors from the selected 65nm technology started around 2011

The study was targeted initially at a TID of up to 200Mrad, but was extended to 1Grad by the pixel community (RD53)

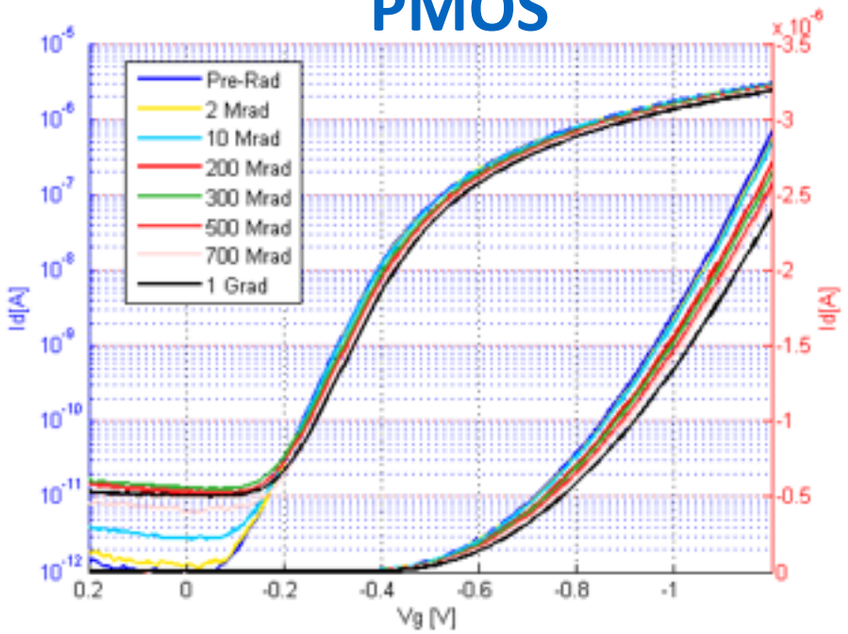
There will be no further comment about leakage currents, because we did not measure significant currents (for typical applications) in either NMOS transistors or FOXFETs

The degradation of long and large transistors is limited:
the thin gate oxide is radiation hard!

NMOS



PMOS

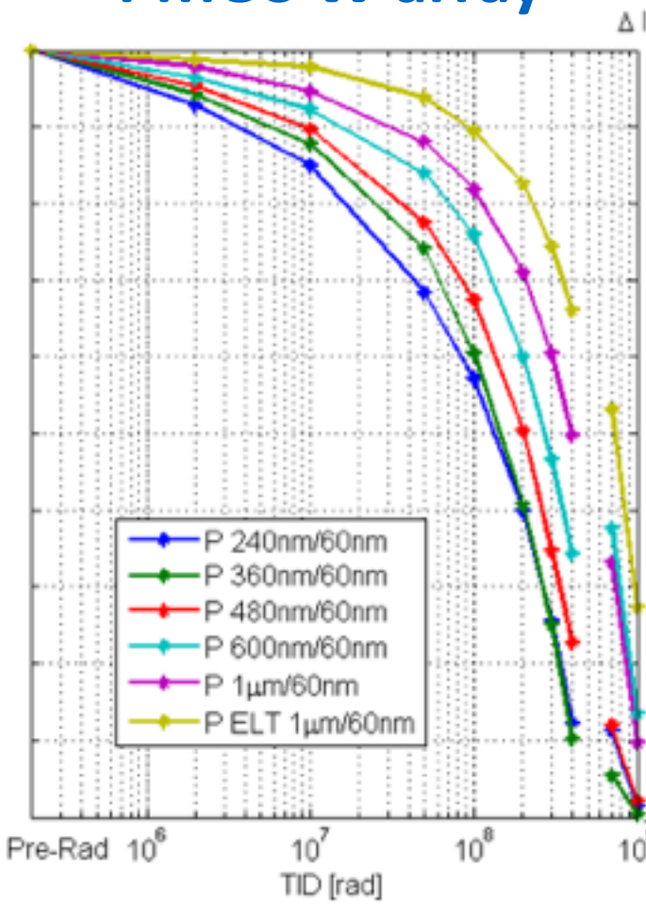


Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V
Curves Id-Vg in saturation

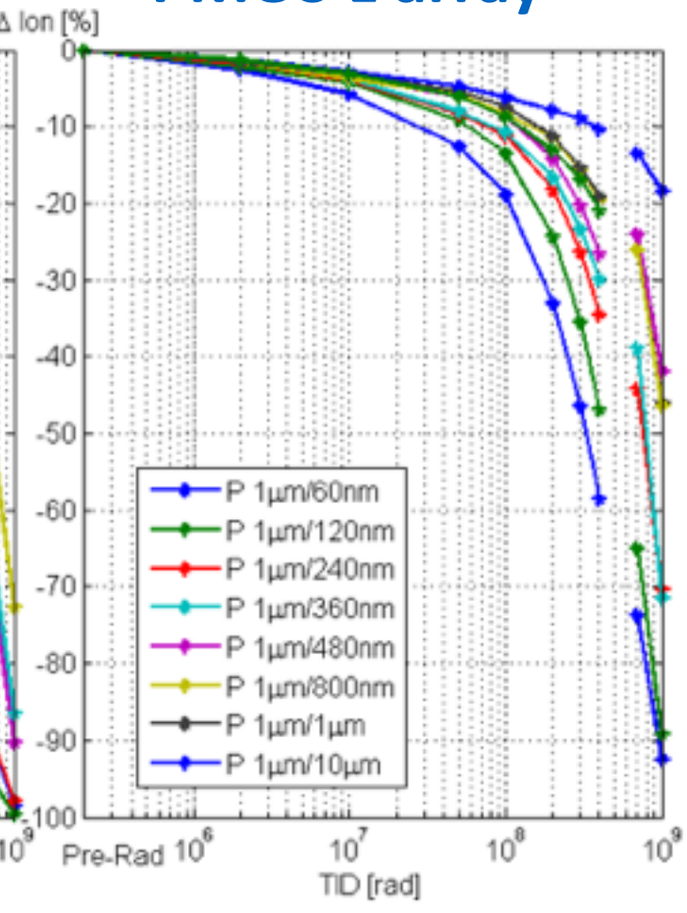
Radiation damage is severe in short and narrow channel transistors, where it depends on the bias and temperature applied both during and after irradiation

Radiation-Induced Narrow Channel Effect (RINCE)
Radiation-Induced Short Channel Effect (RISCE)

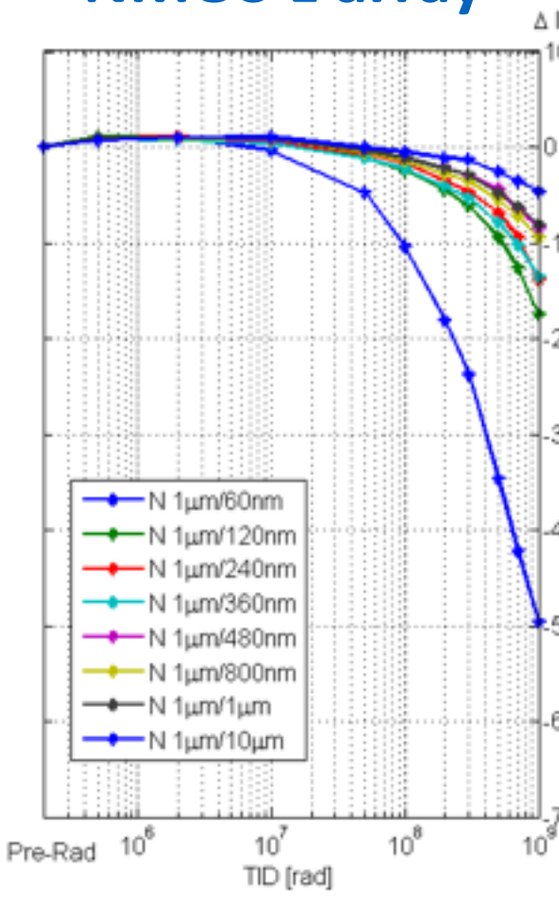
PMOS W array



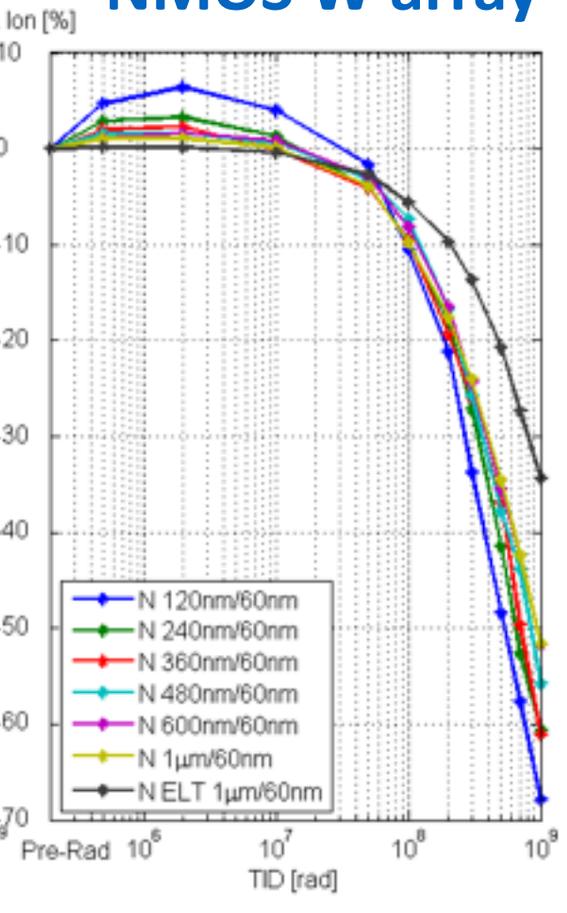
PMOS L array



NMOS L array



NMOS W array

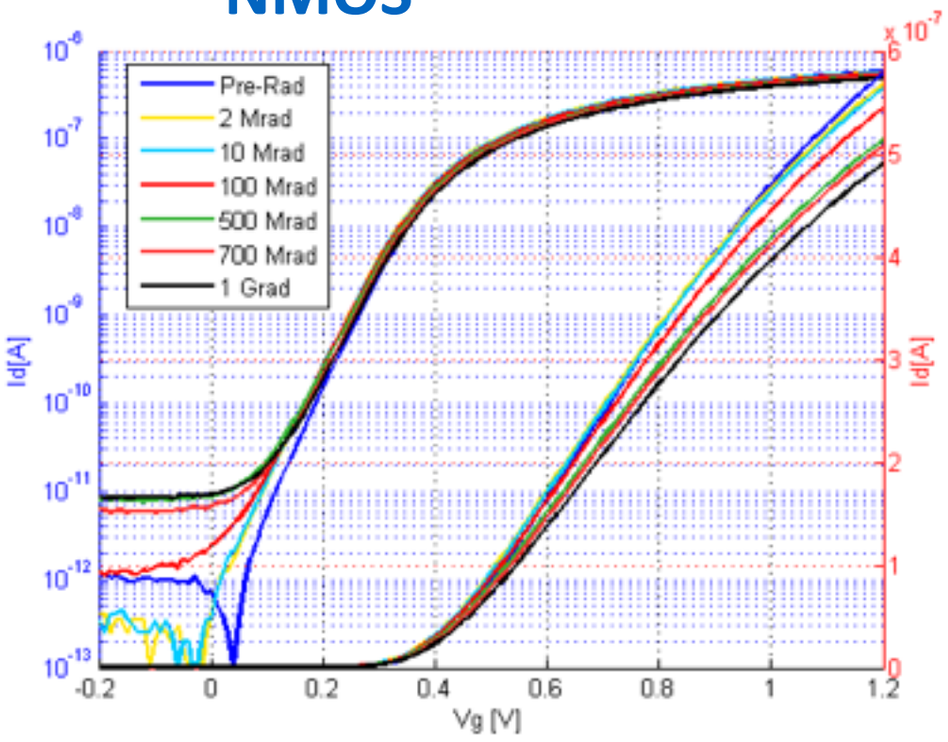


T = 25C

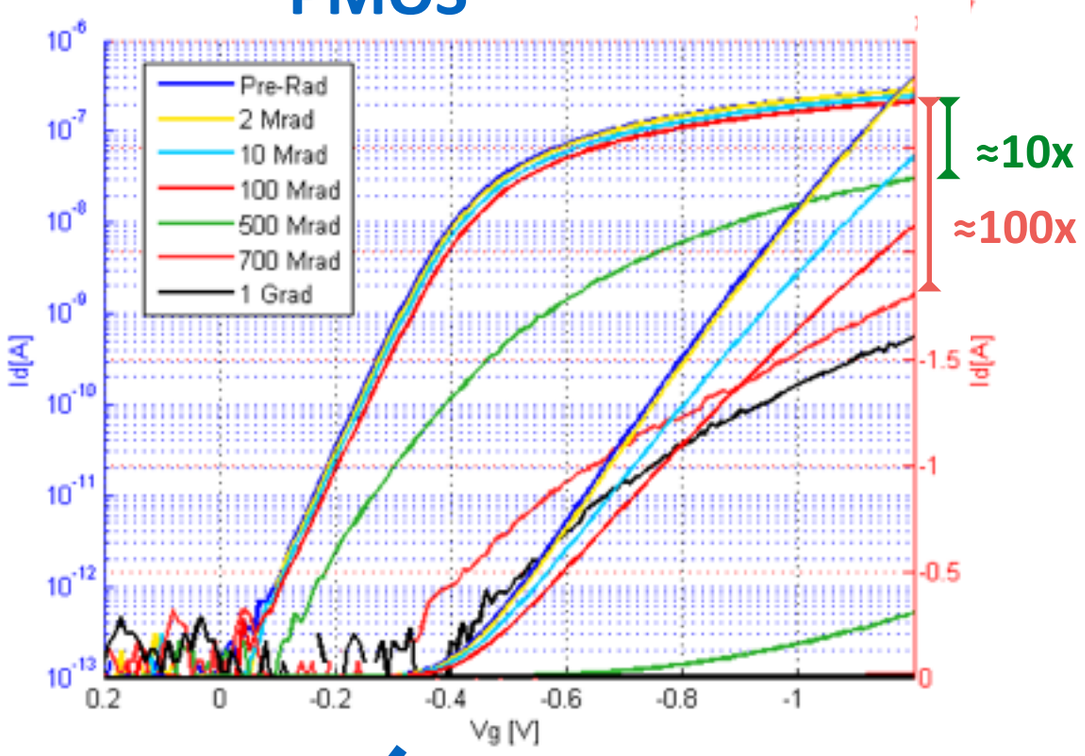
Bias: |Vgs|=|Vds|=1.2V

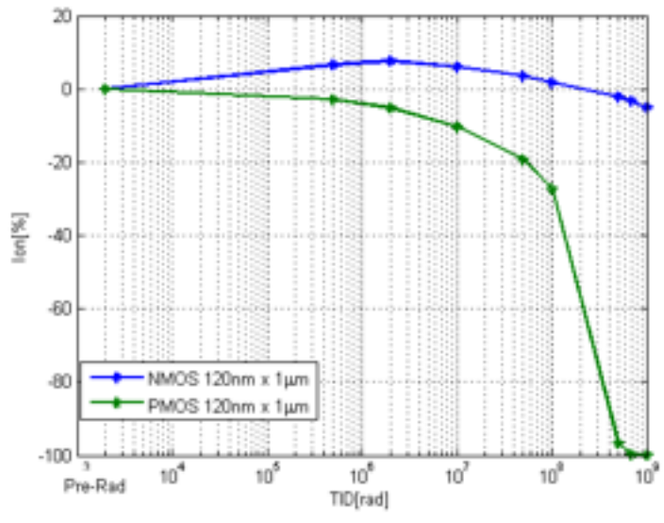
RINCE: Narrow channel PMOS transistors do not work above 500Mrad, while NMOS are working without large damage up to 1Grad

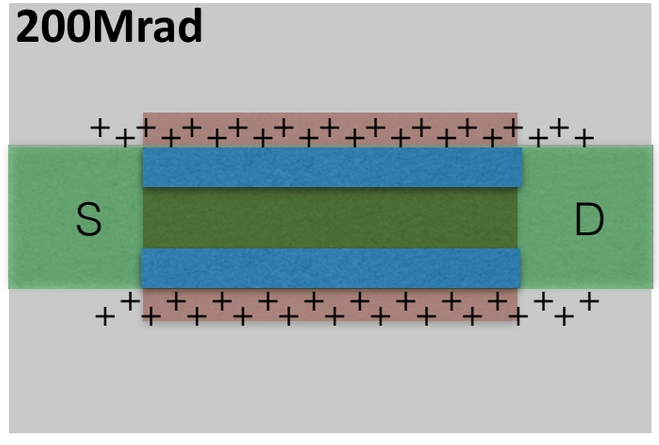
NMOS



PMOS



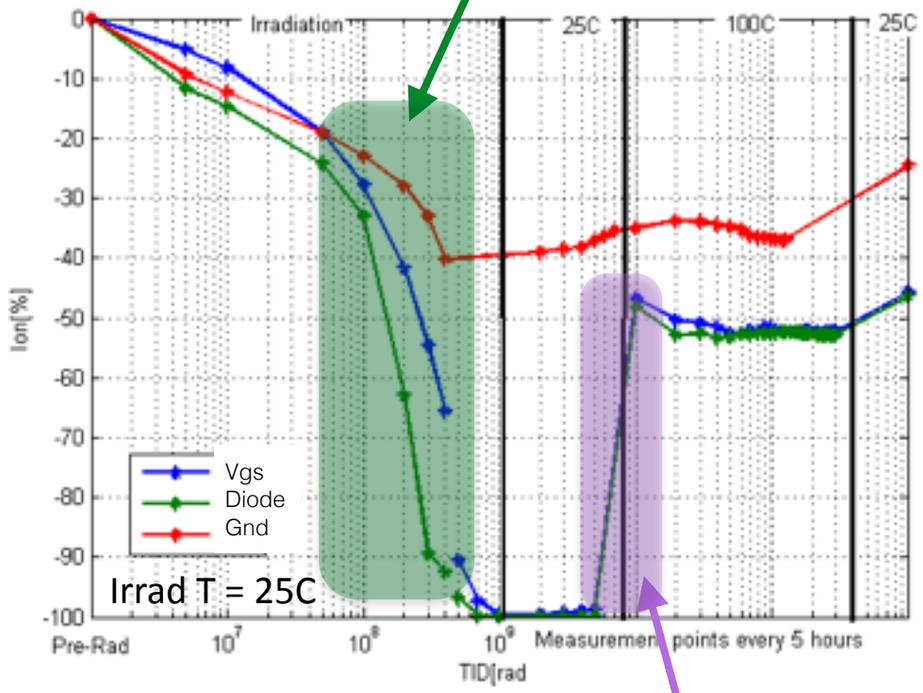




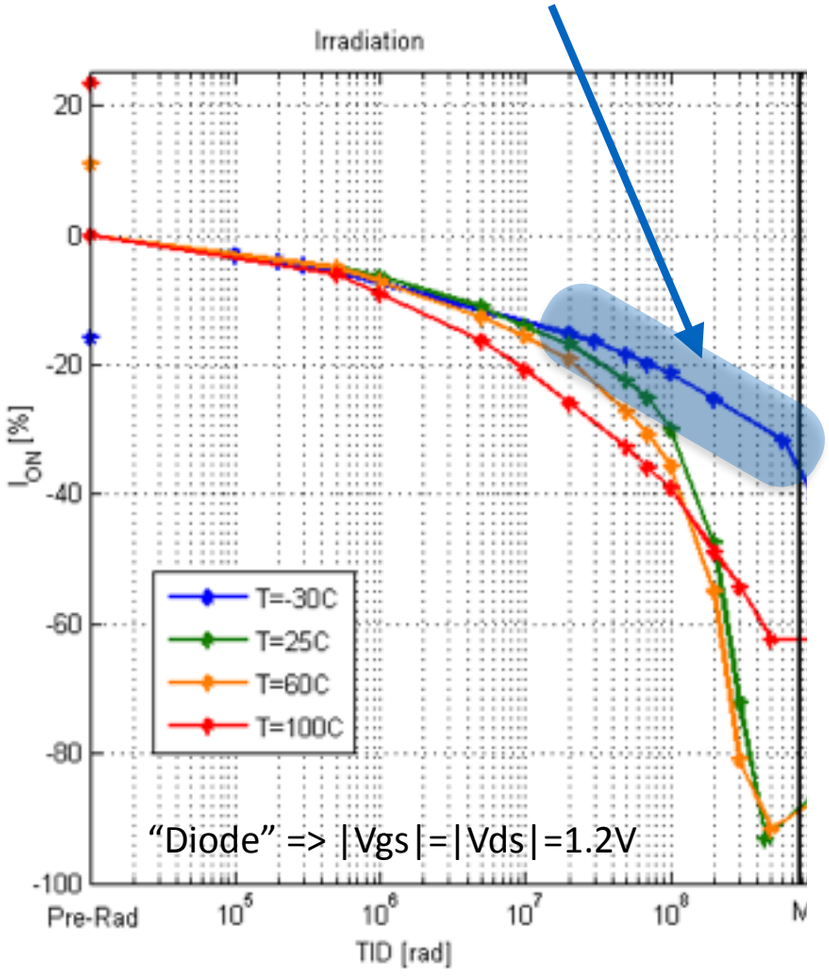
Transistors' size: W=120nm, L=1um
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

RINCE in PMOS depends on bias and temperature

Bias during irradiation is bad!



Sub-zero T during irradiation is good



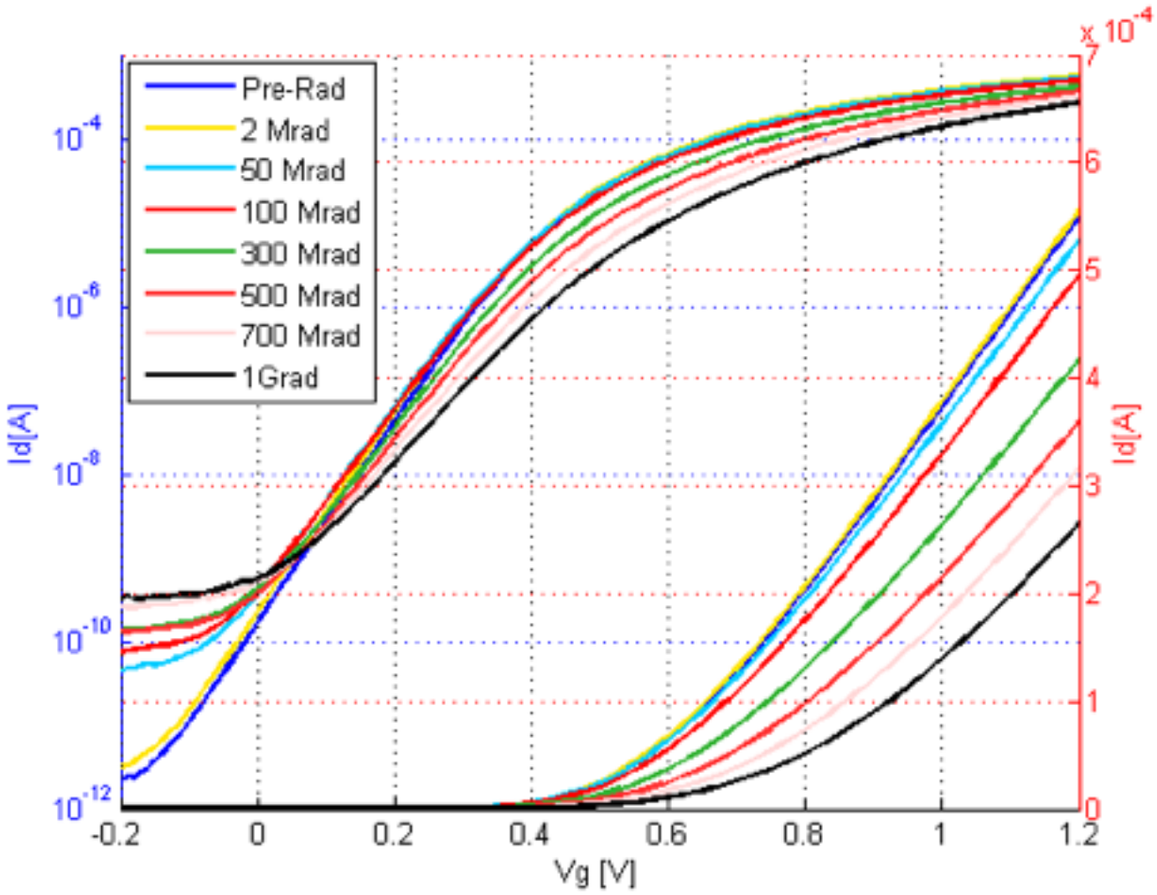
Annealing at high T is good!

Transistors' size: W=120nm, L=1um
Irradiation conditions:
* Bias:
"Vgs" => |Vgs|= 1.2V, Vds=0V
"Diode" => |Vgs|=|Vds|=1.2V
"Gnd" =>|Vgs|=Vds=0V

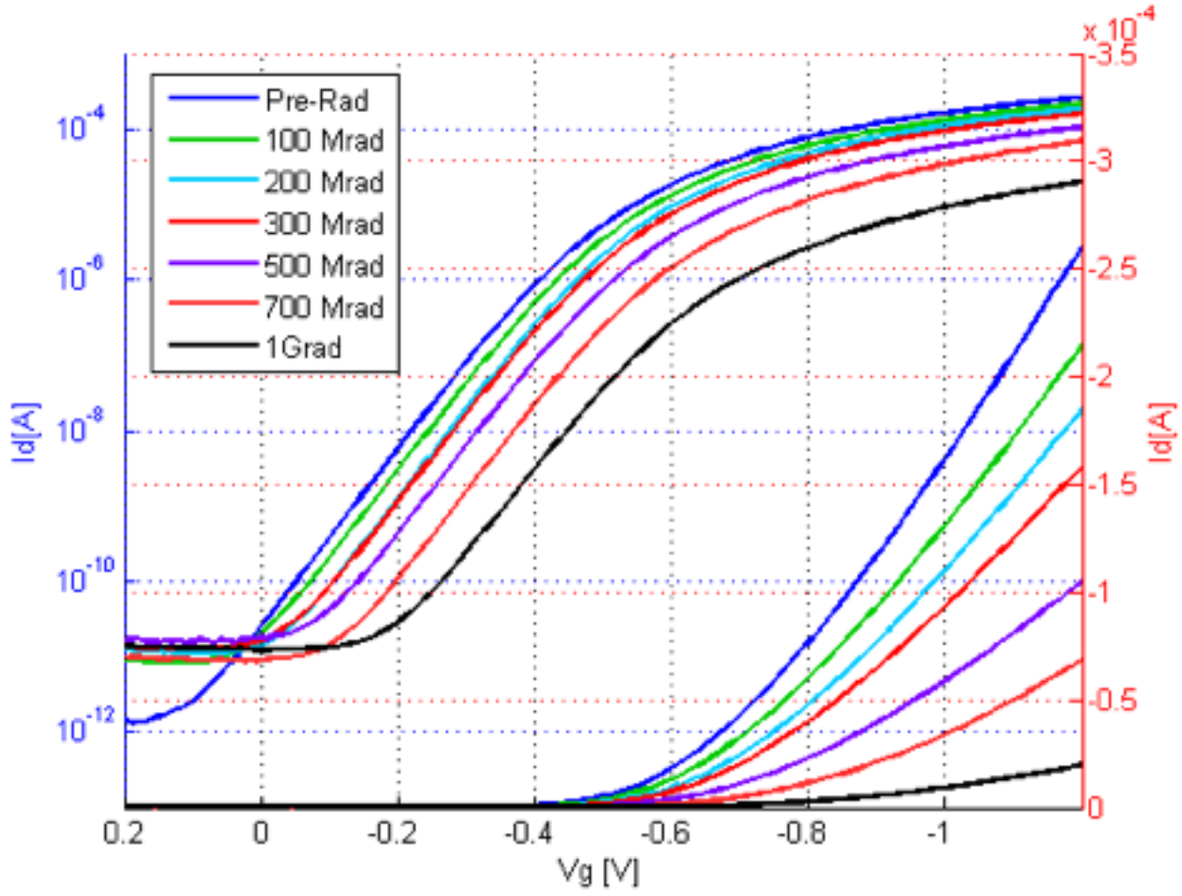
RISCE: Short channel PMOS are more damaged than NMOS

Damage occurs also in ELT transistors, hence it can not be due to the STI oxide

NMOS

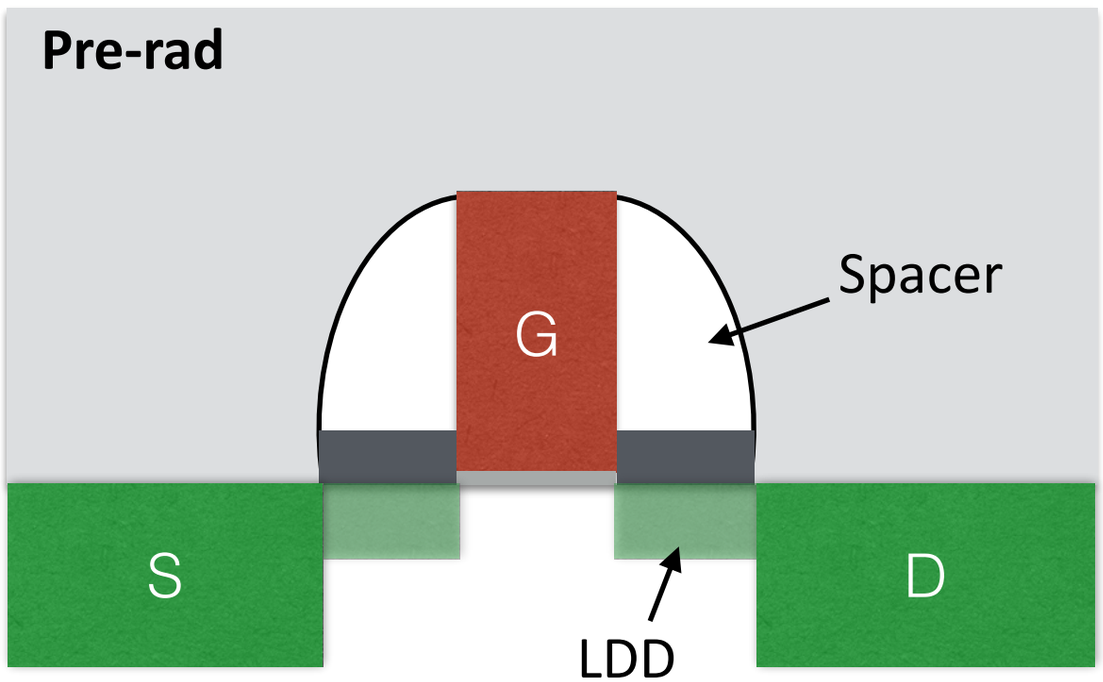


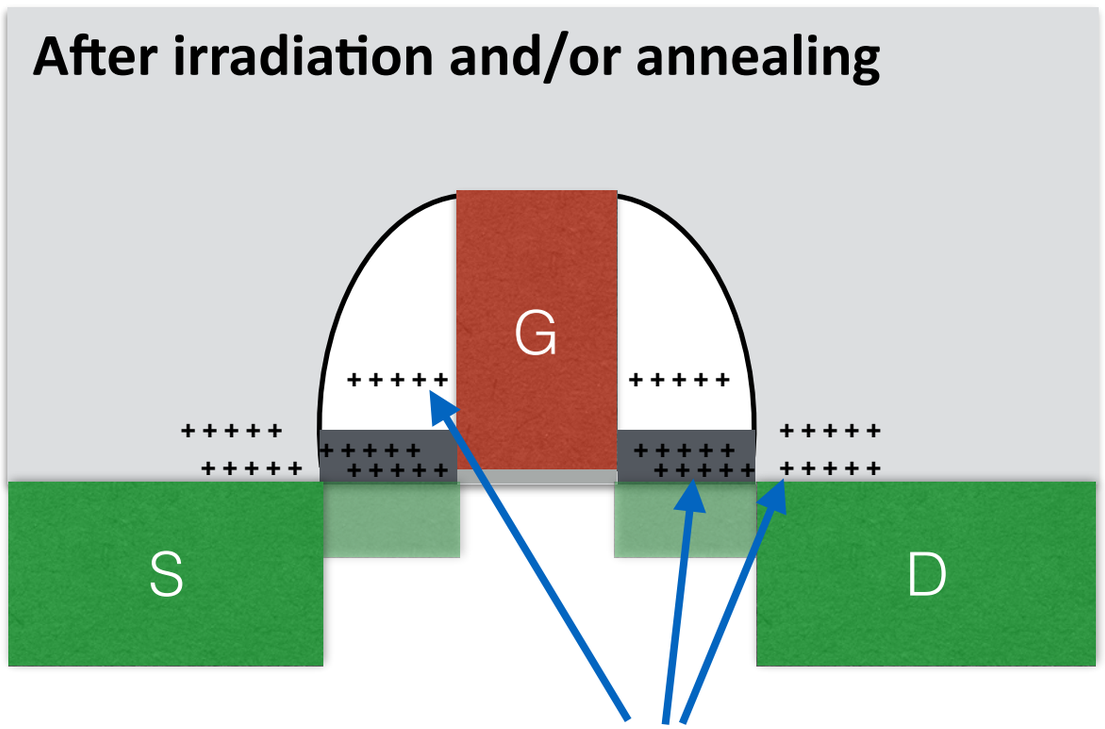
PMOS



Transistors' size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

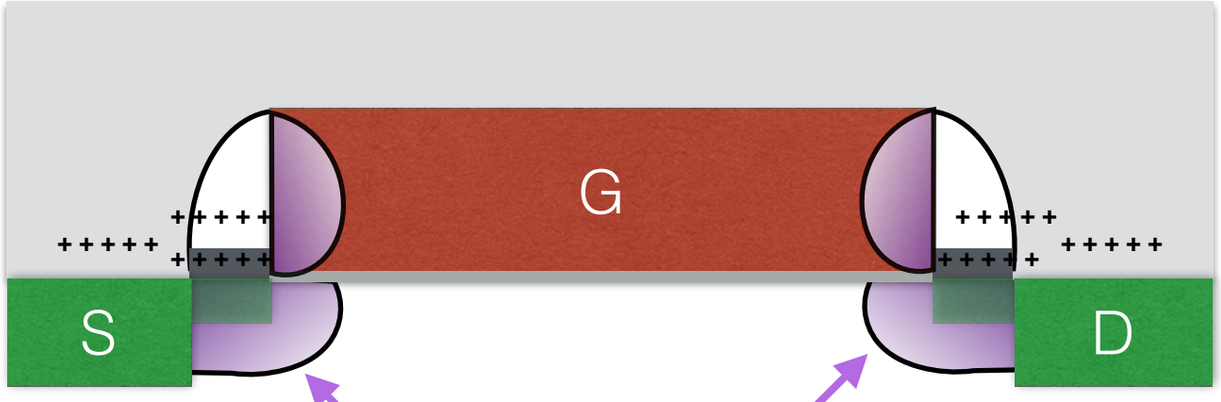
RISCE can be conceptually represented by this cartoon





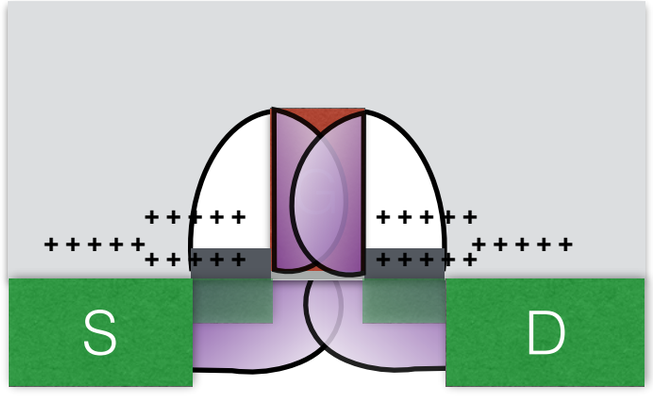
Which defect? Which charge trapped? Where?

L=moderate size



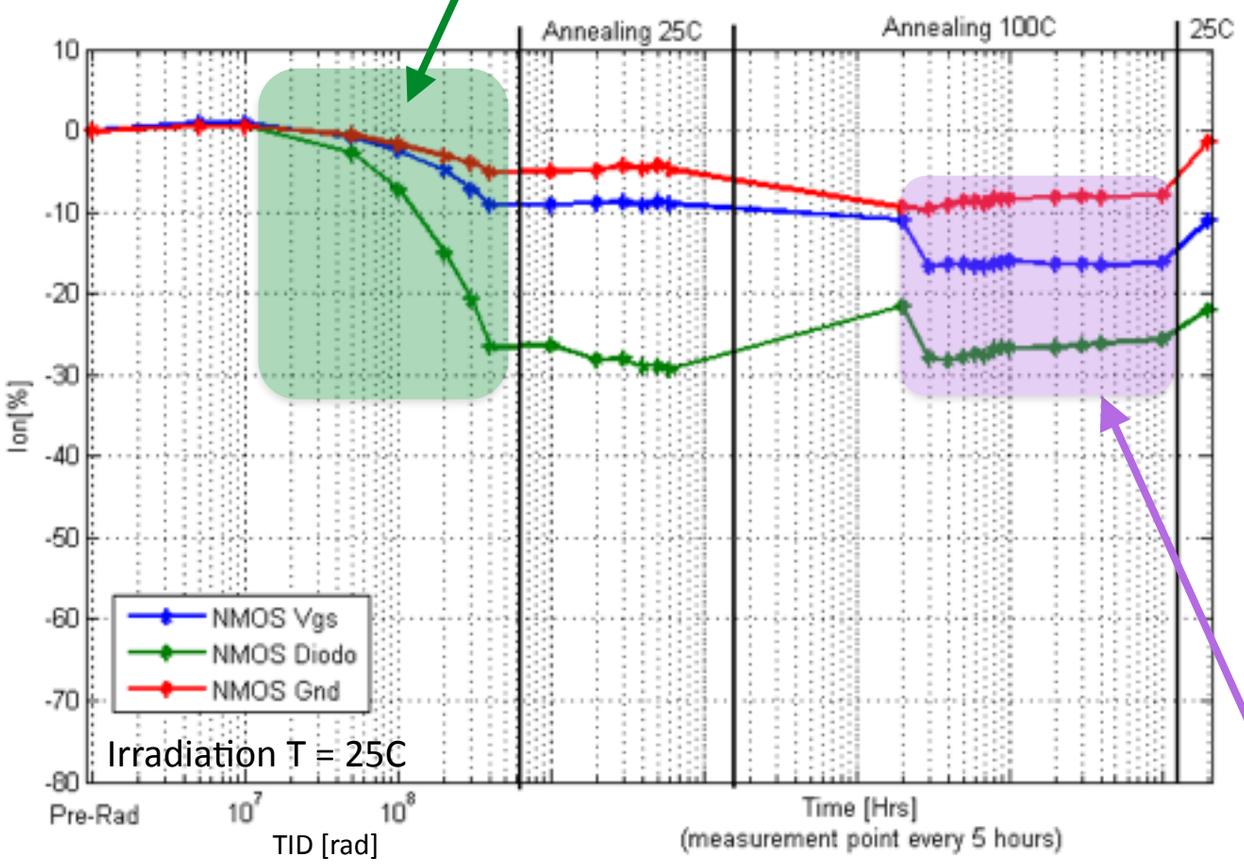
Regions strongly influenced by the trapped charge

L=min size

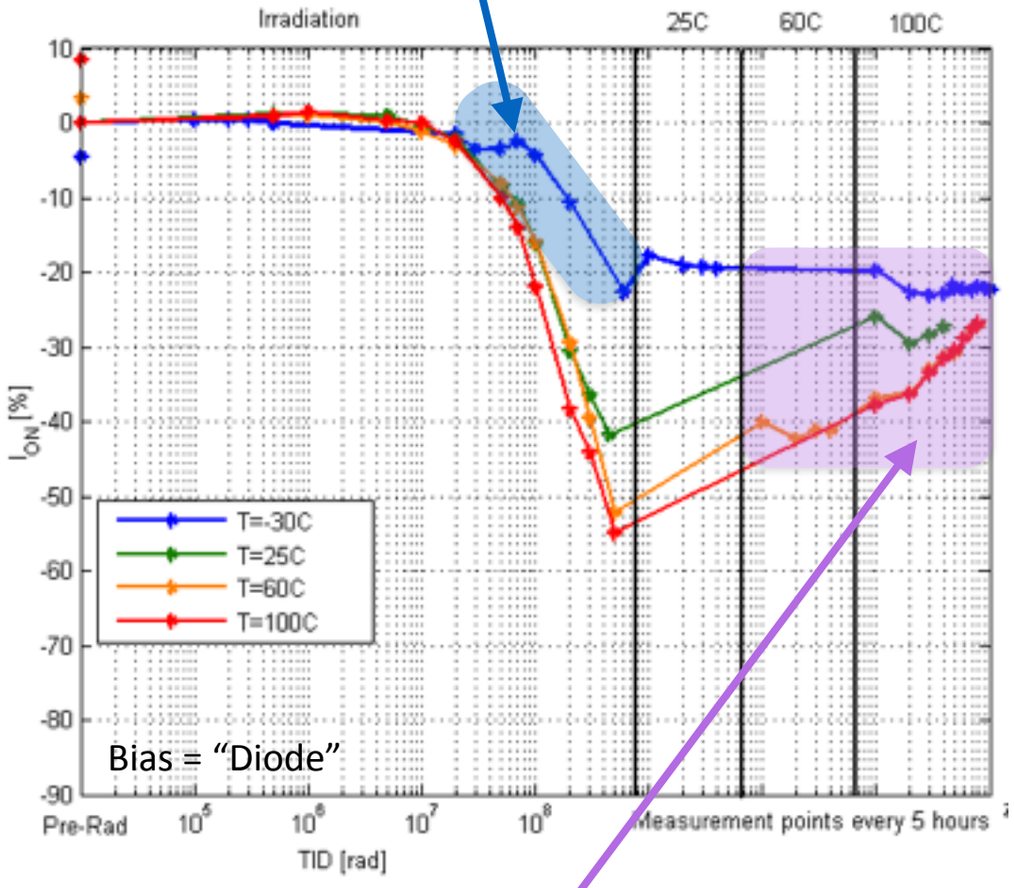


RISCE in NMOS

Bias during irradiation is bad!



Sub-zero T during irradiation is good



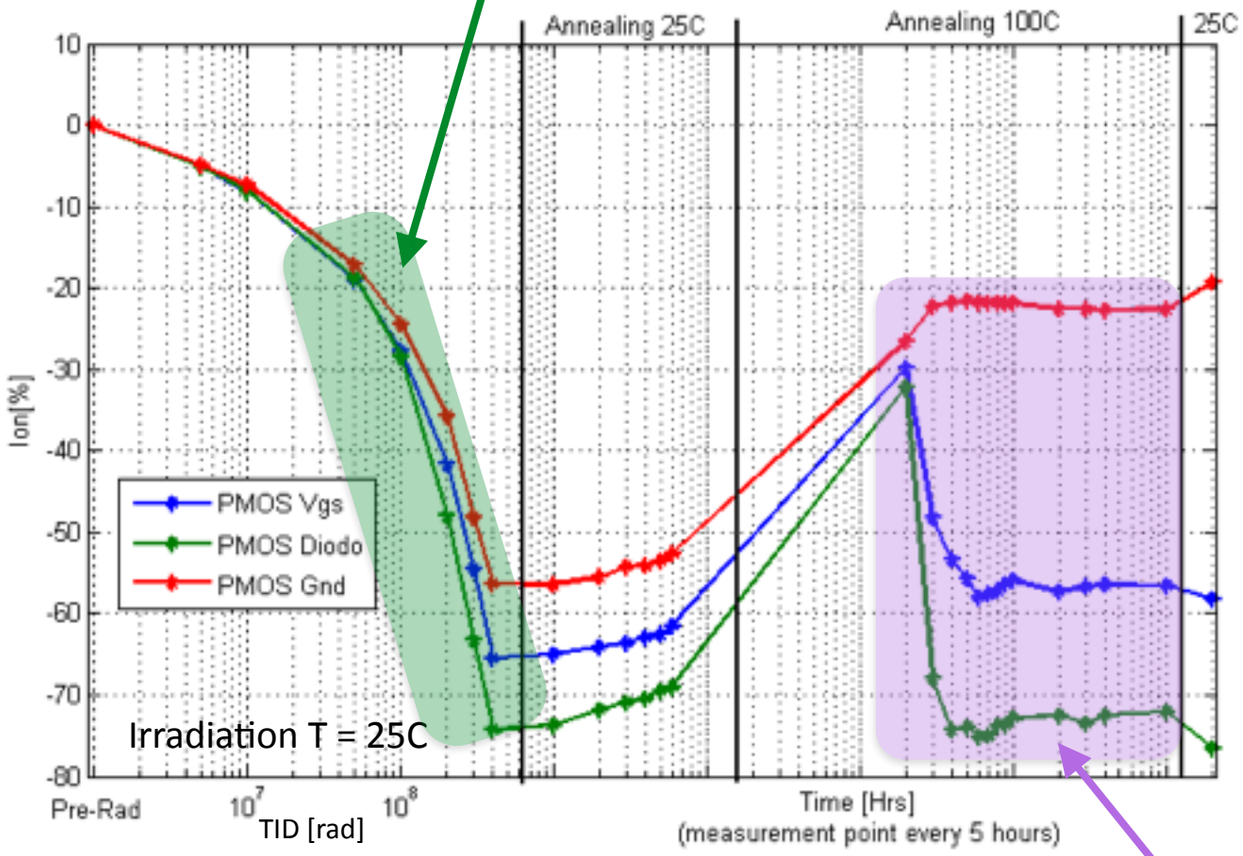
Annealing at high T is neutral or good (for the most damaged devices)!

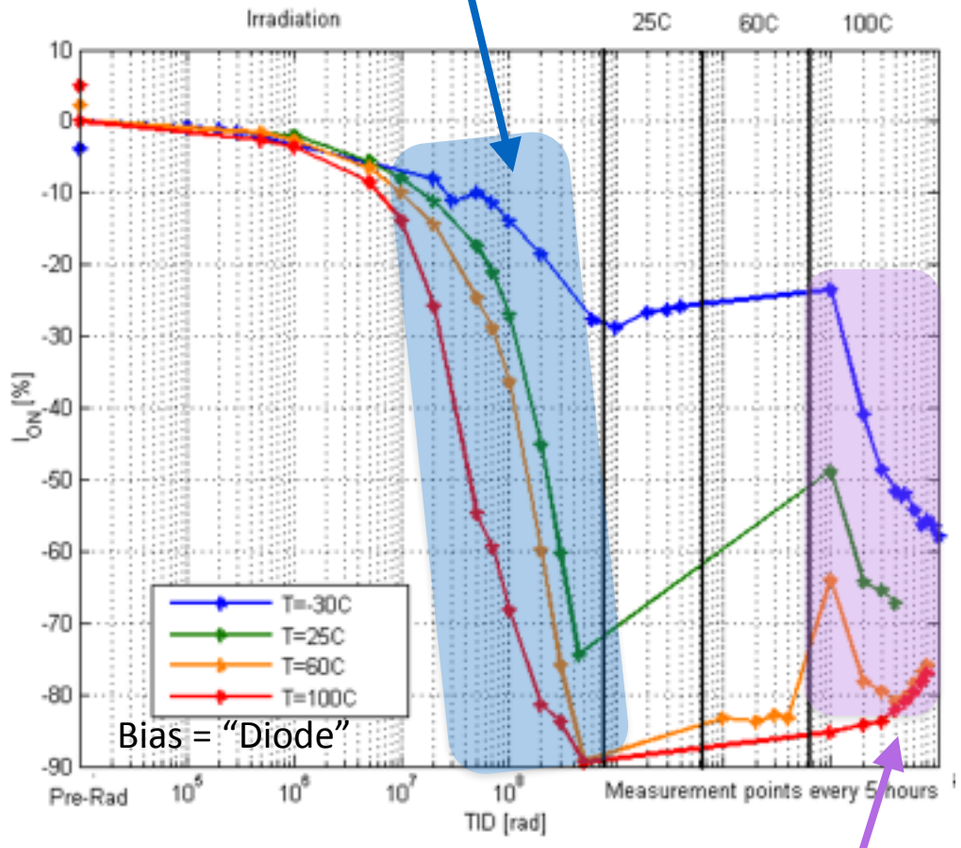
Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Vgs" => |Vgs|= 1.2V, Vds=0V
"Diode" => |Vgs|=|Vds|=1.2V
"Gnd" =>|Vgs|=Vds=0V

RISCE in PMOS

Bias during irradiation is mildly influential

Thermal energy during irradiation is bad!



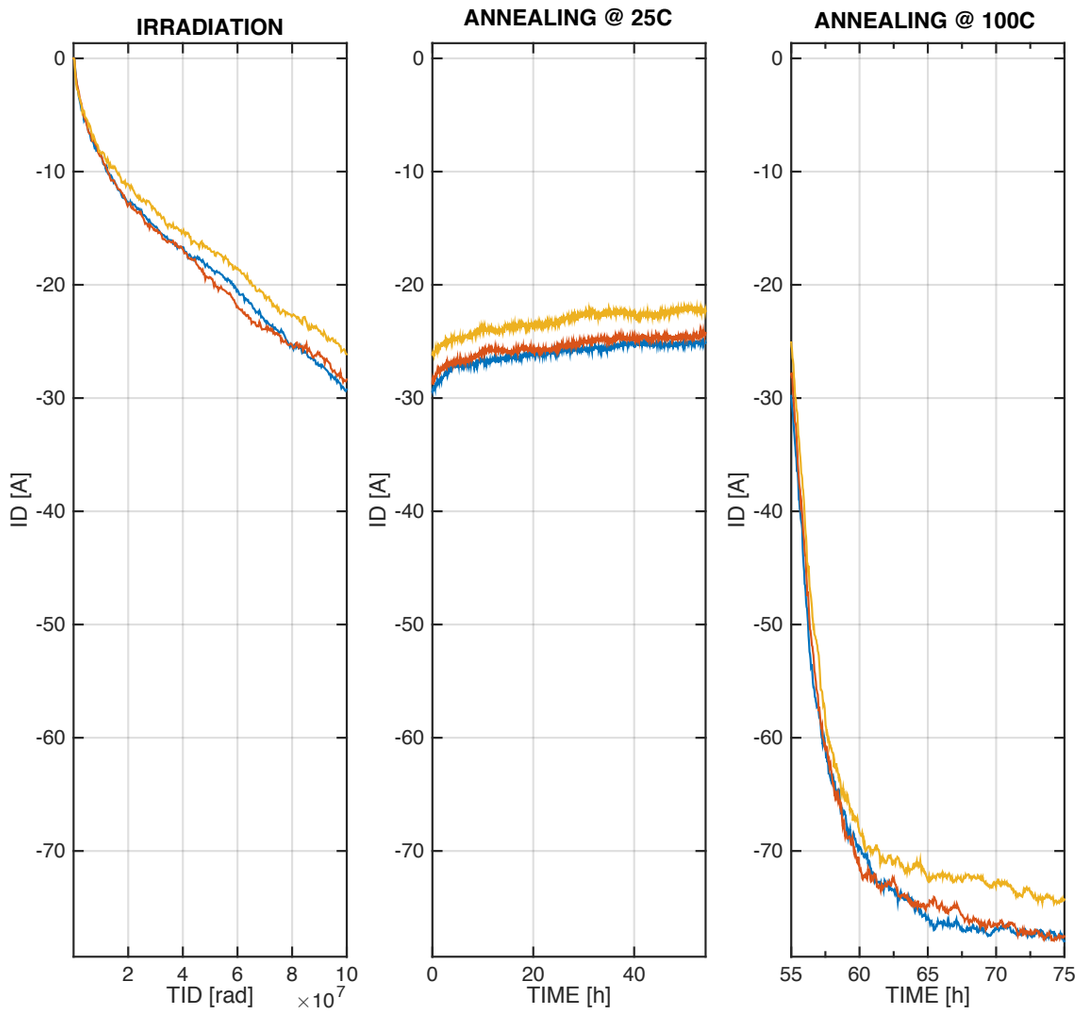


Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Vgs" => |Vgs|= 1.2V, Vds=0V
"Diode" => |Vgs|=|Vds|=1.2V
"Gnd" =>|Vgs|=Vds=0V

Annealing at high T is very bad if performed under bias!!

The qualification procedures for CMOS foresee a 1-week annealing period post-irradiation at 100°C. This considerably worsens the performance of PMOS transistors.

Delta Id (%)



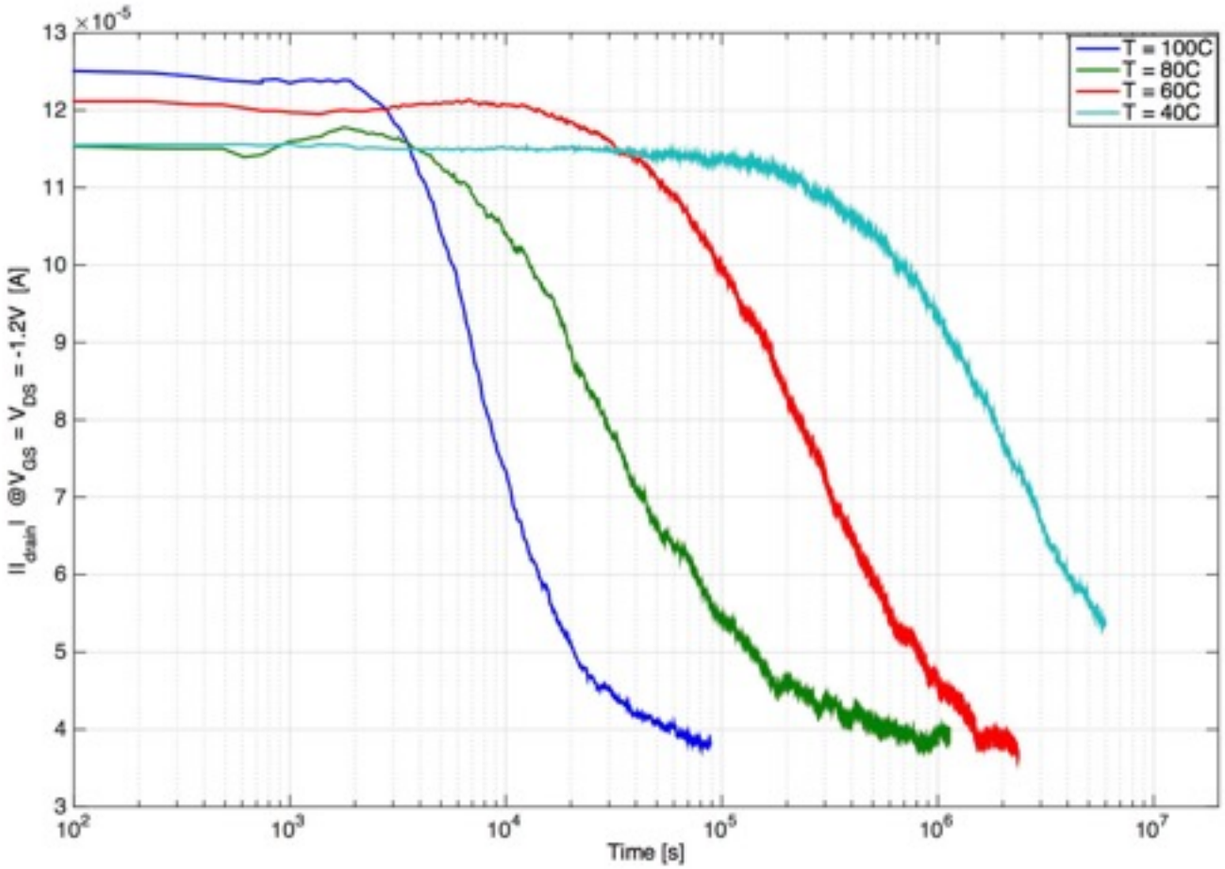
g_m degradation

V_{th} shift

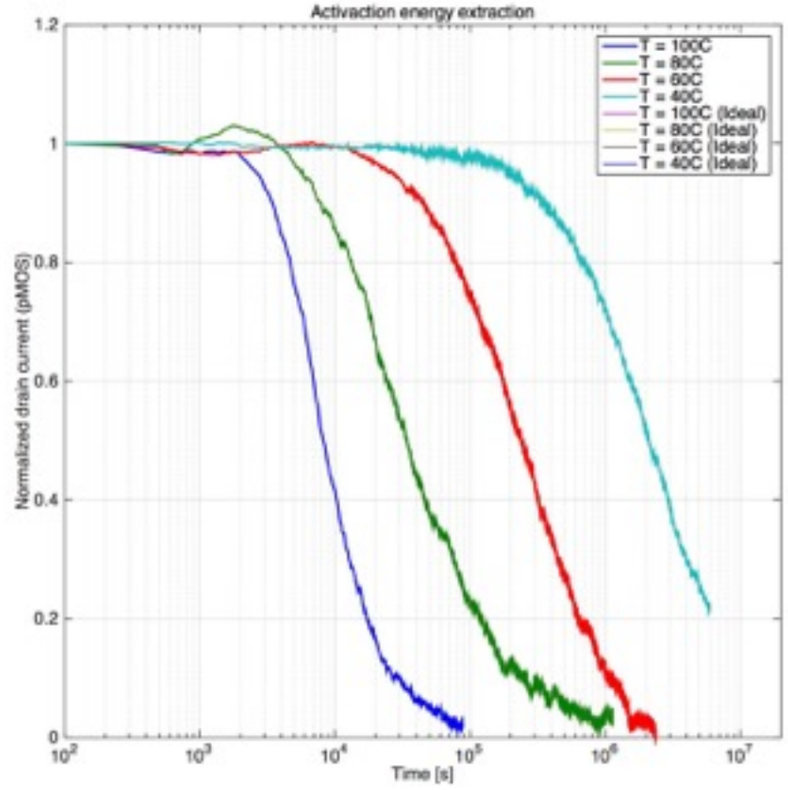
Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Diode" => |Vgs|=|Vds|=1.2V

The post-irradiation evolution in PMOS (V_{th} shift) is clearly a thermally activated process requiring the presence of bias!

Measurements and energy extraction by G.Borghello



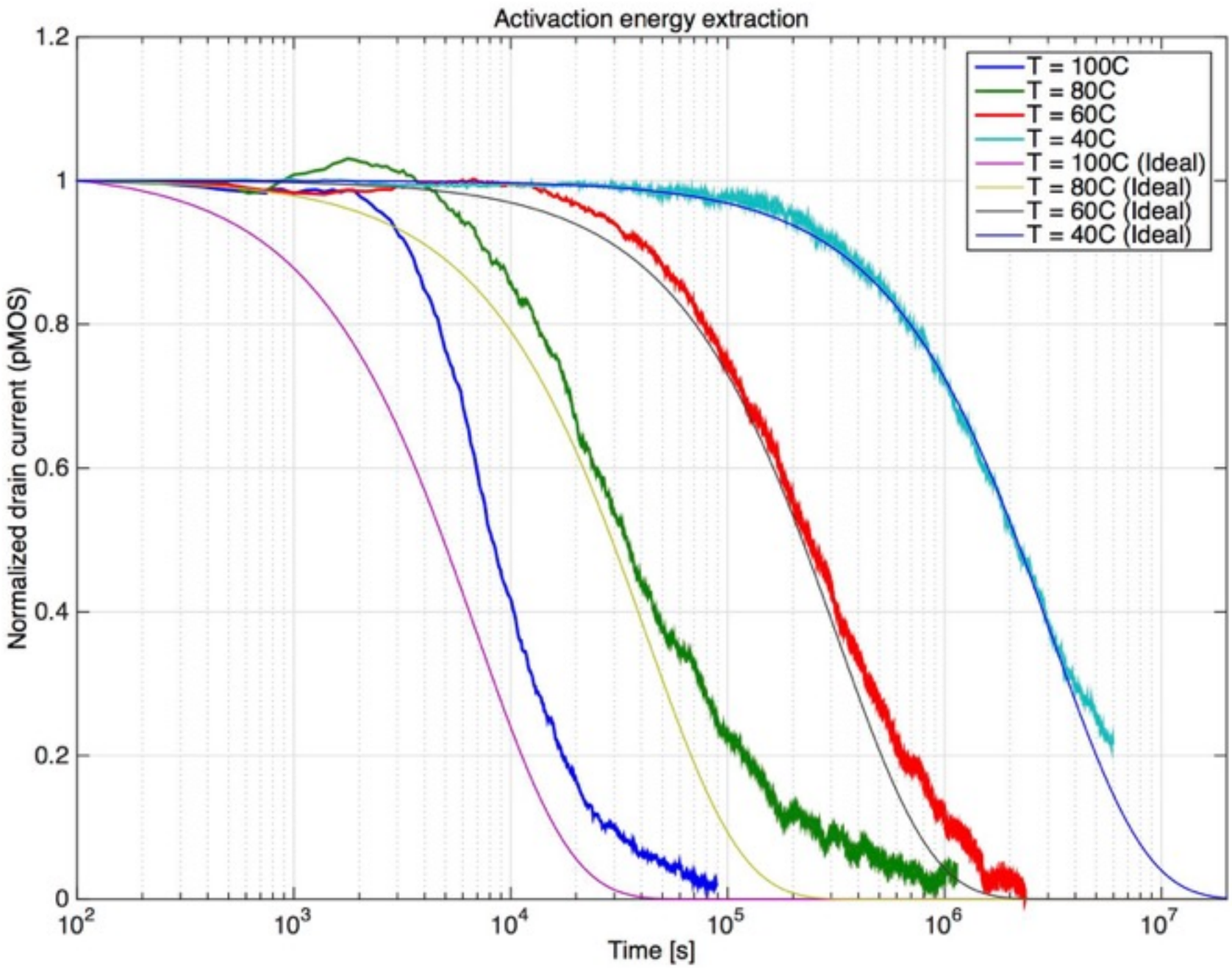
Normalisation



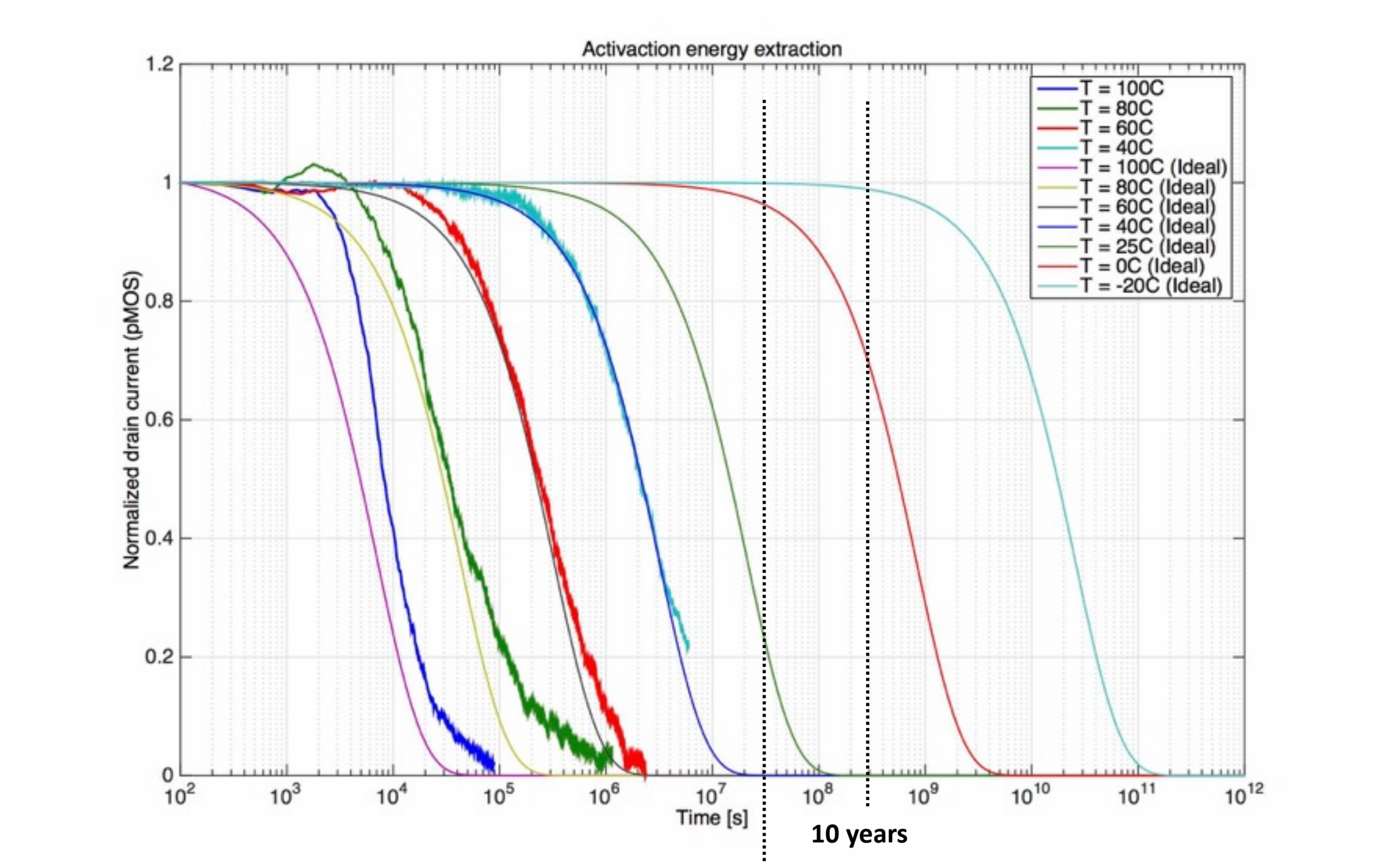
Start of annealing at high T is at 50-55hours

Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Diode" => |Vgs|=|Vds|=1.2V

In the hypothesis of a single activation energy, it is possible to extract it (very approximately) from the 4 experimental points at different temperature.
The model does not fit well the data, but it is useful to estimate the trend of the phenomenon with temperature.



According to the simple model, the post-irradiation evolution of the PMOS (Vht shift) should be considerably slowed at -20°C



Analog design

RISCE and RINCE can be hindered in analog design, where the designer can choose to avoid excessively narrow and short transistors. This has been confirmed in analog designs developed for radiation tolerance and irradiated to large doses.

Digital design

In digital design, the use of commercially available standard cells with minimum L transistors (and narrow ones as well) can lead to ASICs failure in some conditions at high doses. To ensure reliable functionality, we need to:

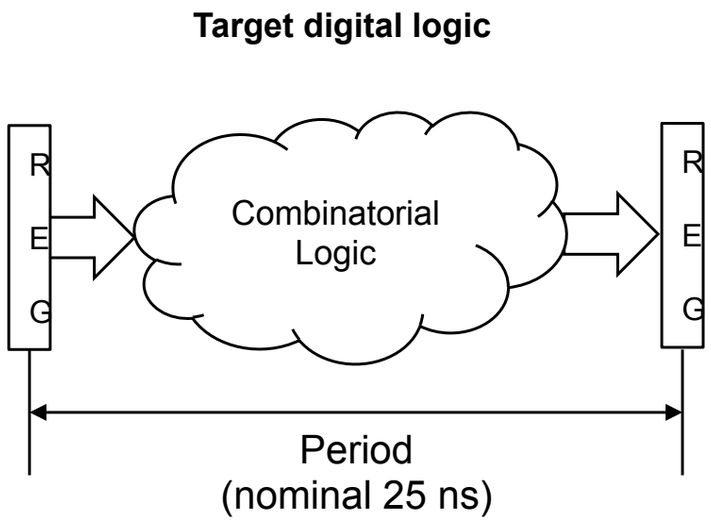
- **use appropriate design safety margins**
- **use an appropriate qualification procedure**

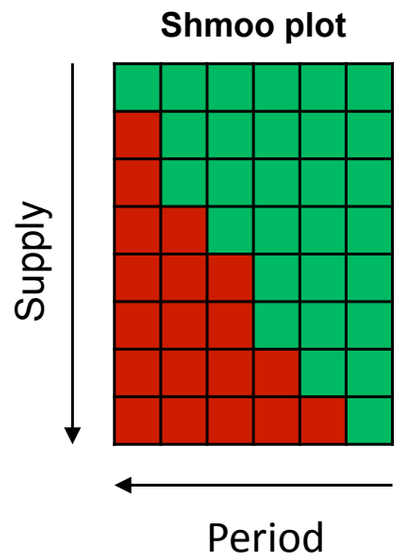
Are results of individual transistors under DC bias representative of the degradation of a digital circuit?

The large bias dependence of some of the observed degradations questions the applicability of the transistor-level results to estimate the response of digital circuits. In particular this is true for the short-channel PMOS and their post-irradiation evolution.

A specific study has been carried on an existing digital prototype (CMS tracker readout). The circuit was running at 40MHz during irradiation and annealing.
The results hereafter are extracted from this work - courtesy of D.Ceresa and the MPA team.

IDEA: Find a data path failing at a certain voltage and frequency and observe how these vary with TID



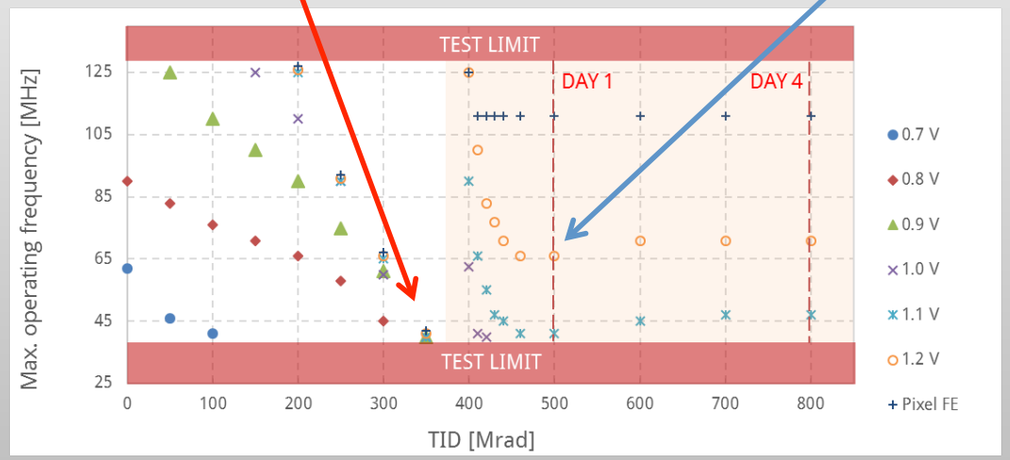


Conclusions from the test of a digital prototype - in agreement also with measurements on 2 different SRAM designs

A qualification procedure could involve irradiation at room T followed by annealing at 100°C, the circuit having to pass both tests

Test during irrad. at room T catches this failure
(due to narrow channel transistors)

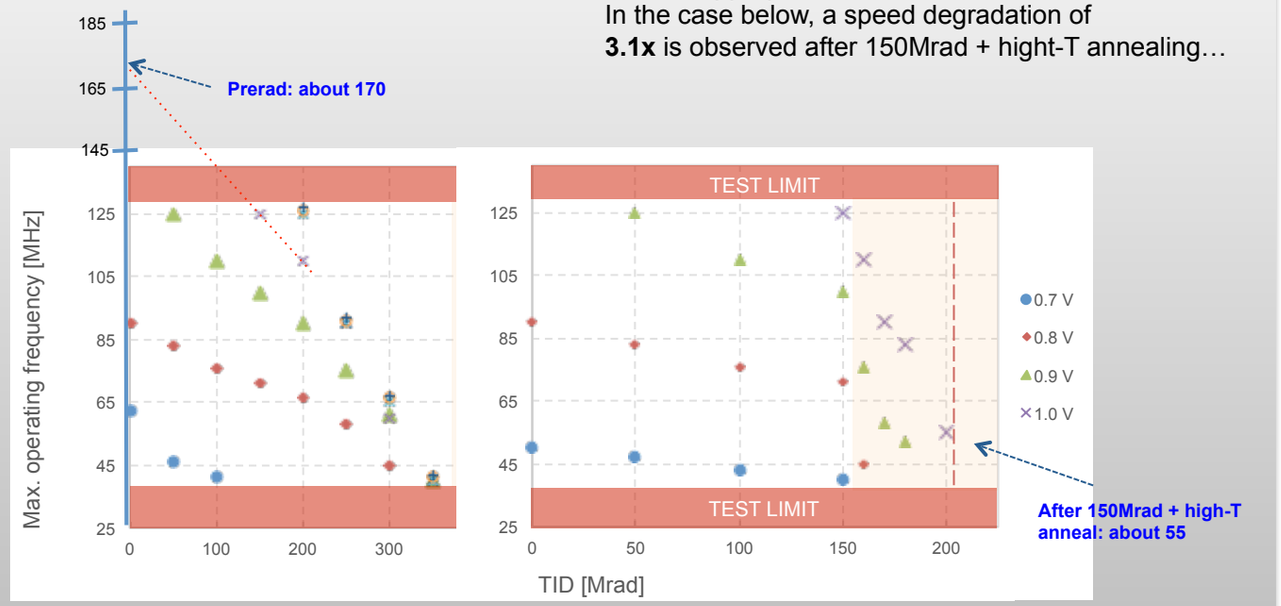
Test after high-T annealing catches this degradation
(due to short channel transistors)



The response of a digital circuit to TID can be correlated with the degradation induced by radiation on individual transistors, both for the narrow and the short channels

Digital designers **MUST take appropriate margins** that take into account the proven speed degradation of logic cells.

What is appropriate?
In the case below, a speed degradation of
3.1x is observed after 150Mrad + hight-T annealing…



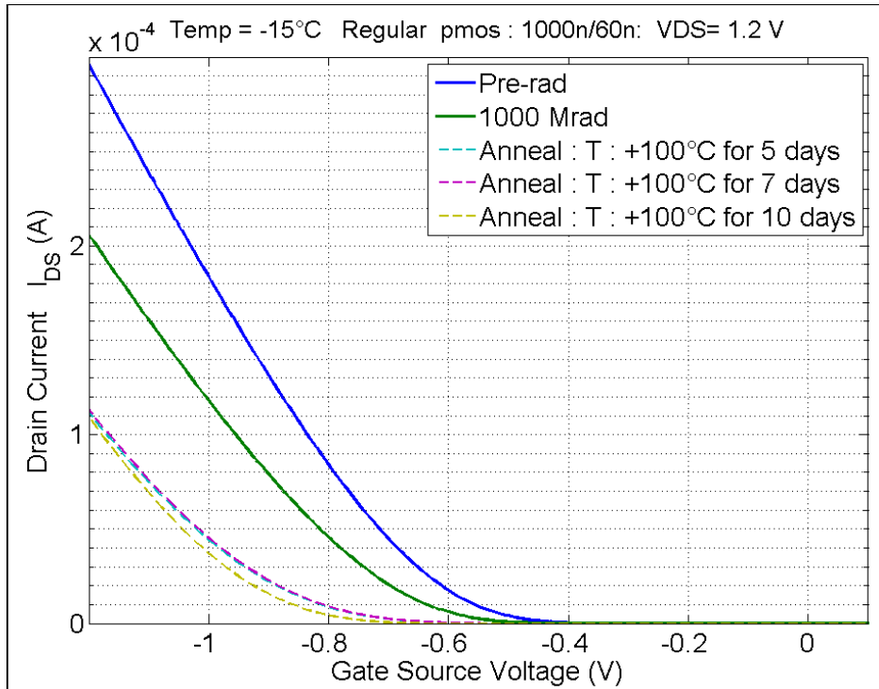
Within RD53 (with the GBT and MPA teams) a work is ongoing to ‘modify’ the digital library and achieve larger tolerance to TID

Different modified cells are designed and tested, and a choice will be made by comparing their TID performance.
Results are expected in summer

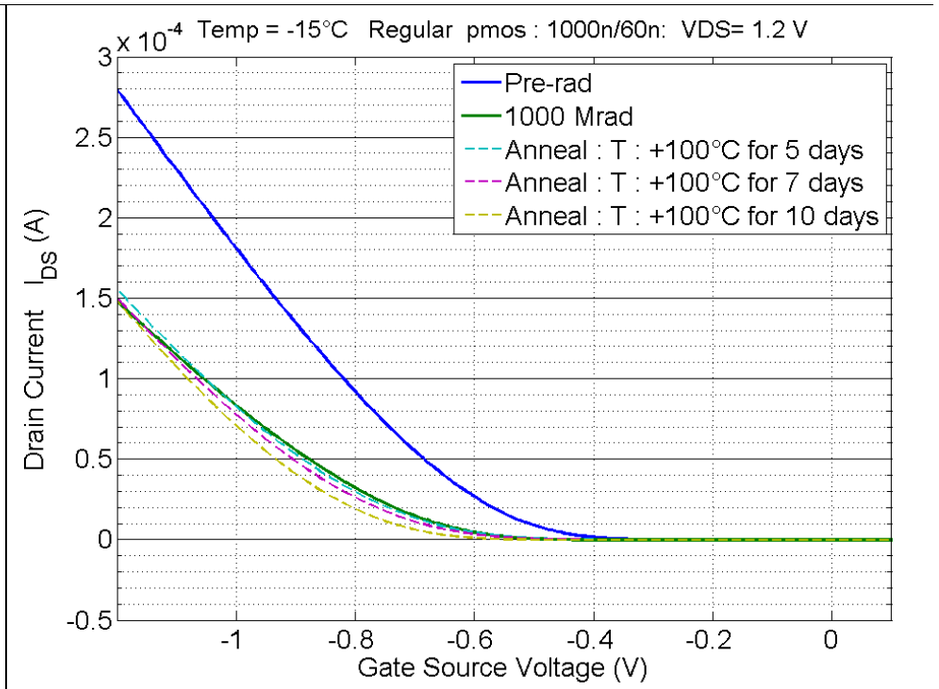
We do not know if the observed phenomenology is common to all 65nm processes or if it is specific to the one we are using

The same irradiation test, at -15°C and followed by high-T annealing, was performed up to 1Grad on transistors from 2 different manufacturers by CPPM Marseille (figures courtesy of M.Menouni and co-workers, CPPM). Irradiation results are overall similar, but the post-irradiation evolution of PMOS is not.

Our 65nm technology

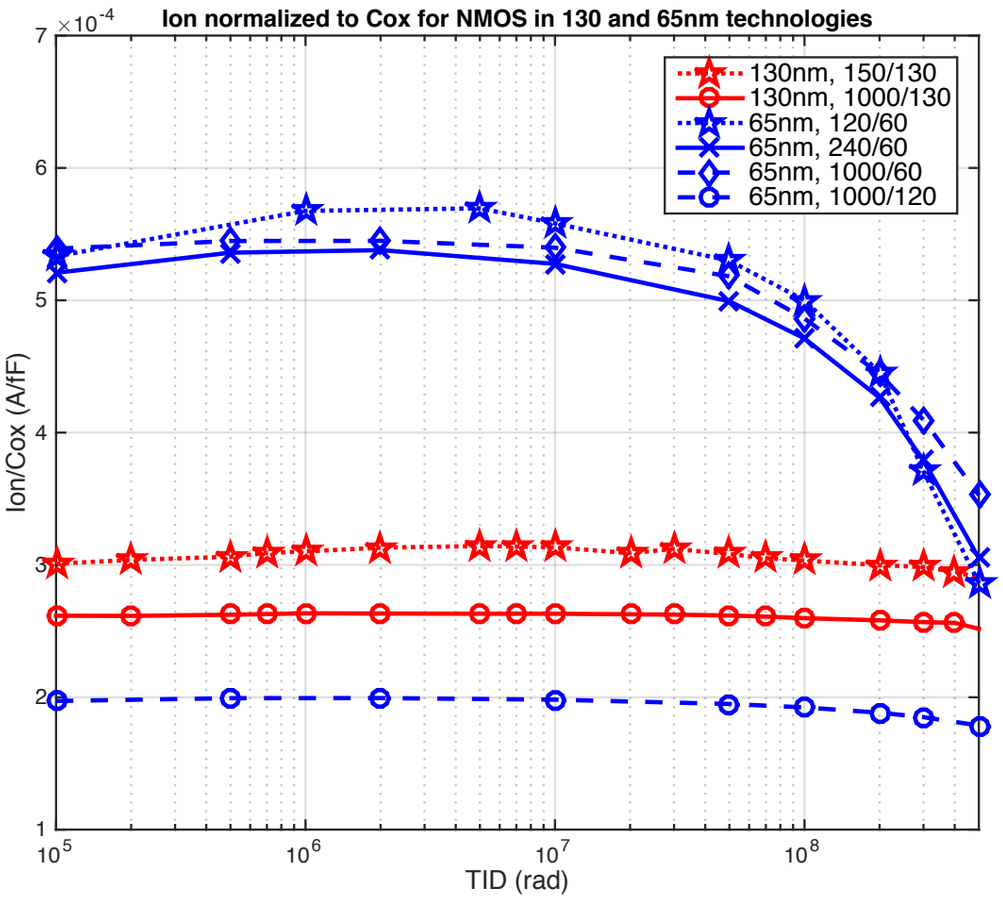


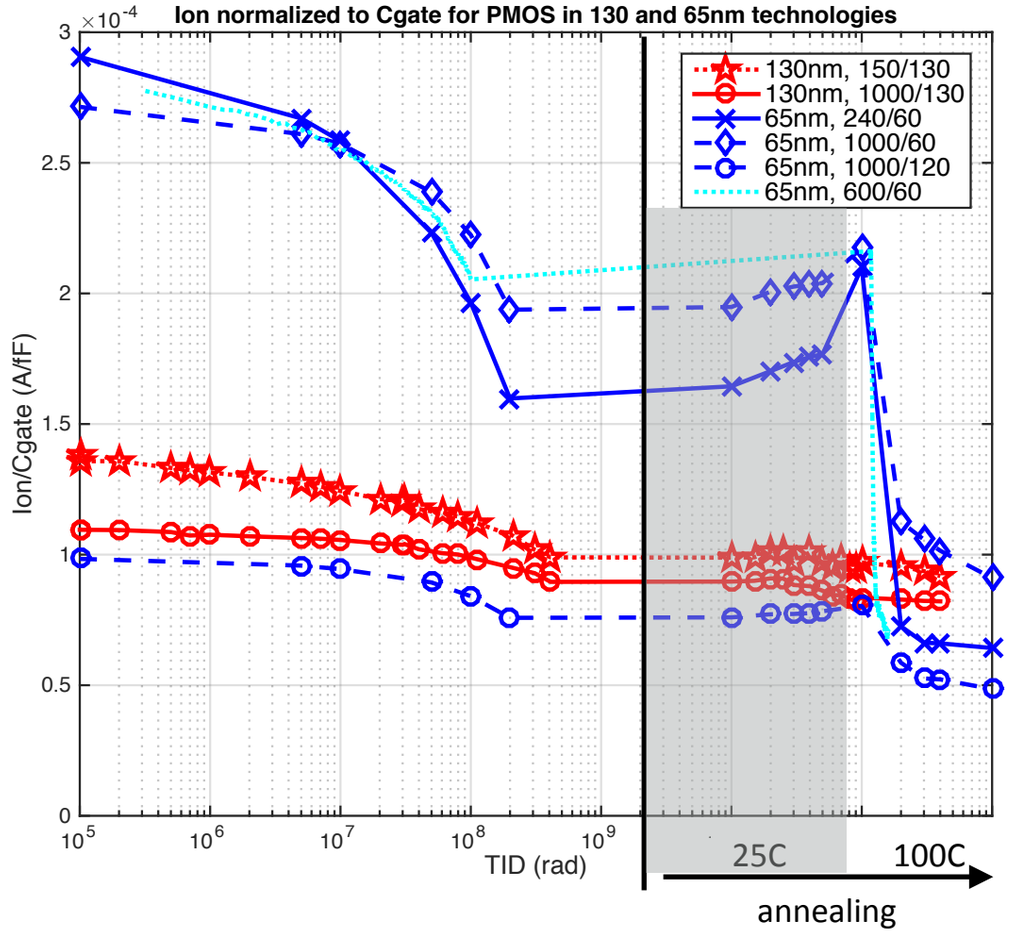
Another 65nm technology



The performance of small-size PMOS transistors in 65nm and 130nm gets comparable after irradiation to 100-200Mrad and high-T annealing

The performance is here indicated by the ratio I_{on}/C_{gate}

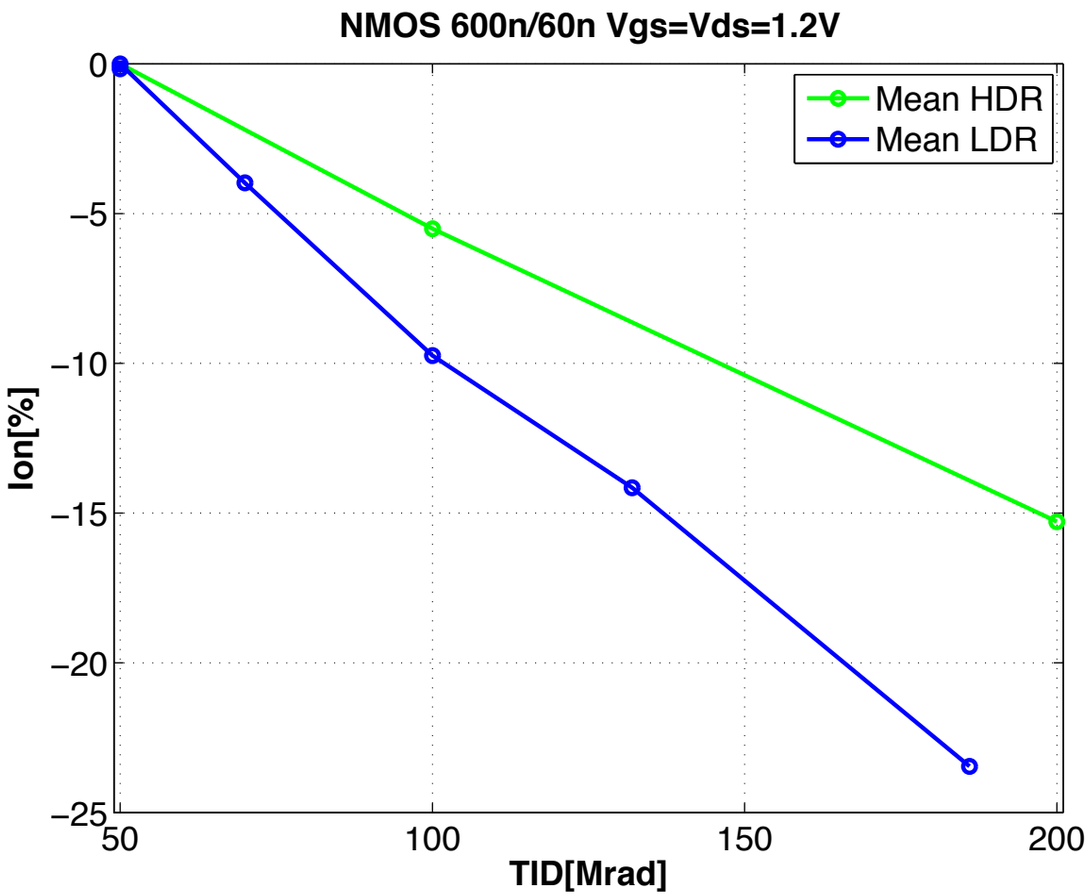


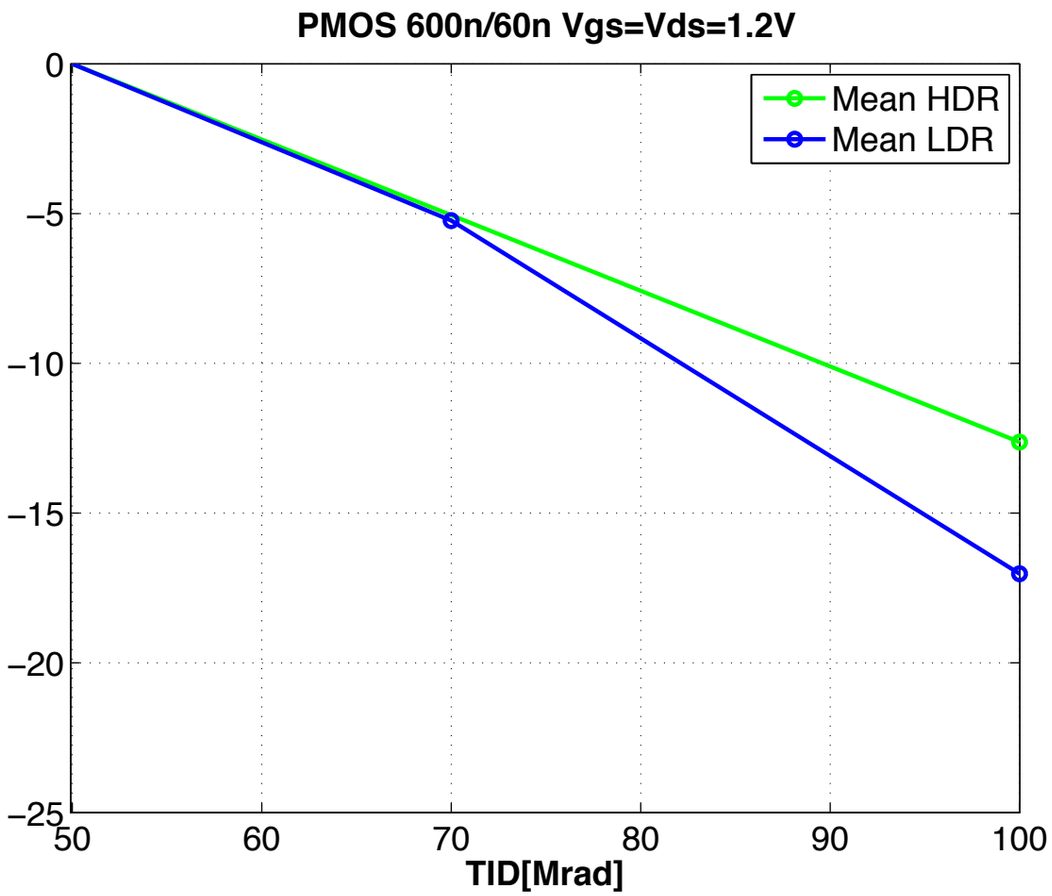


In some of the results above we can see analogies with the phenomenology observed in bipolar technologies subject to ELDRS (Enhanced Low Dose Rate Sensitivity)

A first experiment comparing damage at 2 different dose rates seems to point to an increased damage at lower dose rate

Given the variability between transistors, this first result needed confirmation by more accurate experiments





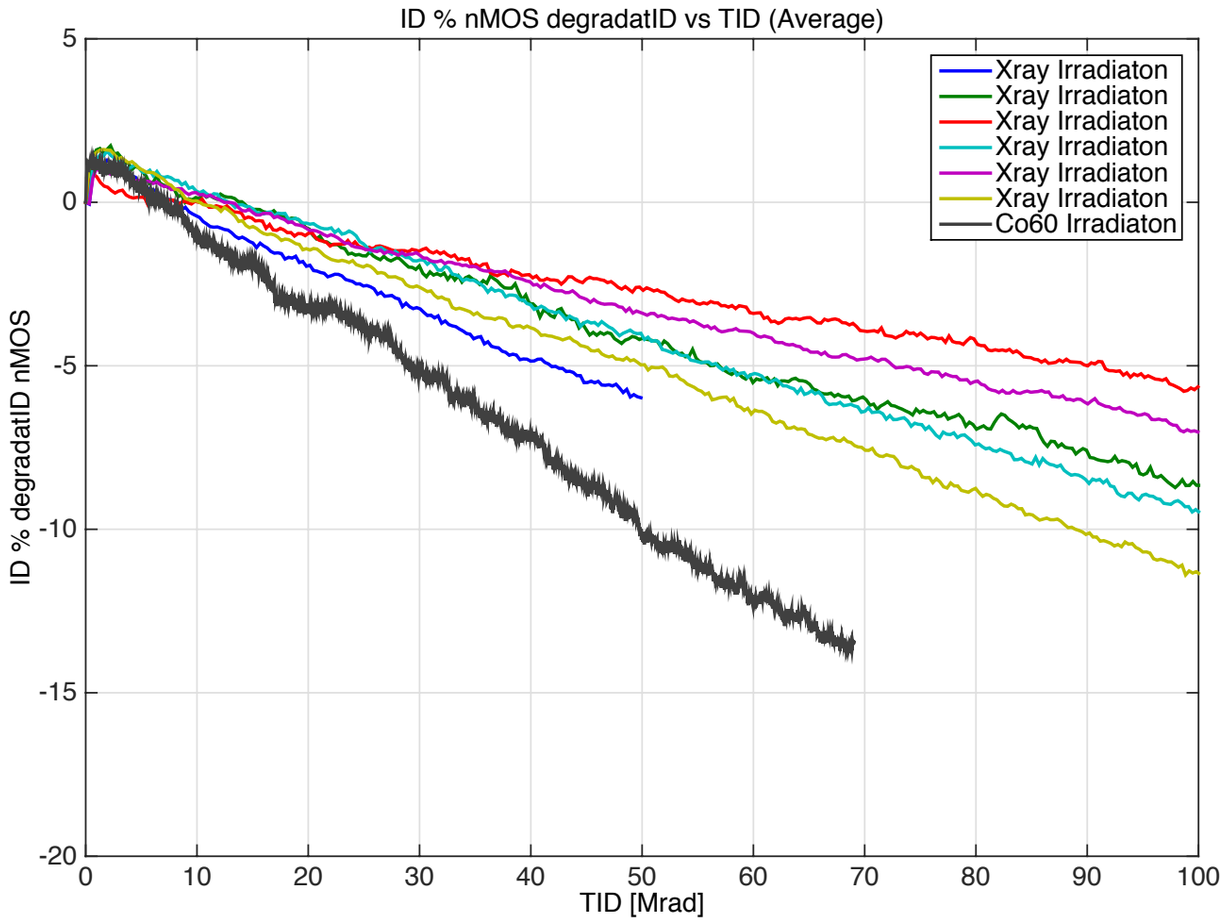
T = 25°C
HDR = 9Mrad/hour
LDR = 325krad/hour
ratio of the dose rate HDR/LDR=27.7
all samples irradiated at HDR up to 50Mrad, then either at HDR or LDR
measurements averaged over 3 samples (HDR) and 2 samples (LDR)

Results from an on-going irradiation with a ^{60}Co source at even lower dose rate: the damage is larger!

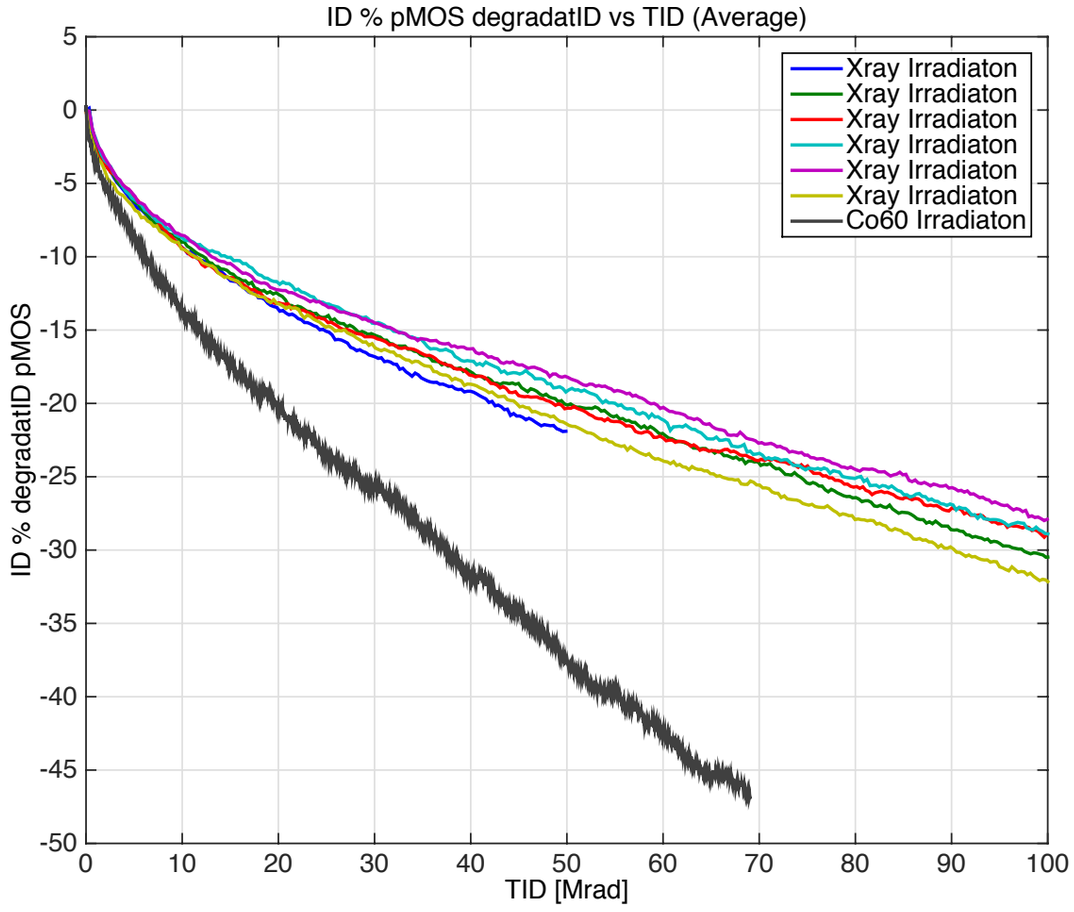
Source at CERN Prevessin (CC60 facility from EN), many thanks to S.Danzeca, A.Thornton, M.Brucoli, M.Brugger, …. for their support in setting up the experiment - in particular for the dosimetry

On-going study within CERN EP-ESE-ME: G.Borghello, S.Michelis, D.Porret, S.Kulis, J.Alozy, …

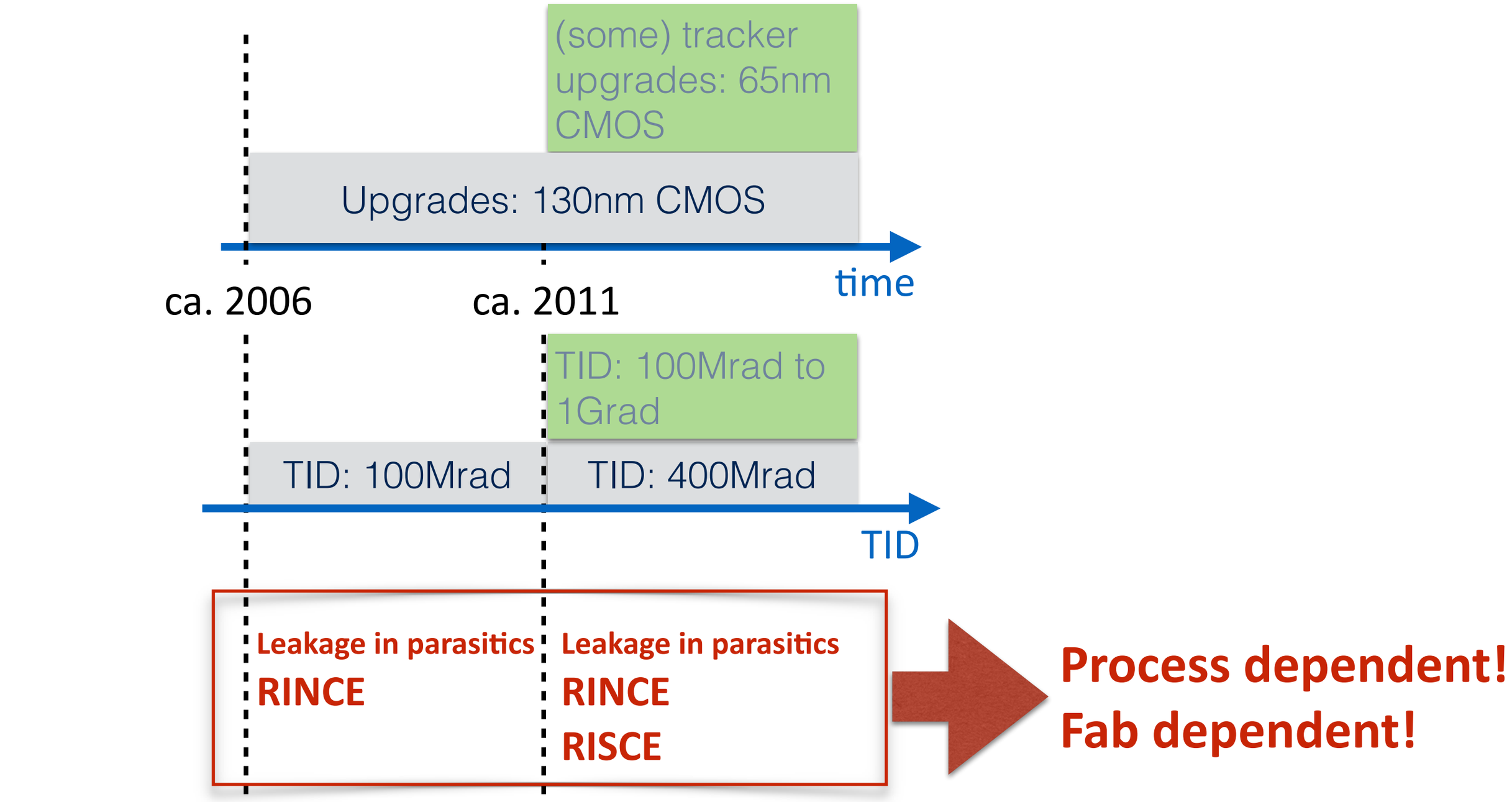
NMOS 600n/60n, Vgs=Vds=1.2V



PMOS 600n/60n, Vgs=Vds=-1.2V



T = 25°C
HDR = 9Mrad/hour
LDR = 35krad/hour
ratio of the dose rate HDR/LDR=257
Average of 3 transistors per Chip


(some) tracker upgrades: 65nm CMOS
Upgrades: 130nm CMOS
time
ca. 2006
ca. 2011
TID: 100Mrad to 1Grad
TID: 100Mrad
TID: 400Mrad
TID
Leakage in parasitics
RINCE
Leakage in parasitics
RINCE
RISCE
Process dependent!
Fab dependent!

130nm

2 Technologies available for ASIC design

- **The present streamline is recommended for all new designs, it appears good for the targeted TID levels**

65nm

Short and narrow channel radiation-induced effects are strong (RINCE, RISCE).
These are complex and make the choice of a qualification procedure and of appropriate design margins difficult, in particular for digital design

all processes

Radiation tolerance varies in different Fabs, and can change over time. We have to:

- **only qualify and use one Fab**
- **monitor regularly the natural radiation tolerance**
- **carefully qualify each ASIC during the prototyping and production phases**

Radiation hard processes

Hardness By Design (HBD) in commercial-grade processes

Production for LHC: 0.25um CMOS

(some) tracker upgrades: 65nm CMOS

Upgrades: 130nm CMOS

time

ca. 1998-2000

ca. 2006

ca. 2011

TID up to 10Mrad

TID: 100Mrad

TID: 100Mrad to 1Grad

TID: 400Mrad

TID

Main transistor
V_{th}, g_m, …
Leakage in parasitics

Leakage in parasitics

Leakage in parasitics
RINCE

Leakage in parasitics
RINCE
RISCE