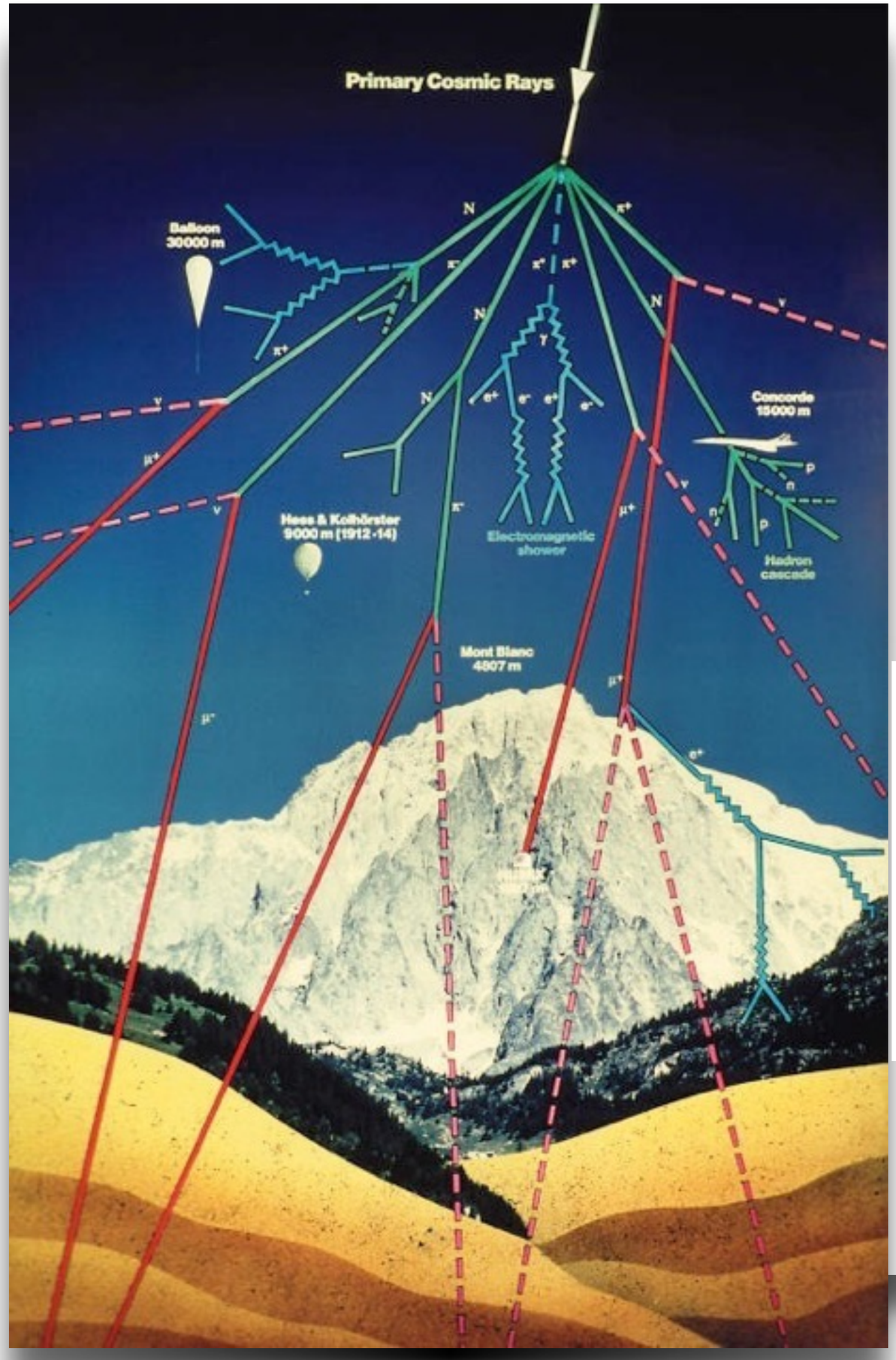
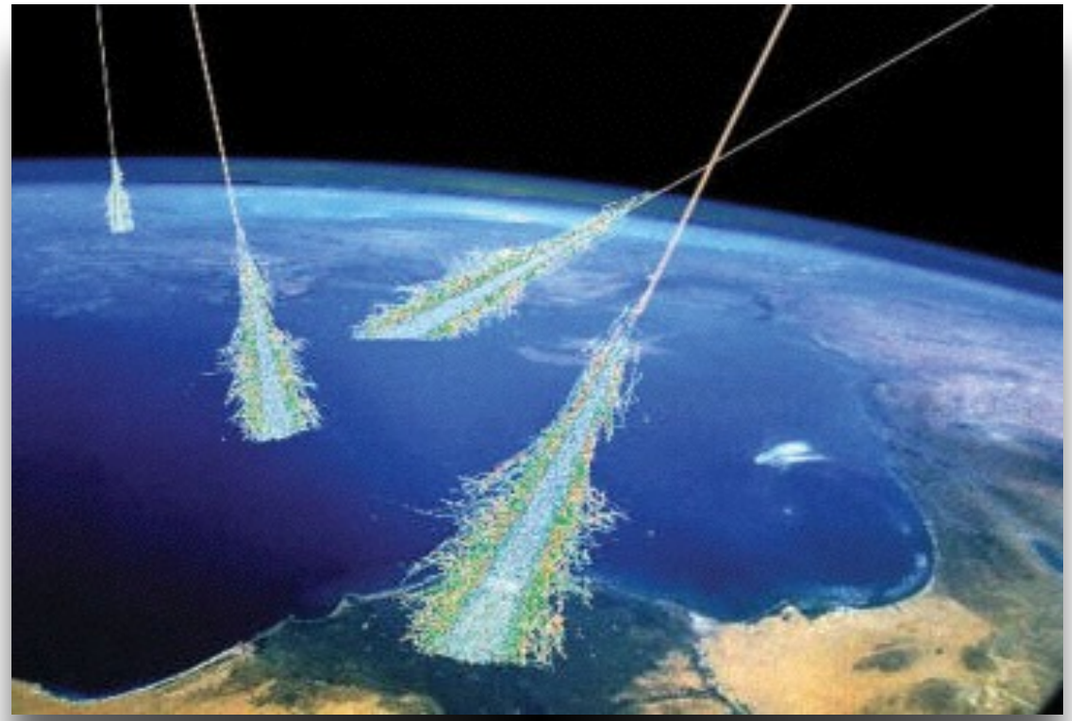
Radiation effects in 65nm CMOS at particle physics detectors: radiation strikes back

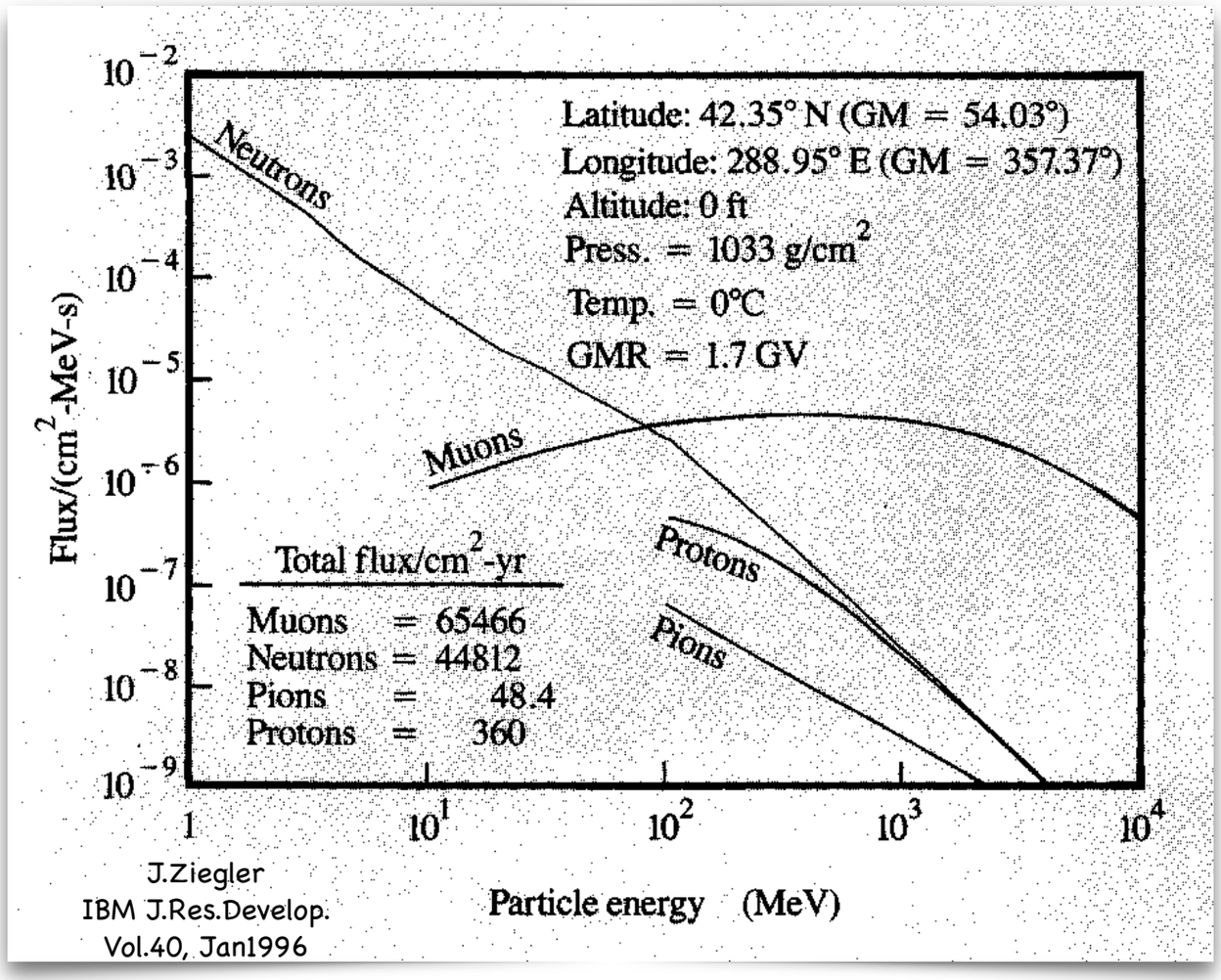
F.Faccio
CERN - EP/ESE

Where is radiation threatening ?





Damage from passengers collisions inside a Quantas Airbus A330 in October 2008. All potential causes for the failure of the plane's flight control system have been found unlikely, except for a radiation-induced error (SEU)



J.Ziegler
IBM J.Res.Develop.
Vol.40, Jan1996

Alpha radiation activity of some common materials utilized in microelectronic packages
(S.Kumar et al., Rev.Adv.Mater.Sci. 34(2013) 185-202)

Material	Alpha radiation flux (a/khr cm^2)
Processed wafers	0.9
Cu metal (thick)	1.9
Al metal (thick)	1.4
Mold compound	24 to < 2
Underfill	2 to 0.9
Pb solders	7200 to < 2
LC II Pb (HEM)	50 to 3
LC I Pb (HEM)	1000 to 130
Alloy 42 (Hitachi)	8
Au-plated alloy 42 (HEM)	4
Sn (HEM)	>1000 to <1
AlSiC (Lanxide)	215
LC6 Al (HEM)	8

Terrestrial

Single Event Upset at Ground Level

Eugene Normand, *Member, IEEE*
Boeing Defense & Space Group, Seattle, WA 98124-2499

Abstract
Ground level upsets have been observed in computer systems containing large amounts of random access memory (RAM). Atmospheric neutrons are most likely the major cau upsets based on measured data using the Weapons Research (WNR) neutron beam.

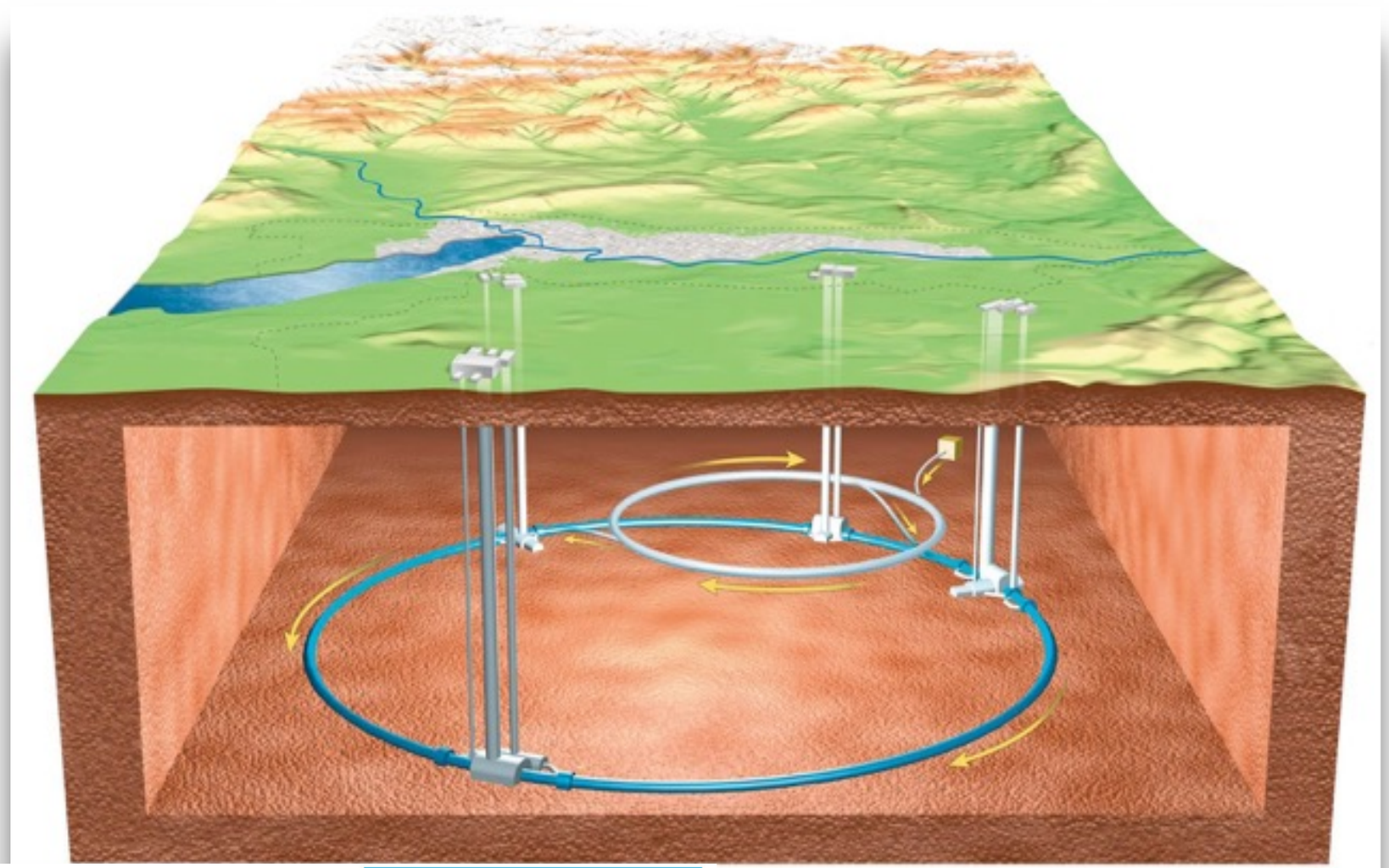
a sophisticated ground-based detector system made at 100, 5000 and 10,000 feet above sea level indicate that the 10-100 MeV flux falls off approximately linearly with altitude [8]

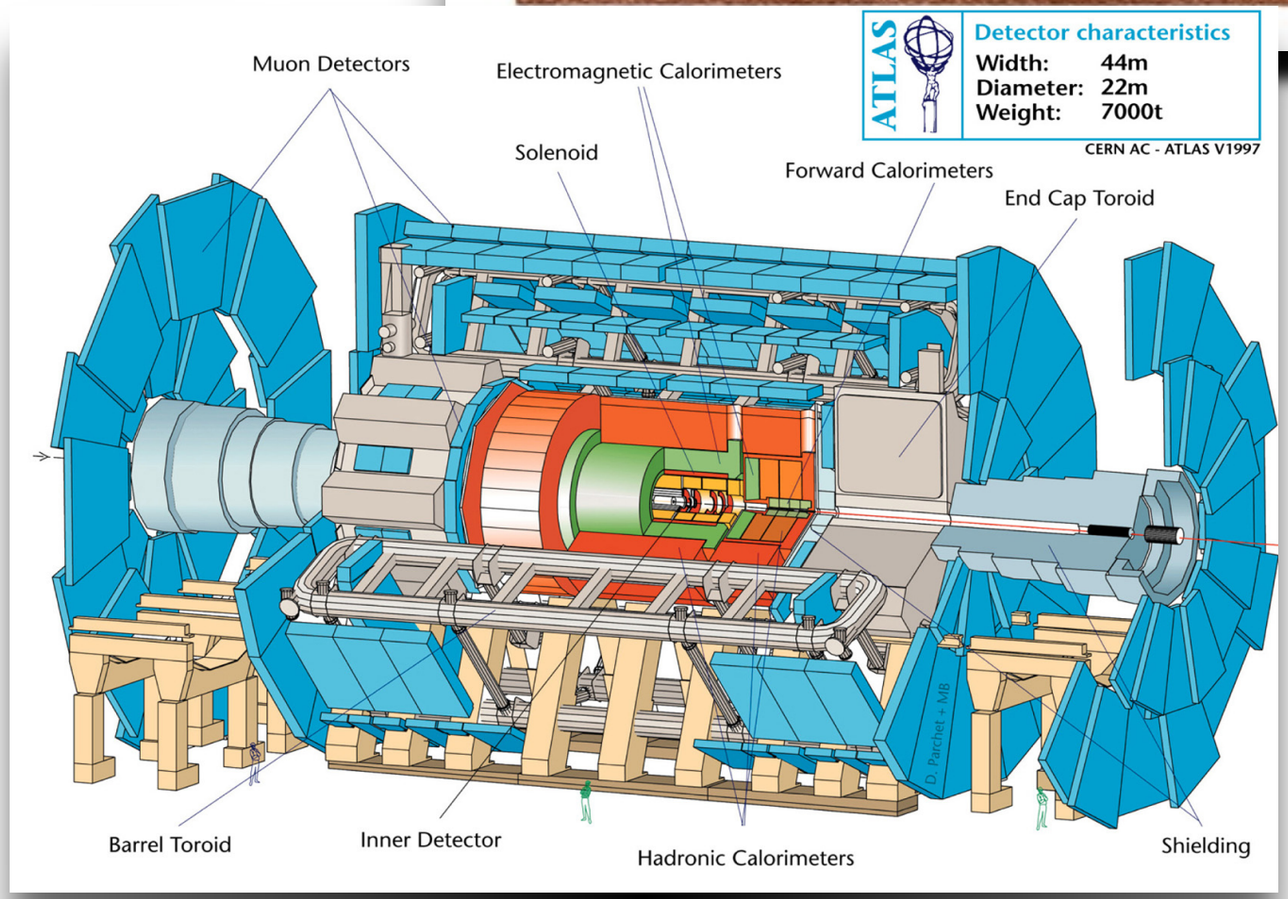
Single Event Upsets in Implantable Cardioverter Defibrillators

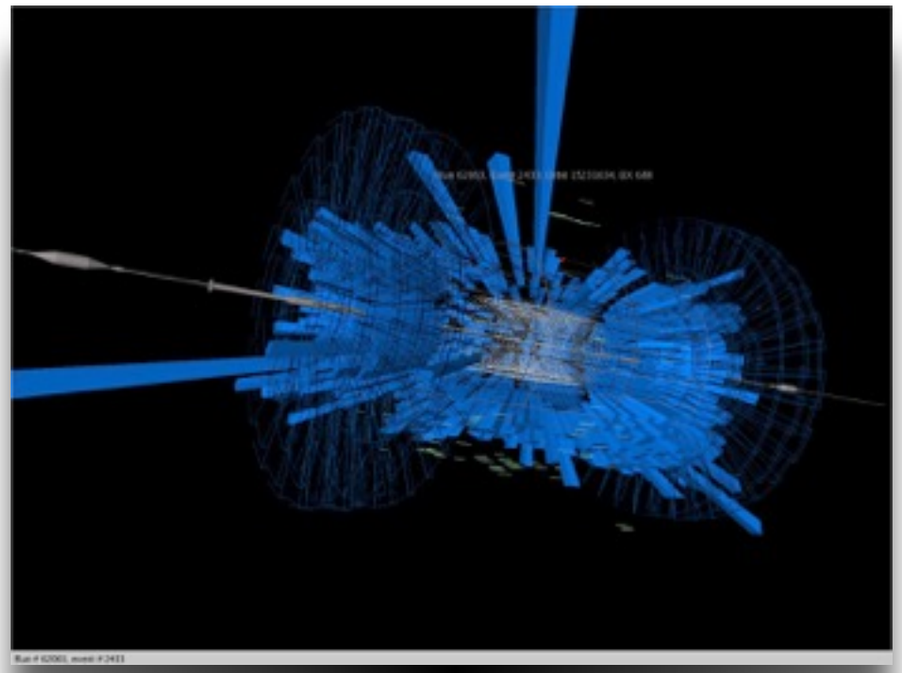
P.D. Bradley[1] and E. Normand[2]
[1] Department of Engineering Physics, University of Wollongong, 2522, Wollongong, Australia.
[2] Boeing Defense and Space Group, Seattle, WA 98124-2499 USA

Nuclear power

Military




Muon Detectors
Electromagnetic Calorimeters
Solenoid
Forward Calorimeters
End Cap Toroid
Barrel Toroid
Inner Detector
Hadronic Calorimeters
Shielding
ATLAS
Detector characteristics
Width: 44m
Diameter: 22m
Weight: 7000t
CERN AC - ATLAS V1997
D. Parchet + MB



How?

Single Event Effects

Traceable to the interaction of a single particle
Can lead to temporary or permanent failure

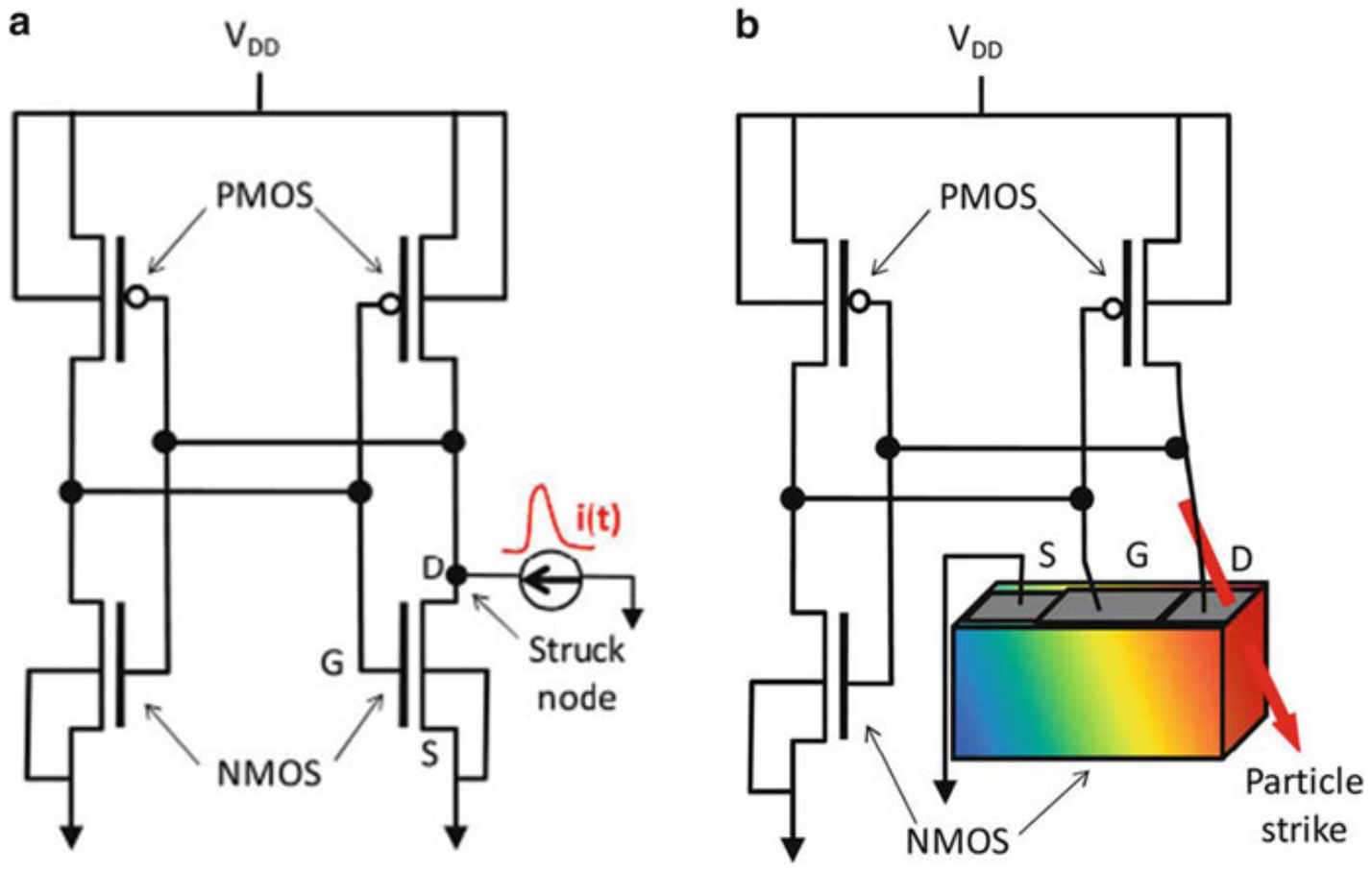
Total Ionising Dose

This is the ‘classical’ problem for CMOS technologies

Displacement Damage

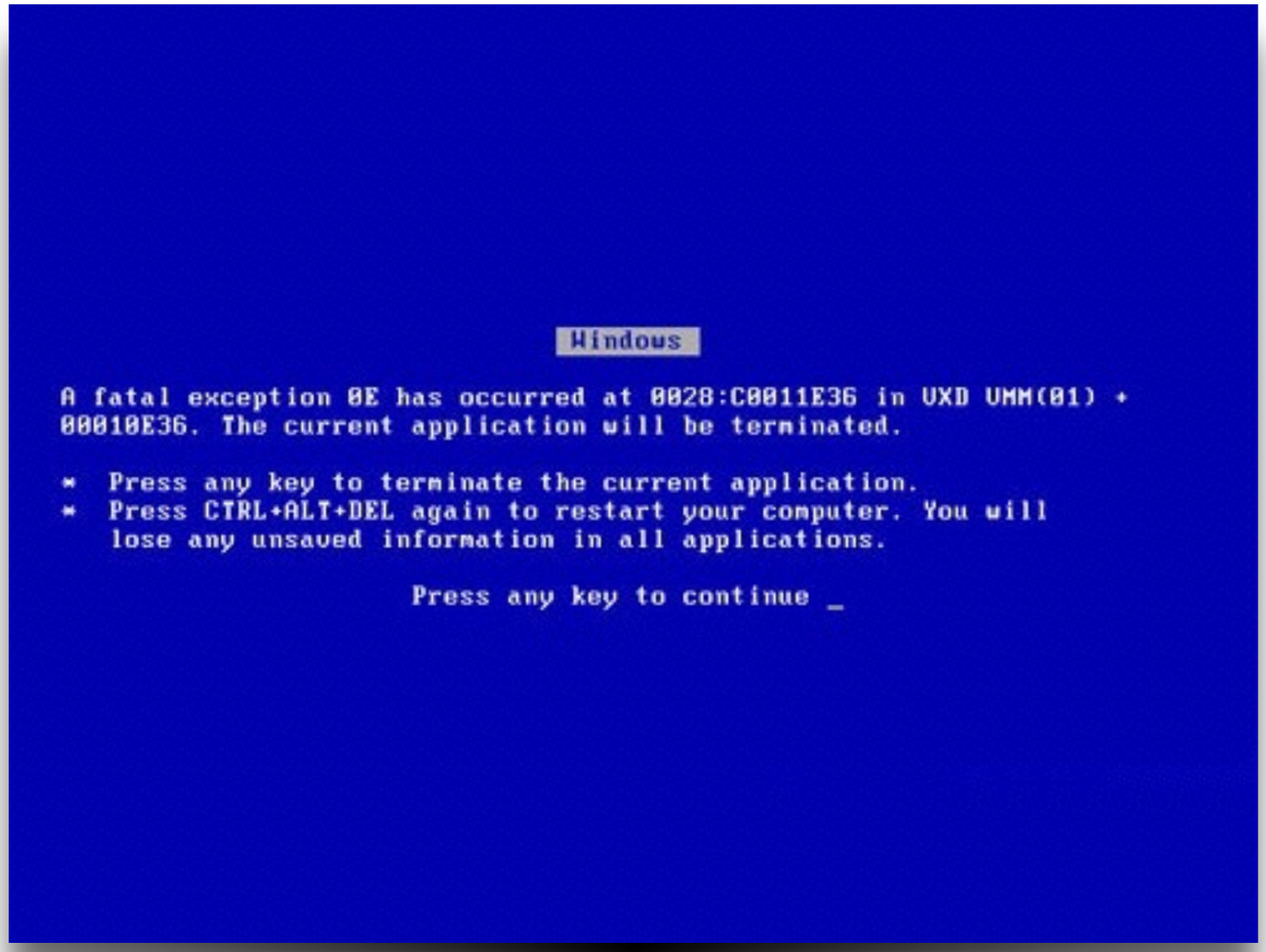
Only relevant for circuits using diodes or parasitic bipolar devices in CMOS

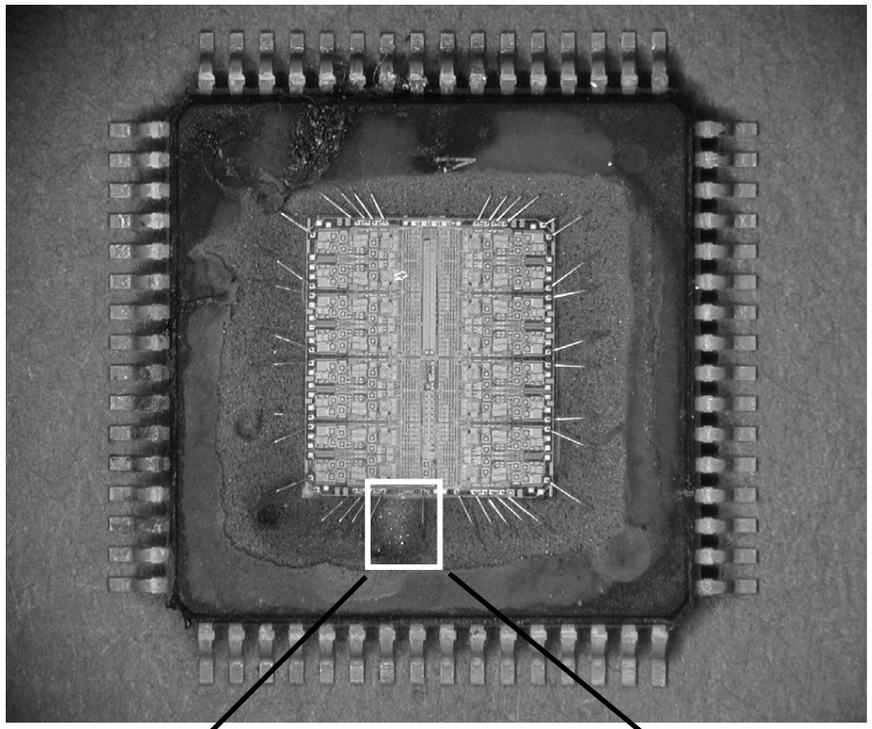
Single Event Upset (SEU)



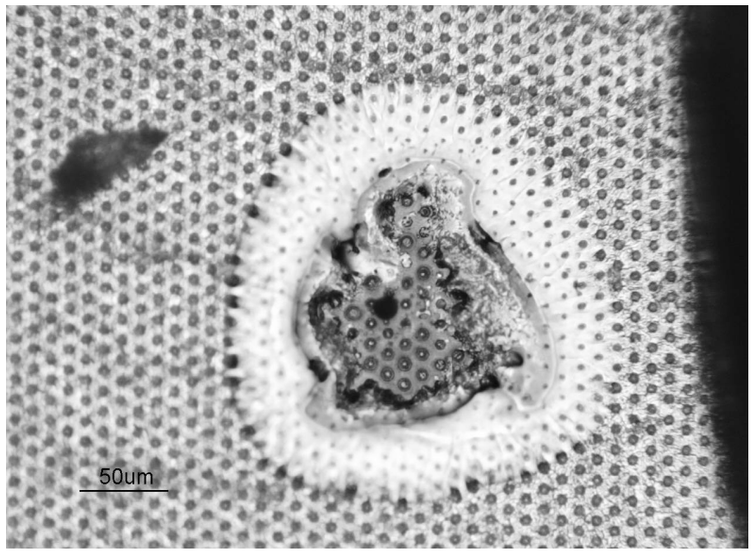
D. Munteanu, and J.-L. Autran, “Modeling and simulation of single-event effects in digital devices and ICs”, IEEE Trans. Nucl. Sci., vol. 55, no. 4, pp. 1854–1878, Aug. 2008

Single Event Functional Interrupt (SEFI)





Single Event Latchup (SEL) of a high voltage driver for MEMS (vaporized bond wires)



Single Event Burnout (SEB) of a power MOSFET

M.O'Bryan et al., "Current Single Event Effects and Radiation Damage Results for Candidate Spacecraft Electronics", NSREC Radiation Effects Data Workshop 2002

Single Event Effects

Traceable to the interaction of a single particle
Can lead to temporary or permanent failure

Total Ionising Dose

This is the ‘classical’ problem for CMOS technologies

Displacement Damage

Only relevant for circuits using diodes or parasitic bipolar devices in CMOS

TID levels in different applications

1rad 10rad 100rad 1krad 10krad 100krad 1Mrad 10Mrad 100Mrad 1Grad

LHC

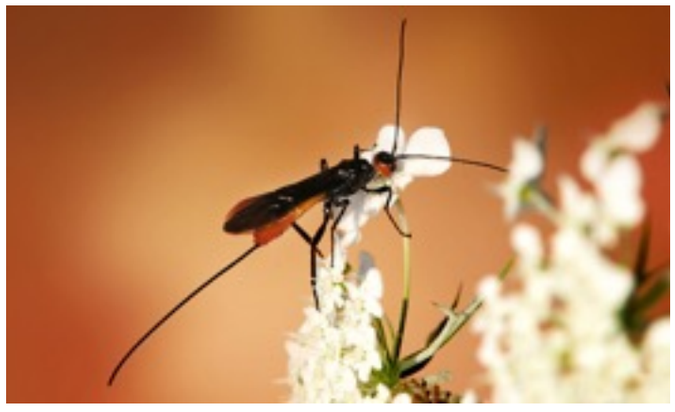
HL-LHC

satellites

deep space probes

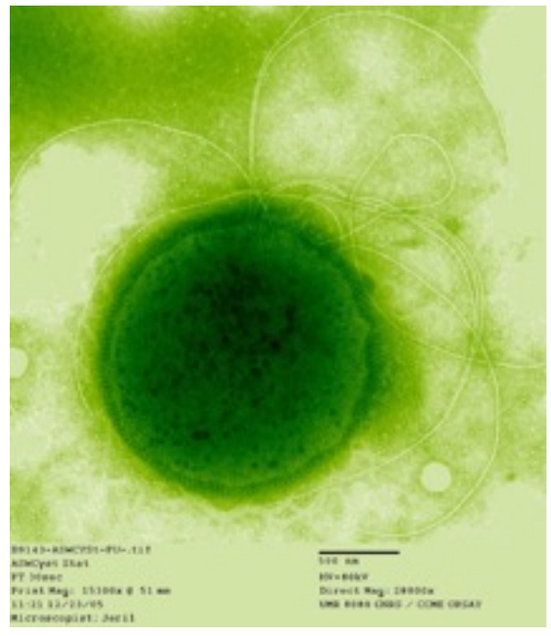
Homo Sapiens Sapiens (Mammals), 0.4-1krad

Braconidae (Insect), 180krad



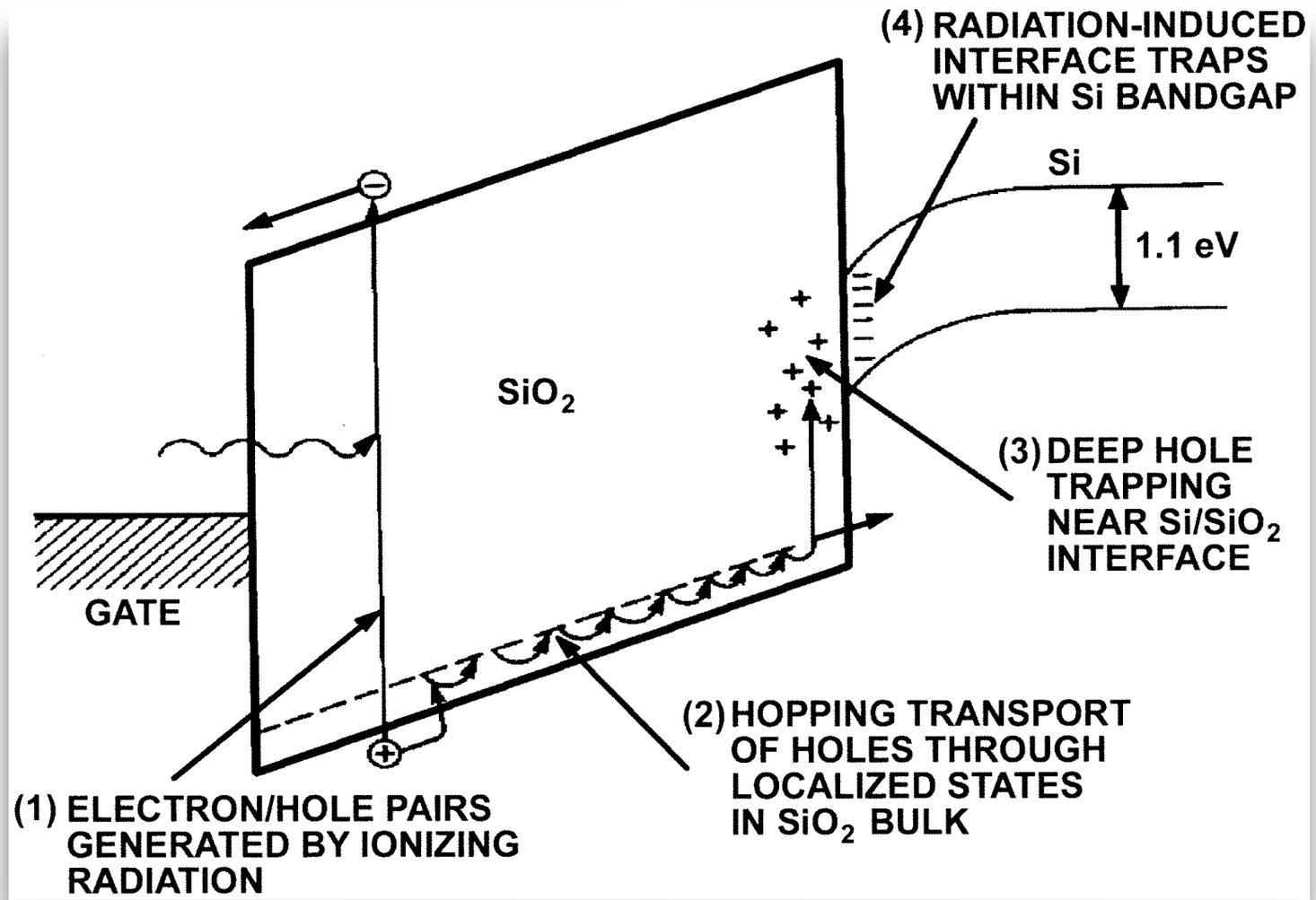
Deinococcus Radiodurans (Bacteria), 1.5Mrad

Thermococcus gammatolerans (Archaea), 3Mrad



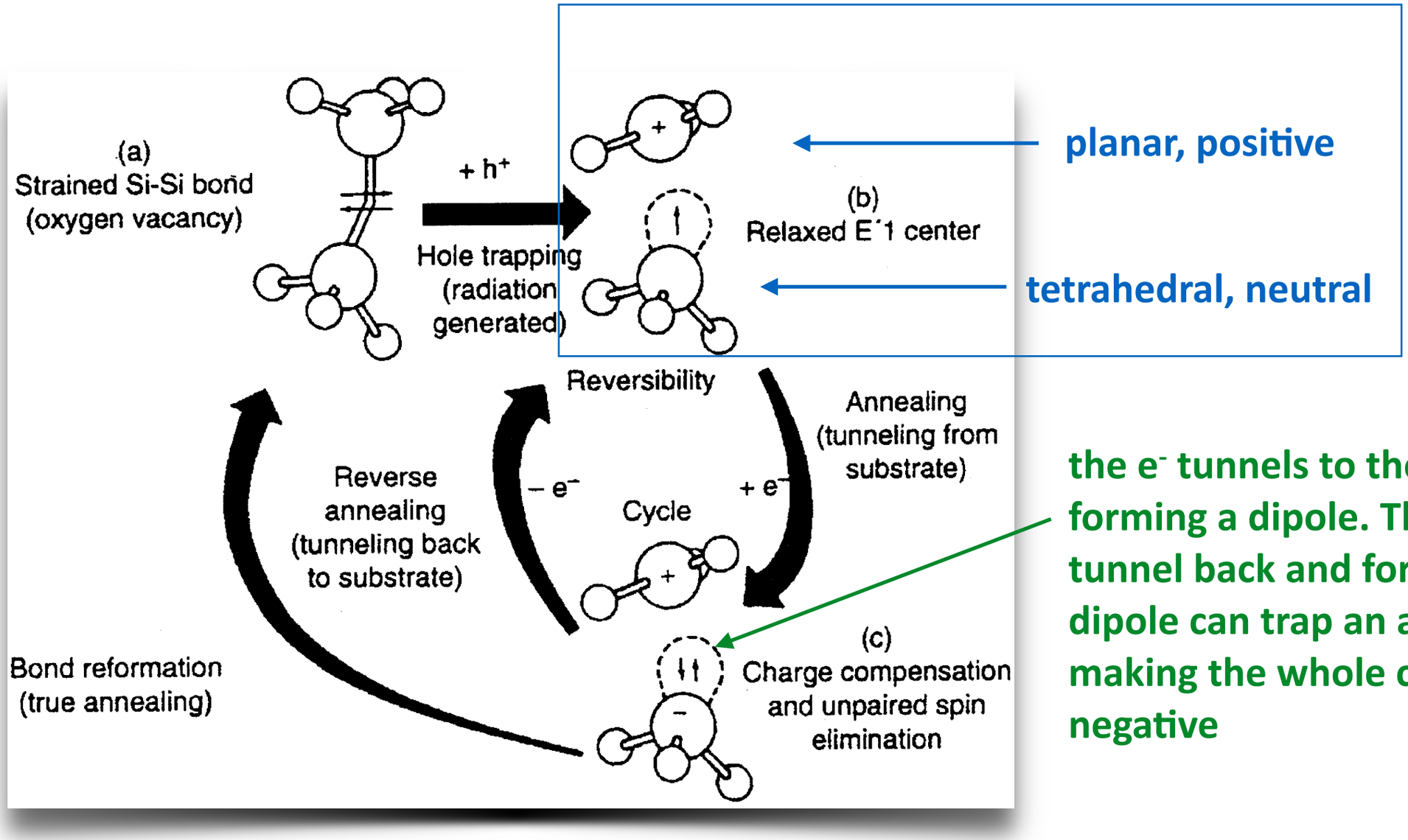
can be killed in 20minutes in our X-ray facility

The basis of TID effects in CMOS structures



T.R.Oldham and F.B.McLean, “Total Ionizing Dose Effects in MOS Oxides and Devices”, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 50, NO. 3, JUNE 2003

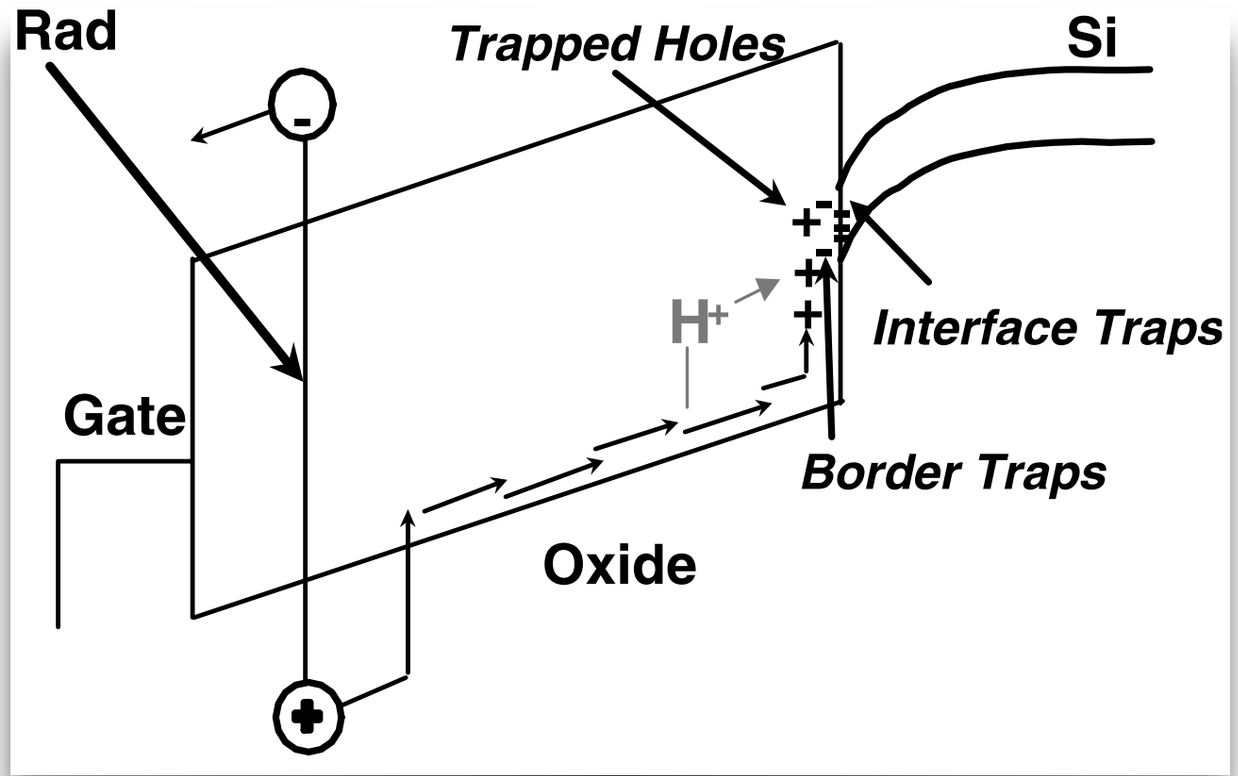
Deep hole trapping occurs at an oxygen vacancy site close to the interface



the e⁻ tunnels to the neutral Si, forming a dipole. The e⁻ can tunnel back and forth, and the dipole can trap an additional e⁻, making the whole complex negative

T.R.Oldham and F.B.McLean, "Total Ionizing Dose Effects in MOS Oxides and Devices", IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 50, NO. 3, JUNE 2003

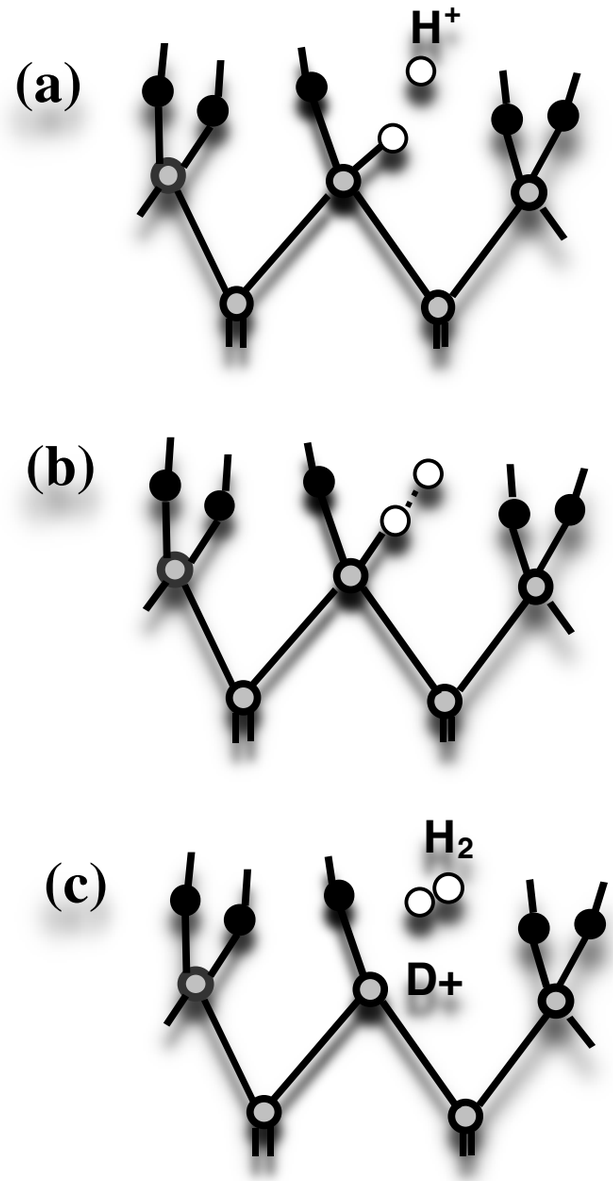
Interface traps require the migration of hydrogen to the interface. Their formation is known as a "two-stage" process.

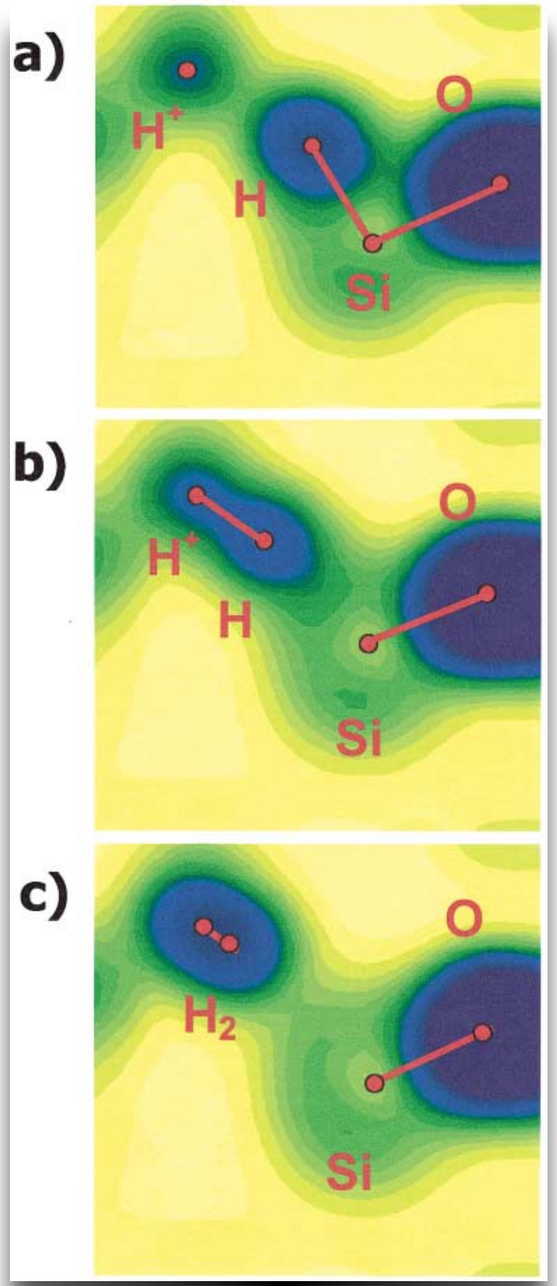


D.M.Fleetwood, "Effects of hydrogen transport and reactions on microelectronics radiation response and reliability ", Microelectronics Reliability 42 (2002) 523–541

The reaction of H^+ with the 'passivated' dangling bond at the interface leaves a charged Si atom that can exchange e^- with the silicon

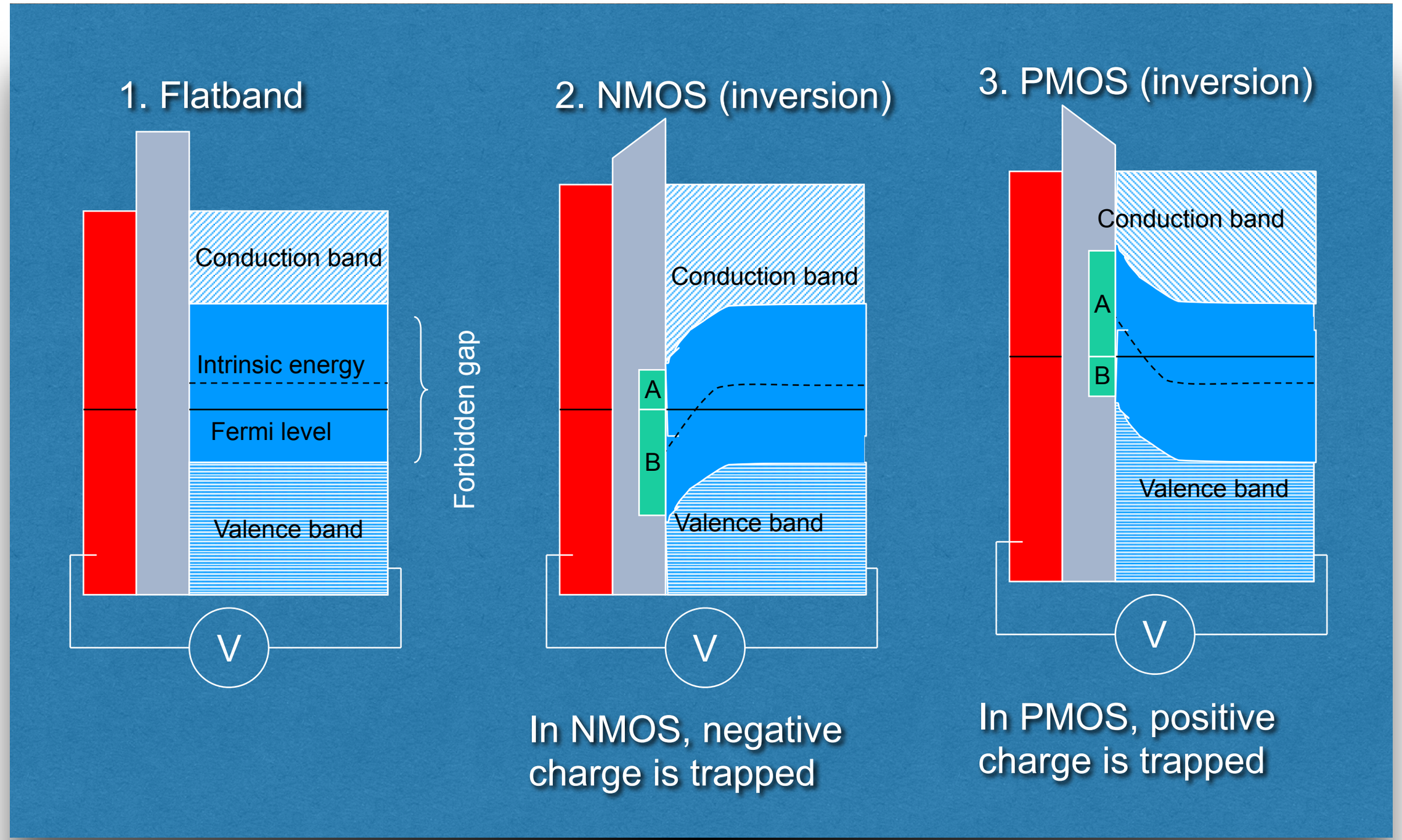
$$Si\text{-}H + H^+ \longrightarrow D^+ + H_2$$





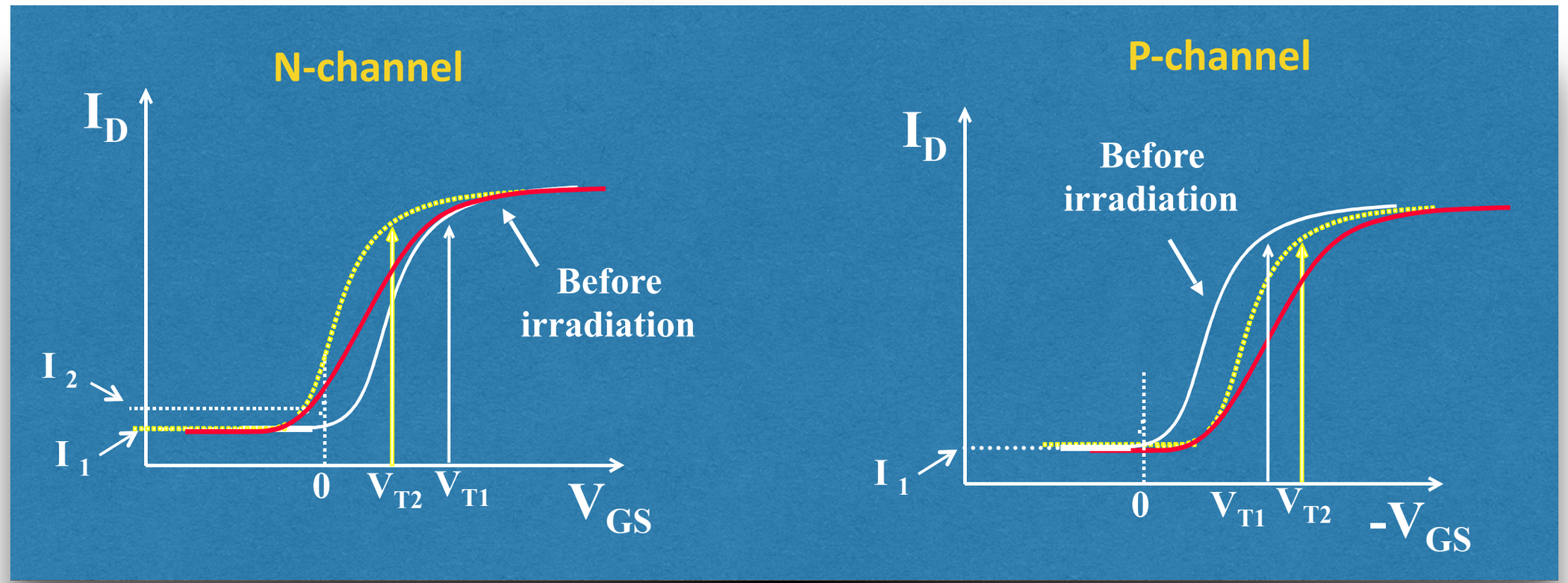
S.N.Rashkeev et al., "Defect generation by hydrogen at the Si-SiO2 interface", Phys.Rev.Lett., Vol.87,2001

Interface states are amphoteric: they can trap either electrons or holes depending on the Fermi energy at the interface



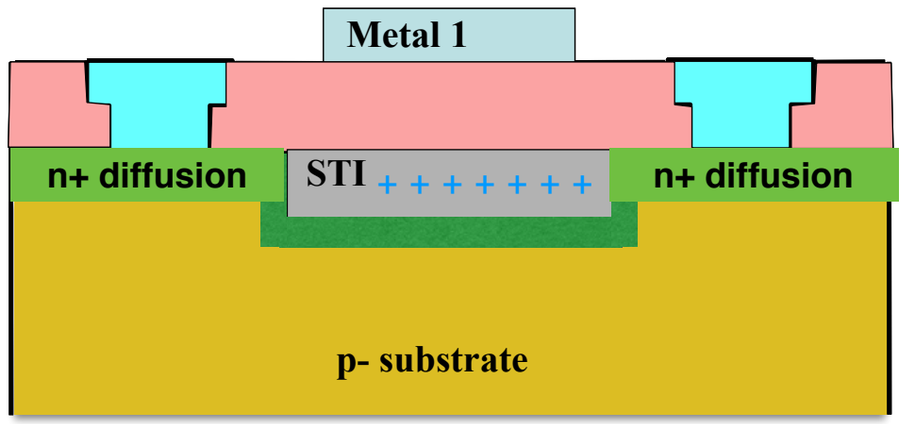
Result on the threshold voltage of MOS structures

	n-channel	p-channel
Oxide charges	+	+
Interface states	−	+

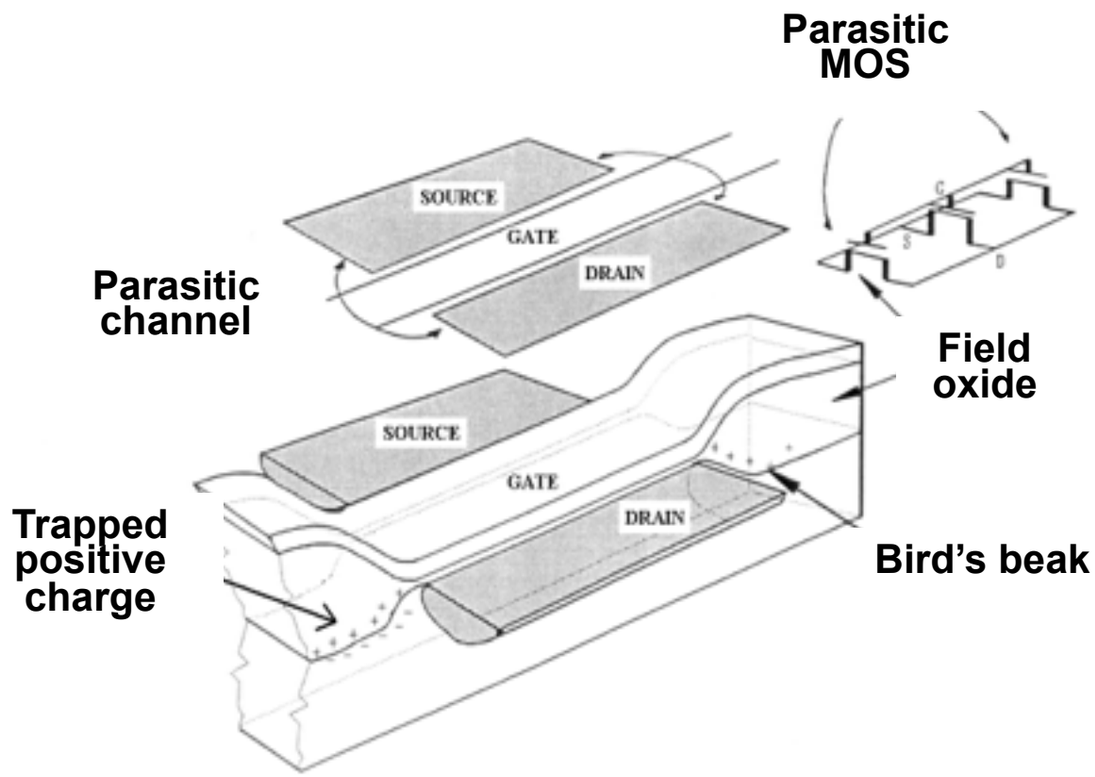


Charge buildup in the oxides and at their interface influences the electrical parameters of transistors (for the gate oxide) and of parasitic structures unavoidable in CMOS

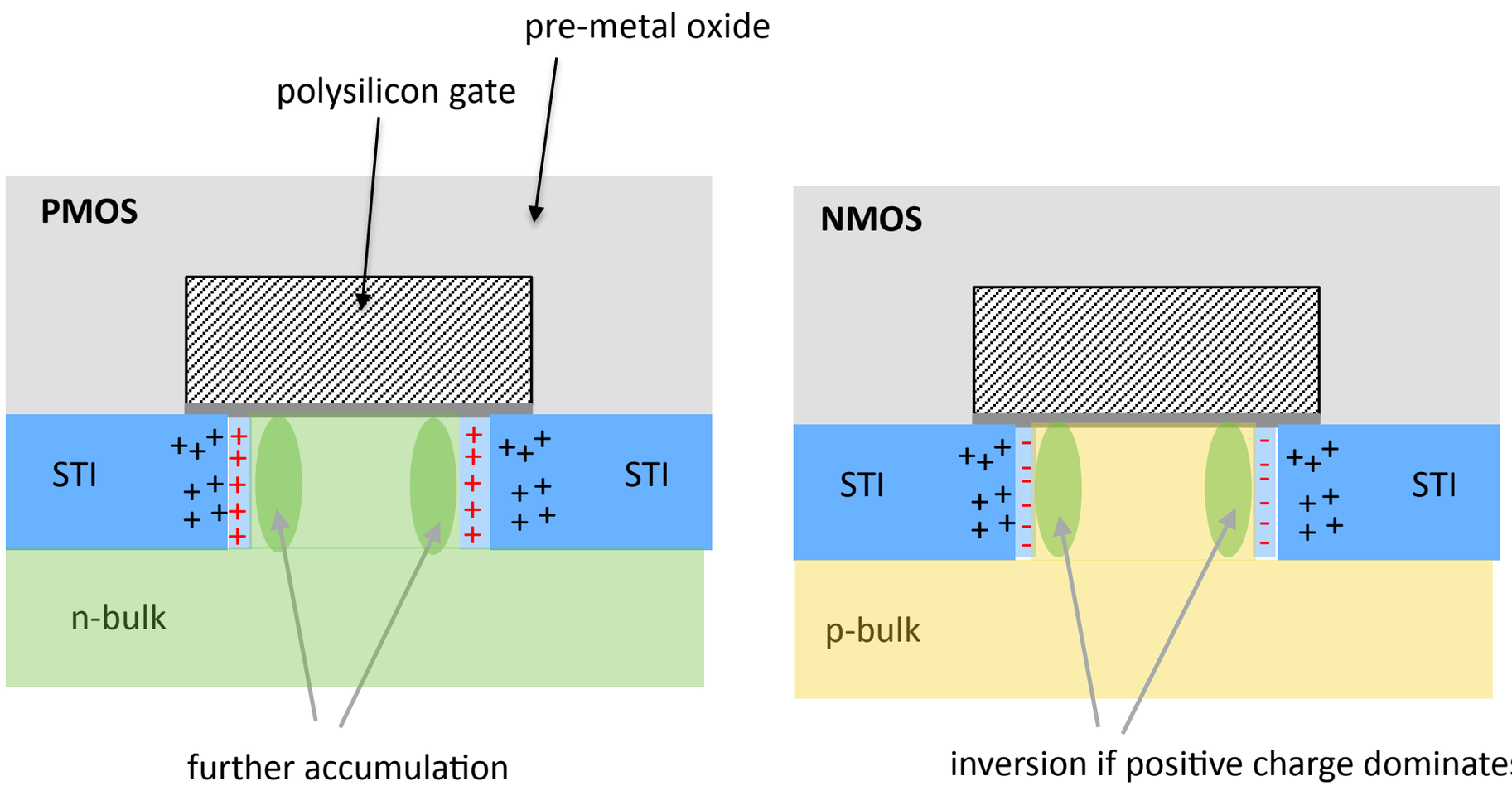
Leakage between adjacent n-diffusions



Source-Drain leakage in NMOS



Source-Drain leakage in NMOS is due to positive charge trapped in the bulk of the STI oxide

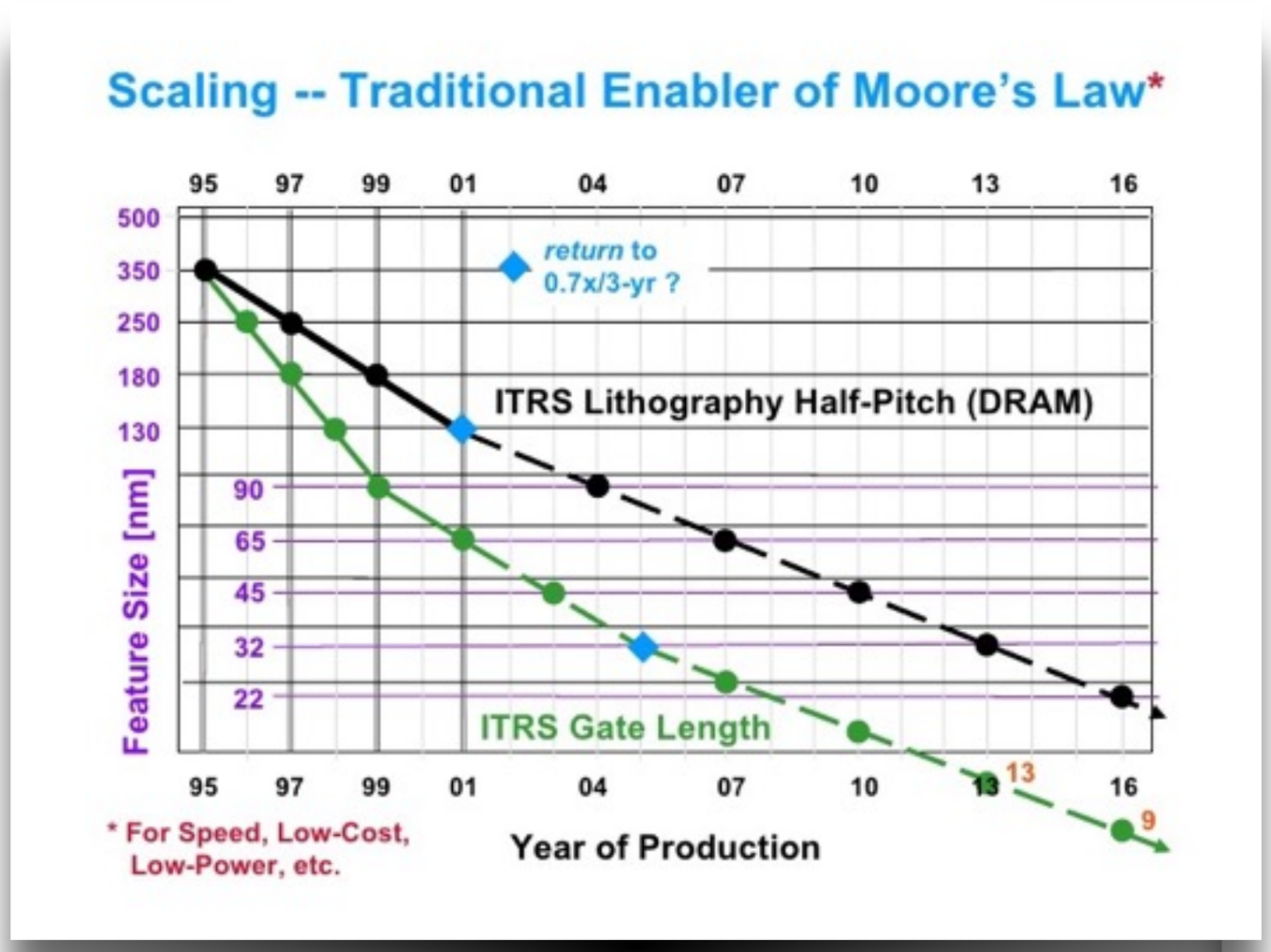


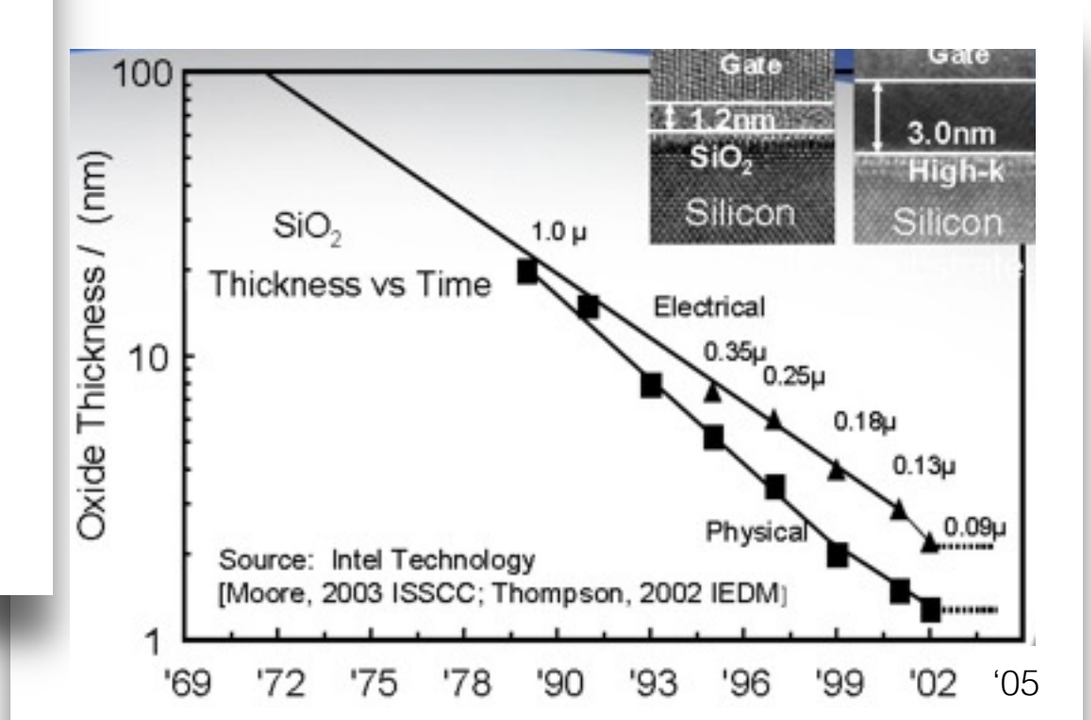
Radiation-hard processes

low volume (yield)
very high cost
far from state-of-the-art
dependence on single source

Episode IV:
A New Hope

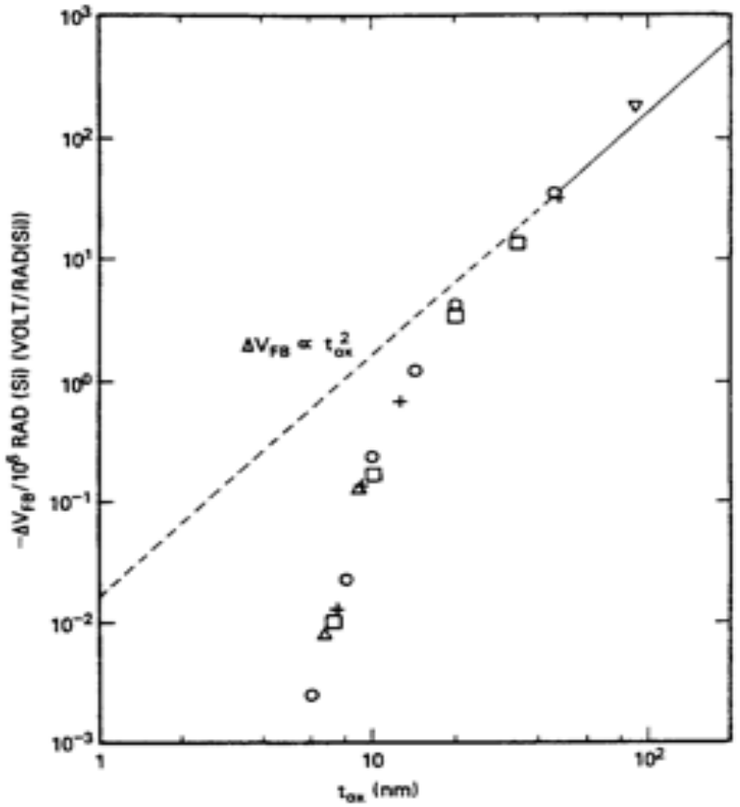
The gate oxide thickness scales in each technology node (up to a point)



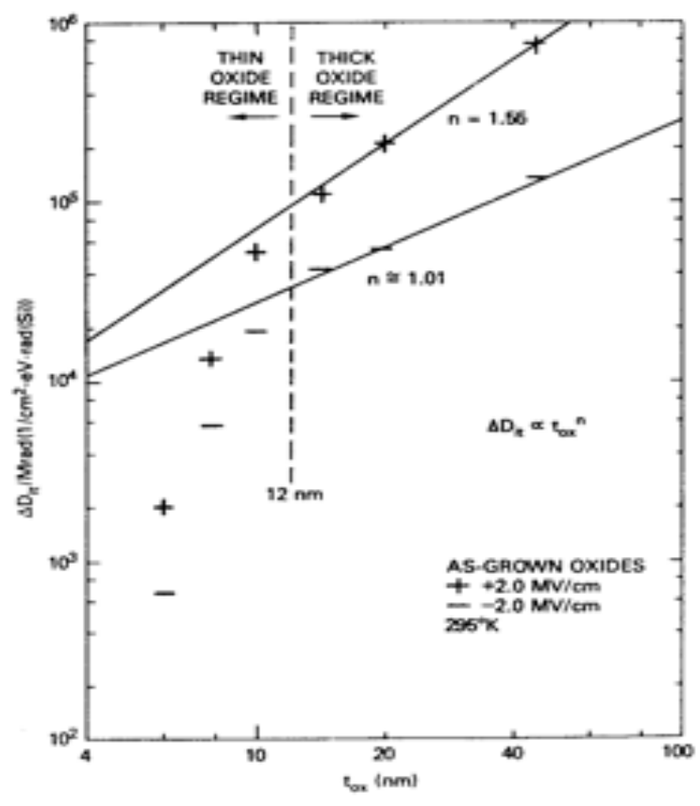


The accumulation of TID-inducd ‘defects’ in an oxide decreases with the thickness of the oxide

Oxide trapped charge



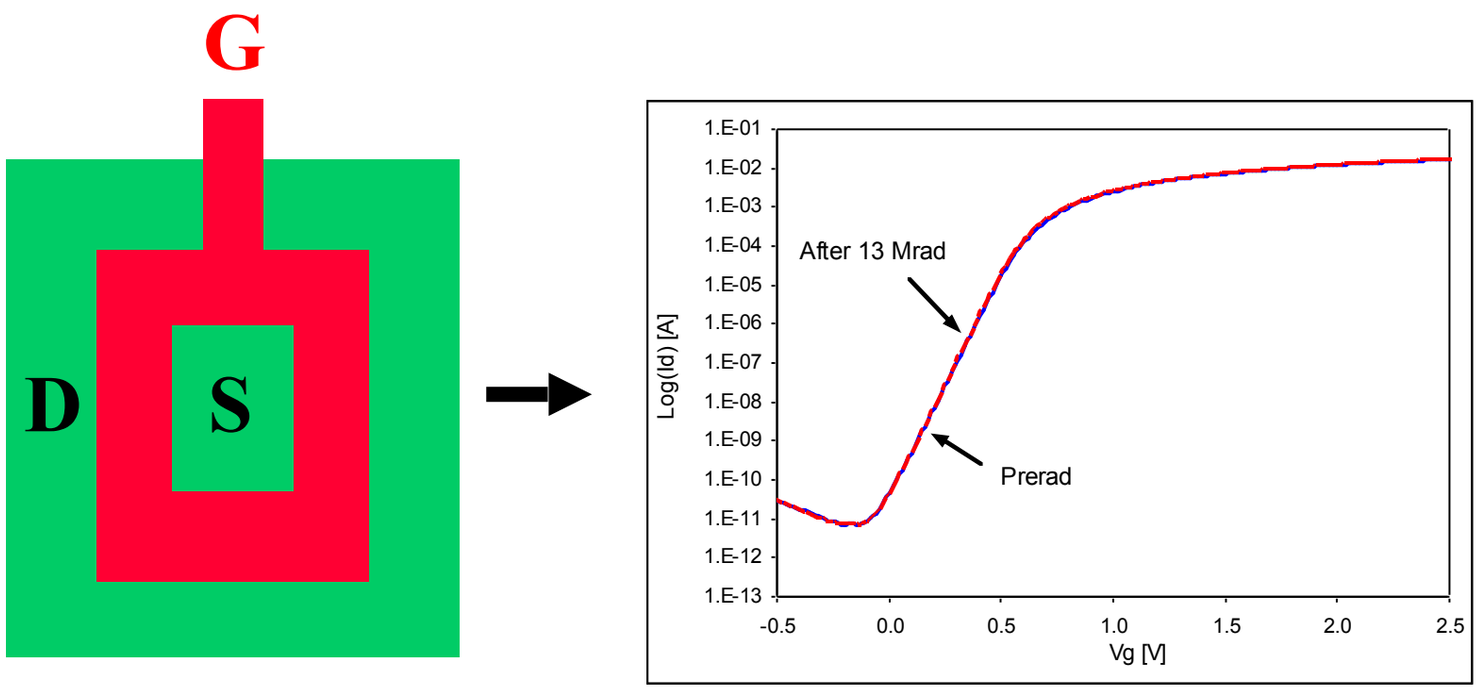
Interface states



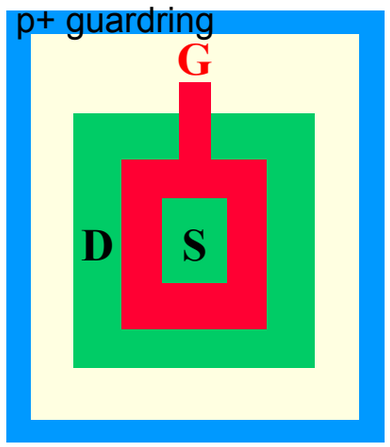
N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

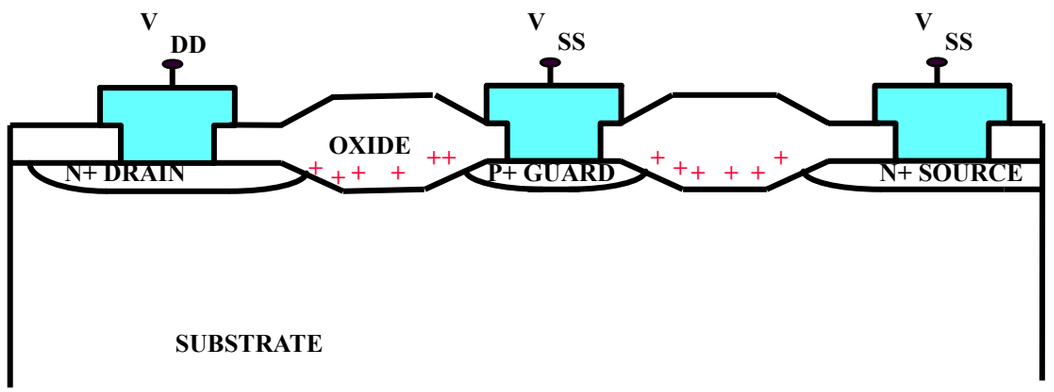
If the gate oxide is sufficiently thin, problems arise in the parasitic structures where the oxide thickness does not follow any scaling rule

Source-Drain leakage is eliminated by the Enclosed Layout Transistor (ELT)…



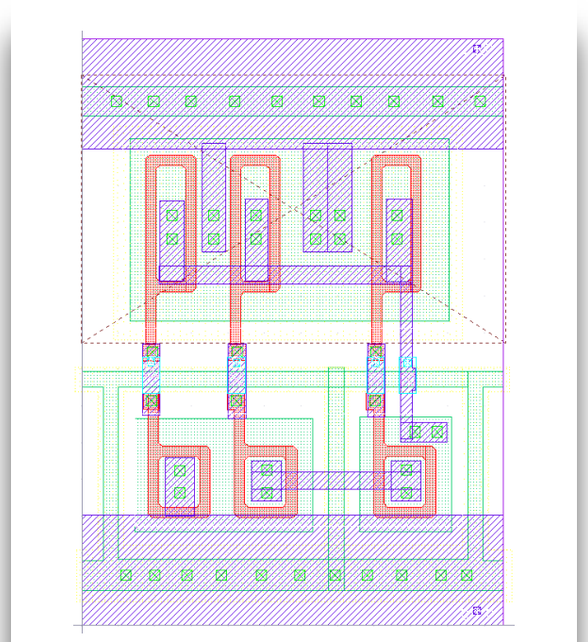
Inter-diffusion leakage is eliminated by p+ guard rings…

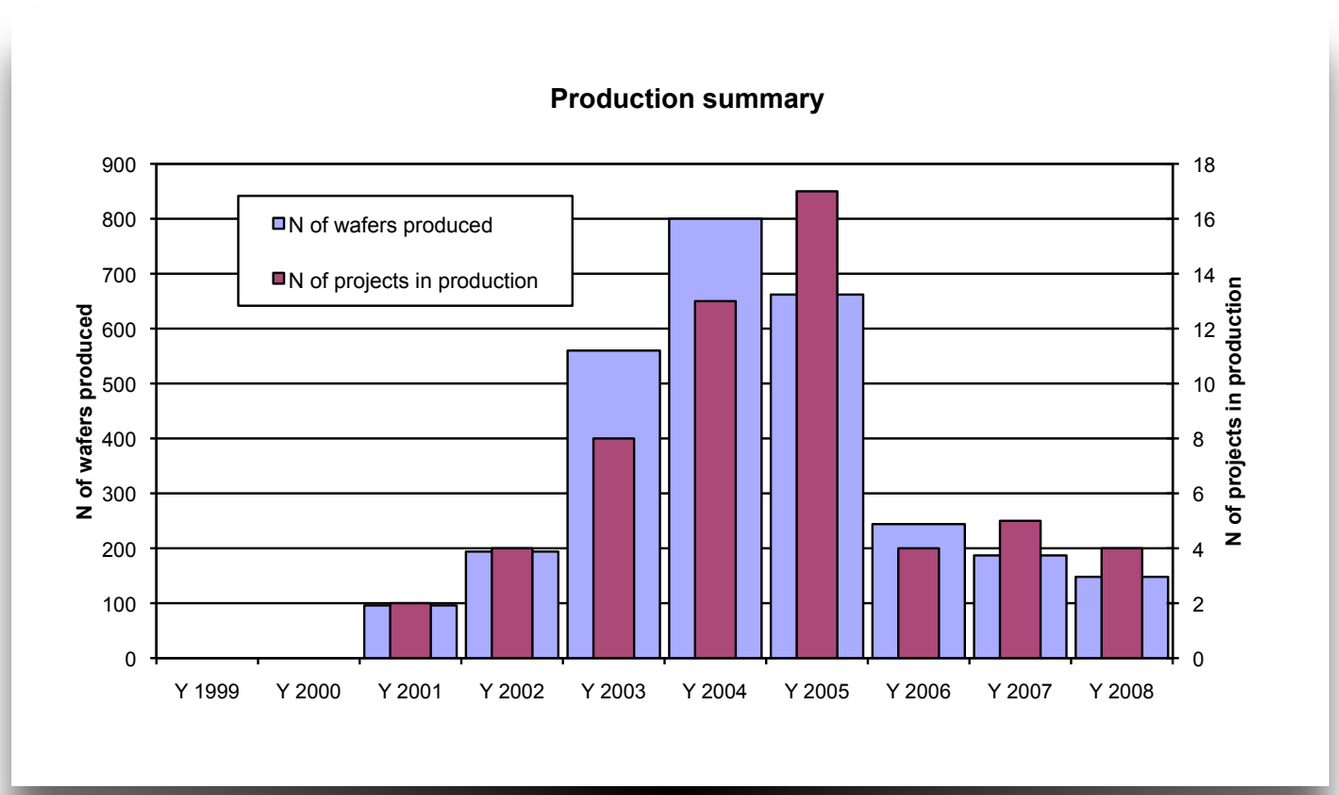




The equation used for the design of ASICs used in today's LHC experiments and manufactured in an (affordable) commercial-grade 0.25um process is:

Thin gate oxide + HBD techniques = Radiation tolerance





ELT was not such an original idea in the ‘90s…

C²L: A New High-Speed High-Density Bulk CMOS Technology

ANDREW G. F. DINGWALL, MEMBER, IEEE, AND ROGER E. STRICKER

Abstract—C^2L, or *c*losed *C*OS/MOS *l*ogic, is a new structural approach to high-speed bulk-silicon COS/MOS logic. C^2L is a self-aligned silicon-gate CMOS Technology where the gate completely surrounds the drain. The use of such geometry maximizes the transconductance to capacitance ratio for devices and thus allows high on-chip speed. The CDP 1802 single-chip 8-bit microprocessor, as well as several memory and I/O circuits announced recently by the RCA Solid State Division, are fabricated in this new technology.

Generally, C^2L devices show an improvement in packing density by a factor of 3 over standard CMOS and operate at frequencies approximately 4 times faster than standard CMOS. The fabrication sequence for C^2L devices requires 6 photomasks (one less than standard CMOS).

INTRODUCTION

RCA Corporation recently introduced C^2L, or *c*losed *C*OS/MOS *l*ogic, devices into its commercial CMOS logic family. This new structural form of CMOS devices offers several advantageous design features. C^2L is a self-aligned silicon-gate technology which can approach the maximum speed performance possible for bulk-silicon CMOS devices. It has high packing density, and a simple processing sequence with fewer photomasking and processing steps. These have contributed to excellent yield performance. Since the entire C^2L chip surface is heavily doped either p+ or n+, potential reliability problems due to unwanted surface inversion effects are eliminated. Further, the closed structures circumvent the need to guardband individual MOS transistors, thus achieving low parasitic leakage over a 3–15 V operation range. Such performance characteristics have been demonstrated in

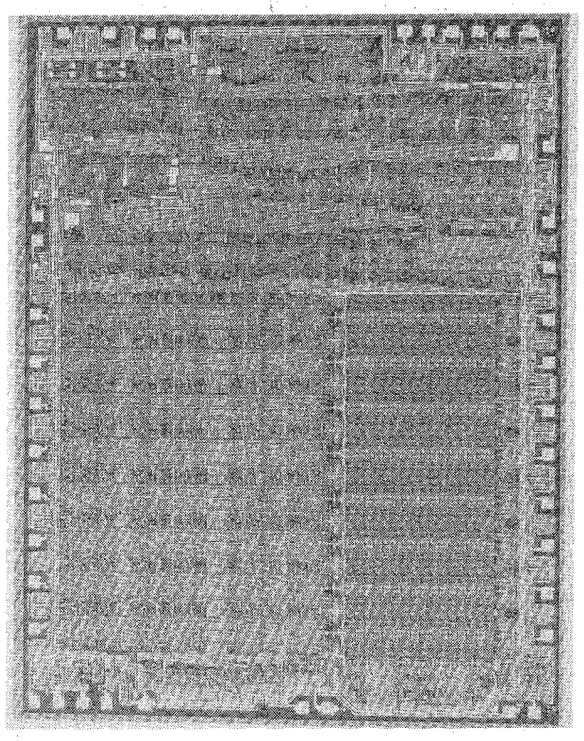


Fig. 1. Microphotograph of CDP 1802 C^2L 8-bit microprocessor (178 × 234 mil²).

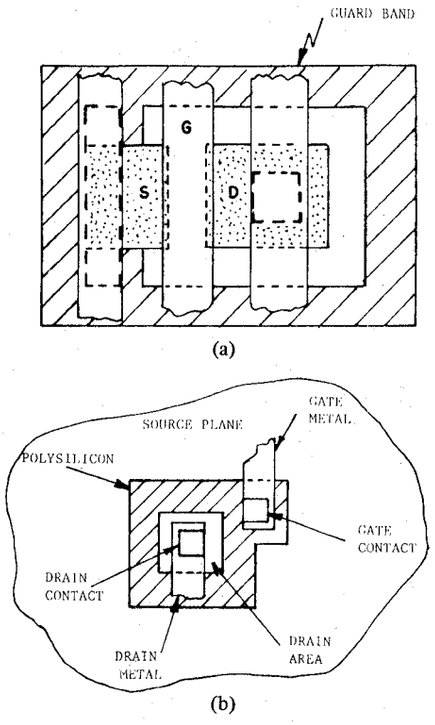
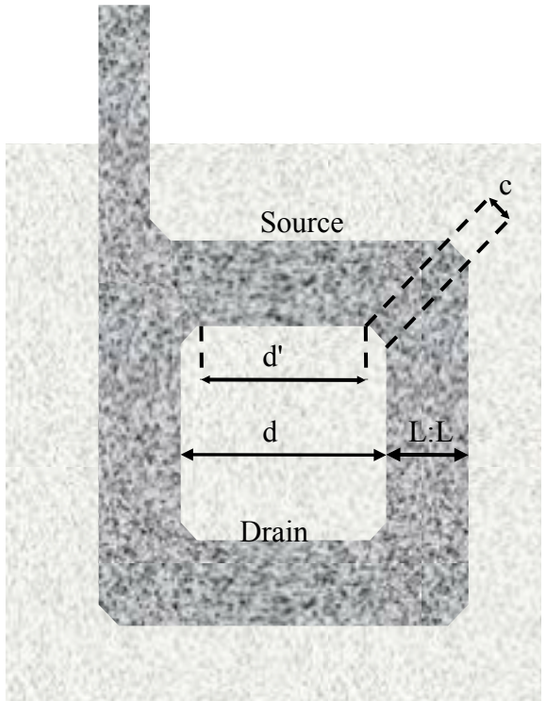


Fig. 2. Comparison of standard Al-gate CMOS and C^2L transistors.

Enclosed layout!



No precise model

Lack of commercial library

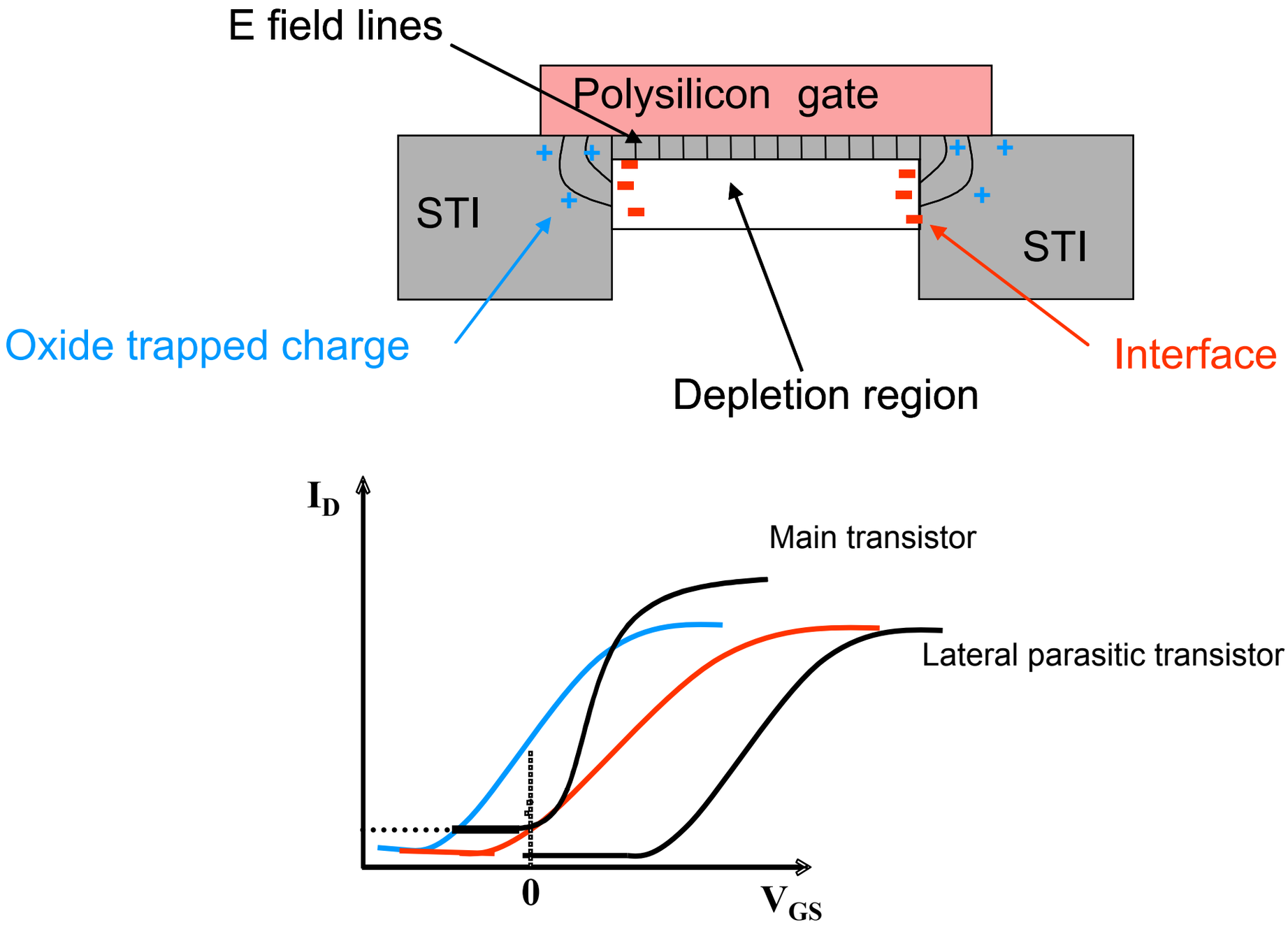
Size constraints

Larger area and capacitance

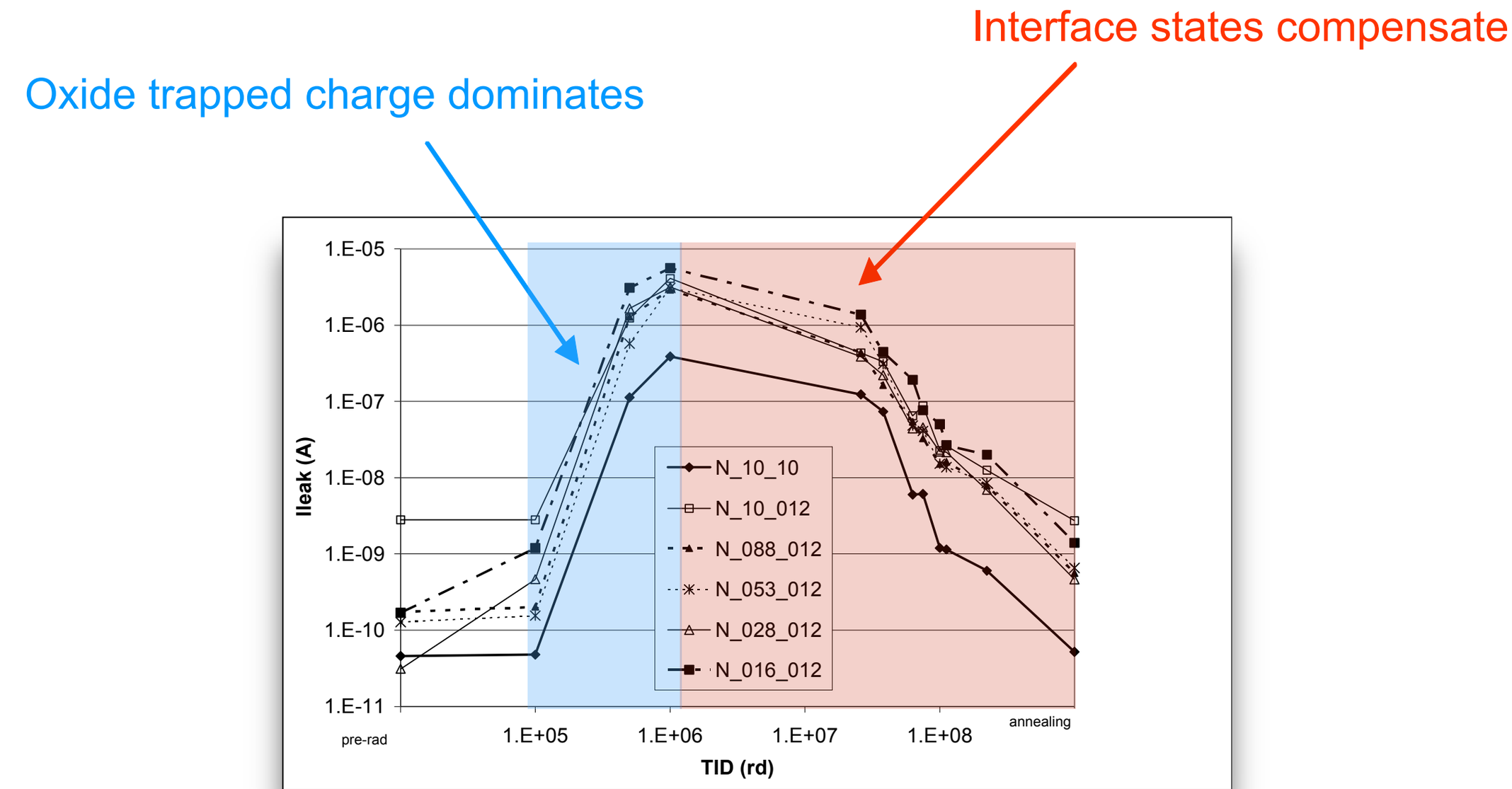
Is the systematic use of ELT transistors really needed?

Is the answer to this question dependent on the technology node and process?

The time evolution of the two types of defects in the STI oxide is different: interface states activation is requires H^+ migration, which is a slow process



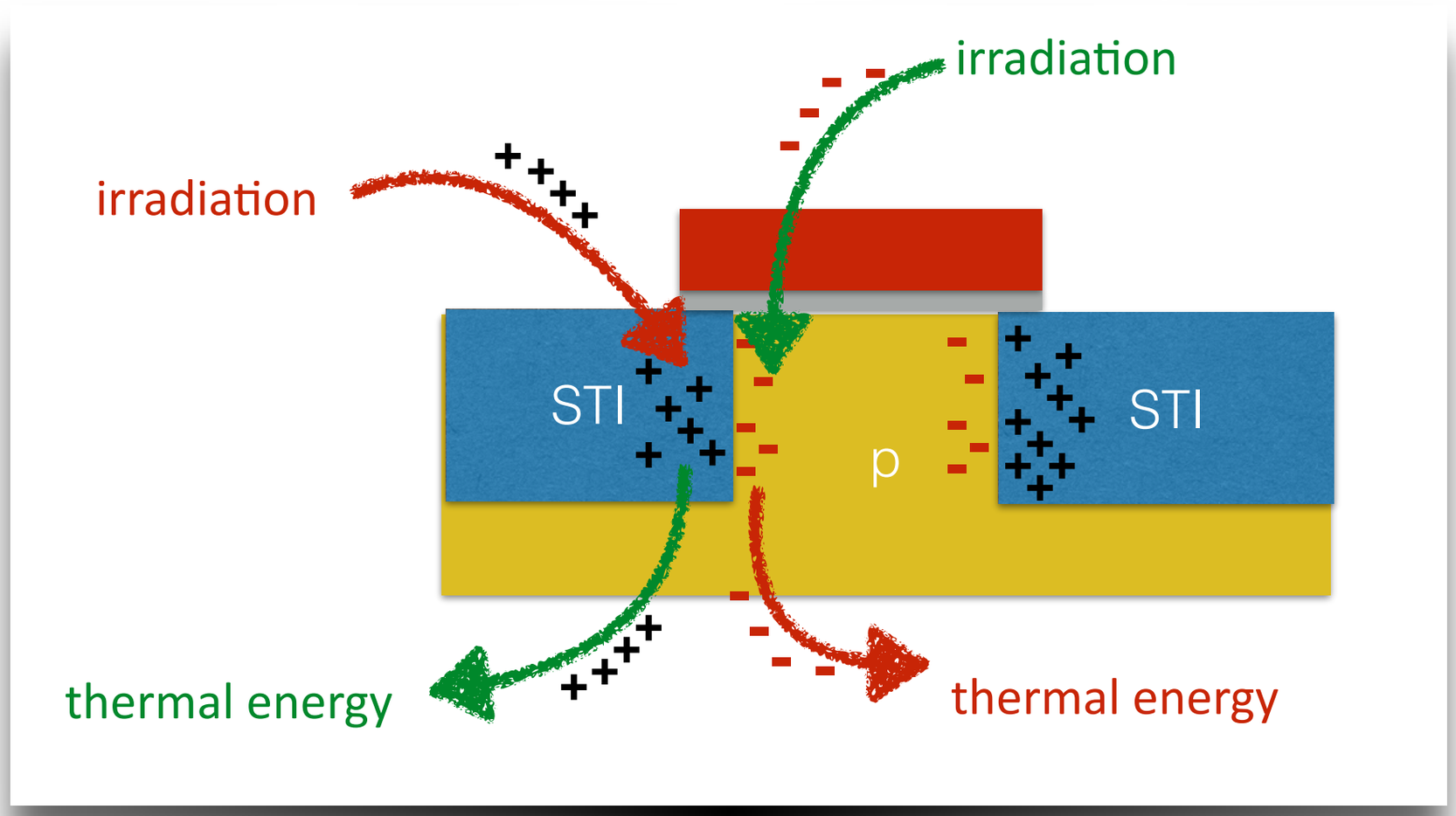
The typical result for a ‘fast’ irradiation (high dose rate):



The leakage current is the sum of different mechanisms involving:

- **the creation/trapping of charge (by radiation)**
- **its passivation/de-trapping (by thermal excitation)**

These phenomena are Dose Rate and Temperature dependent!

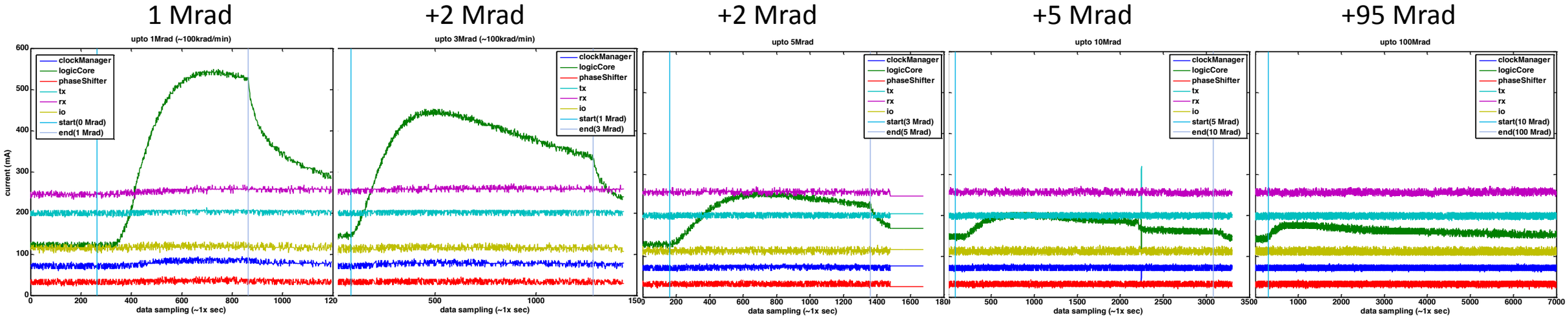


The properties of the defects (hole traps, interface states) have been studied in these two publications:

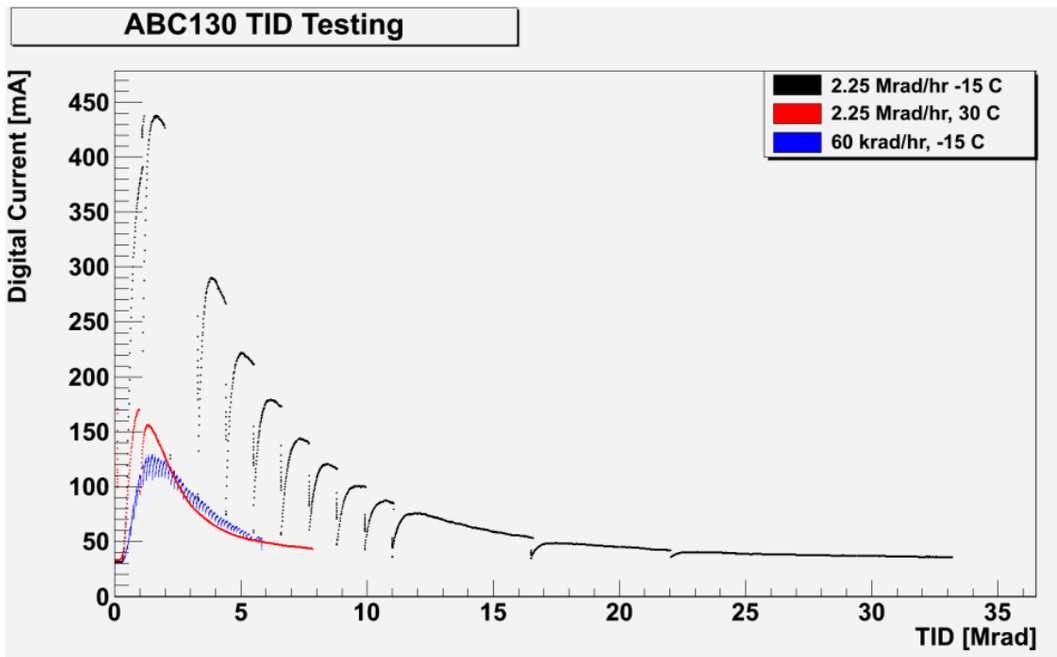
- F.Faccio, G.Cervelli, “Radiation-induced edge effects in deep submicron CMOS transistors”, IEEE Trans. Nucl. Science, Vol.52, No.6, December 2005, pp.2413-2420
- F.Faccio et al., “Total ionizing dose effects in shallow trench isolation oxides”, Microelectronics Reliability 48 (2008) 1000-1007

The leakage increase is visible in complex logic ASICs developed in this technology

Logic core current consumption in the GBTx at room T: green curve (courtesy P.Moreira and GBT Team)

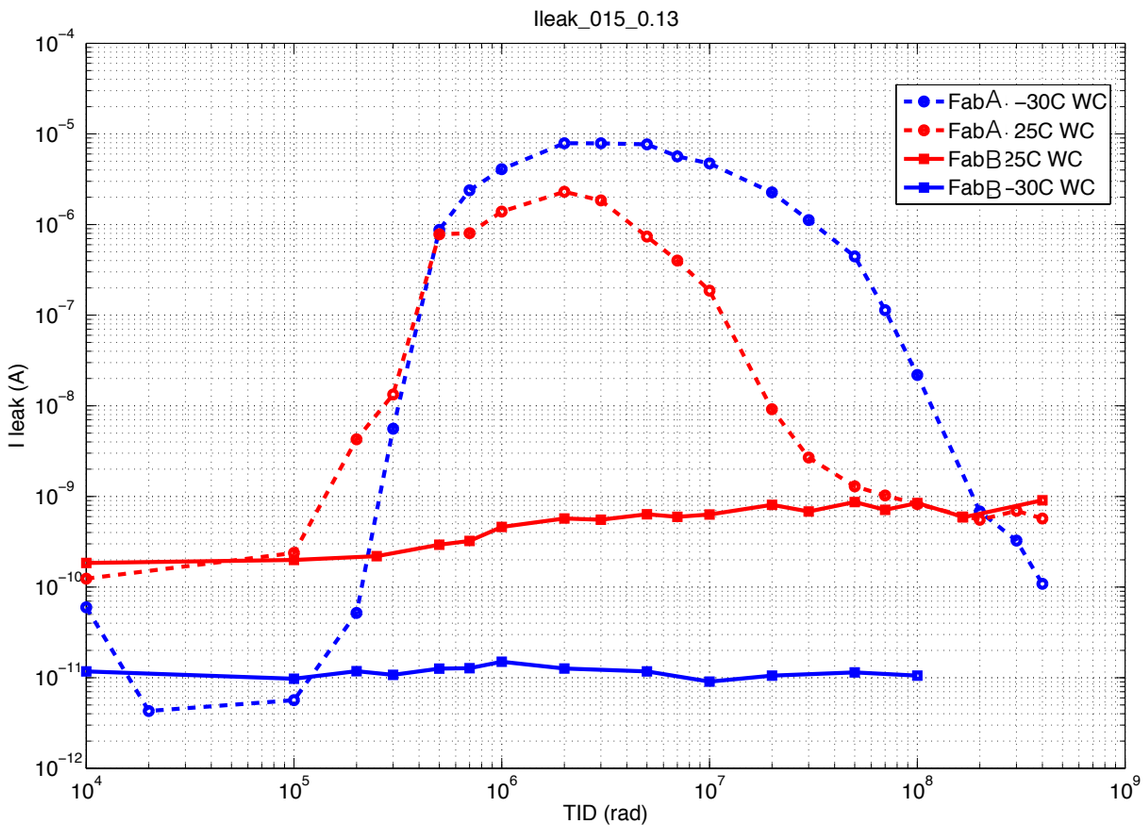


Logic core current consumption of the ABC130 at different T and dose rates (courtesy F.Anghinolfi and ABC130 Team)



The leakage increase depends on processing details beyond (our) control, that can be changed without warning

Leakage in 0.15/0.12um MOS
Same manufacturer
2 different Fabs



Recap in 250-130nm

Technology downscaling has endowed transistors with TID-tolerant gate oxides.

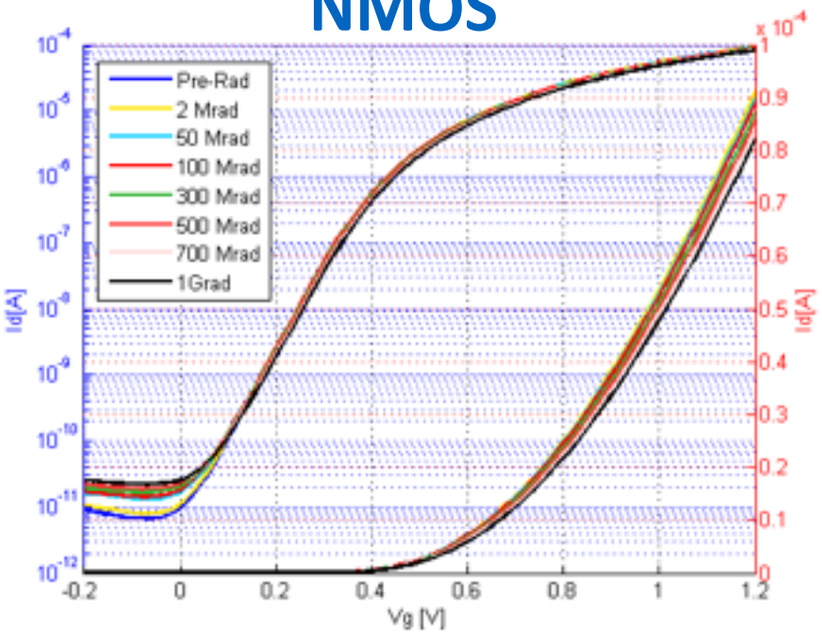
Leakage currents in parasitic structures (NMOS source-drain, adjacent n-doped diffusions) is dependent on balancing of charges in interface states and traps in the bulk of the STI oxide.
We found 130nm technologies where ELTs and guarding were not needed to achieve multi-Mrad tolerance…

Episode V:
Radiation Strikes Back (in 65nm CMOS)

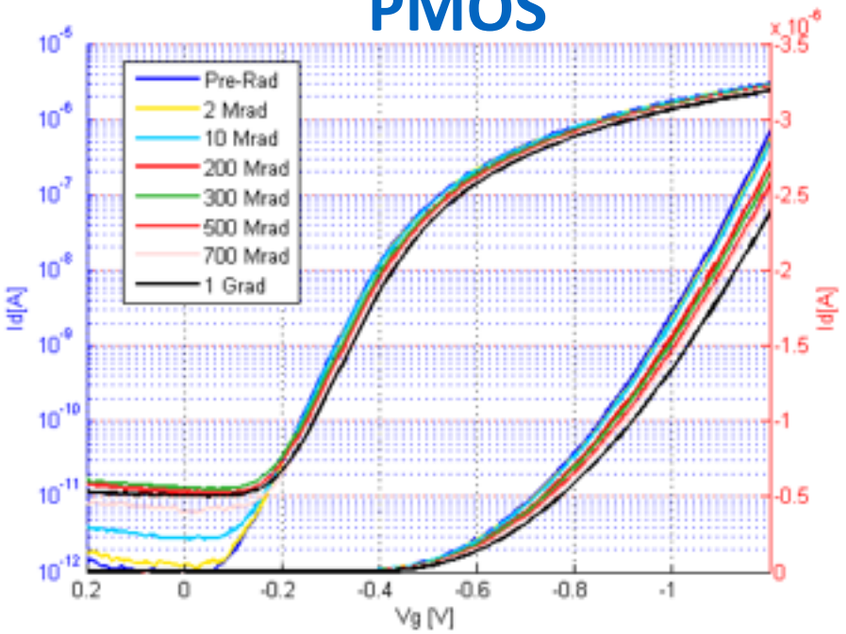
There will be no further comment about leakage currents, because we did not measure significant currents (for typical applications) in either NMOS transistors or FOXFETs

The degradation of long and large transistors is limited:
the thin gate oxide is radiation hard!

NMOS



PMOS

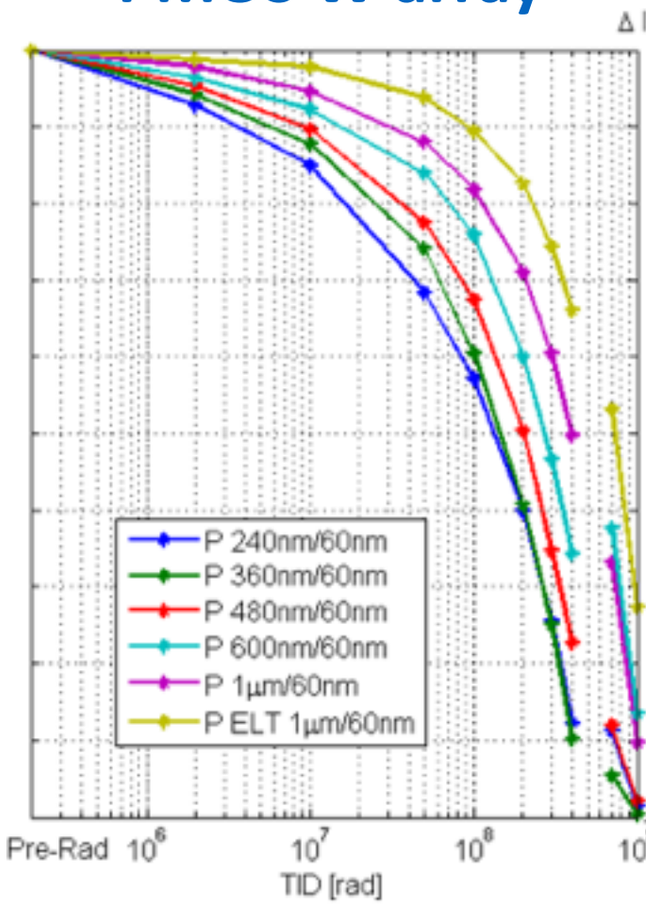


Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V
Curves Id-Vg in saturation

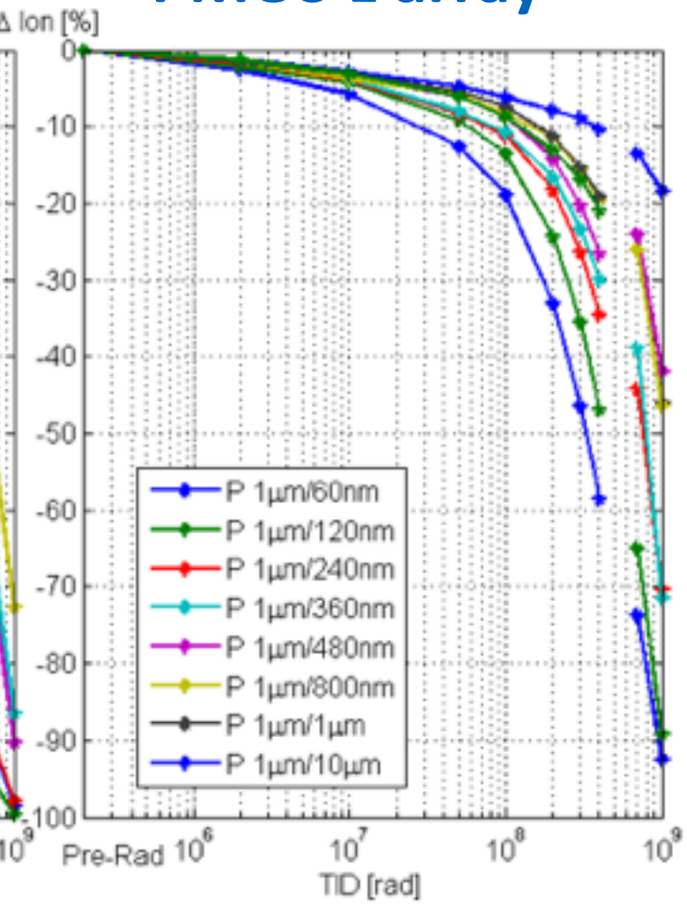
Radiation damage is severe in short and narrow channel transistors, where it depends on the bias and temperature applied both during and after irradiation

Radiation-Induced Narrow Channel Effect (RINCE)
Radiation-Induced Short Channel Effect (RISCE)

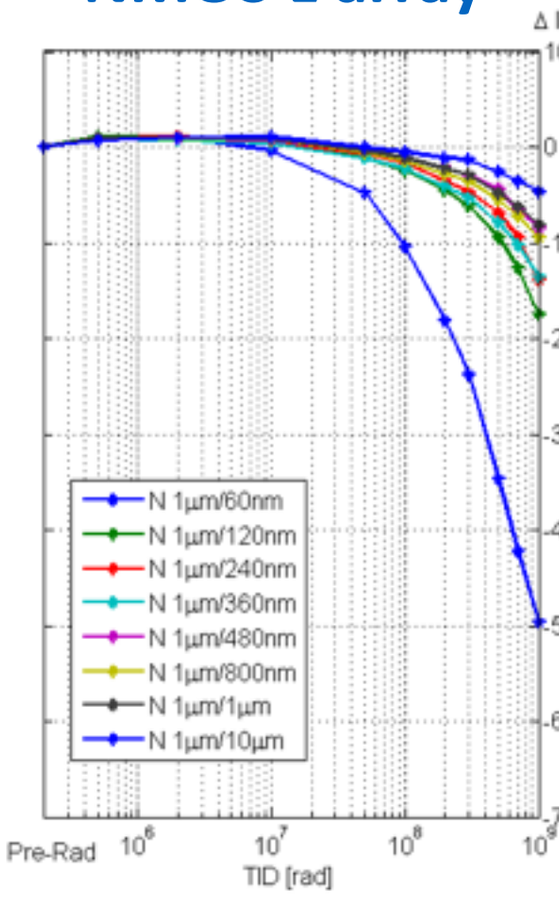
PMOS W array



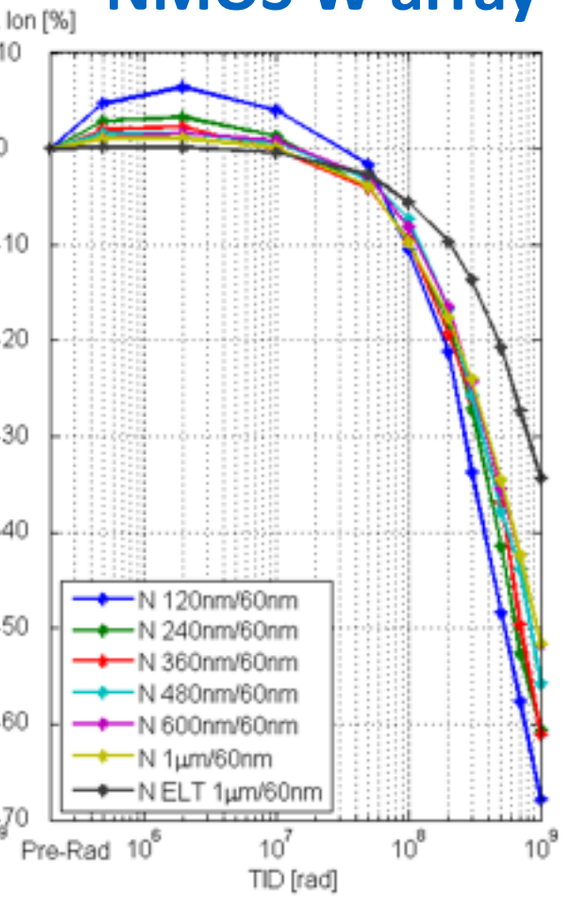
PMOS L array



NMOS L array



NMOS W array

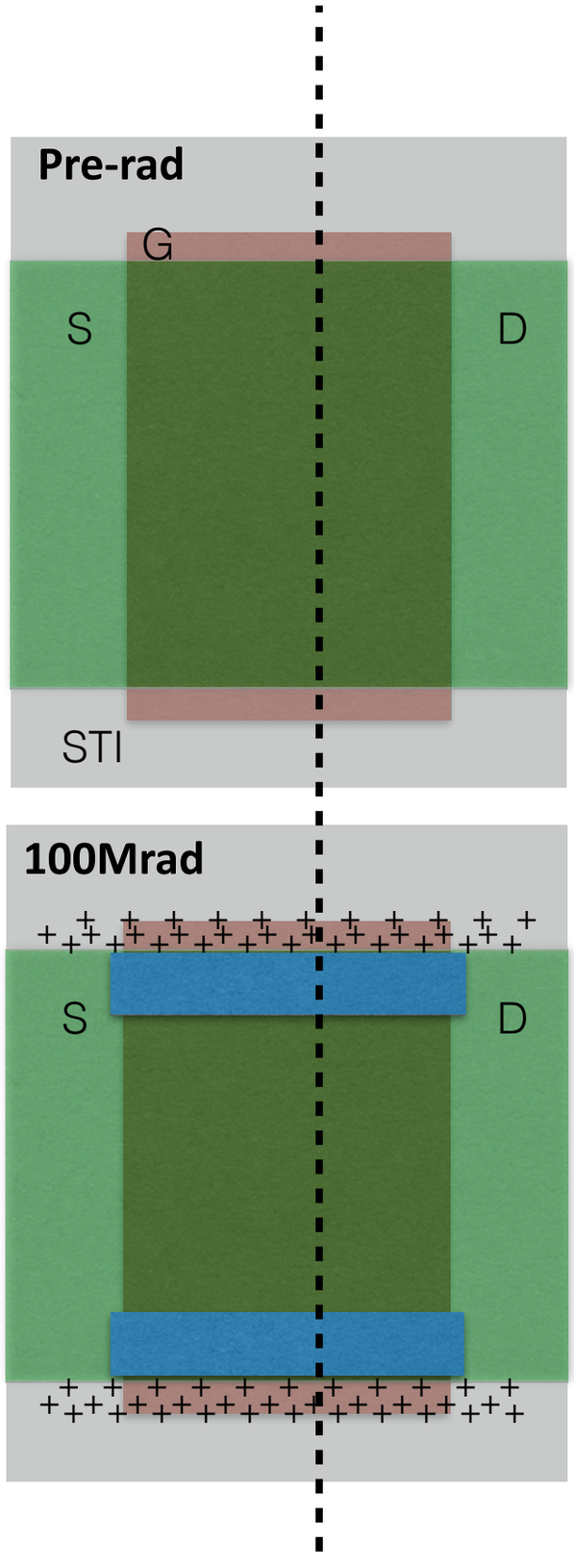


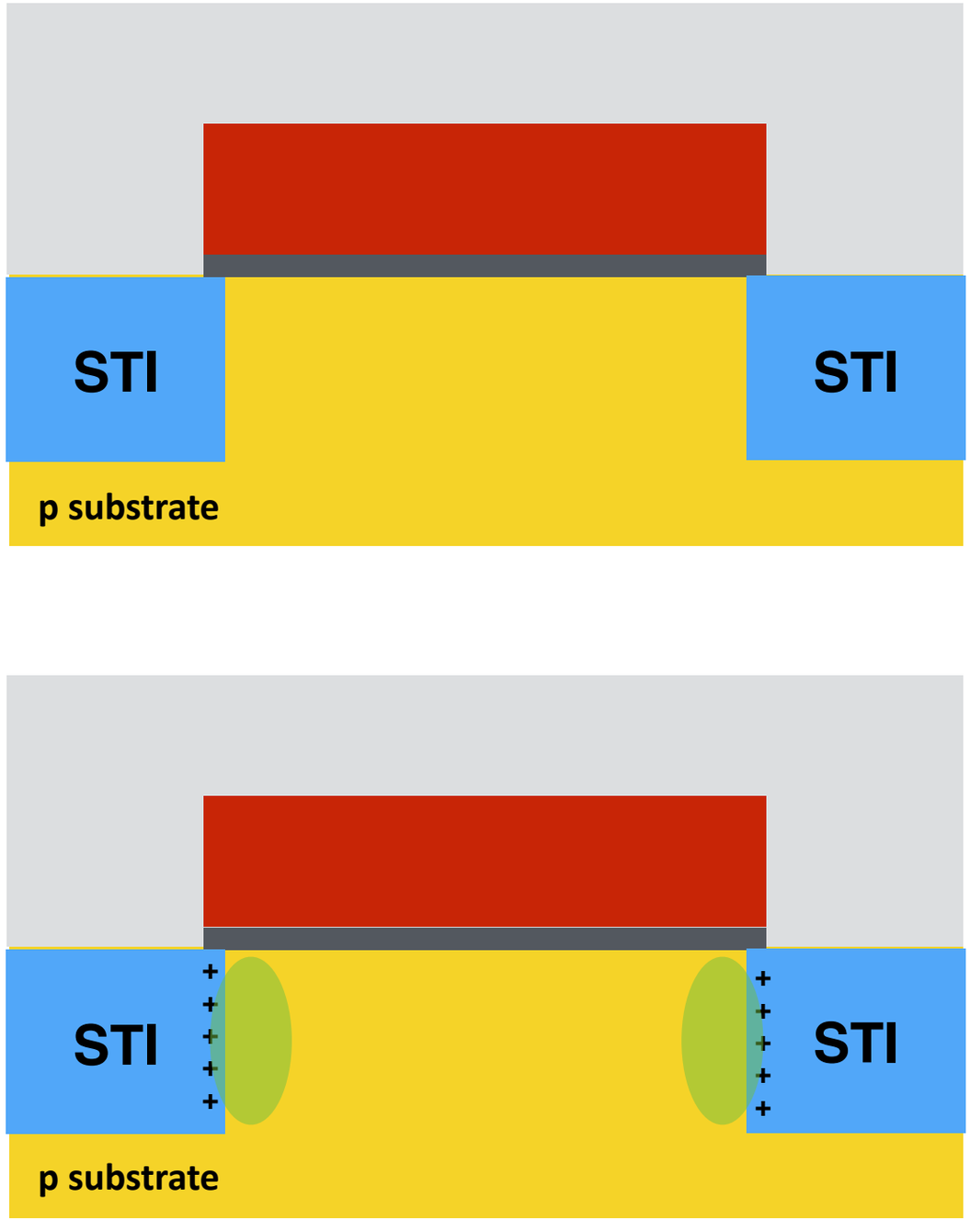
T = 25C

Bias: |Vgs|=|Vds|=1.2V

RINCE can be conceptually represented by this cartoon

W = large size

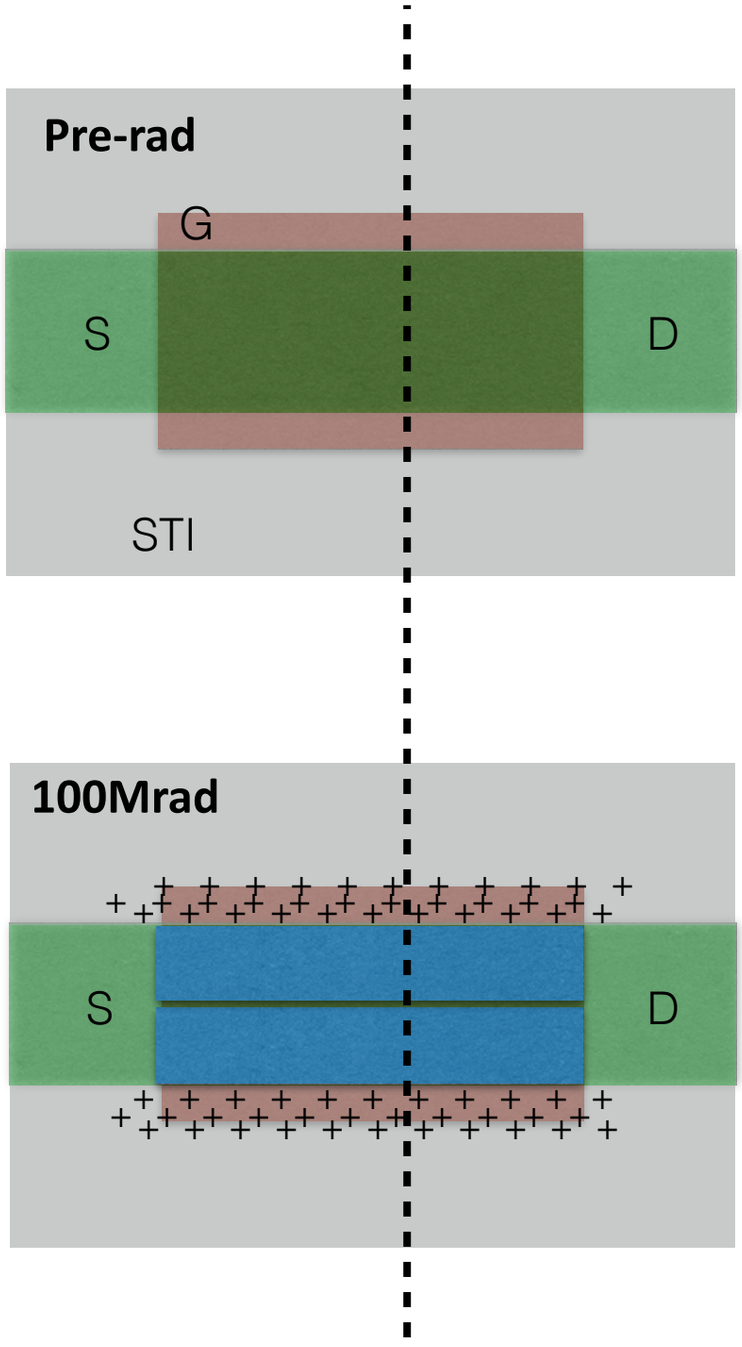


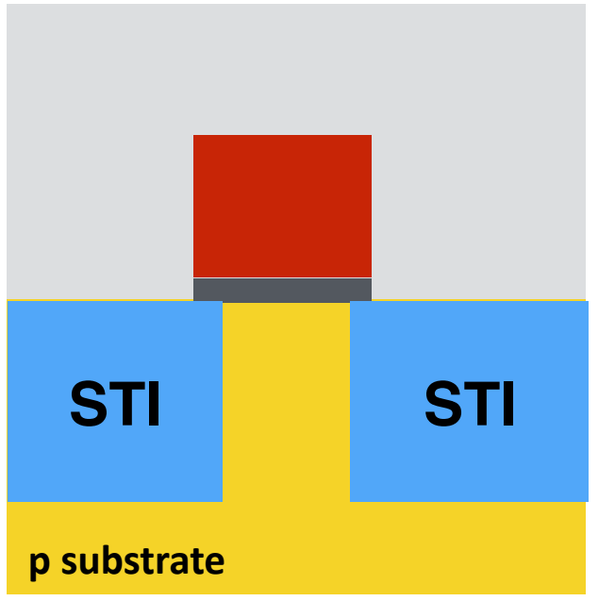


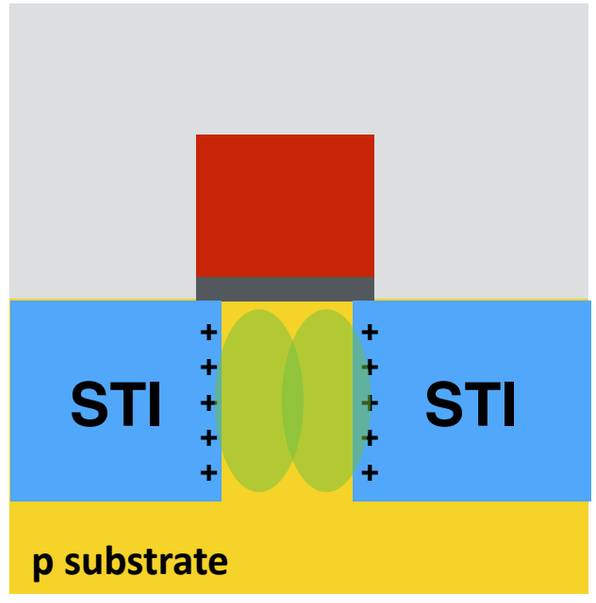
NOTE: In this cartoon, there is no distinction between the positive charge trapped in the oxide or in interface traps

RINCE can be conceptually represented by this cartoon

W = minimum size



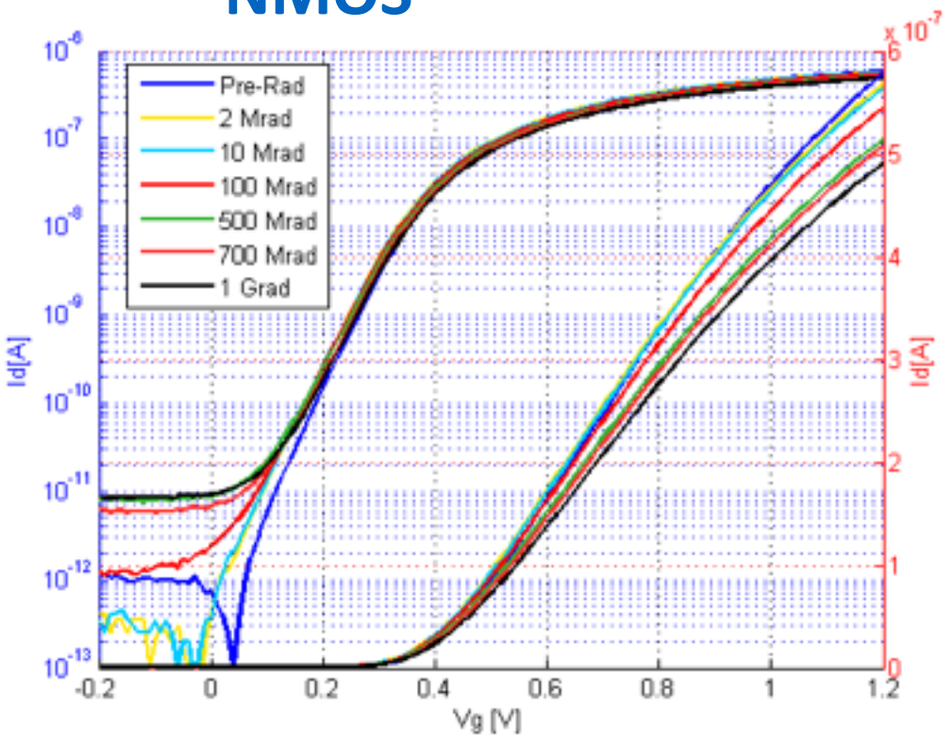




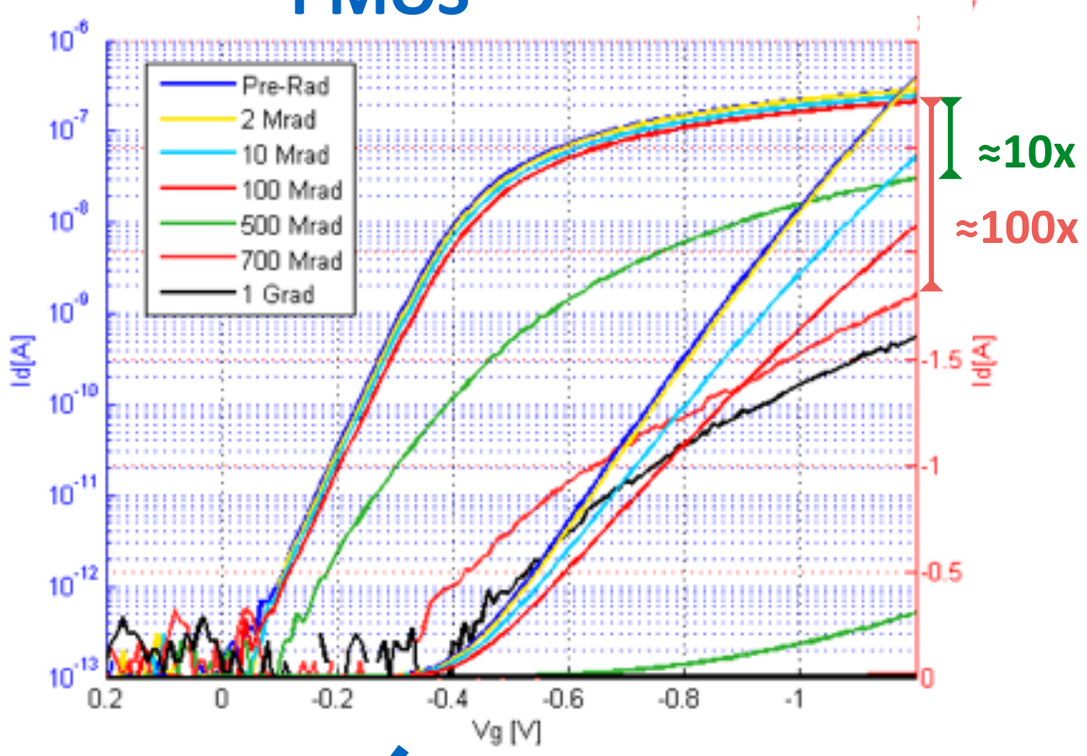
NOTE: In this cartoon, there is no distinction between the positive charge trapped in the oxide or in interface traps

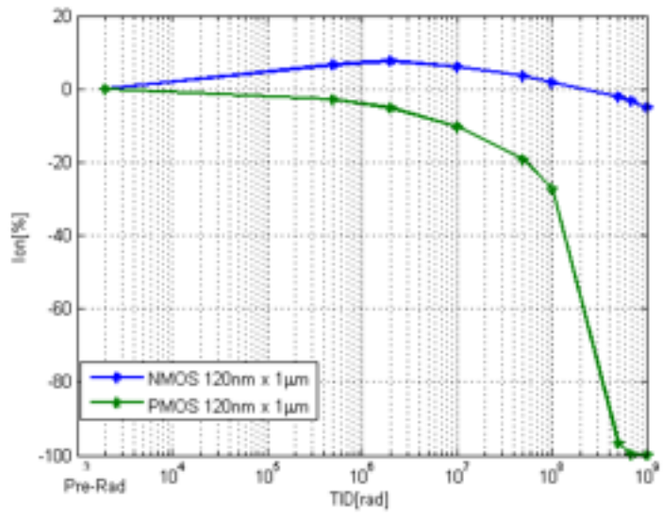
RINCE: Narrow channel PMOS transistors do not work above 500Mrad, while NMOS are working without large damage up to 1Grad

NMOS



PMOS

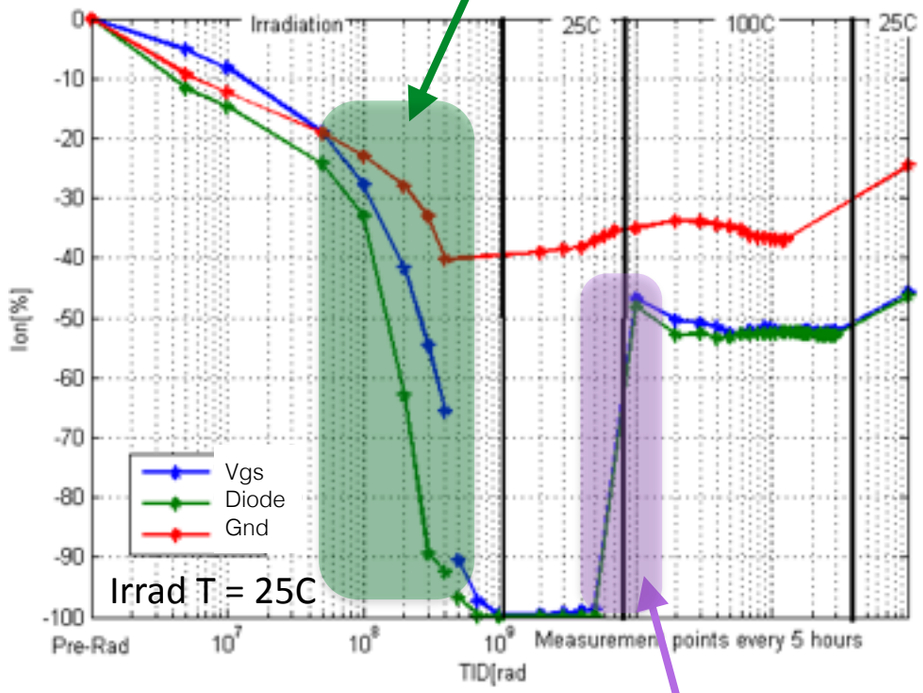




Transistors' size: W=120nm, L=1um
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

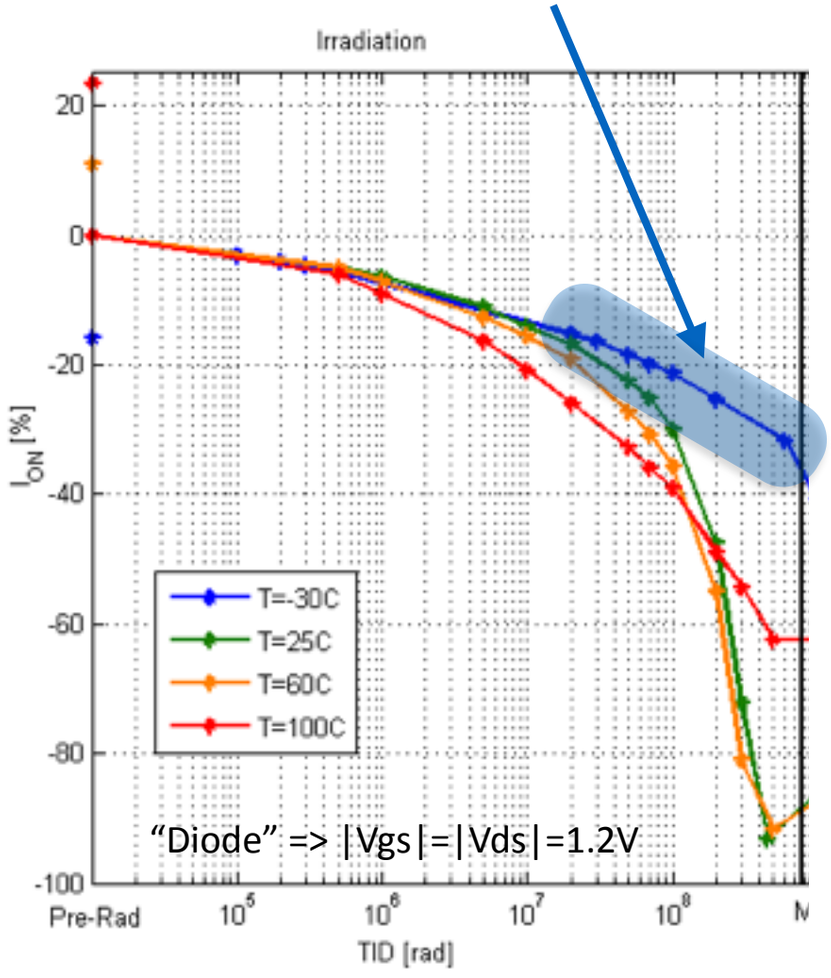
RINCE in PMOS depends on bias and temperature

Bias during irradiation is bad!



Annealing at high T is good!

Sub-zero T during irradiation is good



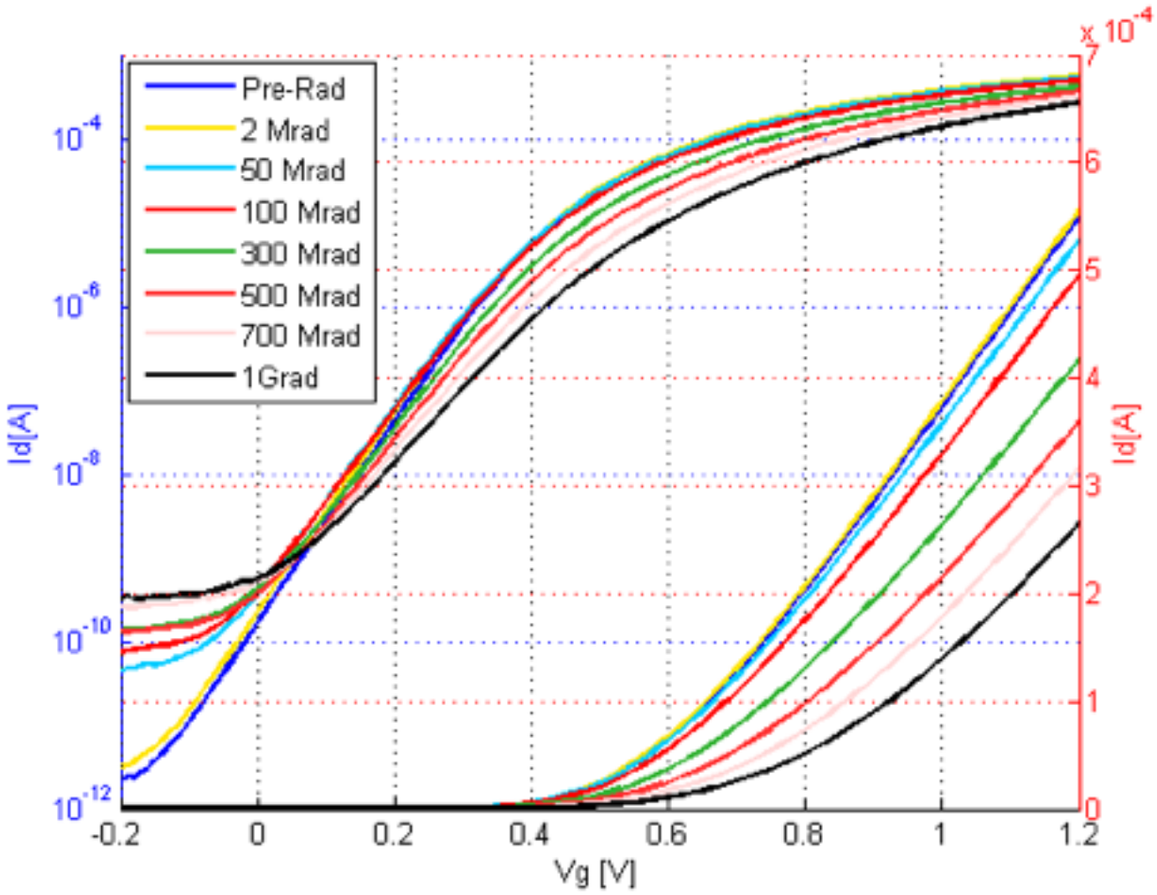
Transistors' size: W=120nm, L=1um
Irradiation conditions:

* Bias:
  - "Vgs" => |Vgs|= 1.2V, Vds=0V
  - "Diode" => |Vgs|=|Vds|=1.2V
  - "Gnd" =>|Vgs|=Vds=0V

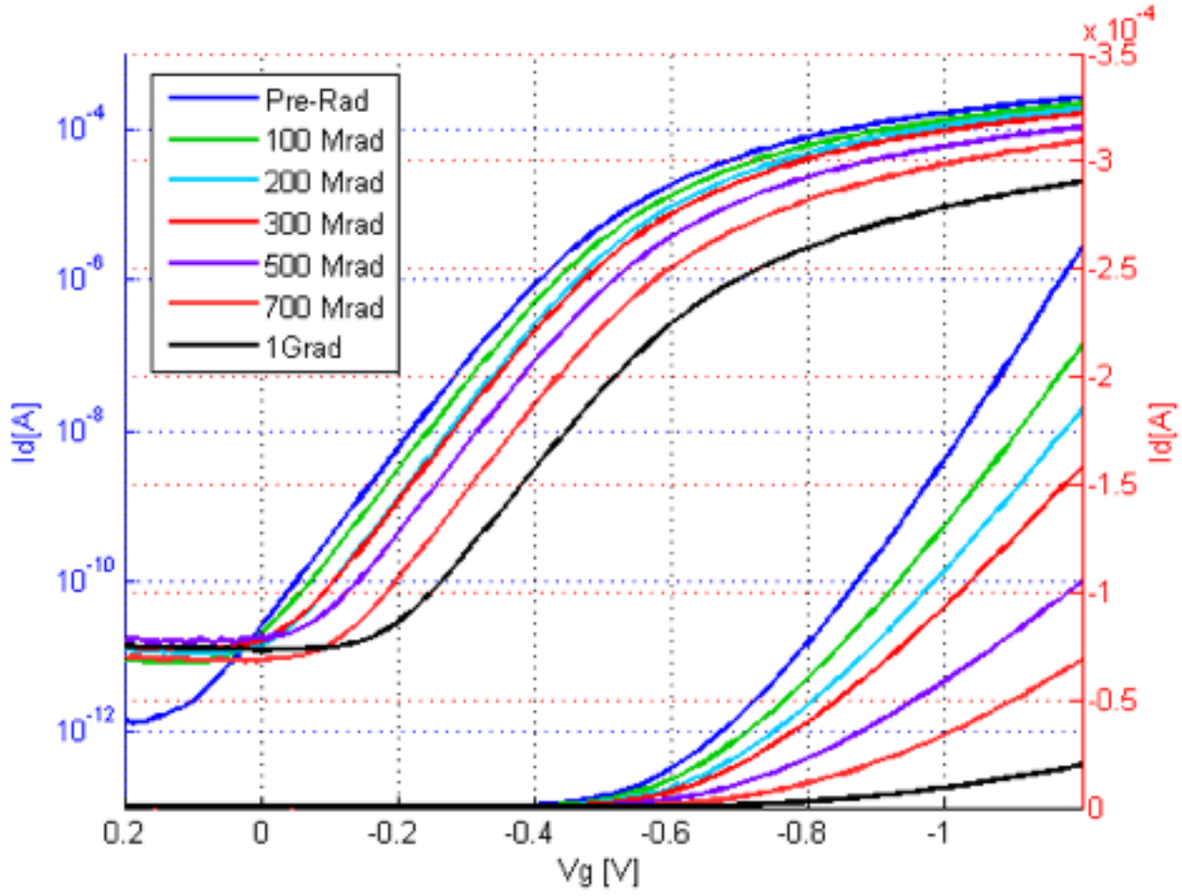
RISCE: Short channel PMOS are more damaged than NMOS

Damage occurs also in ELT transistors, hence it can not be due to the STI oxide

NMOS

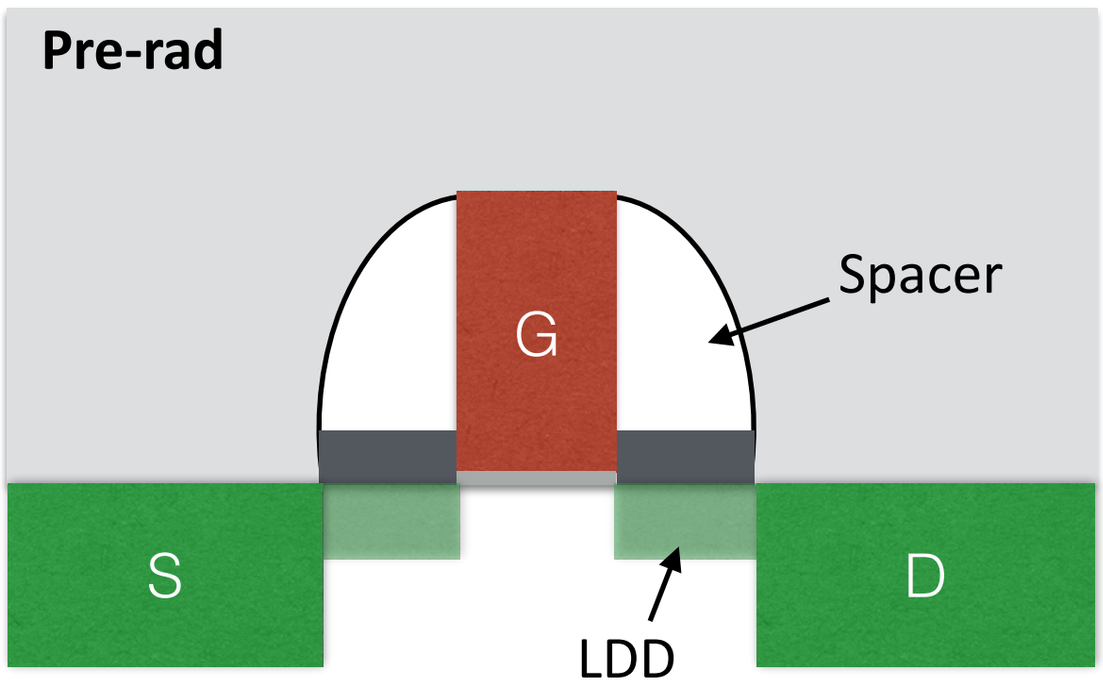


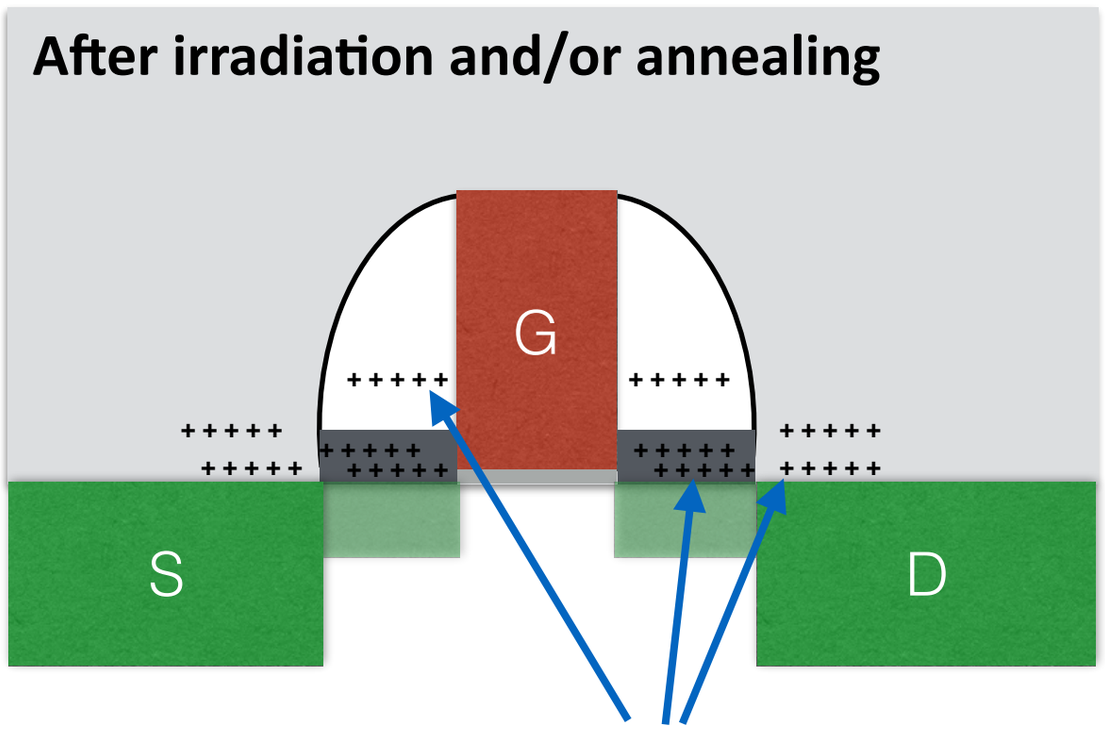
PMOS



Transistors' size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

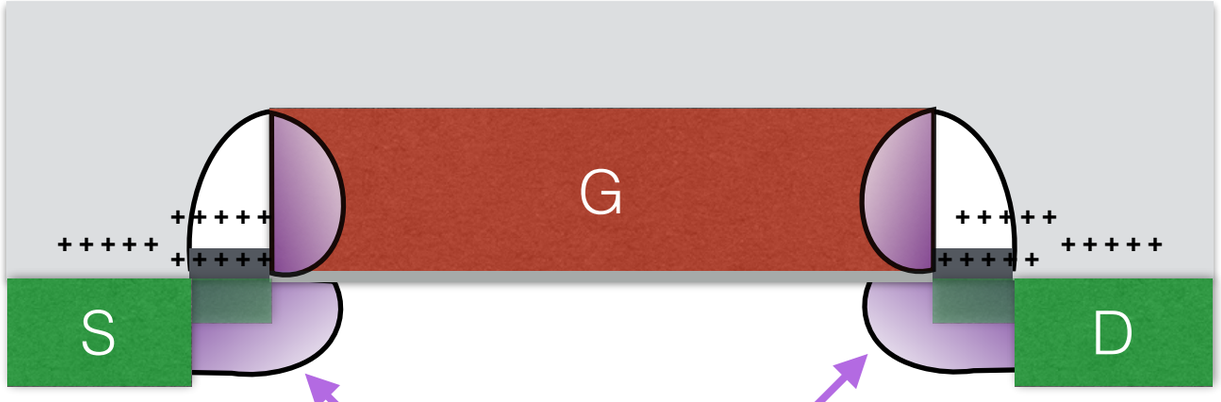
RISCE can be conceptually represented by this cartoon





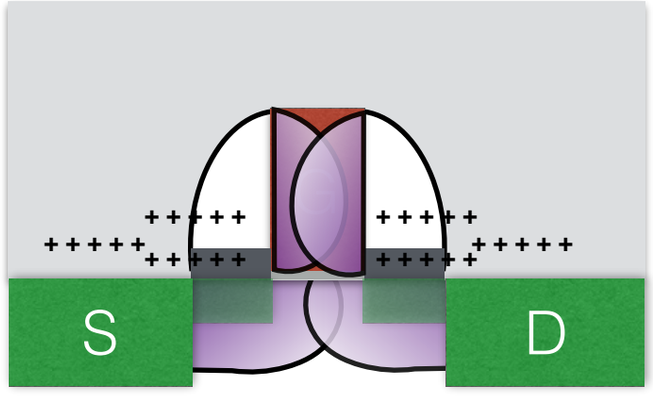
Which defect? Which charge trapped? Where?

L=moderate size



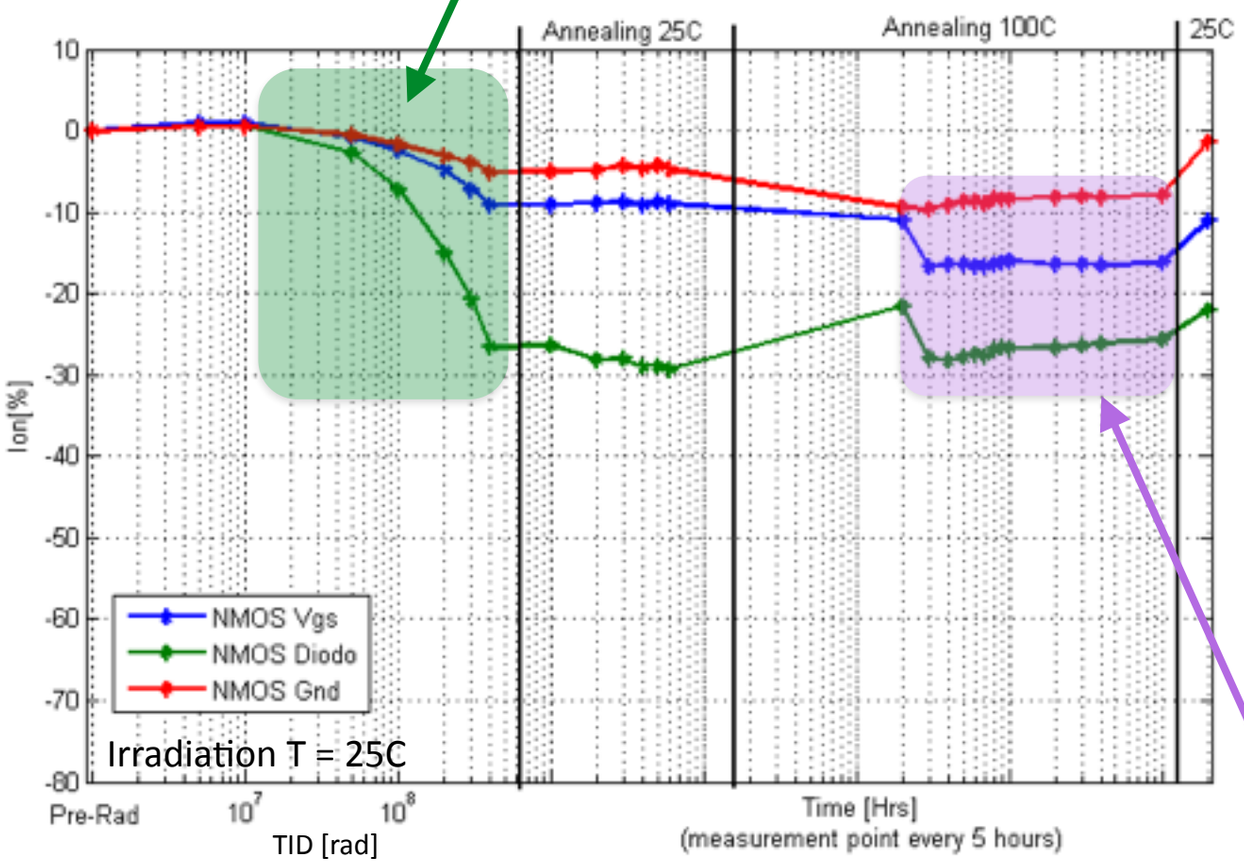
Regions strongly influenced by the trapped charge

L=min size

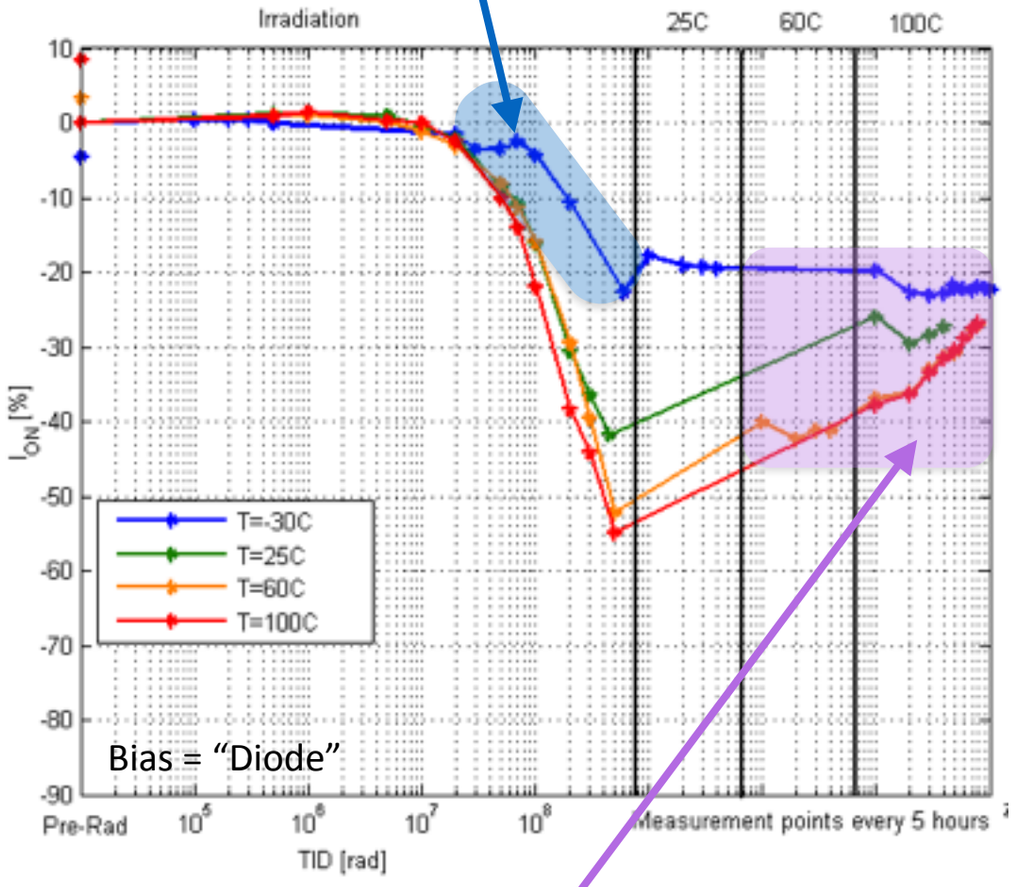


RISCE in NMOS

Bias during irradiation is bad!



Sub-zero T during irradiation is good



Annealing at high T is neutral or good (for the most damaged devices)!

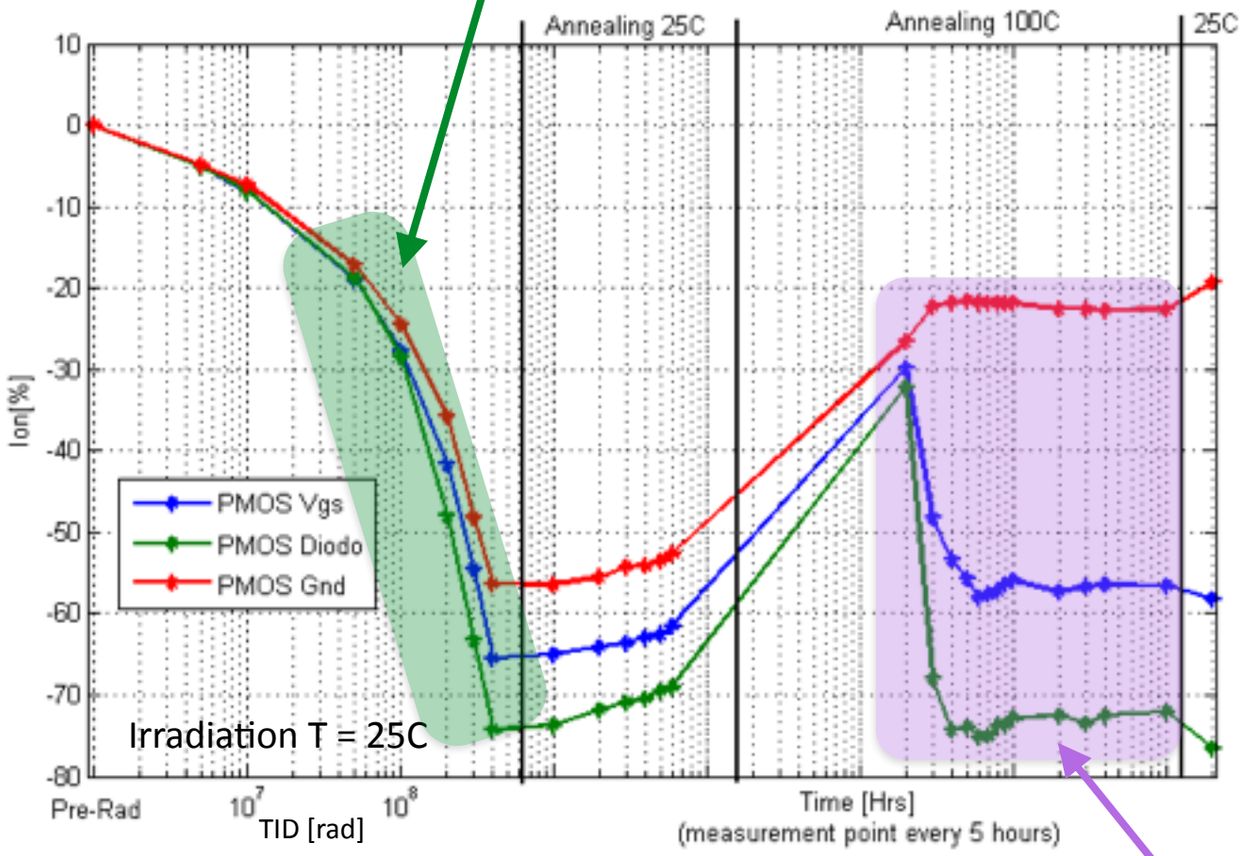
Transistors' size: W=0.6um, L=60nm
Irradiation conditions:

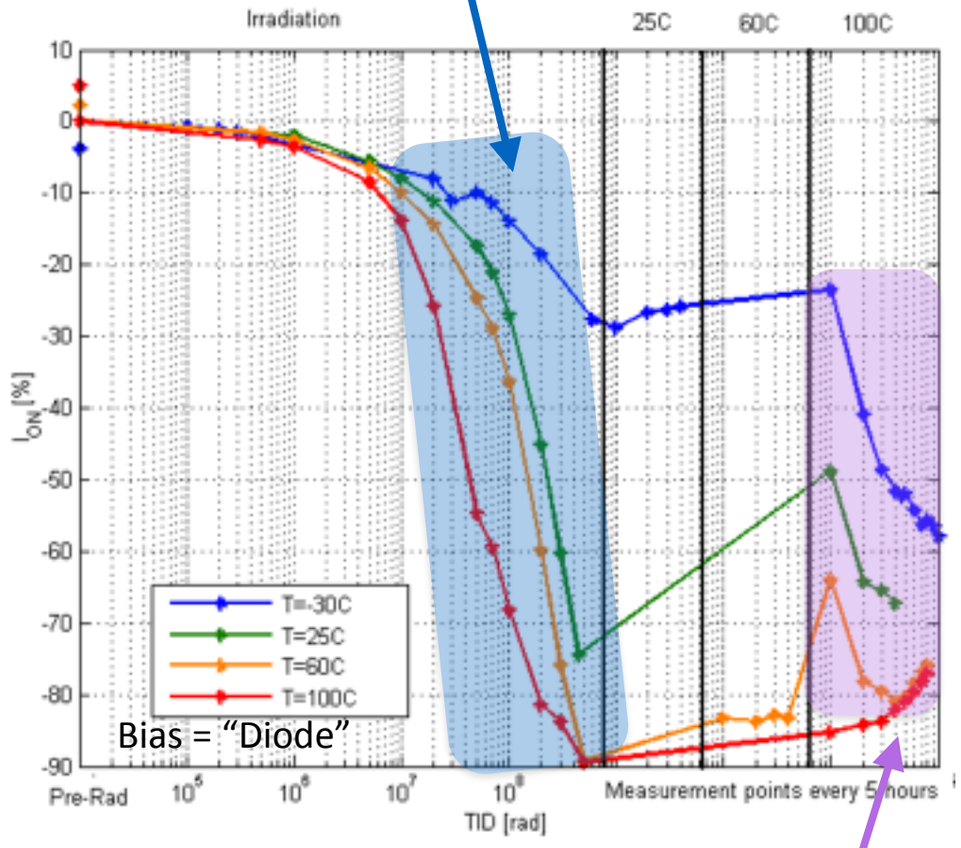
* Bias:
  "Vgs" => |Vgs|= 1.2V, Vds=0V
  "Diode" => |Vgs|=|Vds|=1.2V
  "Gnd" =>|Vgs|=Vds=0V

RISCE in PMOS

Bias during irradiation is mildly influential

Thermal energy during irradiation is bad!



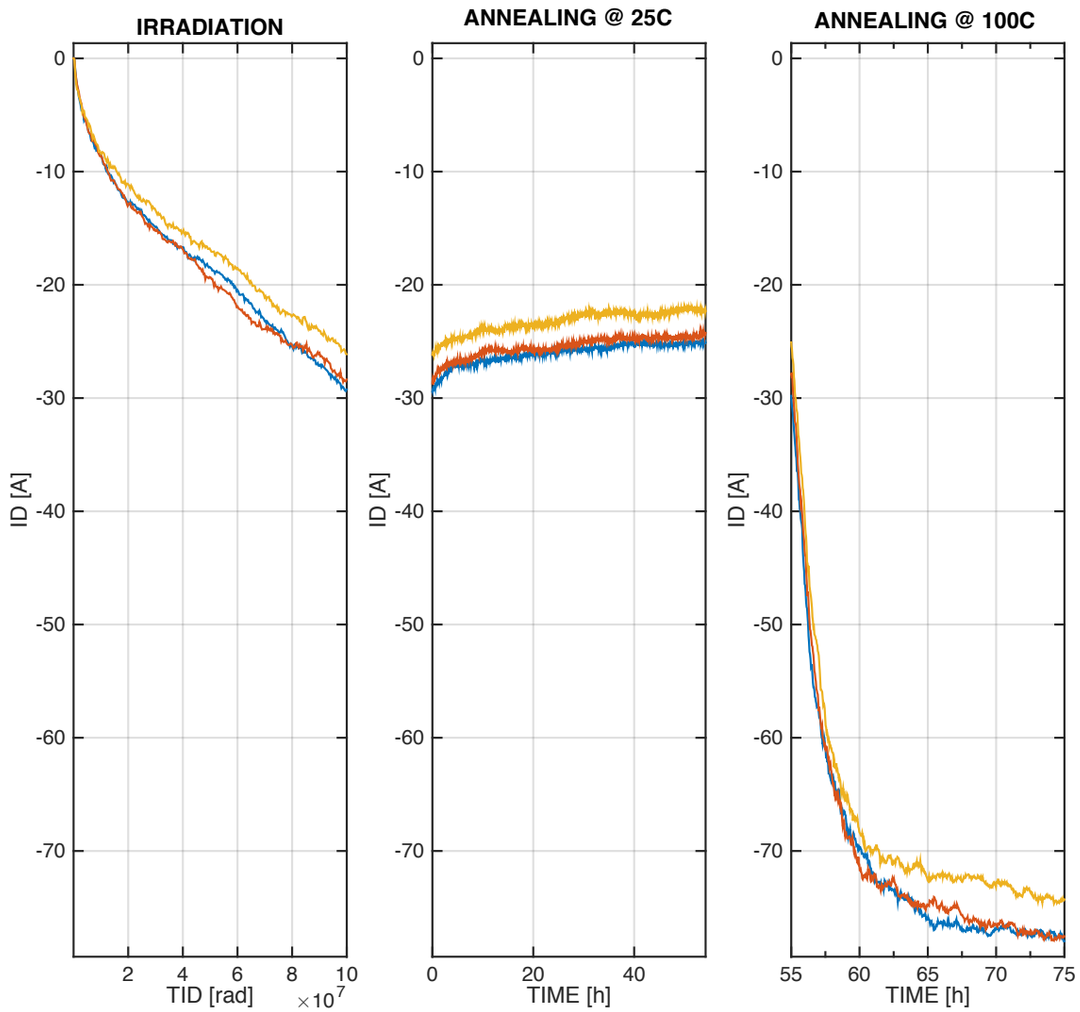


Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Vgs" => |Vgs|= 1.2V, Vds=0V
"Diode" => |Vgs|=|Vds|=1.2V
"Gnd" =>|Vgs|=Vds=0V

Annealing at high T is very bad if performed under bias!!

The qualification procedures for CMOS foresee a 1-week annealing period post-irradiation at 100°C. This considerably worsens the performance of PMOS transistors.

Delta Id (%)



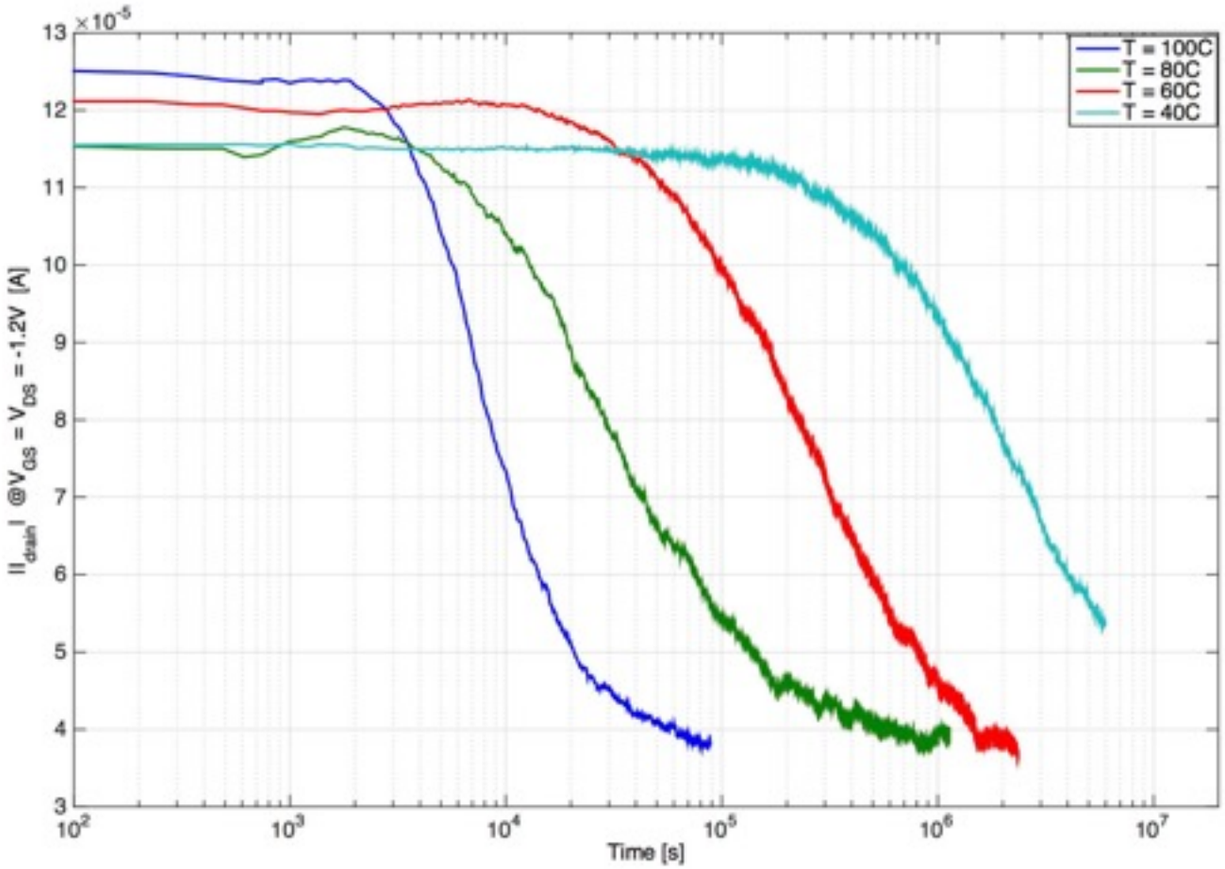
g_m degradation

V_{th} shift

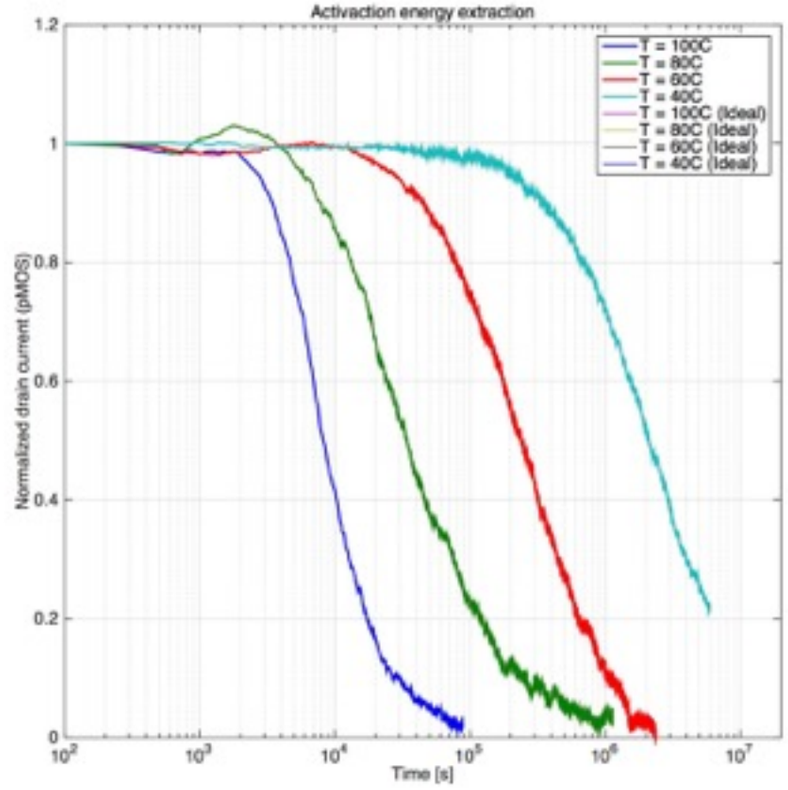
Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Diode" => |Vgs|=|Vds|=1.2V

The post-irradiation evolution in PMOS (V_{th} shift) is clearly a thermally activated process requiring the presence of bias!

Measurements and energy extraction by G.Borghello



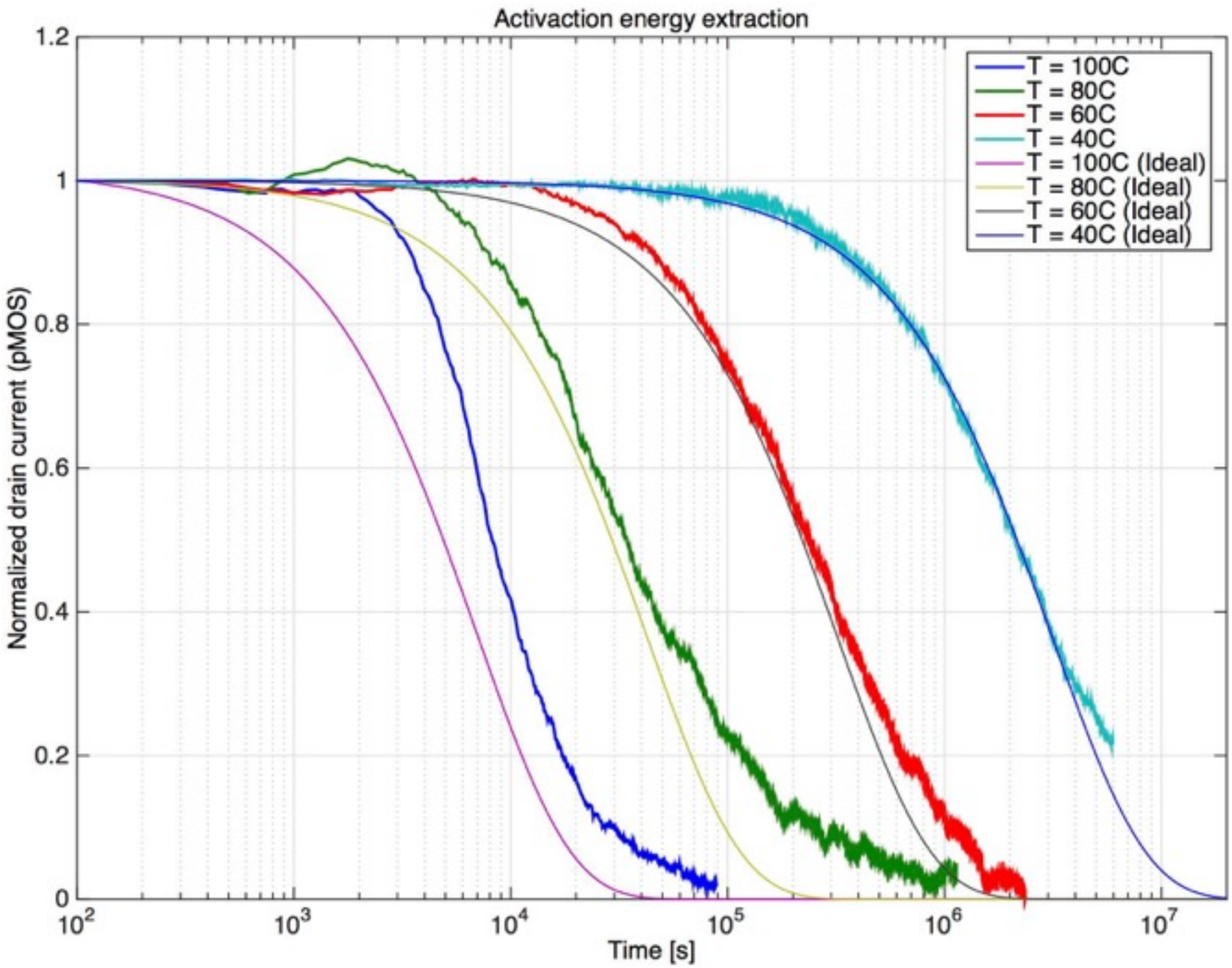
Normalisation



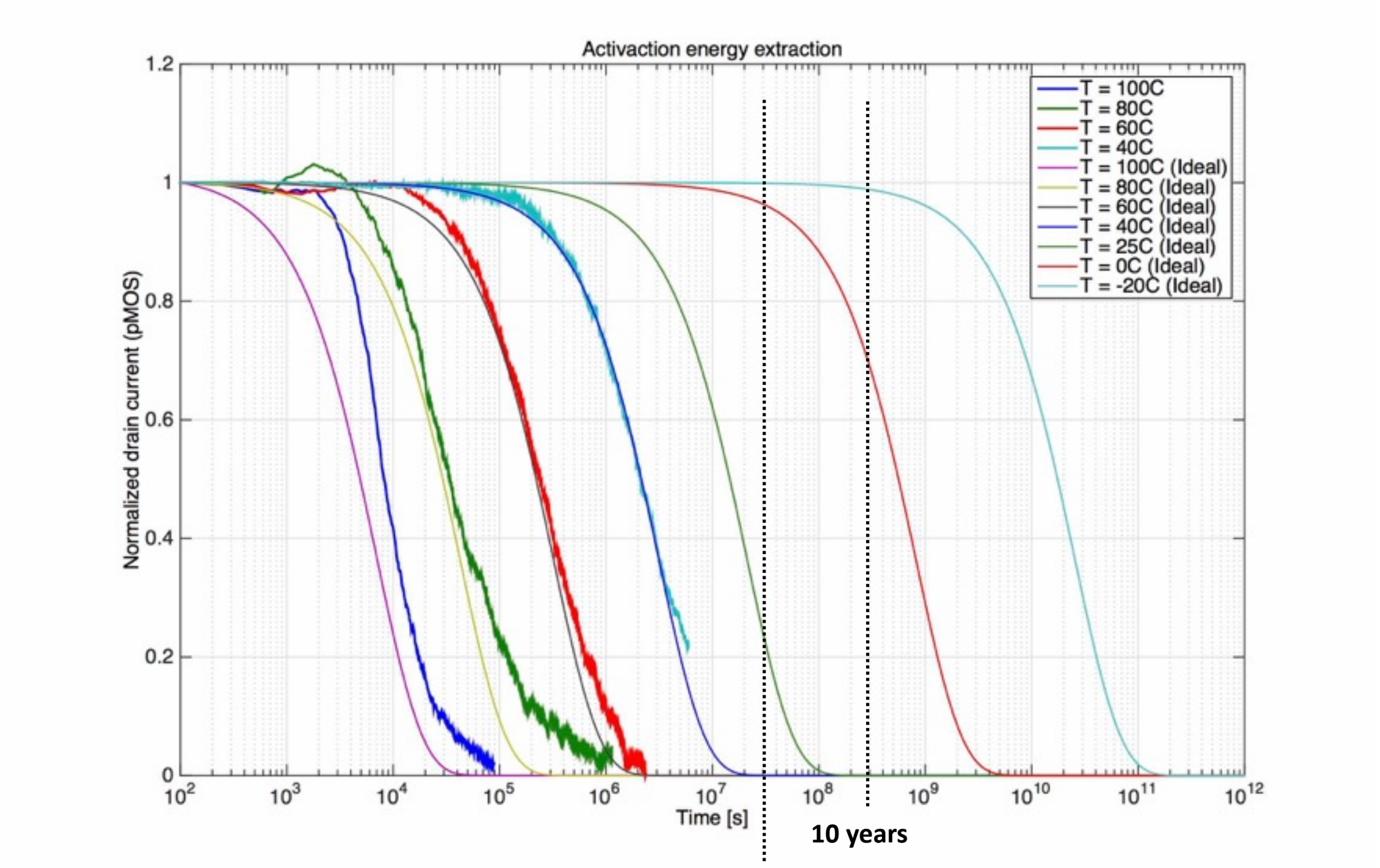
Start of annealing at high T is at 50-55hours

Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Diode" => |Vgs|=|Vds|=1.2V

In the hypothesis of a single activation energy, it is possible to extract it (very approximately) from the 4 experimental points at different temperature.
The model does not fit well the data, but it is useful to estimate the trend of the phenomenon with temperature.



According to the simple model, the post-irradiation evolution of the PMOS (Vht shift) should be considerably slowed at -20°C

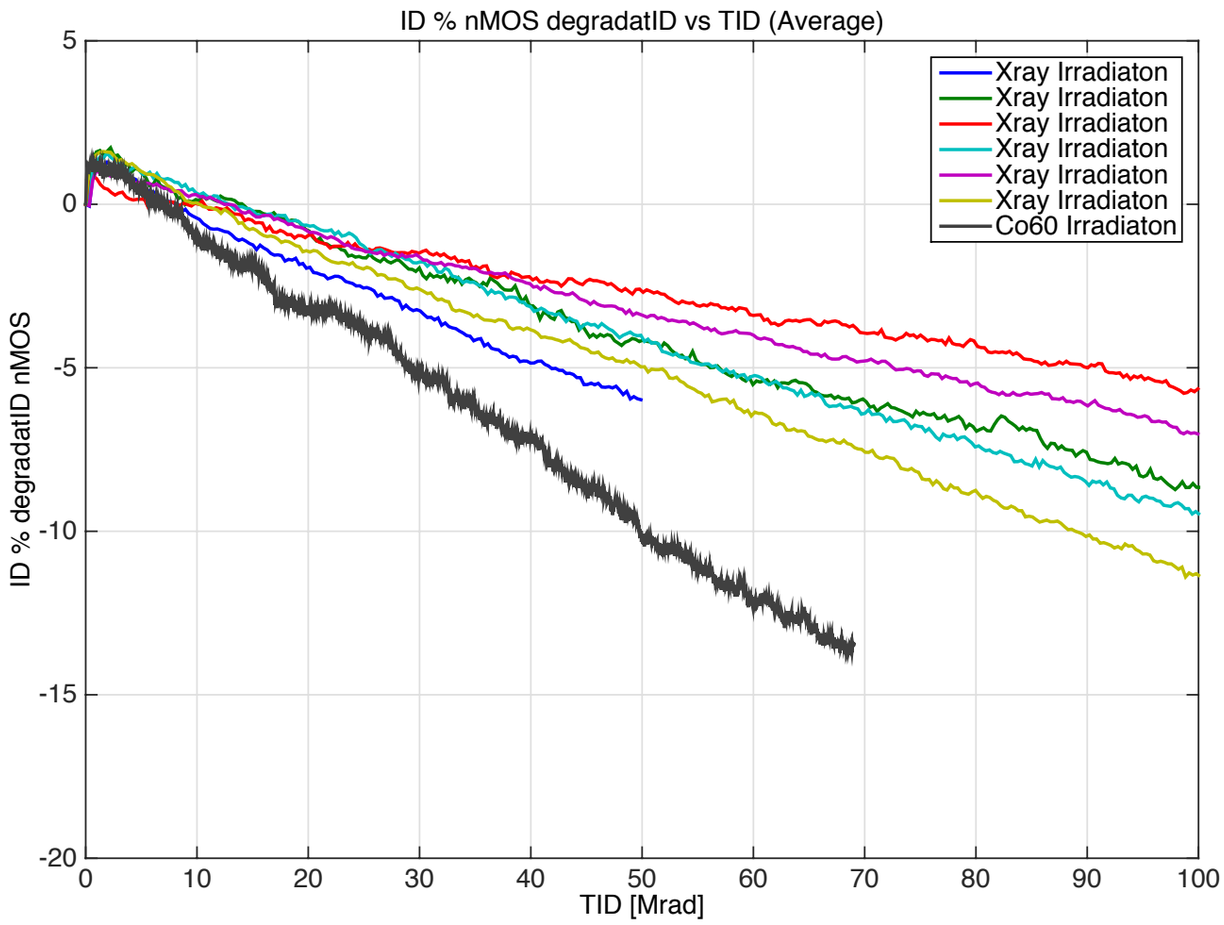


In some of the results above we can see analogies with the phenomenology observed in bipolar technologies subject to ELDRS (Enhanced Low Dose Rate Sensitivity)

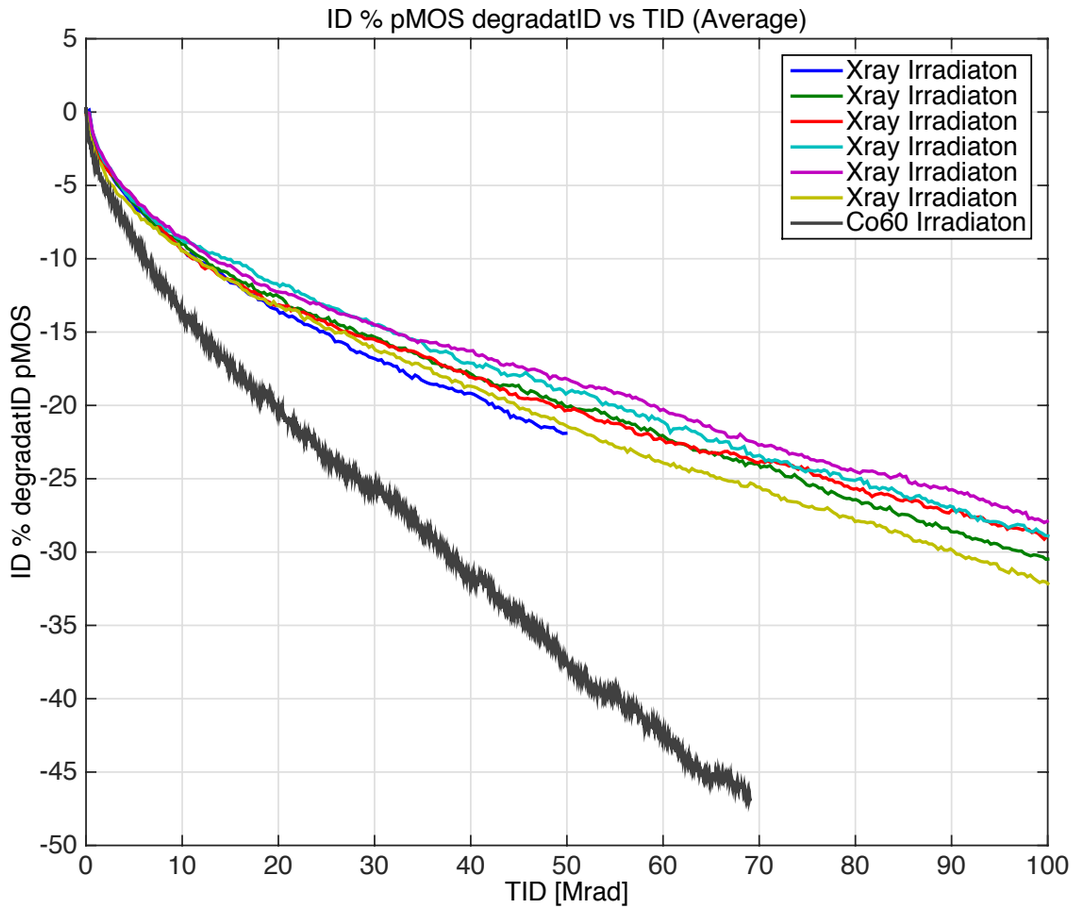
Results from an on-going irradiation with a ^{60}Co source at lower dose rate: the damage is larger!

Beware: tests are done with different radiation sources

NMOS 600n/60n, Vgs=Vds=1.2V



PMOS 600n/60n, Vgs=Vds=-1.2V



T = 25°C
HDR = 9Mrad/hour
LDR = 35krad/hour
ratio of the dose rate HDR/LDR=257
Average of 3 transistors per Chip

Summary

The Radiation response (TID) is determined by the properties of parasitic structures.
It is not a constant property in a given technology node, and can change with supplier, Fab, and with time.

Therefore we have to:

- **only qualify and use one Fab**
- **monitor regularly the natural radiation tolerance**
- **carefully qualify each ASIC during the prototyping and production phases**

In the studied 65nm:

Short and narrow channel radiation-induced effects are strong (RINCE, RISCE).

These are complex and make the choice of a qualification procedure and of appropriate design margins difficult, in particular for digital design