Module Electrical QC & Reporting

Timon Heim, Marija Marjanovic, Lingxin Meng, Hideyuki Oide,
Elisabetta Pianori, Giordon Stark, **Emily Anne Thompson**

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https://indico.cern.ch/event/1353986/

BERKELEY LAB

ATLAS ITk

Outline

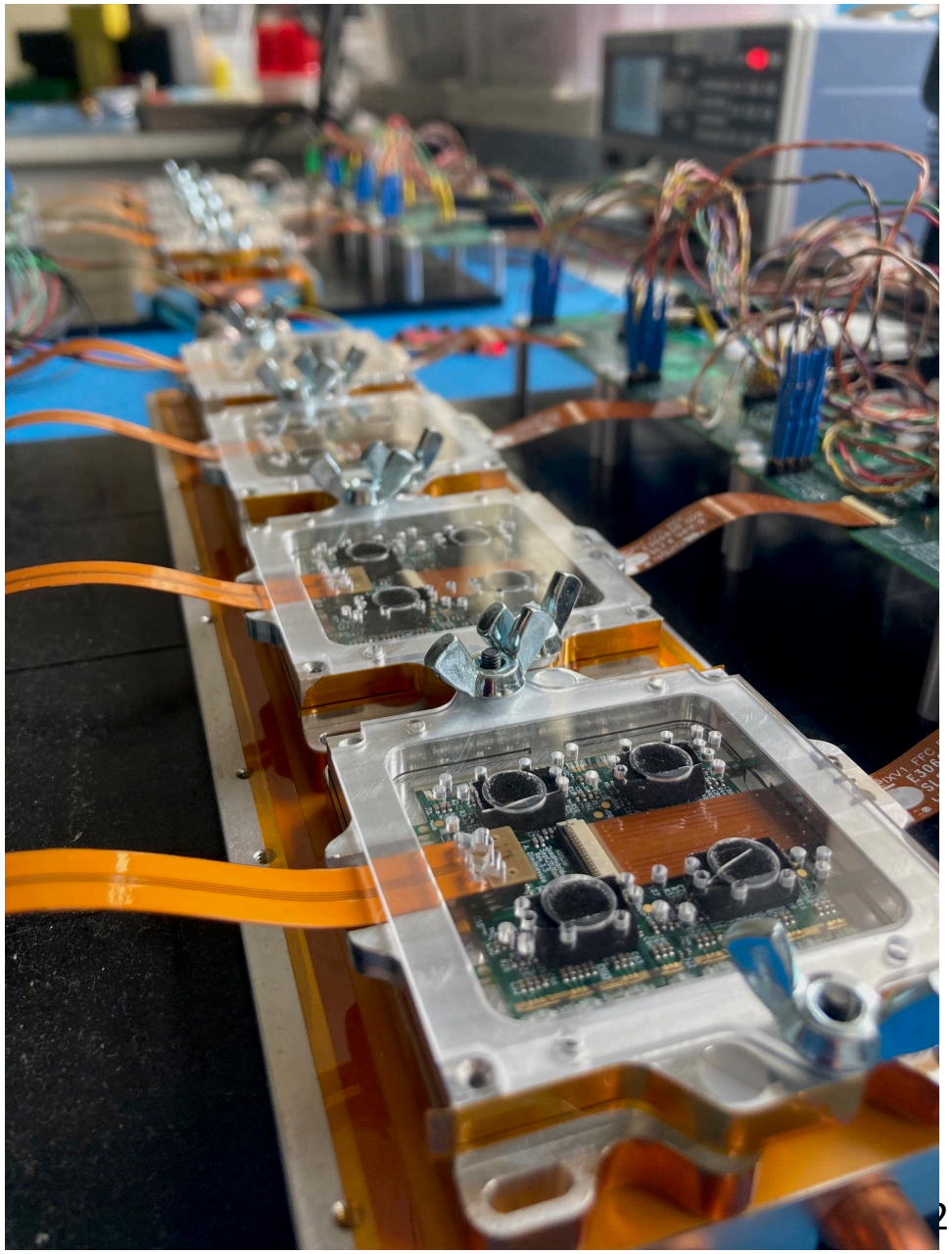
1. Latest updates from module electrical QC

2. Reflection on electrical QC from preproduction so far

    - How much data do we have in PDB?
    - What have we learned so far from QC tests?
    - Which issues would we like to see understood before module PRR?

3. Next steps:

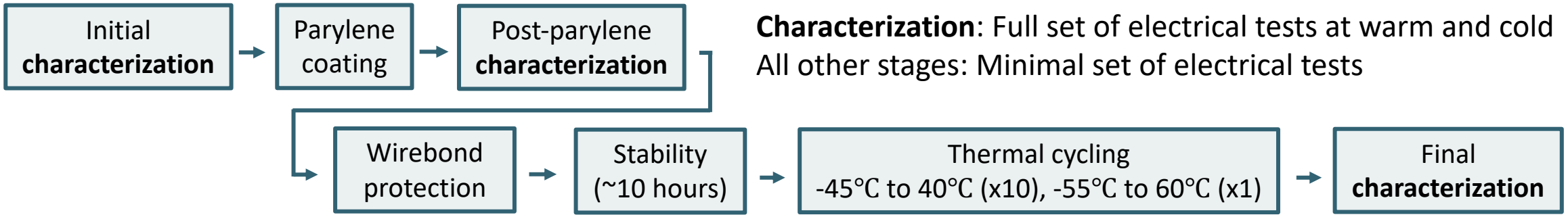
    - Speeding up testing procedure
    - Module QC reporting



Overview of module electrical QC – stages and tests

Module electrical quality control (QC): Define testing procedures and specifications to ensure that **all** modules perform electrically well, providing tools for testing

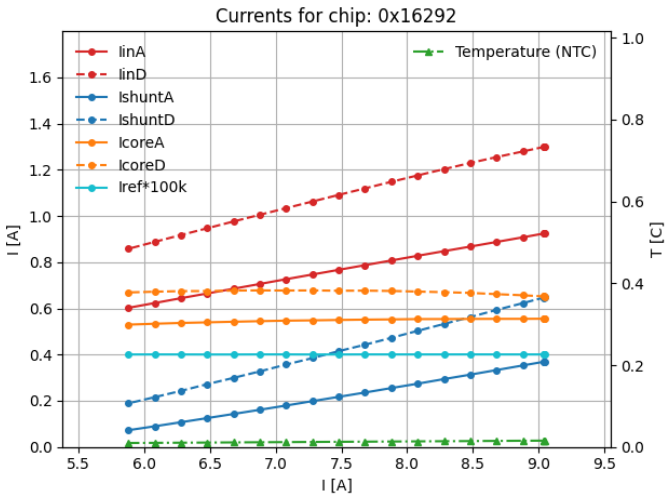
Testing stages:

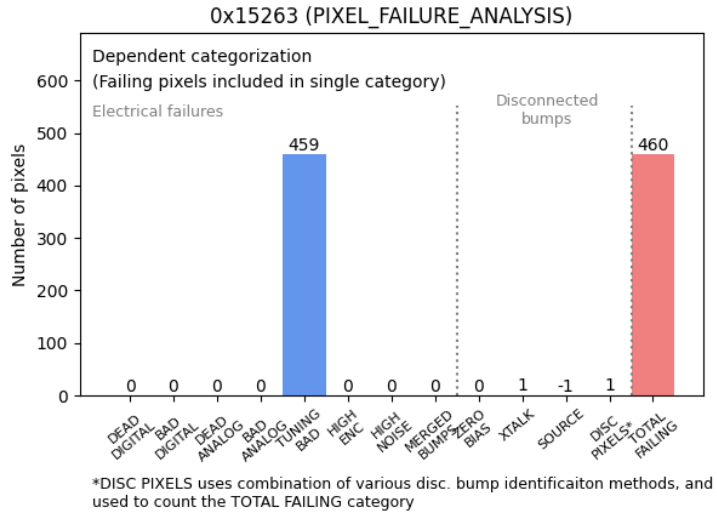


Characterization: Full set of electrical tests at warm and cold
All other stages: Minimal set of electrical tests

Electrical tests:

- Performing calibrations
- Checking powering
- Checking built-in chip protections
- Checking data transmission, merging
- Categorizing performance of each pixel (“advanced scans”)





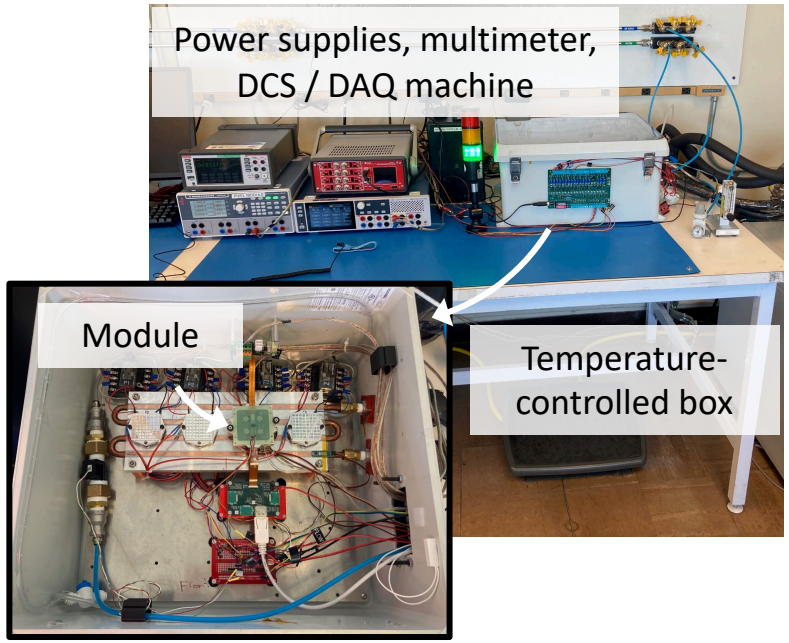
*DISC PIXELS uses combination of various disc. bump identificaiton methods, and is used to count the TOTAL FAILING category

QC-tools and dataflow

Module electrical quality control (QC): Define testing procedures and specifications to ensure that modules perform electrically well, providing tools for testing

Module-QC-Measurement-Tools

Records FE-chip internal voltages and currents



Update chip configs locally

Measurement data

Chip configs

Module-QC-Analysis-Tools

Performs analysis, sets pass/fail status of each FE-chip

Local DB

Web-application viewer and GUI for management of QC data

Module-QC-Database-Tools

Manages flow of module info (chip configurations)

(Local)

(Global)

Electrical-QC summary

Module history

Production database

Latest versions

Latest versions of tools:

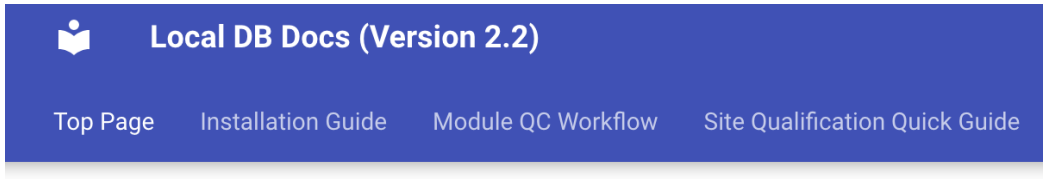
- module-qc-**measurement**-tools: v2.2.1
- module-qc-**analysis**-tools: v2.2.2
- module-qc-**database**-tools: v2.2.5
- **YARR**: v1.5.0
- **LocalDB**: v2.2.8

Recent features:

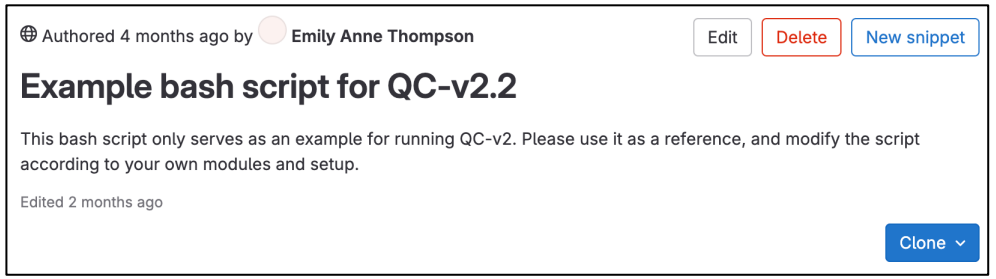
- Smoother dataflow and error handling (Giordon)
- Allow for testing of ITkPixv2 modules (Charlie)
- Check target current/voltage is reached before proceeding with script (Matthias)
- Bug fixes! (Everyone)

New to setting up a workflow?

Check instructions on setting up LocalDB:



Use example QC bash script:



Reflections on QC procedure so far

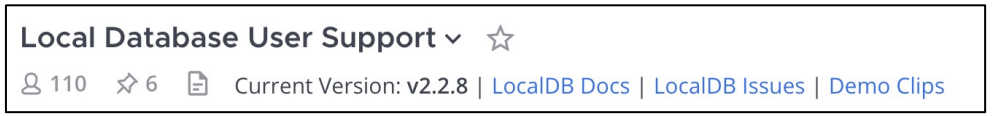
Community contributions are important.

Developers of these tools (i.e. at LBNL) have not yet received preproduction modules – debugging difficult without support of community. If you run into issues testing modules, please:

- ✓ Open a git issue describing the problem
- ✓ Ask quick questions on the relevant mattermost channel

Link

Link

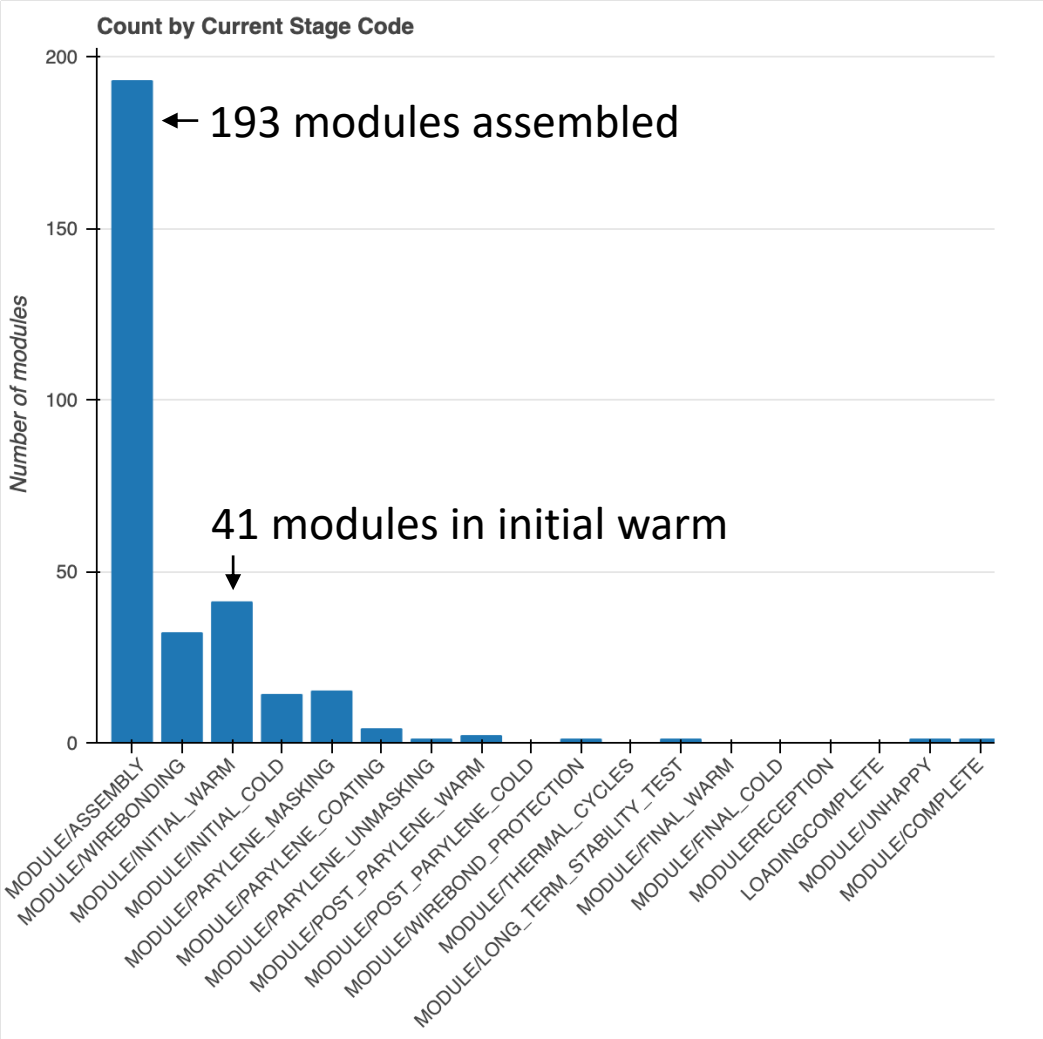


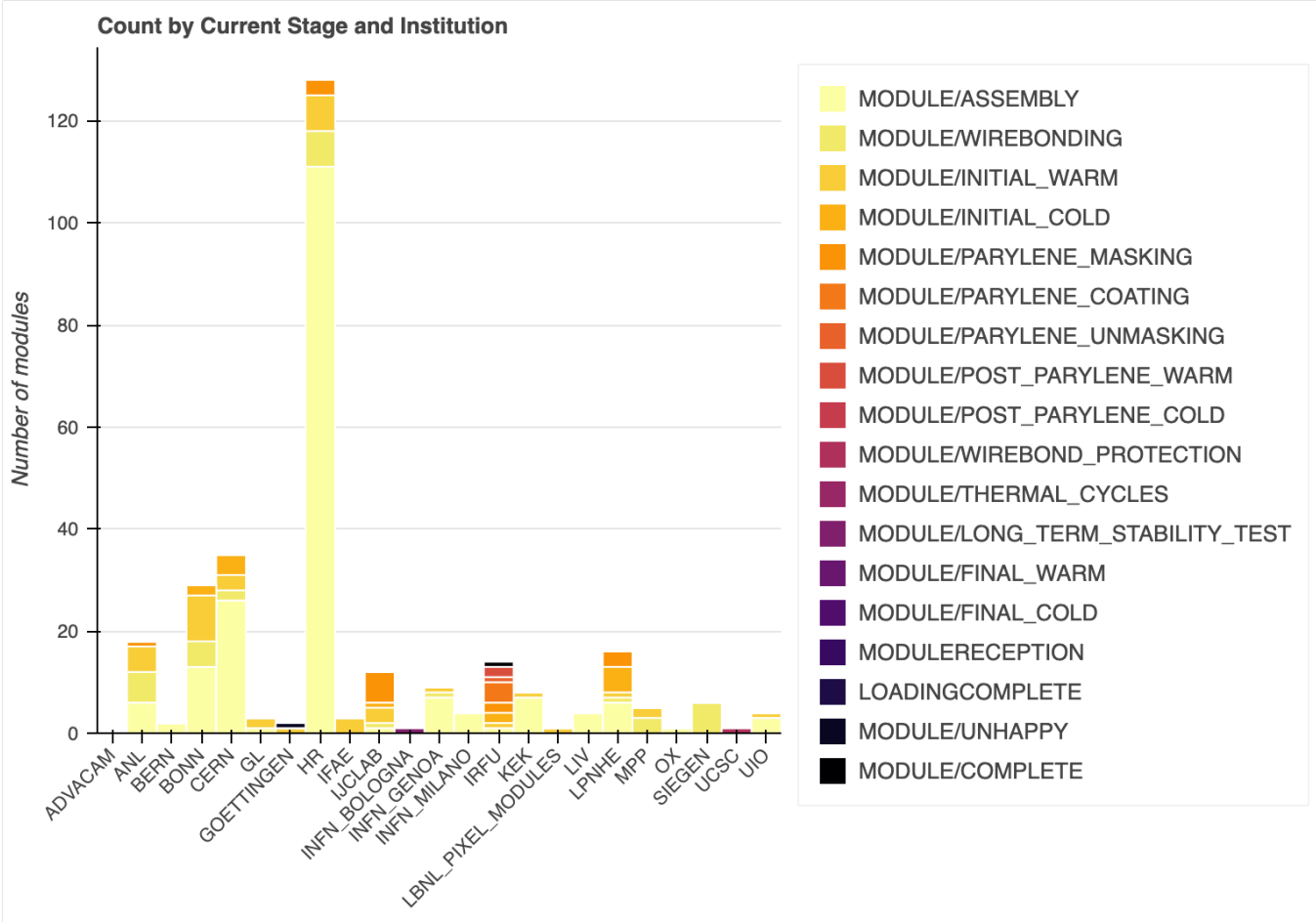
- ✓ Open a merge request if you have identified quick fixes for your problems
- X Don’t email us – crowd-sourced debugging is better

This is working well. Keep it up.

Data in production database

Information on all pre-production modules with data from the production database:

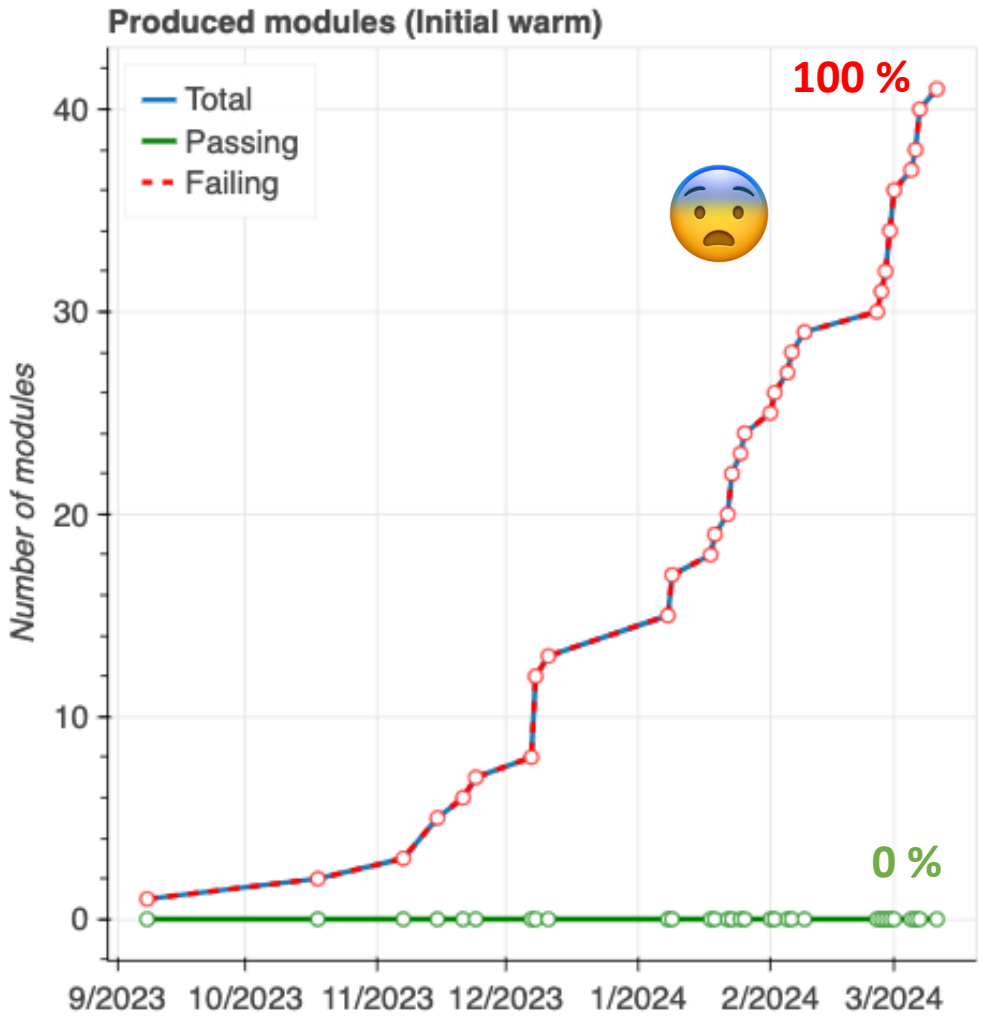




Only 40 modules with electrical data from INITIAL_WARM staged pushed to PDB – please push your data!

Reflections on QC procedure so far

How many “good” modules have we assembled?



Do not panic.

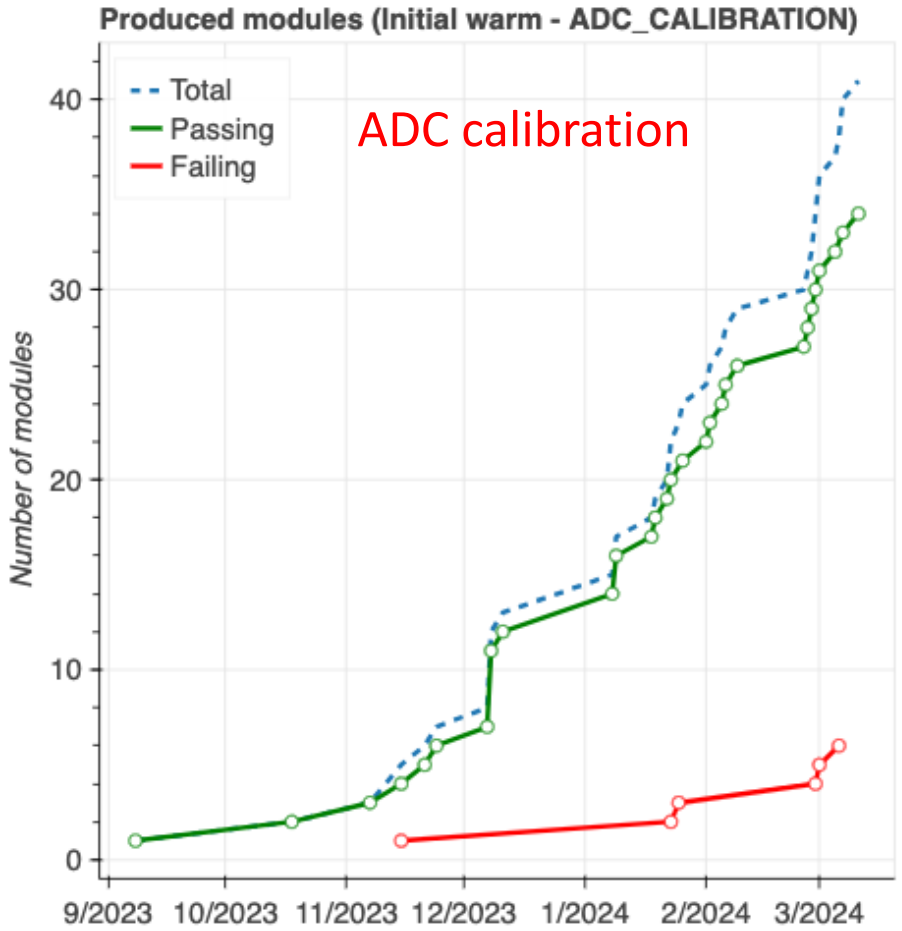
The QC criteria is currently very hard for a module to pass – and this is by design.

Goal in pre-production is to learn as much as possible about these modules as we build them – we flag anytime a module does not behave as expected, even in seemingly trivial ways.

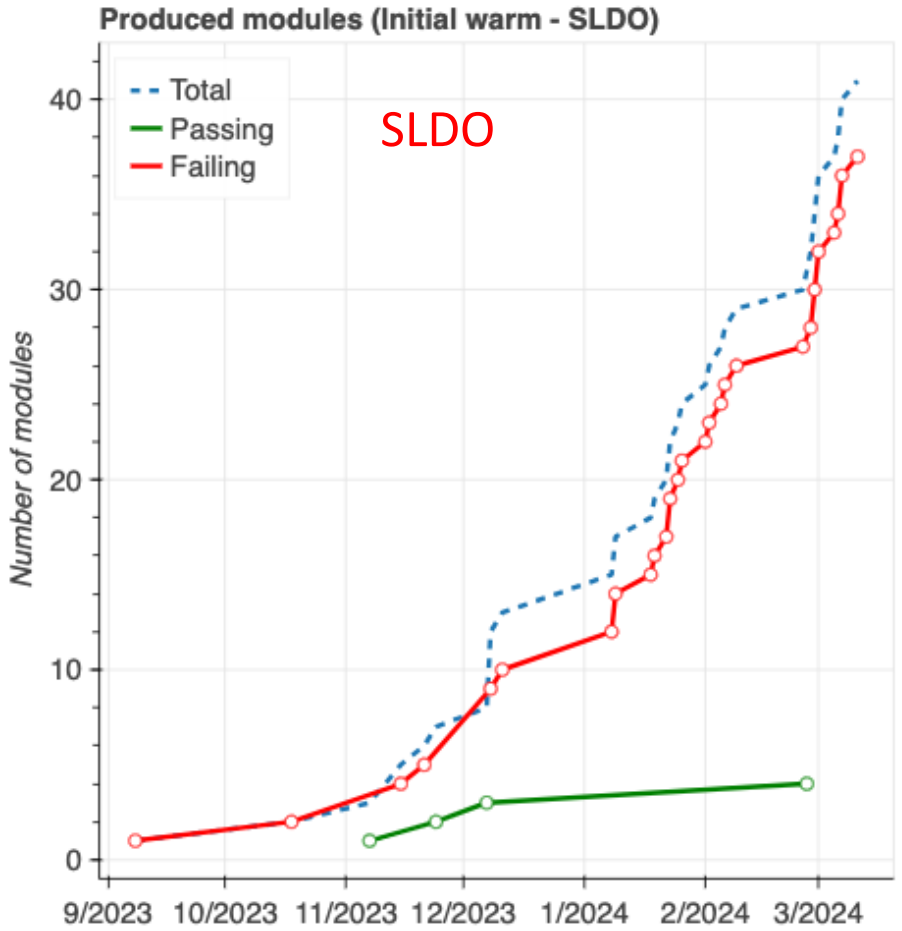
QC criteria are being adjusted and next release will give us results close to actual module yield

Reflections on QC procedure so far

Closer look at test results within module E-summary:



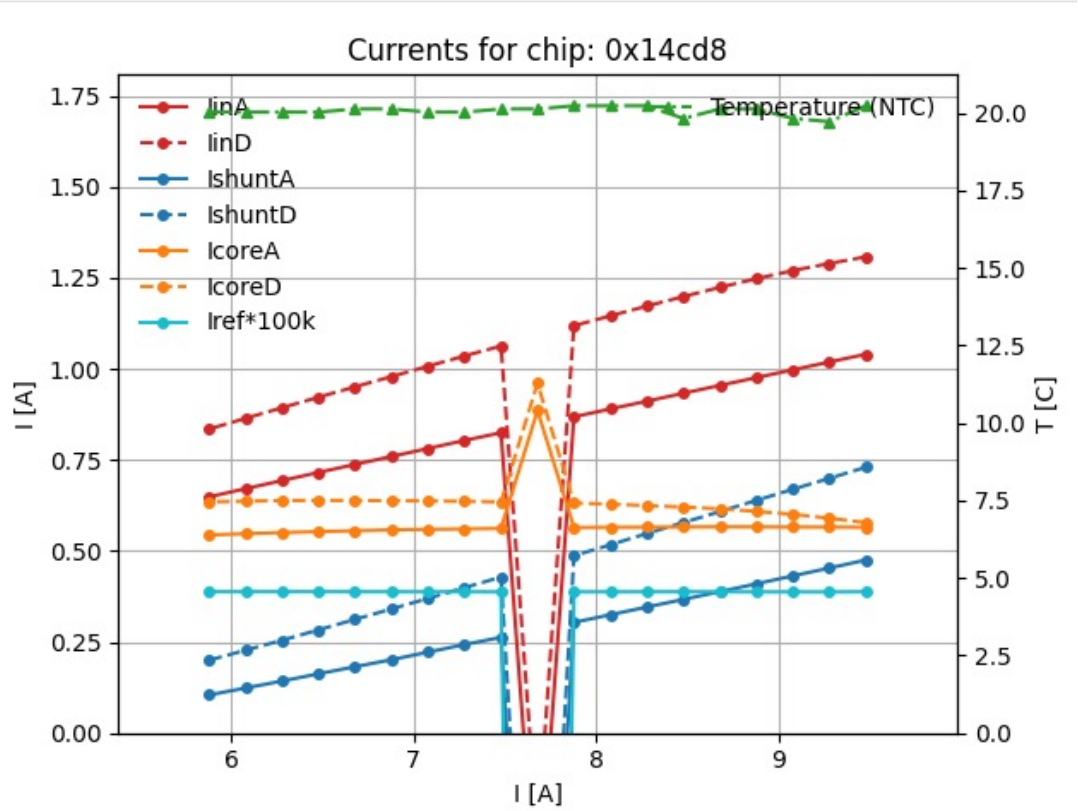
✓ High yield



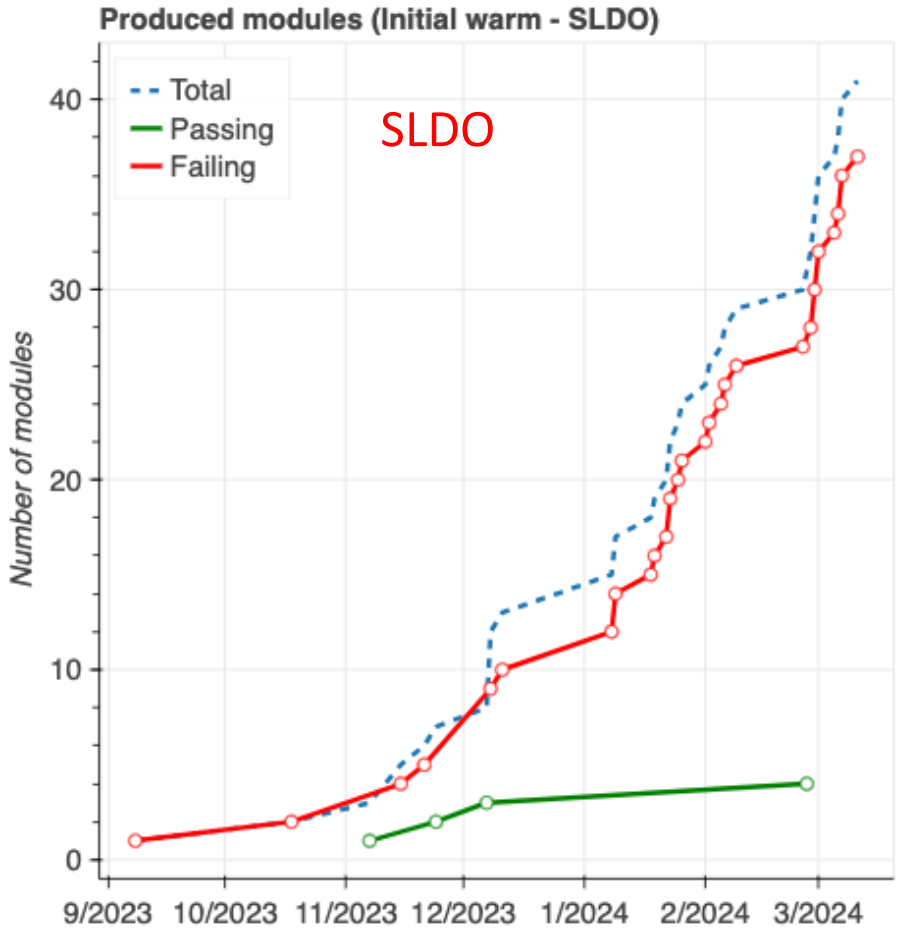
Low yield – Bad modules? QC criteria? Or measurement strategy?

Reflections on QC procedure so far

Closer look at test results within module E-summary:



Sometimes write register fails but script continues – [fix in progress]

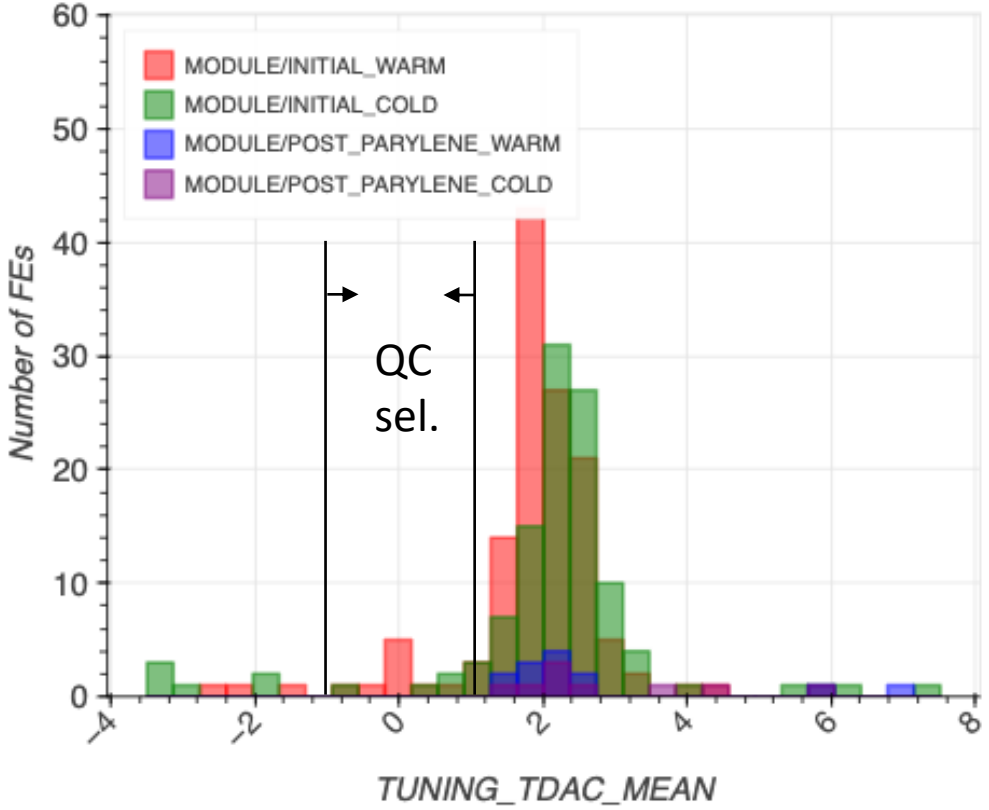


Low yield – Bad modules? QC criteria? **Or measurement strategy?**

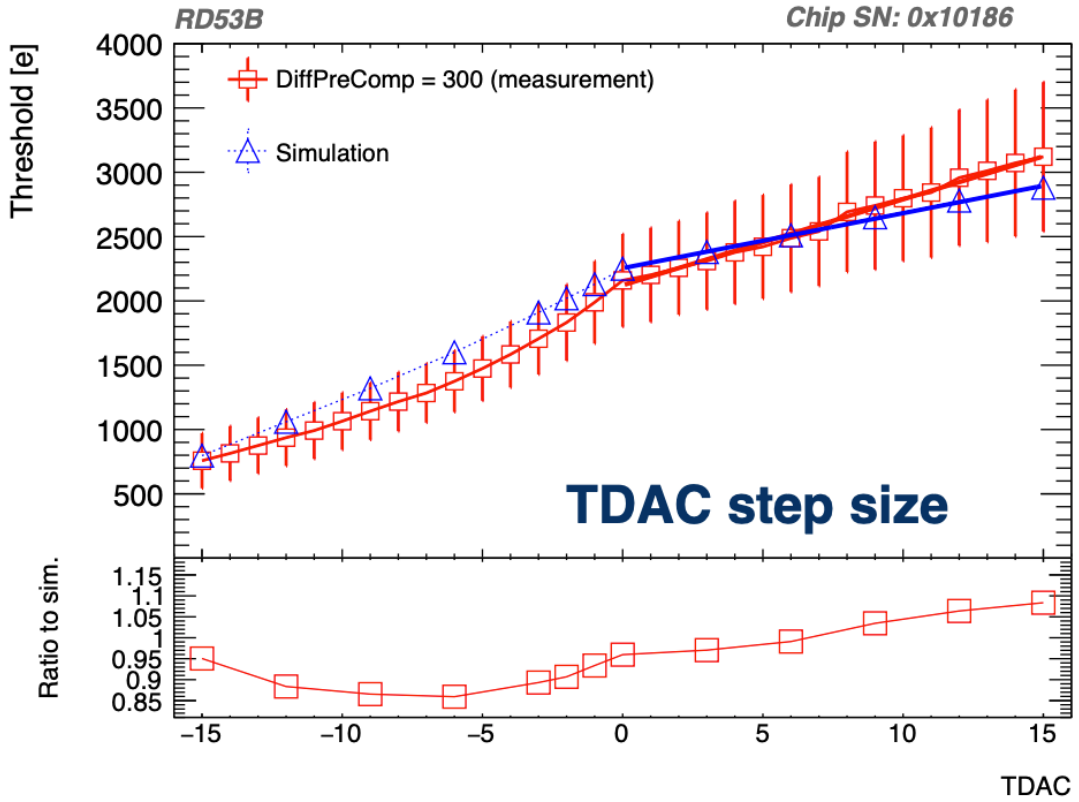
Reflections on QC procedure so far

Example QC selection which surprised us: **TUNING_TDAC_MEAN**

TUNING_TDAC mean/sigma original criteria did not take into account change in TDAC slope



QC criteria will be [updated](#) in next release

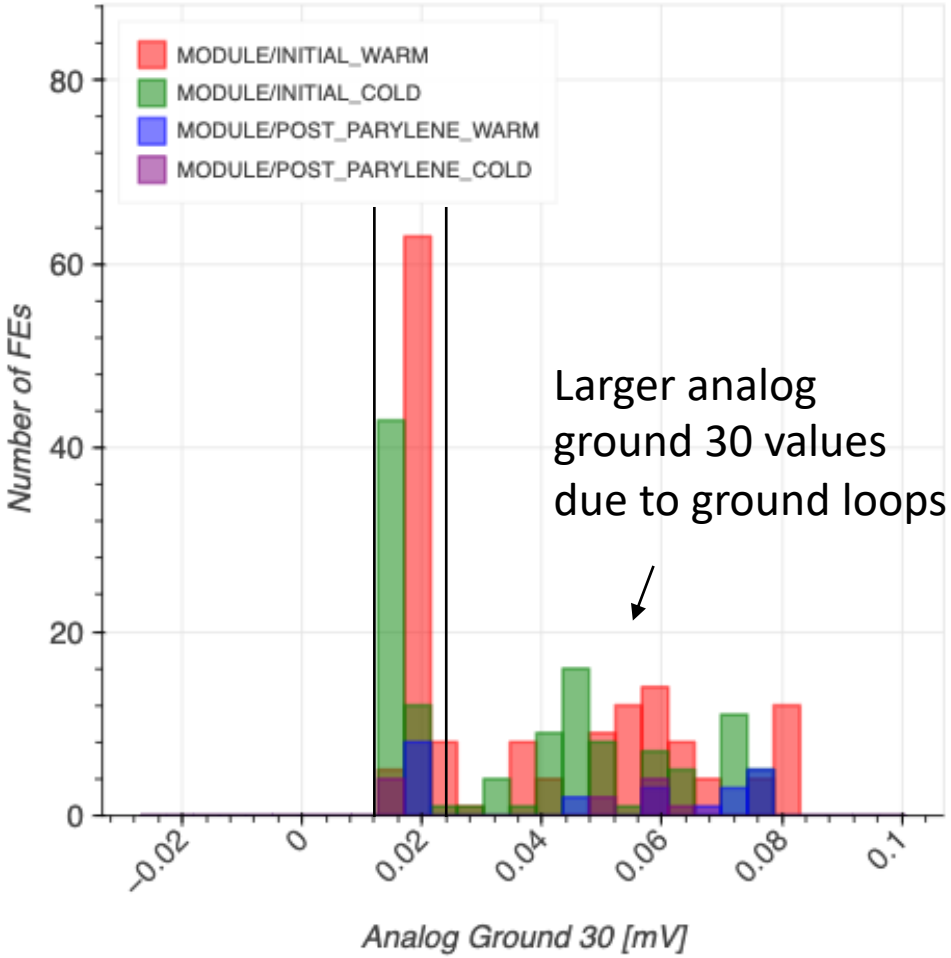


Slopes for positive and negative TDAC values are different → shifted TDAC mean

Reflections on QC procedure so far

Example QC selection which surprised us: **Analog ground 30**

- This is difference between the ground of the FE-chip and the ground of the module. This value is subtracted from every measurement made through the voltage multiplexor when converting raw voltages into meaningful values.
- QC criteria: [0.15, 0.23] mV
- Analog ground 30 is sensitive to ground loops – very useful in debugging grounding scheme in testing setups → still needs to be understood why
- Thanks to Argonne, IRFU and INFN Bologna for investigating this



Module electrical QC issues

We have identified several issues that we would like to understand before the module PRR.

1. IinA/IinD spread larger than expectations. Mis-calculated expectations? Or precision of multimeter?
2. Cooling – large spread observed between temperatures measured in different positions on flex
3. Power up – dependence on ramp-rate at different temperatures – module feature of setup issue?
4. Low-power offset – voltage saturation not taken into account in calculation of expectations
5. VDDD/A vs. trim saturation
6. “Core Column” issue – see next talk from Lingxin

We are actively working on understanding these issues. Please push data to the PDB to help.

Module electrical QC issues

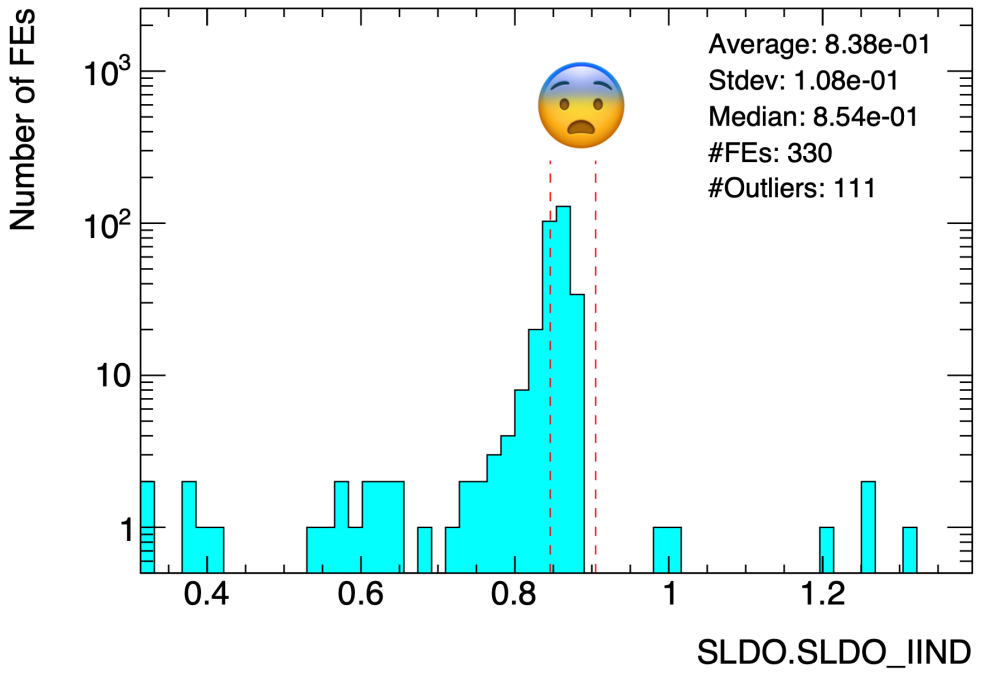
We have identified several issues that we would like to understand before the module PRR.

1. IinA/IinD spread larger than expectations. Mis-calculated expectations? Or precision of multimeter?

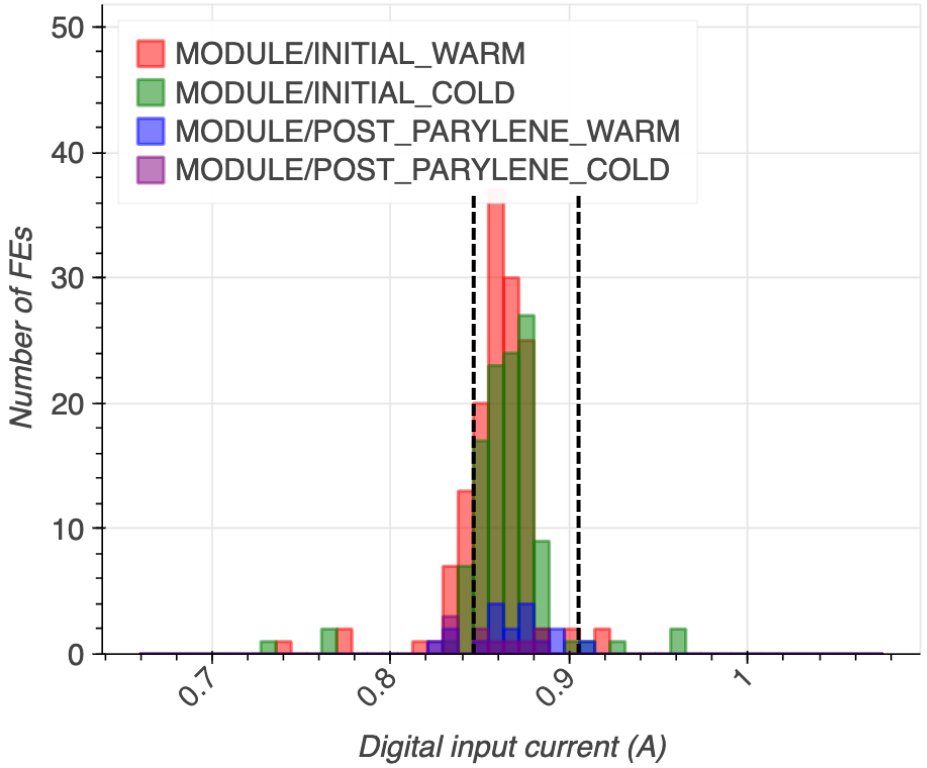
Modules tested in Japan:

~ 1/3 of FE-chips are out of spec:

Ask Japan for permission



Modules on PDB:

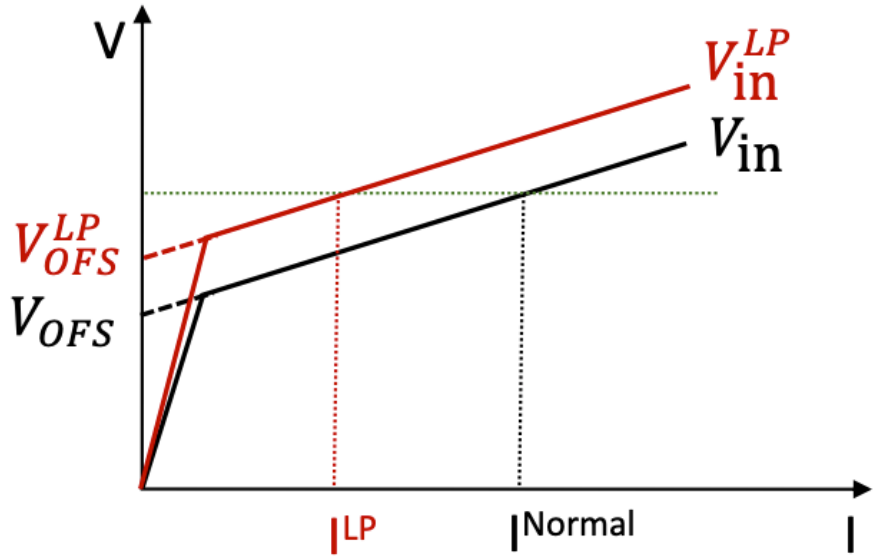


Module electrical QC issues

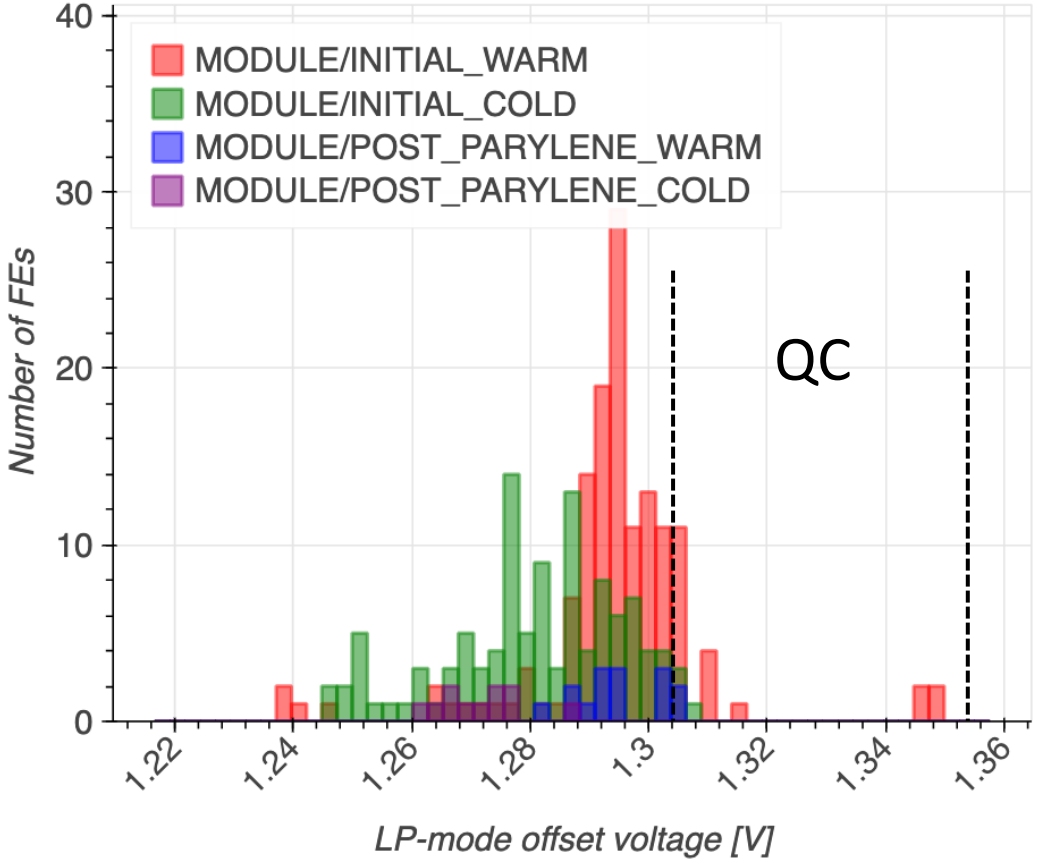
We have identified several issues that we would like to understand before the module PRR.

4. Low-power offset – voltage saturation not taken into account in calculation of expectations

~ 1.32 V
~ 1.00 V



Didn't take saturation of circuit into account when pushing V_{ofs} close to Vin (1.5 V) → could explain observations. But need to confirm in triplets.



Speed speed speed

Speed will become more of a priority as we move towards production.

Simple scans	Measurement (multimeter)	Measurement (calibrated ADC)	Upload + Analysis
ADC Calibration	5 m	-	30 s
Analog Readback	35 m	18 m	30 s
SLDO VI	21 m	7 m	30 s
Vcal Calibration	12 m	4 m	30 s
Injection capacitance	2 m	1 m	30 s
Low power mode	1 m	1 m	30 s
Overvoltage protection	1 m	1 m	30 s
Undershunt protection	3 m	2 m	30 s
Data Transmission	1 m	1 m	30 s
Total	**1h 21m**	**40 m**	**5 m**

* Single module in setup at LBNL using DMM6500 multimeter

Advanced scans	Measurement	Upload + Analysis
Minimum health test	10 m	2 m
Tuning	20 m	3 m
Pixel failure analysis	15 m	3 m
Total	**45 m**	**8 m**

Bottom line: electrical testing takes ~ 2h 20m with multimeter, ~1h 40m with calibrated ADC

Recommendation is still to use the **multimeter** to collect data. In future release we will switch to using the calibrated ADC. This opens the possibility for further time improvements by integrating QC-tests within YARR framework (but user-interface will remain the same).

We can also speed up QC procedure by:

- Parallelization
- Drop/slim tests if QC parameters don't change → need global analysis of more QC data first

Reporting in module QC

See reporting session for more information

Goal of reporting in module QC:

- Are modules meeting our electrical expectations?
- Where can we slim / drop tests in QC procedure?
- Can correlations between different tests results tell us something about critically-failing modules?
- …

We are designing a framework to analyze QC data from the production database (PDB) and make reporting plots.

Framework will work as follows:

1. Query **all** relevant information for pixel modules from the PDB

   → slow (~ 30 minutes for 123 modules, w/o cache). Will happen once per week.

2. Save this information into a flat data structure (pandas dataframe)

   → fast, but ideally will happen only once per week.

   } Converging on design now

3. Perform analysis / make plots

   → fast, performed on demand.

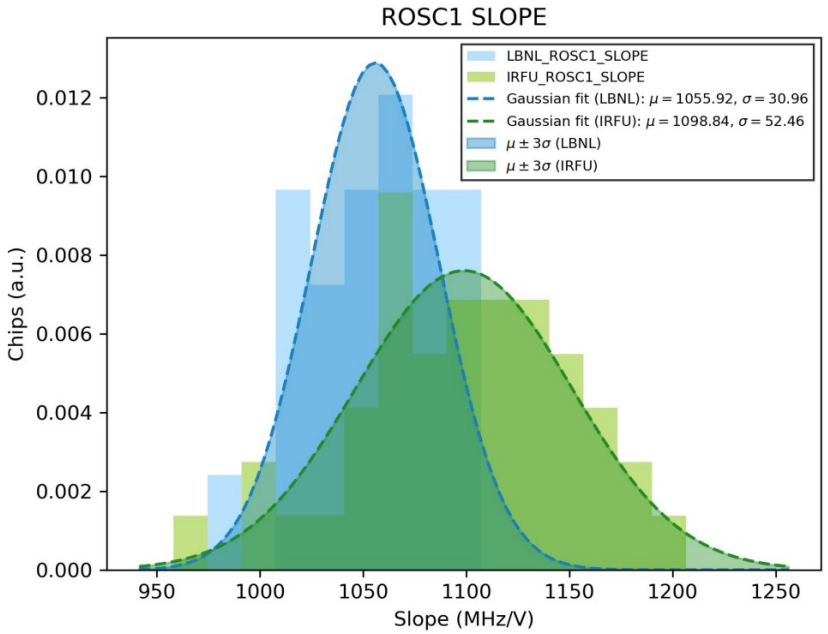
   } Crowd-source

Reporting in module QC

See reporting session for more information

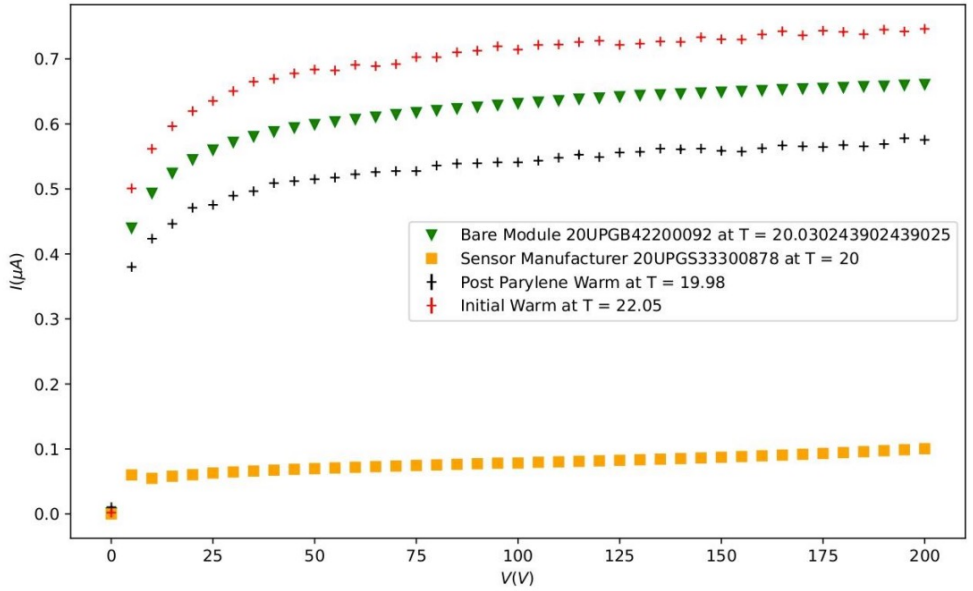
Work on analyzing QC data from production database has already begun – now we are combining efforts

Analysis of ring oscillator data:



Kehang Bai, Christina Dorofeev (link)

Analysis of IV-scan data:



Sayantan Dutta (link)

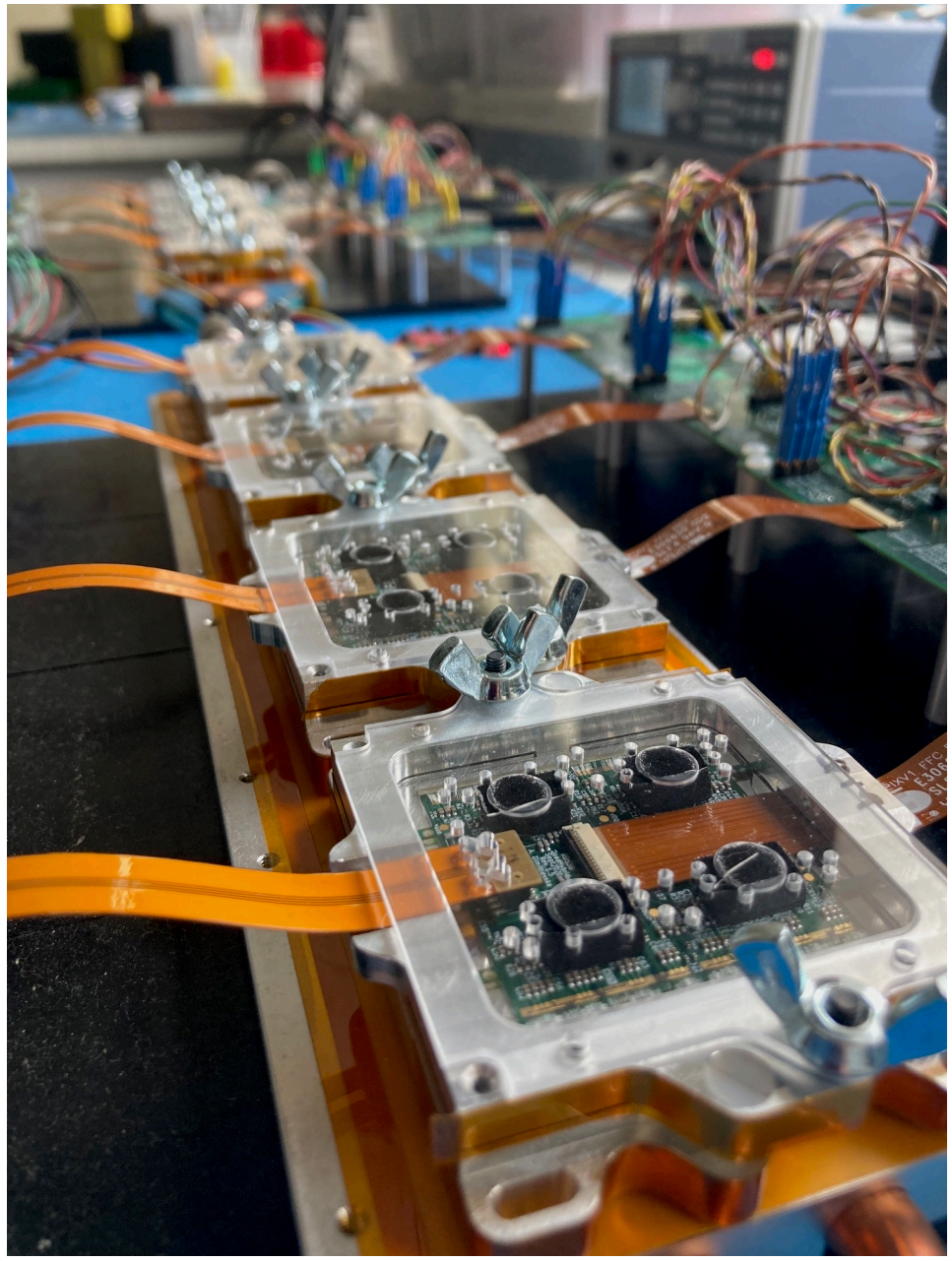
Summary

Module QC in preproduction is going well – keep it up!

Community support / debugging is important – please keep reporting issues.

Our top priorities now are:

1. Converging on QC criteria that will reflect actual yield
2. Understanding several issues before PRR
3. Speeding up QC procedure
4. Developing reporting framework to help with all above points



Backup

Resources

Electrical QC Documentation:

- Module electrical QC document (EDMS, Gitlab)
- Module QC Stages and Tests
- Module Site Qualification
- Template for module QC qualification (11.1-11.3): template

LoclalDB useful links:

Local Database User Support mattermost

LocalDB documentation

LocalDB issue tracker

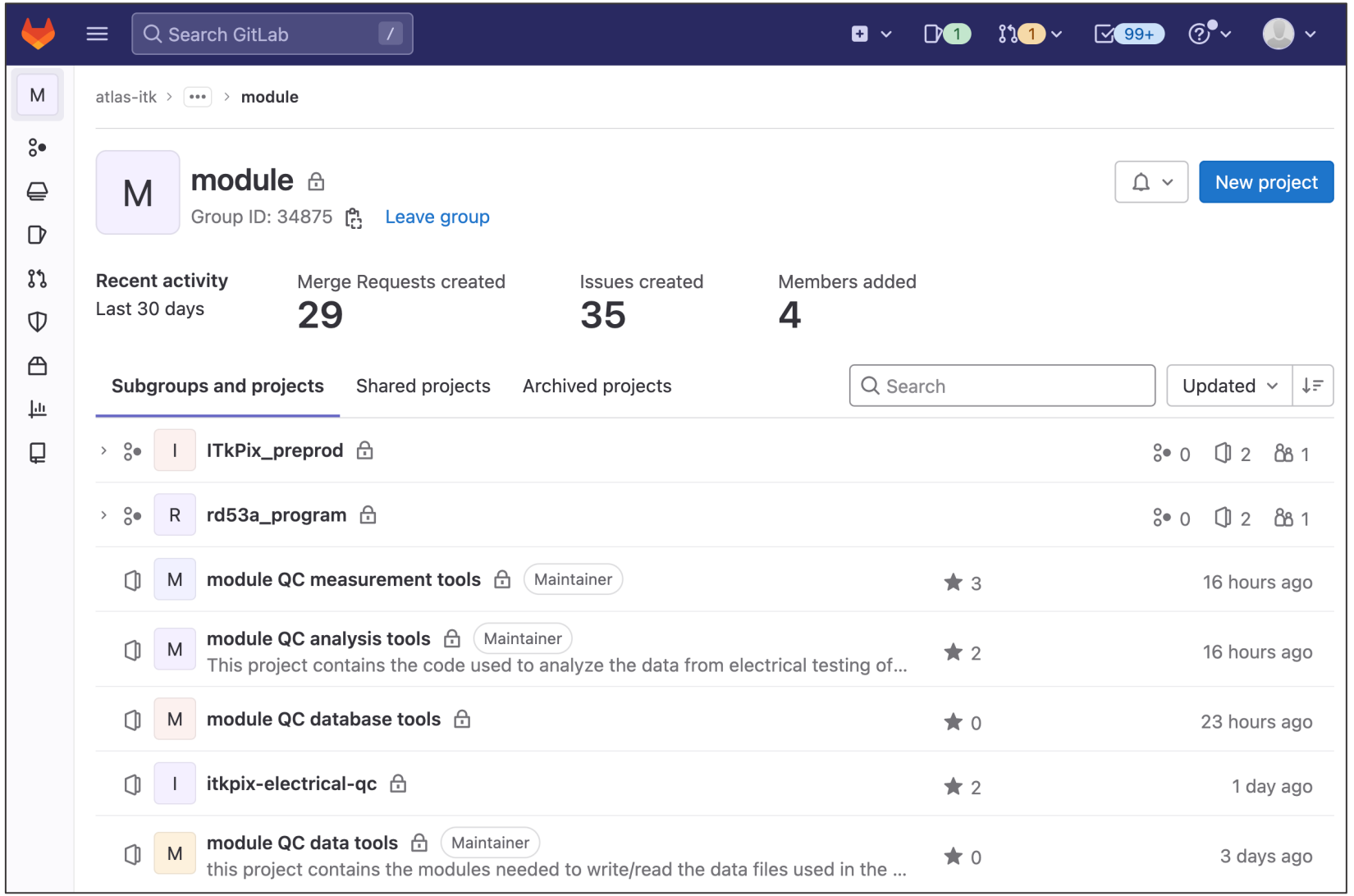
LocalDB demo videos

Support:

- Electrical testing meeting: **Tuesdays, 5 pm CET**
- Follow regular updates from electrical QC in Module WG meeting: **Thursdays, 4 pm CET**
- The Mattermost Electrical Testing channel
- Make an issue on gitlab : report problems encountered during testing, helps keep discussions in the same thread if mattermost gets too hectic
- Above support is sufficient so far, however module QC group will setup “office hours” if needed

Development of tools

https://gitlab.cern.ch/atlas-itk/pixel/module



So far we have received **positive and constructive feedback** – we encourage users to document their difficulties / questions in issues so we can develop in a transparent way

People can contribute! Get in touch with us if you want to help develop.

Follow technical discussion of tools at the Electrical testing meeting (Tuesdays, 5 pm CET)

Reporting in module QC

Requirements for data structure:

- Conceptually easy to understand (like a giant google form)
- Fast access to data (columnar operations)
- Compressed efficiently (columnar storage)

We have converged on using a **flat pandas dataframe** with 1 row / module containing all information for those module's stages and (grand)children.

Dataframe has passed stress tests with dummy information for 12,000 modules.

Analysis of QC data

Eventually we will use QC data from pre-production to optimize QC procedure in production

We are not there yet. At the moment we want to collect data to:

- Adjust QC specifications
- Understand what is the module yield driver
- How frequently do we need to re-perform tests? Do chip parameters change? If so, why?

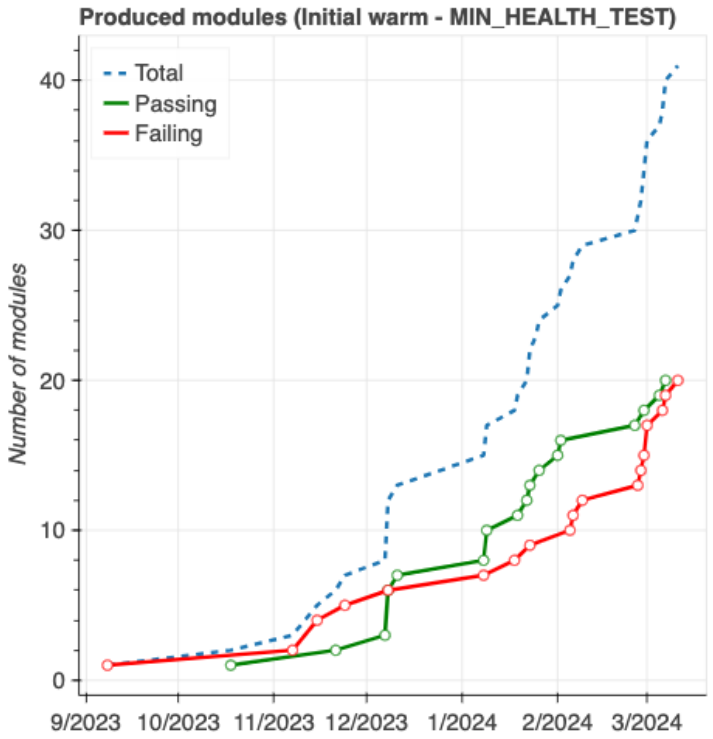
Backup: Electrical pixel failures

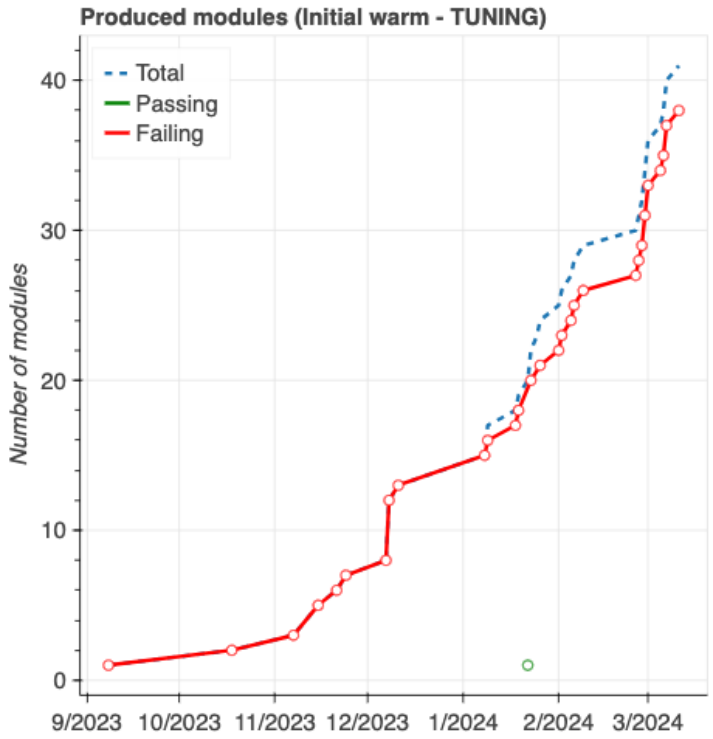
Failure	Scan type	Criteria
Digital Dead	Digital Scan	Occupancy<1% of injections
Digital Bad	Digital Scan	Occupancy<98% or>102% of injections
Analog Dead	Analog Scan	Occupancy<1% of injections
Analog Bad	Analog Scan	Occupancy<98% or>102% of injections
Tuning Bad	Threshold Scan	|Pixel threshold - Mean threshold distribution| $> 5\times40e^*$
High ENC	Threshold Scan	Mean pixel noise $< 200e$ (L0) or $< 300e$ (L1/L2)
Noisy	Noise Scan	Occupancy$> 10^{-6}$ hits per BC
ToT Memory Failure	ToT Memory test	Occupancy <100% of injections

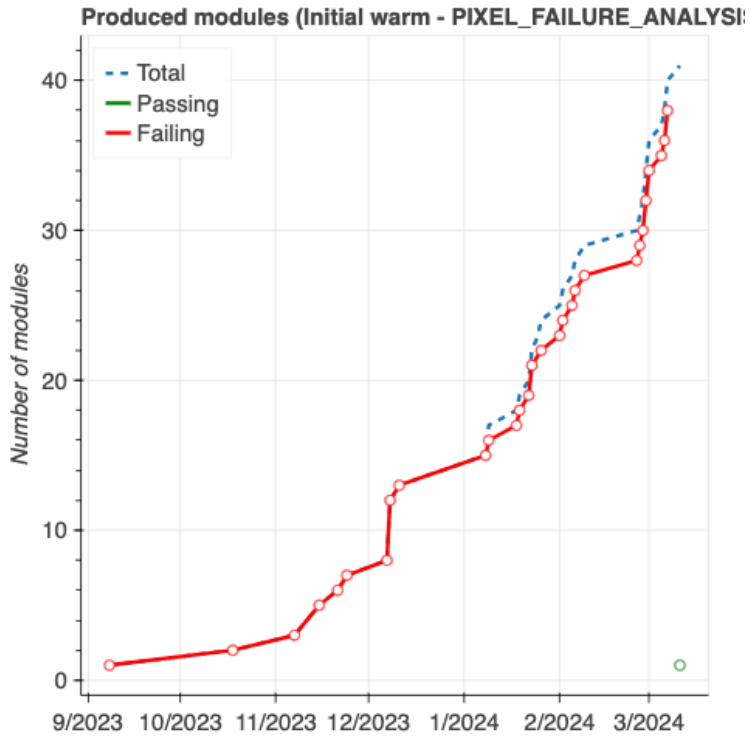
Table 10: Electrical pixel failure categories

From electrical QC document

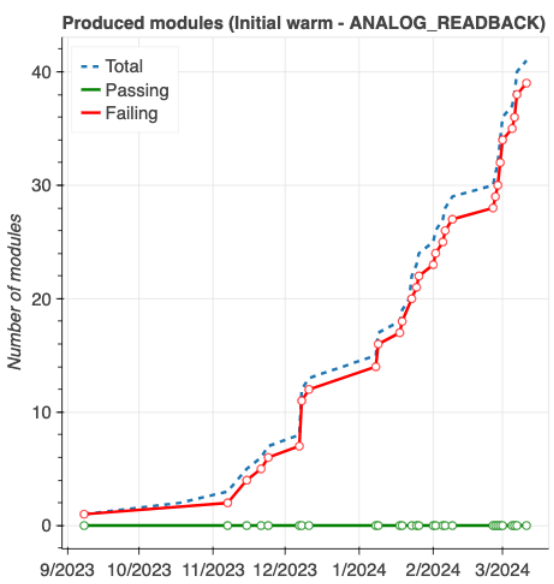
Backup: Module yield

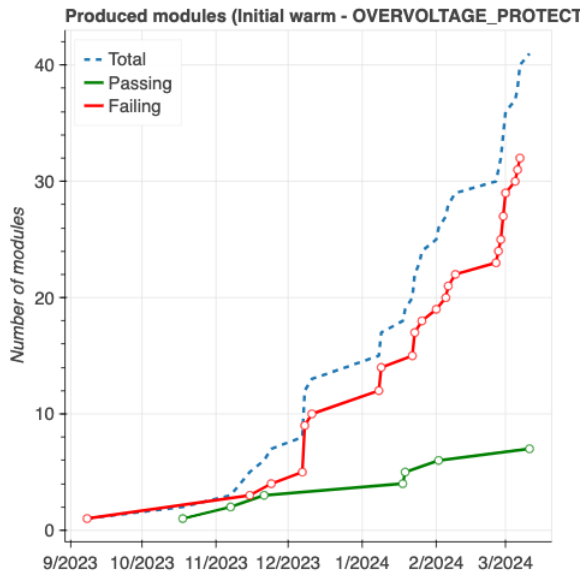


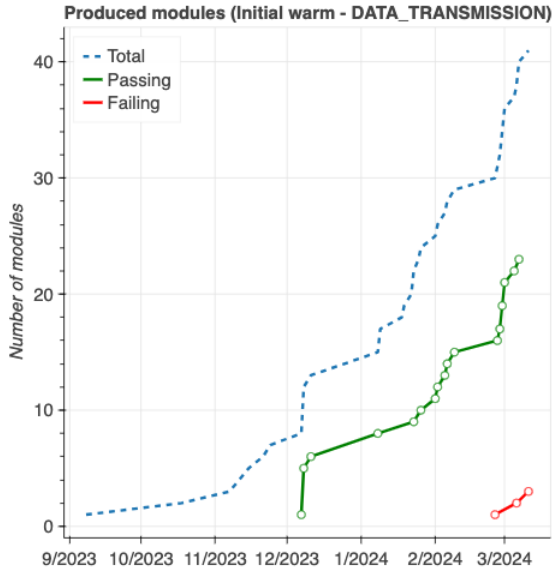


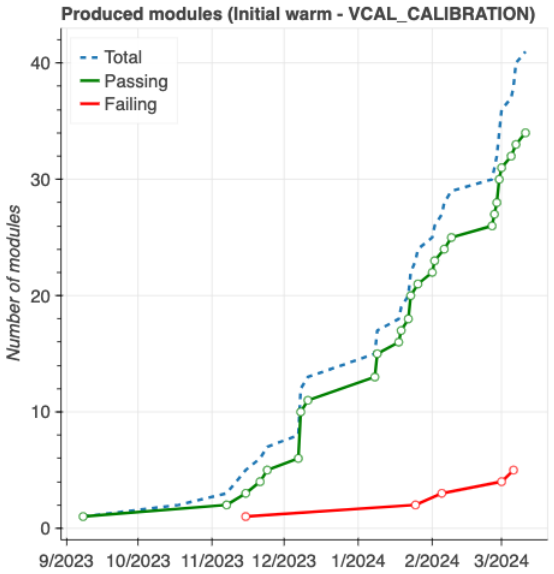


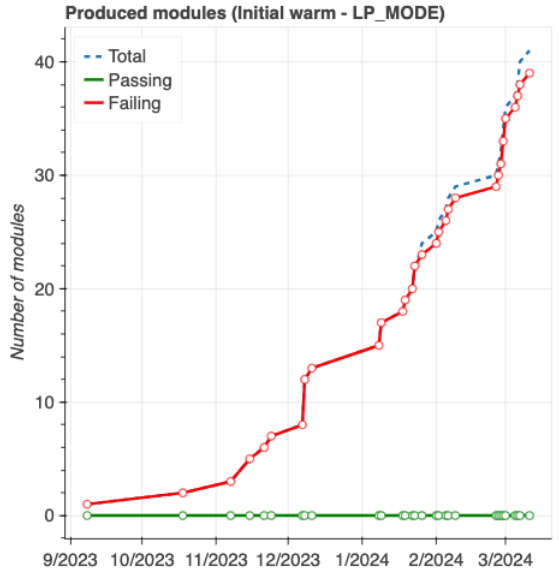
Backup: Module yield

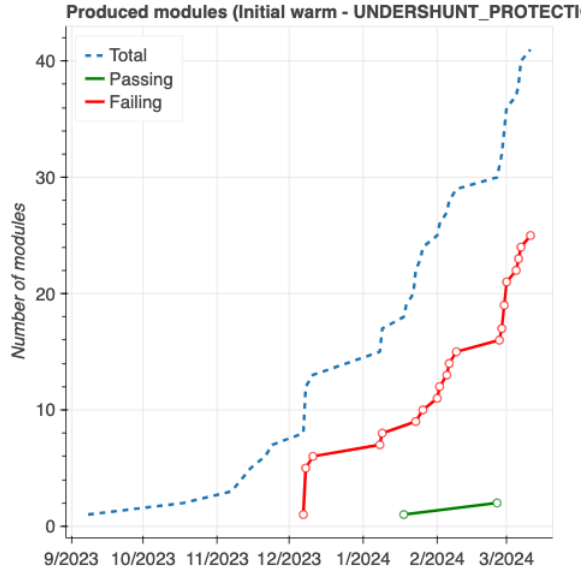


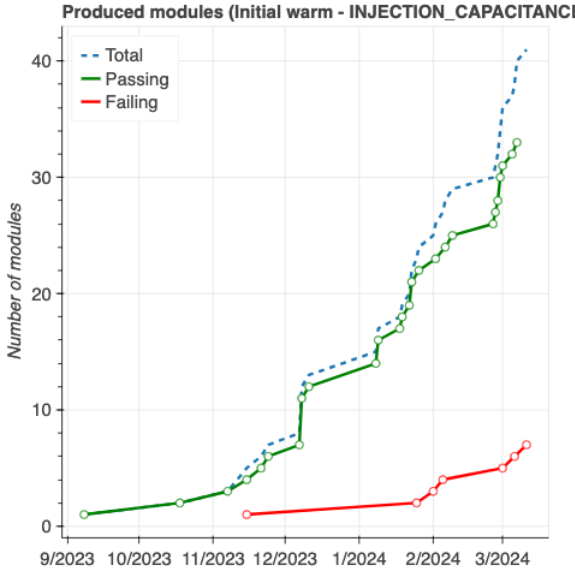












- Put times with calibrated ADC
- We need to run with the multimeter at least once. In the future we will rely more on the ADC side. And then we can optimize further. You can actually fully parallelize them and accelerate them by quite a bit.
- We are reasonably close to ~ 1 hour without the need to drop scans.
- For preproduction all bets are off. we will run everything to get as much data as we can. For production, it would be good if the module coordinators could build a good understanding of what the requirements (in terms of timing). Every site has their own requirements. What if its an unreasonable time?
- Koji was saying we should only test once at the end. Theoretically this is fine as long as you are confident that parylene coating doesn't do anything. Also loading module into TC chamber takes time.
- Ask module coordinators - what are the bottle-necks at each site? Is it really electrical testing? In order to reach a certain rate, how many hours per day do we have? And then once we have that time we can divy up the time - like how much does visual inspection take?. You should be able to do it in a day. Overnight, ideally. Doing it in hours is bonkers. Even if testing was very fast, you would need to do so much to move modules around.
- There is a site qualification block called "rate" - look into this. Ask Richard and Jessica about this.

- I should mention open issues: https://docs.google.com/document/d/1sgnf9MSkElwevPjz9obWe5XSPE_Jv55zk5HKyhbvQps/edit
- Issues that we want to understand before the PRR.
- AnaGnd30: This measurement won't make or break a module. It is just a curiosity that we don't fully understand in some setups, and it is related to ground loops.
- Check QC data with Japan data. Important for Vmux measurement and cooling data.
- Make it clear that we aren't just loosening the QC criteria willy nilly, and also the original QC selections are usually quite motivated.
- What about japanese temperature plot? We are trying to justify why we are being a pain in the ass with QC talks. Don't show the plot. But say that we have seen cases where don't make sense. And its due to sub-optimal setup. Is saverio's system qualification sufficient here?
- We didn't enforce the same setup across all sites, and therefore we do expect differences

- Power-up: likely setup issue with power supply.

- Push triplets under the carpet

- VDD saturation, not understood but its not really a show stopper because saturation is above 1.2V, what do we care?

- Apparently in wafer probing we run at 1.6 V. It's in serial powering mode, but we run at 1.6 V. At the module stage we run at 1.5 V