X-ray irradiation update

Timon Heim, Maurice Garcia-Sciveres, Maria Mironova

Weekly student instrumentation meeting

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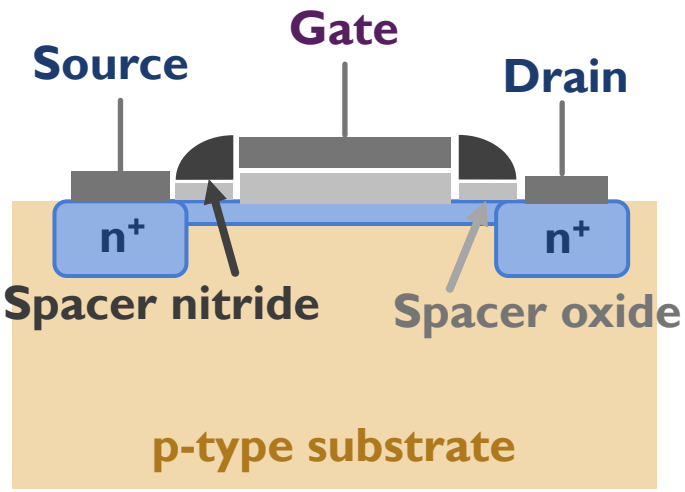
BERKELEY LAB

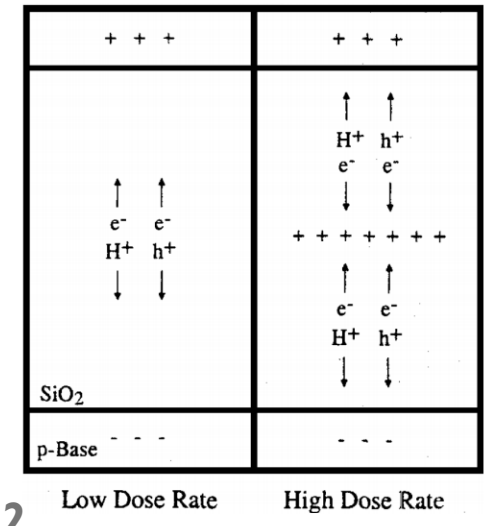
ATLAS EXPERIMENT

Radiation damage in transistors

- Radiation damage in transistors mainly dominated by damage in SiO_2 and at Si-SiO_2 interfaces
- Radiation damage depends on:
  - Technology (i.e. minimum possible feature size) → 65 nm in ITkPix
  - Transistor geometry and layout → W and L of transistor, or W/L, also referred to as transistor strength, smaller transistors suffer more
  - Exact transistor layout
- Environmental and irradiation parameters:
  - Temperature (**more damage at high temperatures**, maximum operational temperature in HL-LHC expected to be -10 C)
  - Supplied voltage (VDDD voltage in ITkPix chips)
  - **Dose rate:**
    - More damage observed at low dose rates

  → Scaling seems to highly depend on the transistor properties, needs to be characterized in detail for ITk





More details in: F. Faccio et al. 1, 2

Expected doses in HL-LHC

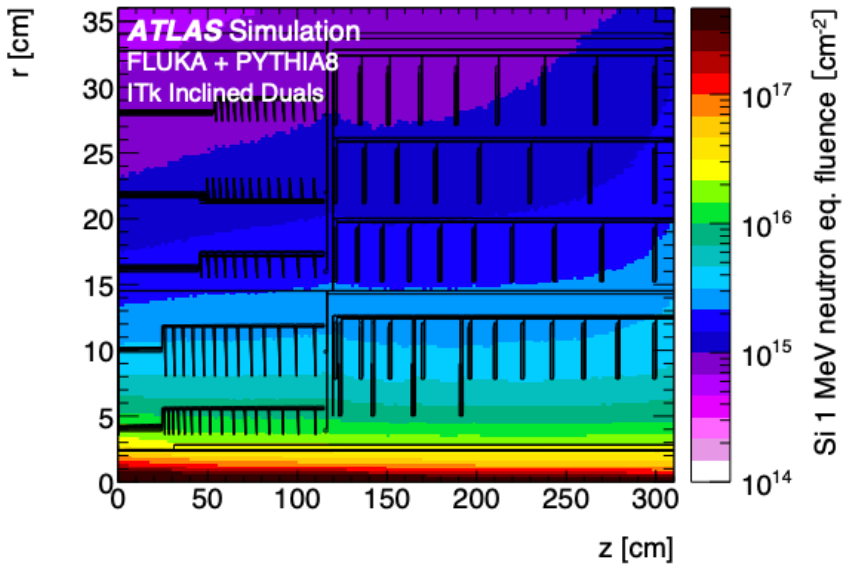
- For HL-LHC, expect maximum TID of **1 Grad** and 1.9 x 10^{16} n_{eq}/cm
- Including 1.5 safety factor

→ Innermost ITk layers are planned to be replaced after half of ITk lifetime (2000 fb^{-1})

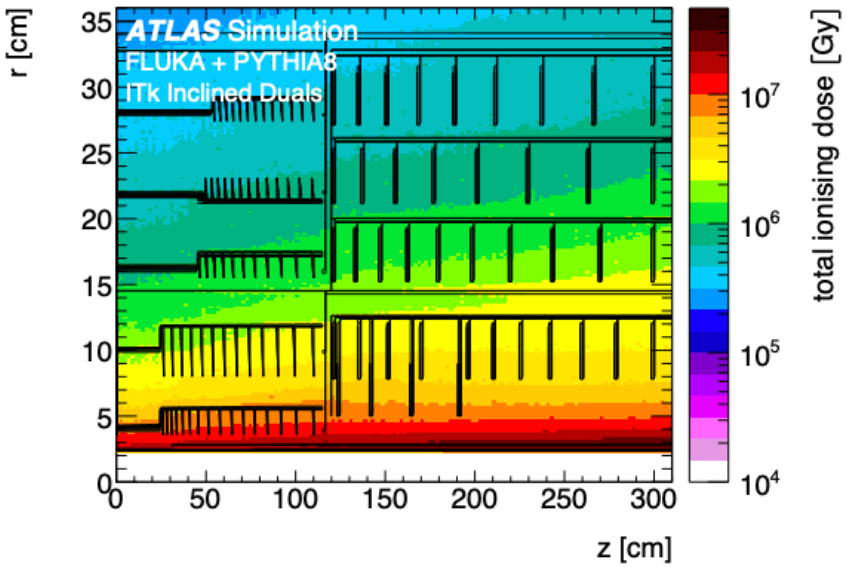
- **Dose rate** expected in the innermost ITk layers: **20 krad/h**

	ATLAS innermost pixel layers	
	Fluence	TID
IBL (300 fb^{-1})	5 x 10^{15} n_{eq}/cm^2	250 Mrad
HL-LHC (2000 fb^{-1})	1.9 x 10^{16} n_{eq}/cm^2	1 Grad

Fluence

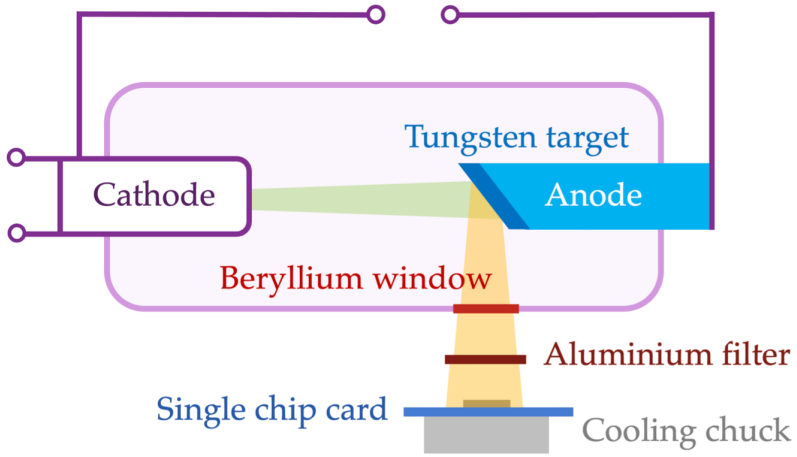


TID



Irradiation procedures

- Performed several irradiation campaigns at varying dose rates for ITkPixV1 and ITkPixV2
- Following common configuration of X-ray setups for all ITkPixV1 irradiations (40 kV tube voltage, 150 µm Aluminium filter)
- Irradiation procedure:
  - Perform pre-irradiation measurements of ring oscillators
  - During irradiation, read the ring oscillator frequency (at least every 0.1 Mrad) and keep the chip busy by running digital scans
  - Keep the chip cold (-10 ± 1 C) → Corresponds to maximum expected **operating temperature of chip of -7.5 C** (Details)
  - Monitor the VDDD voltage and temperature



- Additionally, perform long-term low dose rate irradiation of RD53A chip, using Kr-85 source (at the expected HL-LHC dose rate of 20 krad/h) → (**SL**ow **I**rradiation of **P**hase-2 **Pix**e**l** **R**eadout)

Ring oscillators in ITkPixV1

- ITkPixV1/2 chip includes ring oscillator for radiation testing (located at chip bottom)
- 42 ring oscillators made with different logic cells and different transistor sizes (strength 0, 1 and 4)

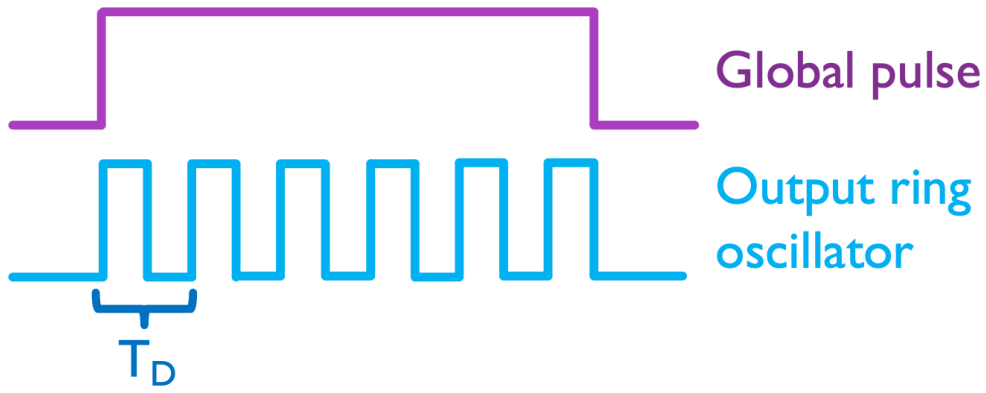
→ ITkPixV1 actual digital logic does not use strength 0 gates anymore

- Bank A has exactly the same ring oscillators as RD53A
- Bank B includes 34 additional ring oscillators
- Each oscillator drives a 12-bit counter, enabled for a given period of time

→ **Calculate frequency f or delay $T_D = 1/(N\ f)$**

- Delay before irradiation of order 0.1 ns
- During irradiation the gate delay increases

→ **Too large (>200%) delay will cause digital logic to fail**



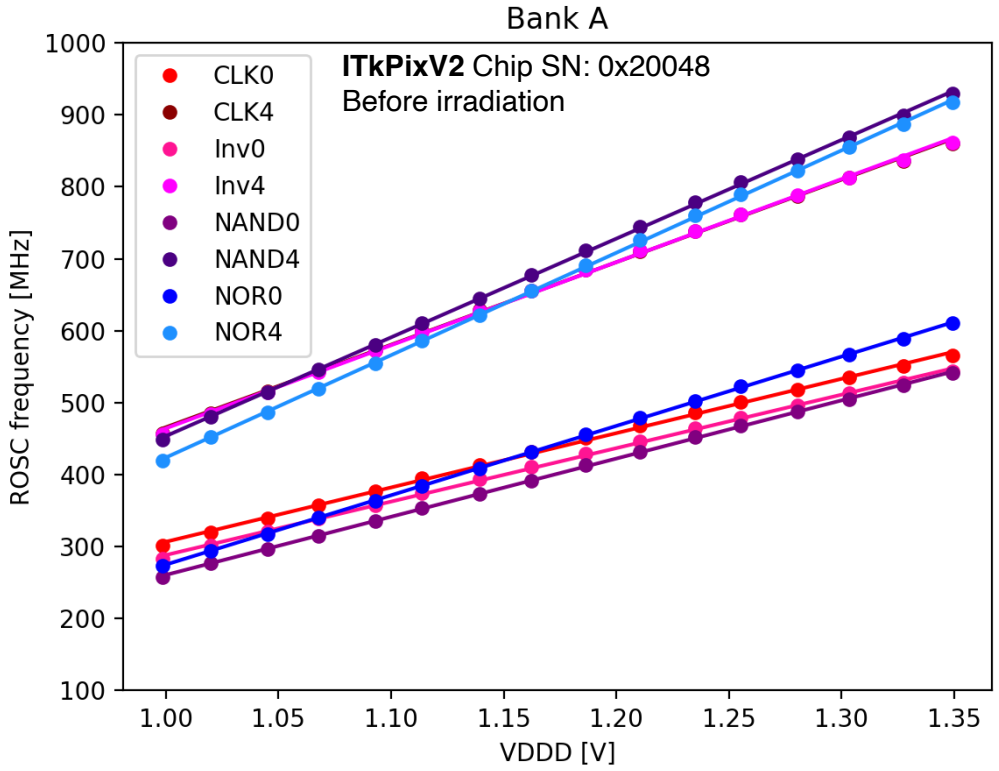
Group	Types	#
A/B	CLK, Inv, NAND, NOR	3 x 8
B FF	Various flip-flop gates	6
B LVT	LVT inverter & 4-input NAND	4
B CAPA	Injection-capacitor loaded 4-input NAND	8

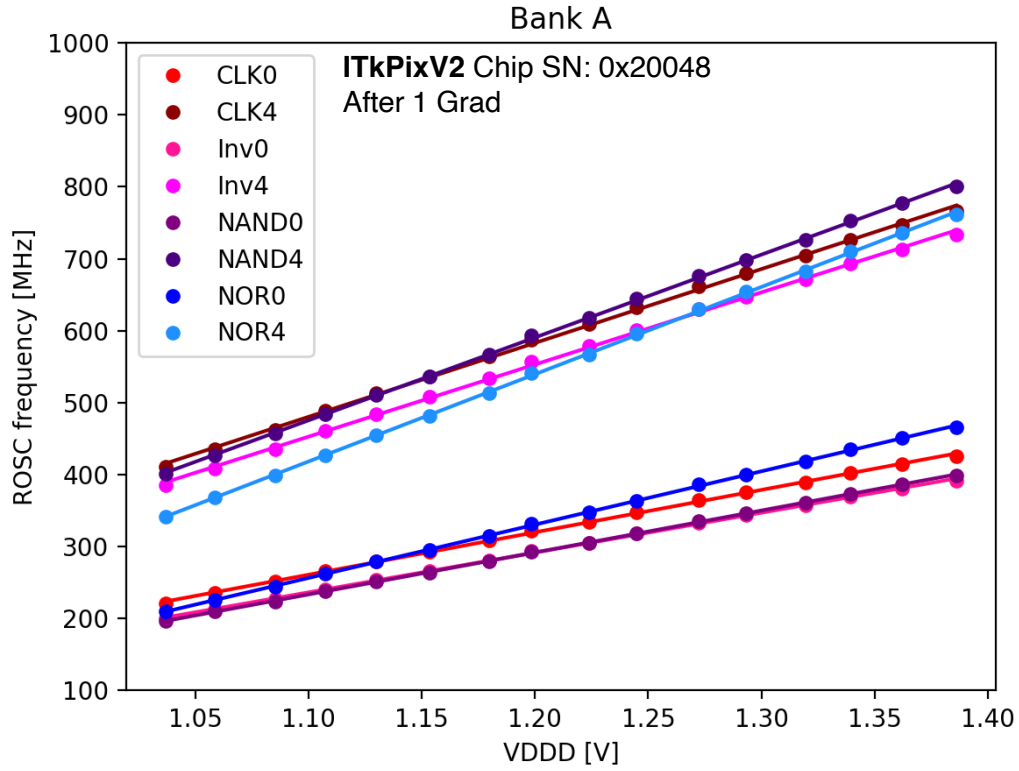
Ring oscillator vs VDDD

- Before irradiation, characterise ring oscillator frequency as a function of VDDD

→ See the expected linear behaviour with VDDD, and can use the slopes to correct ring oscillator frequencies to account for drifts in VDDD with irradiation

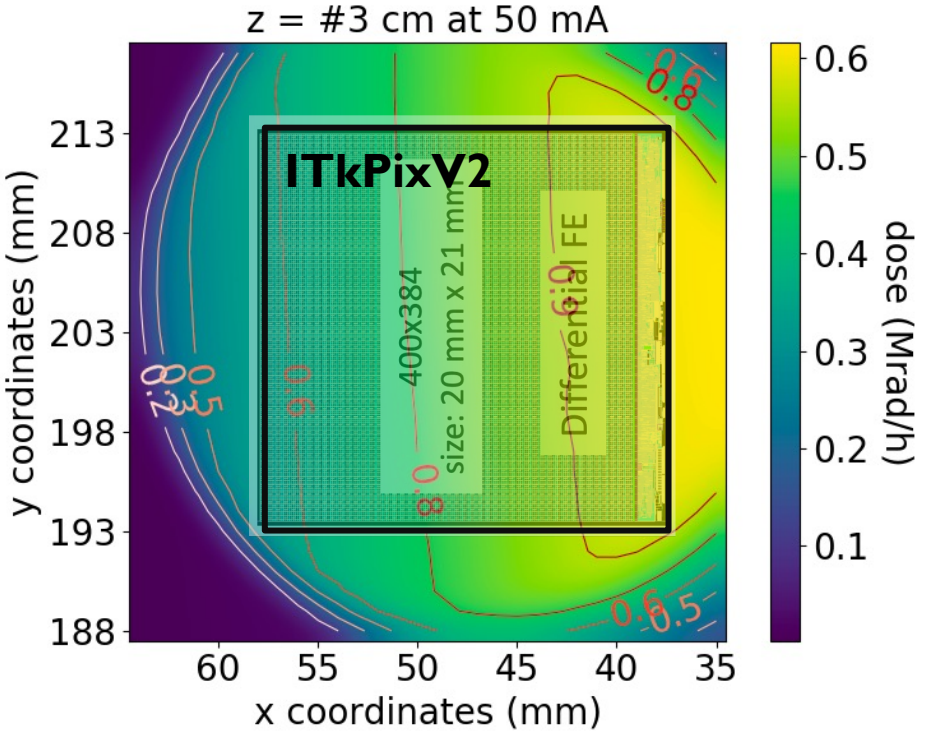
- Repeat the curves after irradiation, as the slopes change with irradiation and interpolate between the two points for the correction





LBL X-ray setup

- Many X-ray irradiations performed to characterise radiation tolerance for ITkPixV1
- Need to repeat measurements for ITkPixV2 and continue characterisation of the different chip features
- Ran one X-ray irradiation in Oxford last year (at 5 Mrad/h), see this update
- Also set up X-ray irradiation at LBL → dose rate of 0.5 Mrad/h and non-uniform beamspot
- Irradiation focused on **end of chip** (i.e. chip voltages and ring oscillators)
- Monitor everything available via the VMUX, and measure ring oscillators



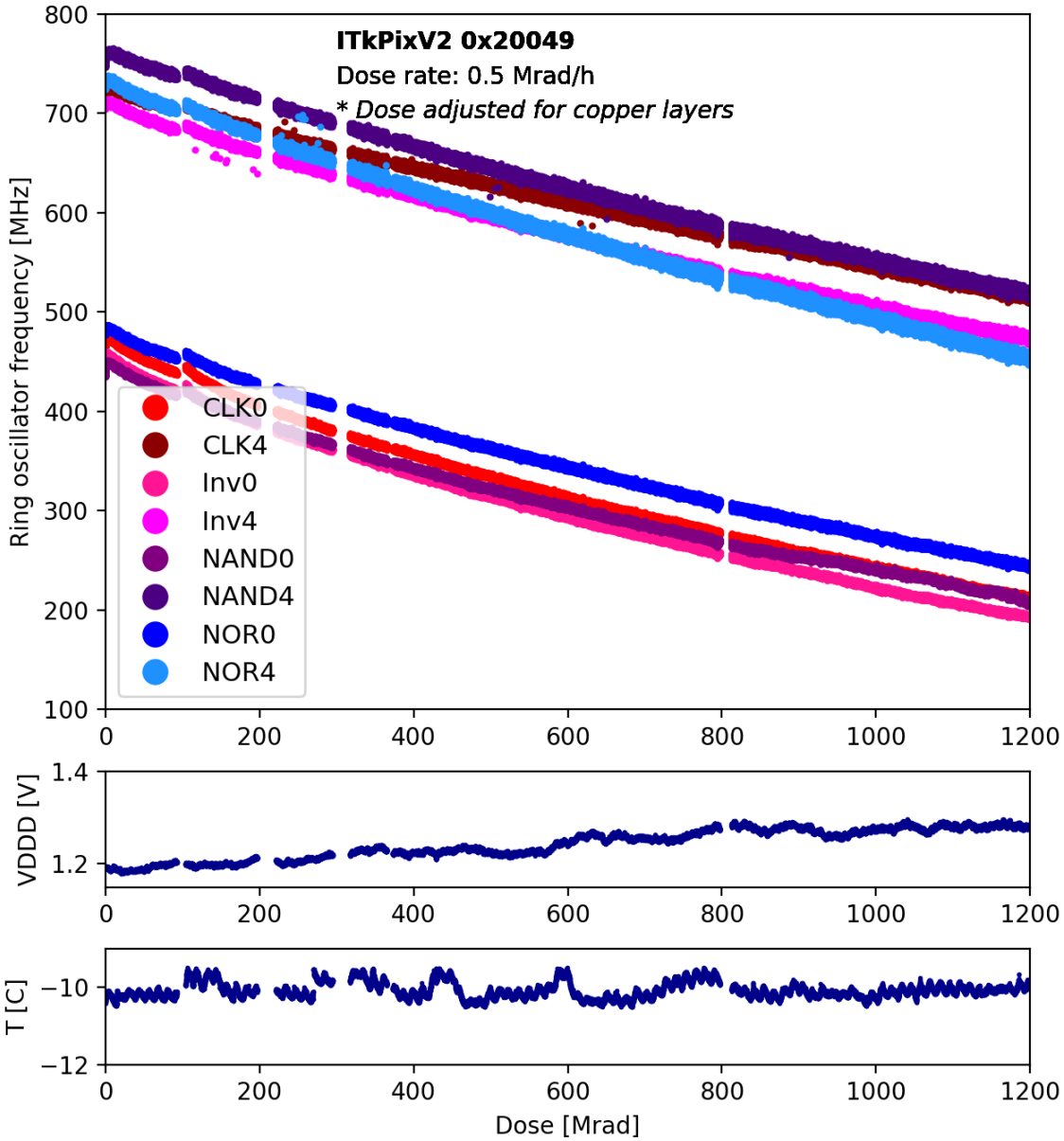
Environmental monitoring

- Irradiation ran from September until the Christmas break
- Set up Grafana to monitor irradiation status
- Generally irradiation ran smoothly
  - Had to power down X-ray machine once due to power outage
  - → Left the chip warm and unpowered
  - Irradiation script crashed a few times
  - → Need to make more reliable and set up alerting for next time
- Reached total dose of 1.2 Grad

Ring oscillators

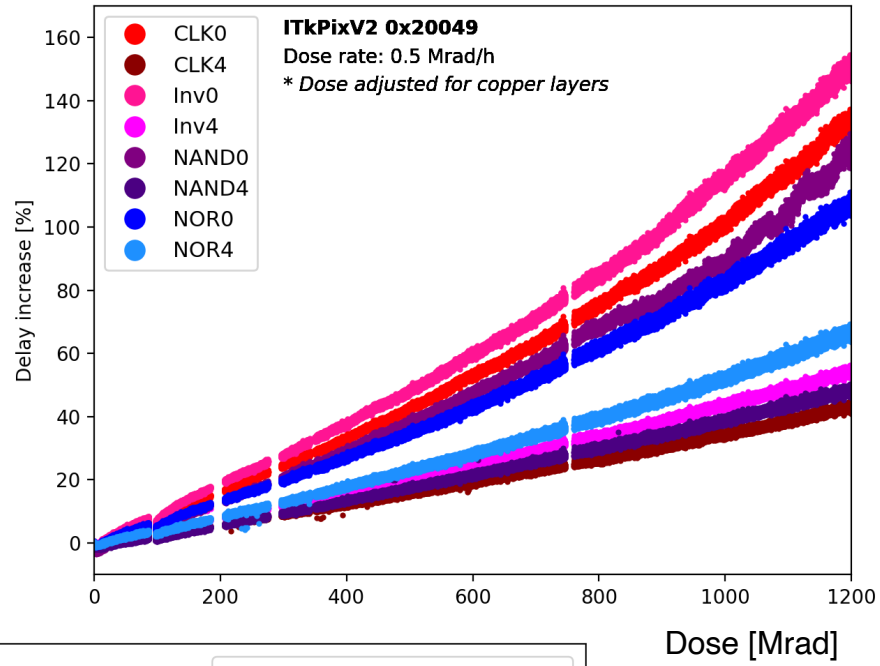
- Ring oscillator frequency with irradiation
- Corrected for drift of VDDD with irradiation
- Stopped irradiation at ~100 Mrad due to power outage

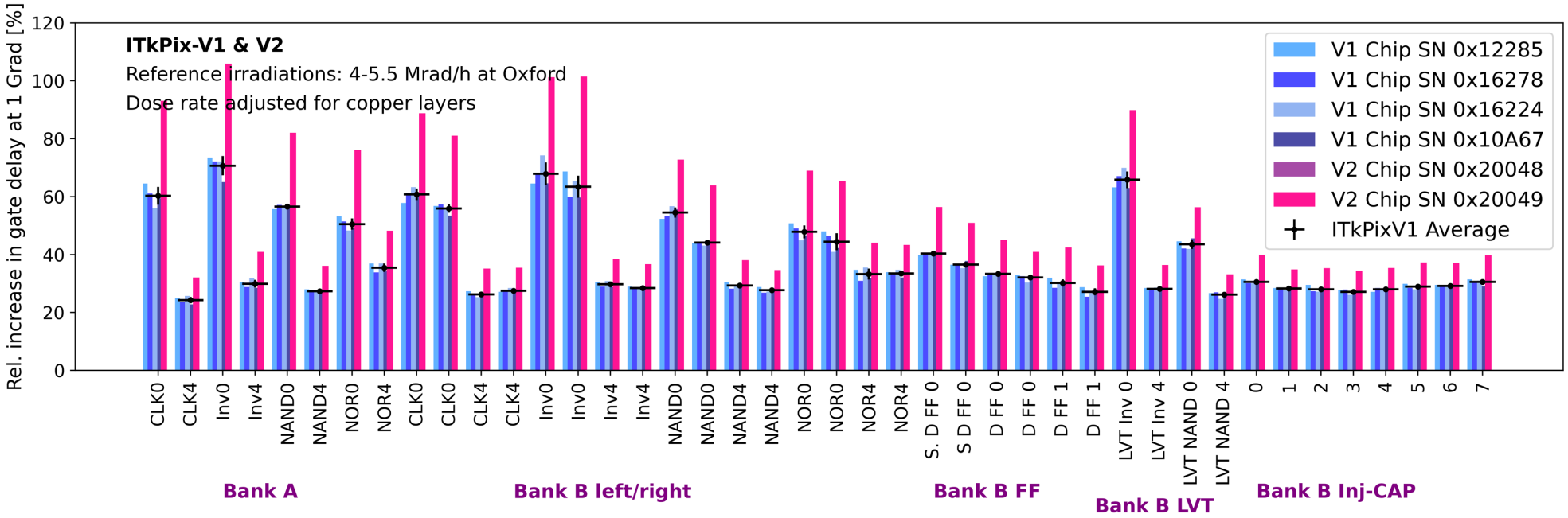
→ Can see some annealing happened but with when restarting irradiation frequency continues with the same trend



Ring oscillators

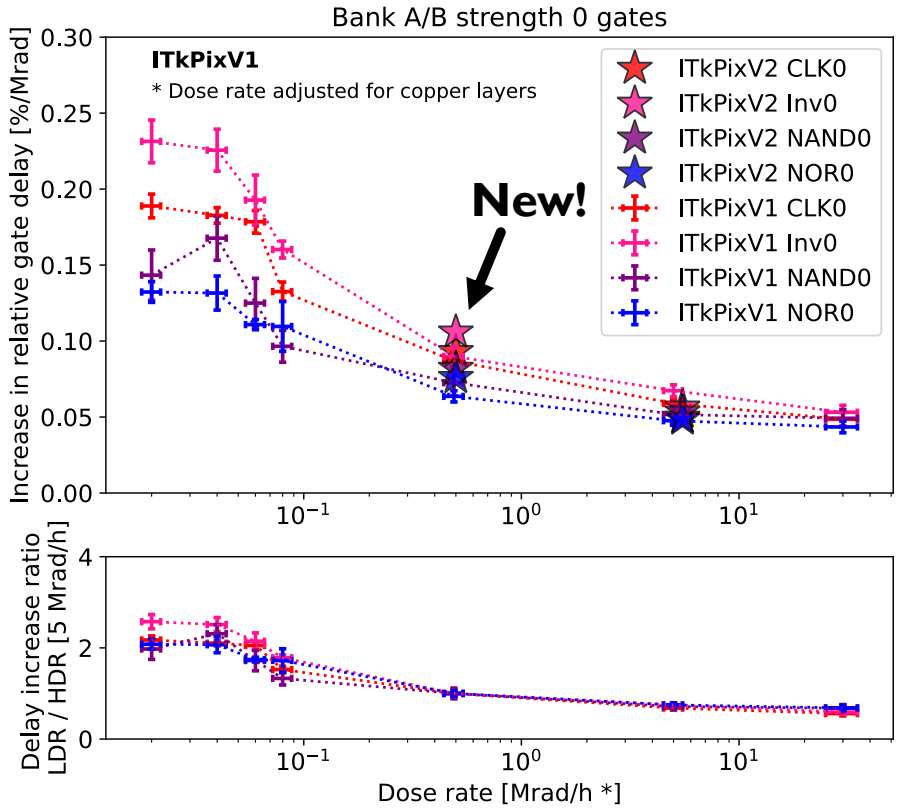
- Can also compute gate delay increase with irradiation (requirement < 200%)
- Steady increase, start to see some non-linearity for the strength 0 gates
- Note: Strength 0 gates not used in digital logic of the chip
- Can compare to irradiations in Oxford at 5 Mrad/h → clearly larger gate delay increase in this irradiation at 0.5 Mrad/h

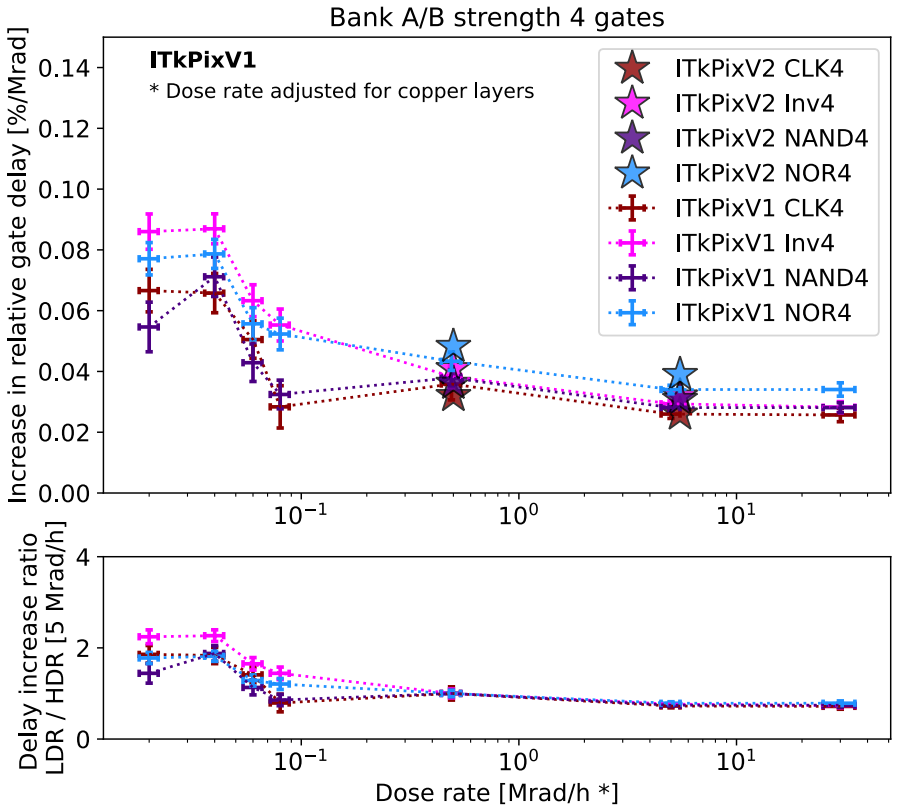




Low dose rate effects

- Well-known dose rate dependence of radiation damage in 65 nm transistors
- Have been collecting data over the past few years using ITkPixV1 → Observe a factor ~2 more damage at the HL-LHC expected dose rates (20 krad/h)
- ITkPixV2 data matches well with existing results



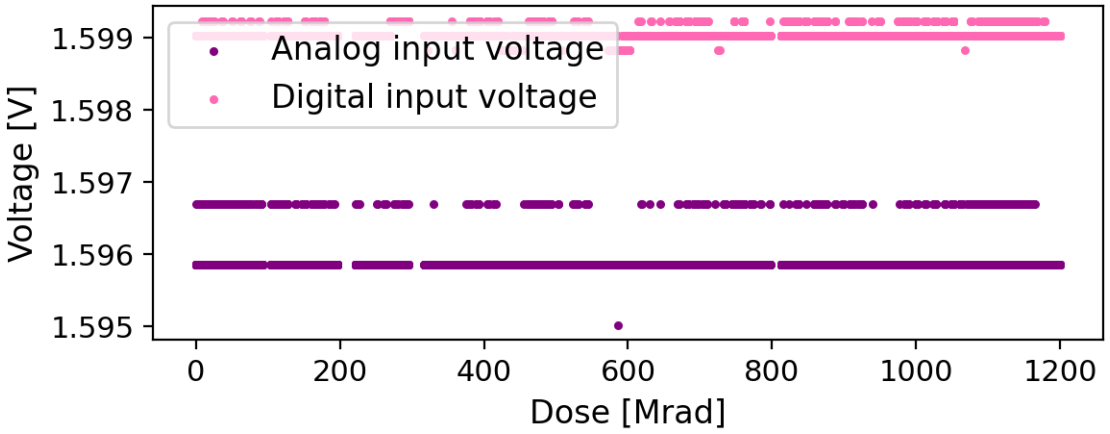


Chip currents

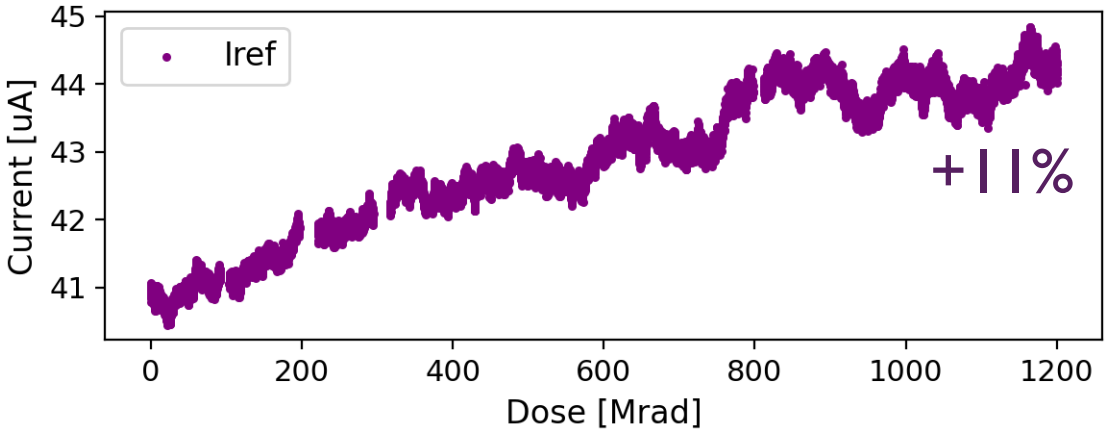
- Main focus of irradiation were chip voltages and currents
- Chip powered in LDO mode → constant input voltage
- Main chip reference current (Iref) drifts with irradiation → expected and consistent with ITkPixV1 results
- Analog currents seems to increase significantly with irradiation

→ surprising, could be non-uniform irradiation, but if real need to think about implications for ASIC powering envelope

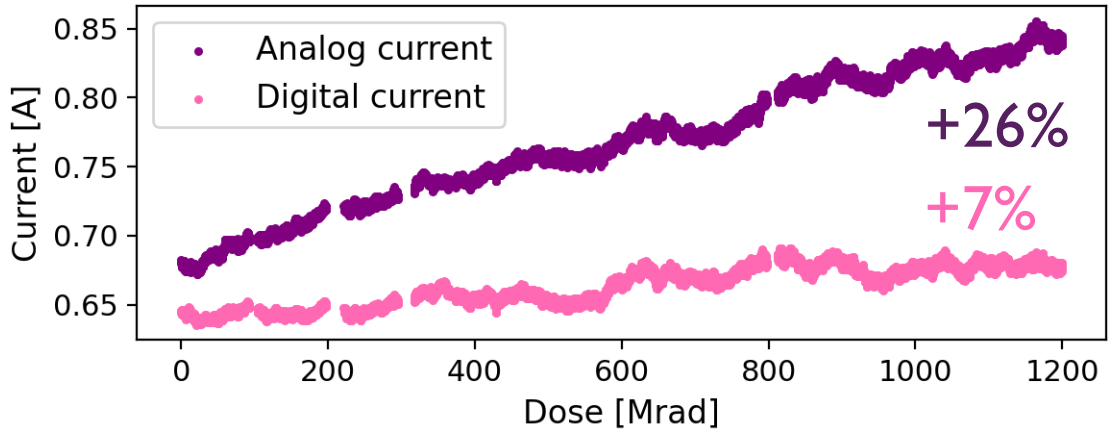
Power supply voltage



Main chip reference current (Iref)_

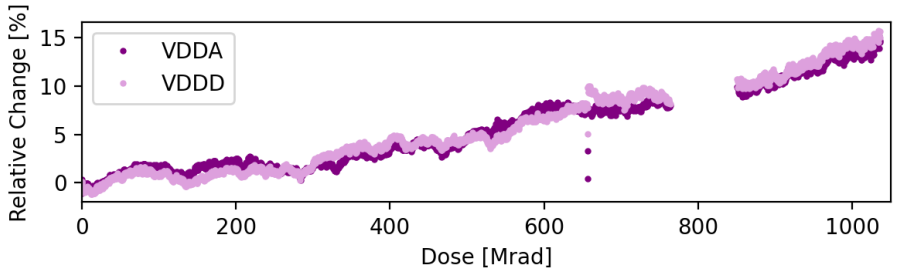


Power supply currents

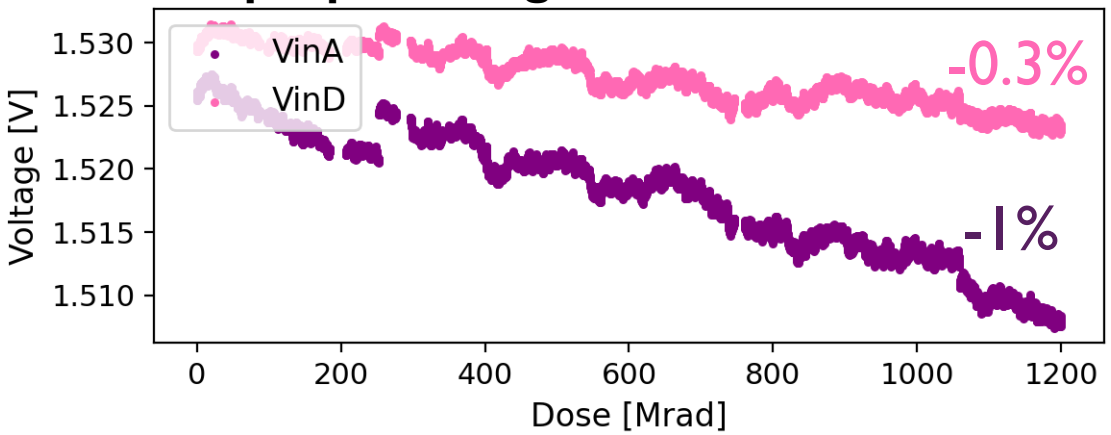


Voltages

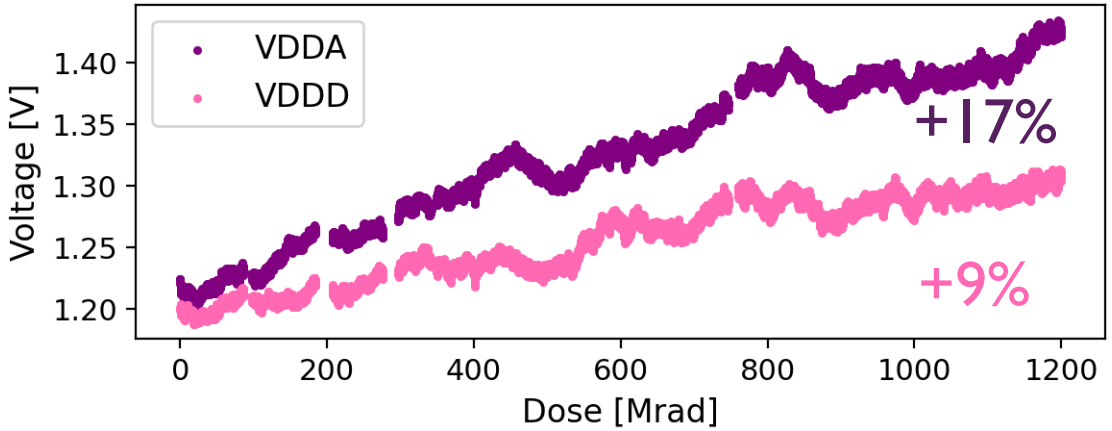
VDDA/D @ Oxford 5 Mrad/h



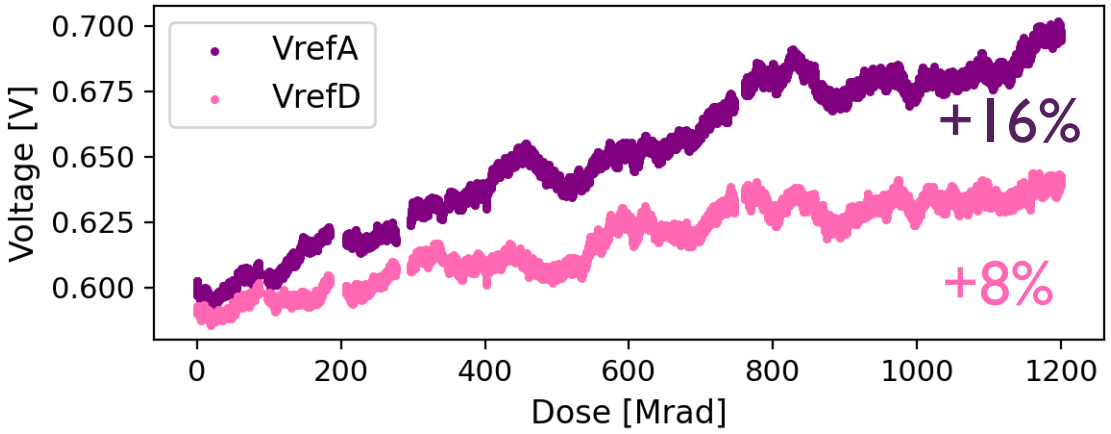
Chip input voltages



VDDA/D



VrefA/D



- Input voltage measured on the chip decreases slightly during irradiation
- Vref and VDD increase with irradiation (as they derive from Iref)
- VDDA increases more than VDDD

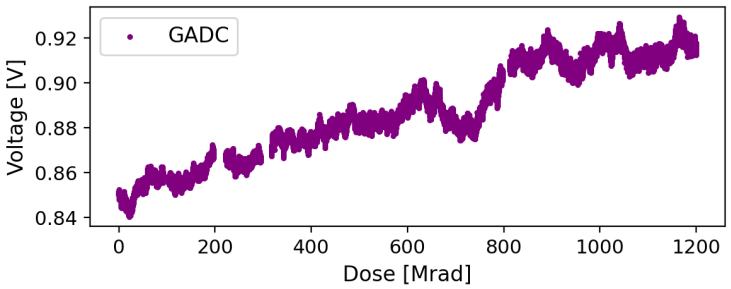
→ surprising, as a fix to metallisation layers was included in ITkPixV2 to make drift more uniform

→ Increase was also more similar ITkPixV2 irradiation in Oxford

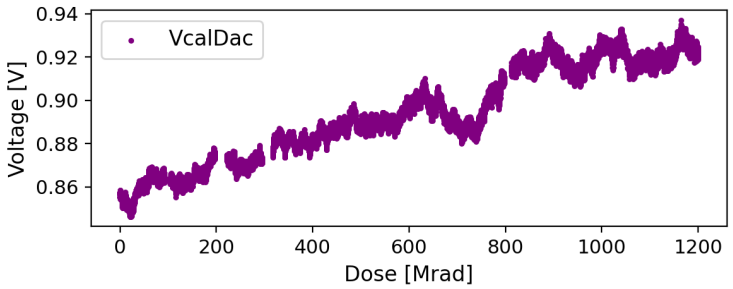
→ Non-uniform irradiation or dose rate effect?

More voltages…

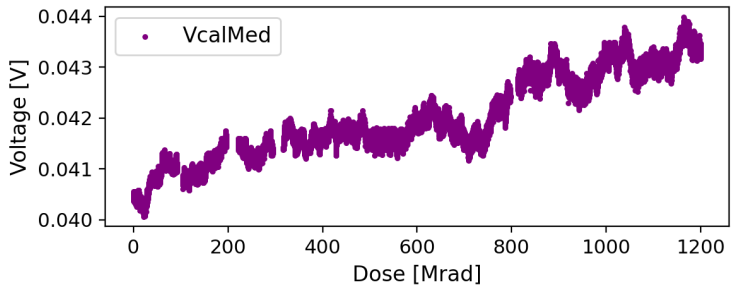
Vref_ADC



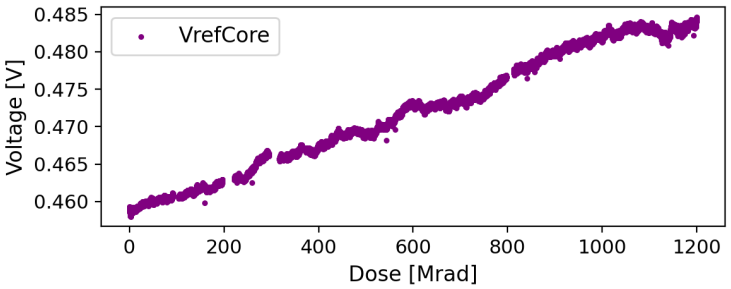
VCAL_DAC



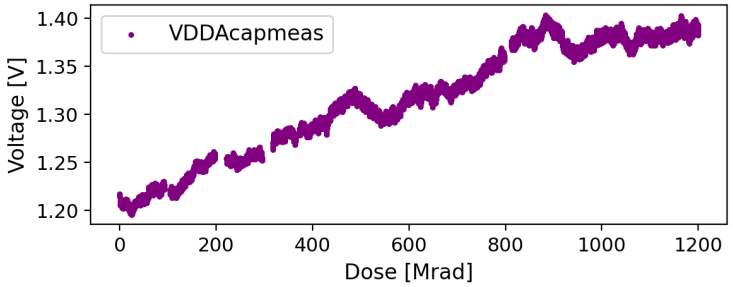
VCAL_MED



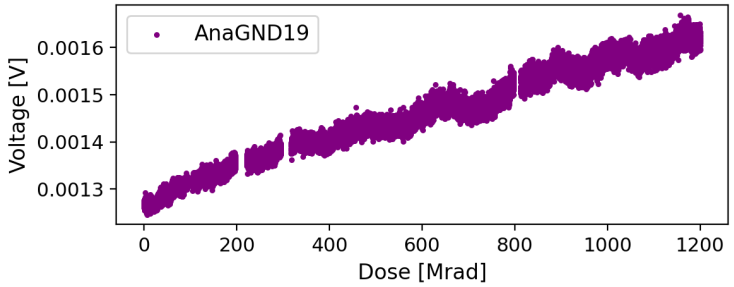
Vref_Core



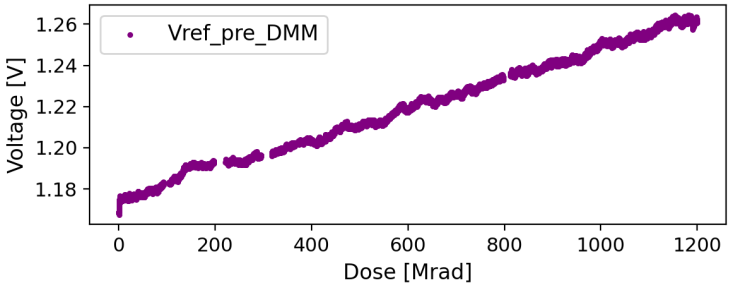
VDDA capmeasure



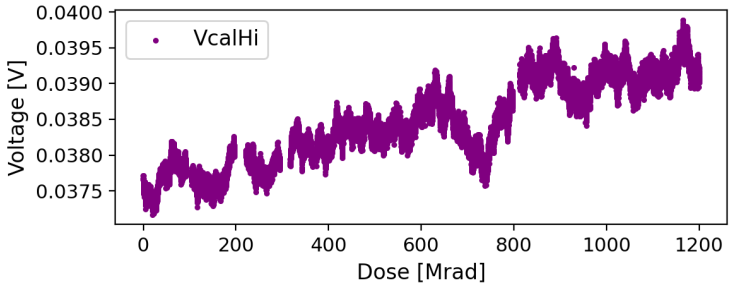
Analog ground



Vref_Pre

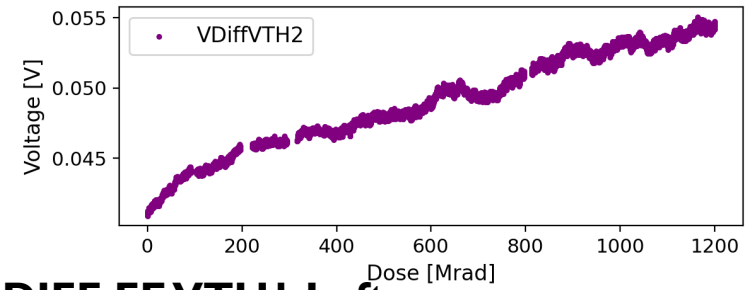


VCAL_HI

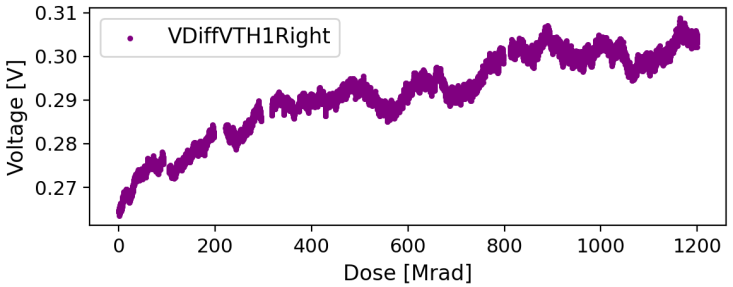


Even more voltages…

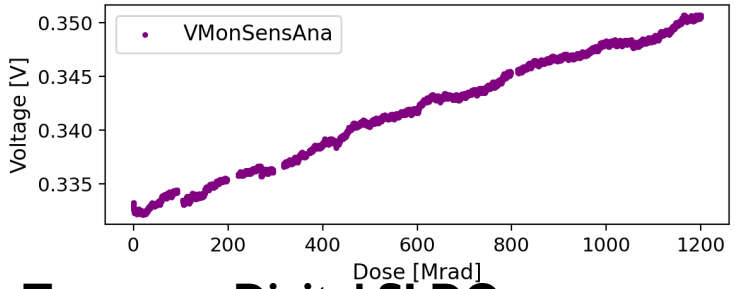
DIFF FE VTH2



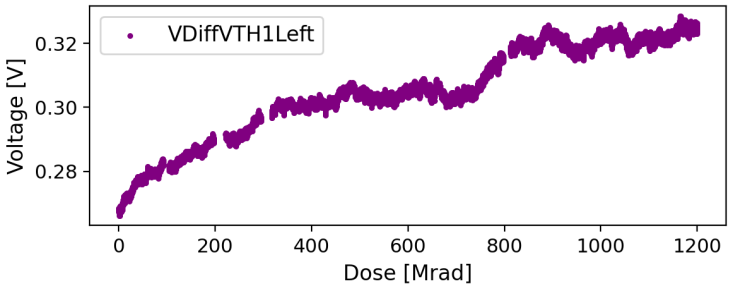
DIFF FE VTH1 Right



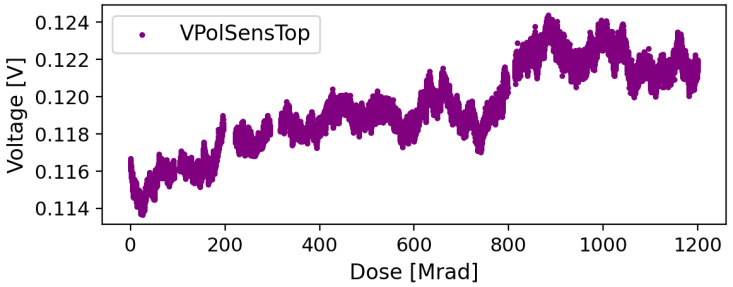
Tempsens Analog SLDO



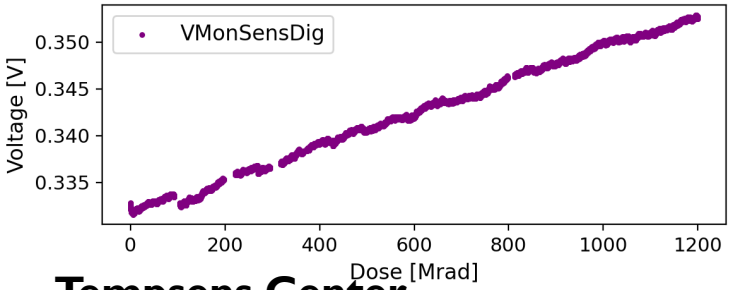
DIFF FE VTH1 Left



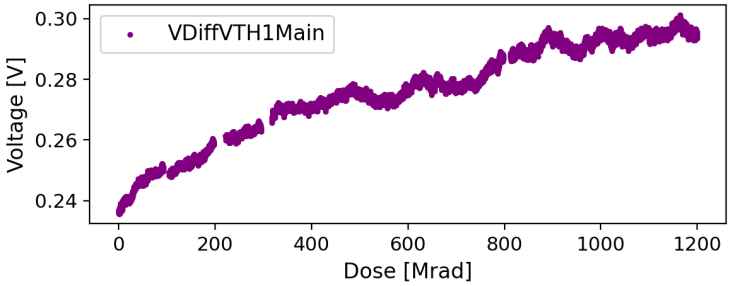
Poly Tempsens top



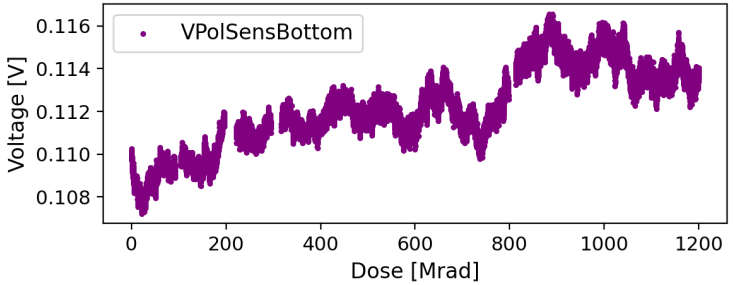
Tempsens Digital SLDO



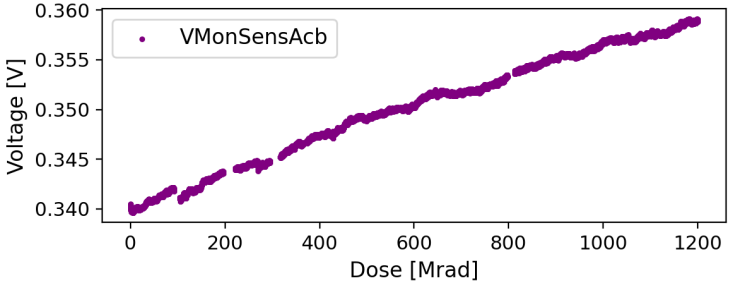
DIFF FE VTH1 Main



Poly Tempsens bottom

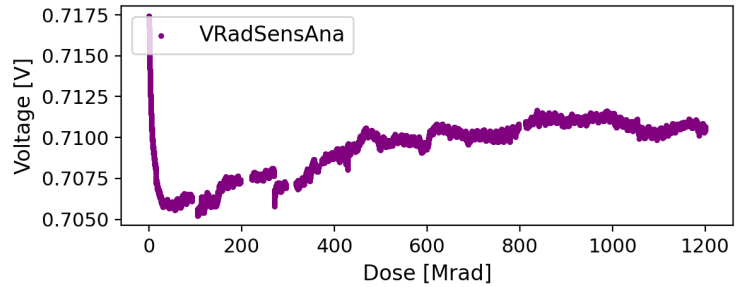


Tempsens Center

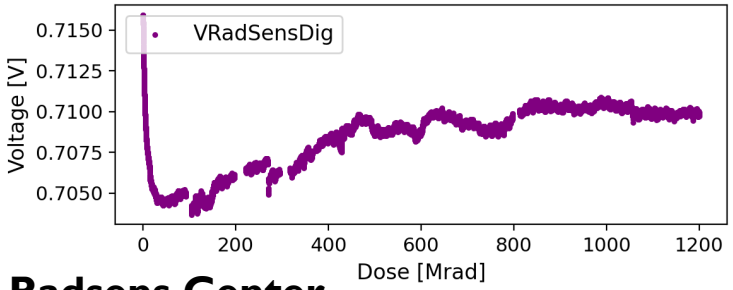


Radiation sensors

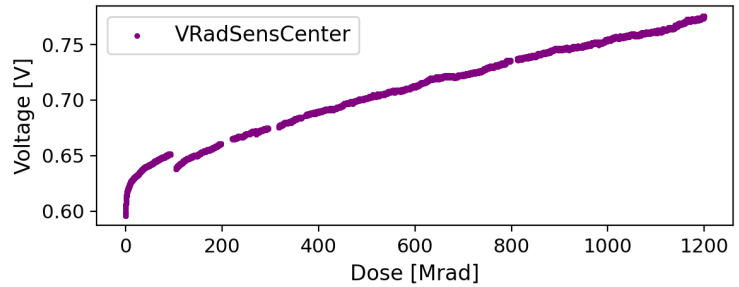
Radsens Analog SLDO



Radsens Digital SLDO

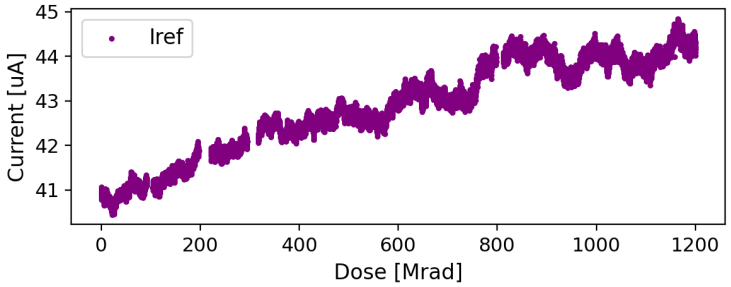


Radsens Center

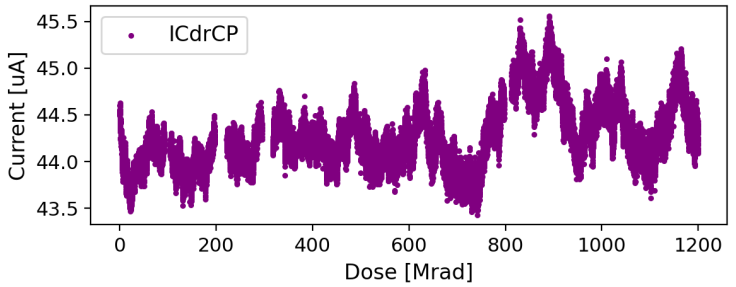


More currents…

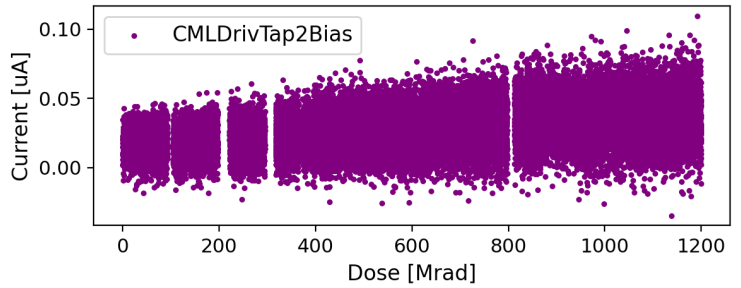
Iref



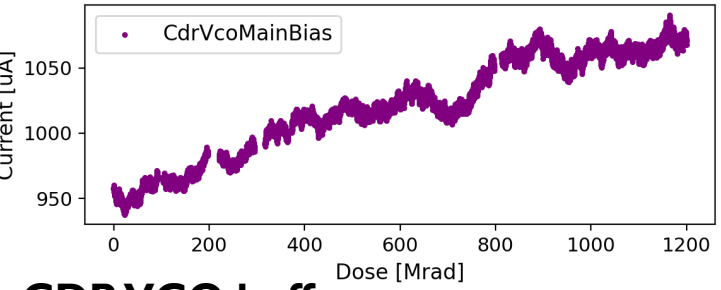
CDR CP current



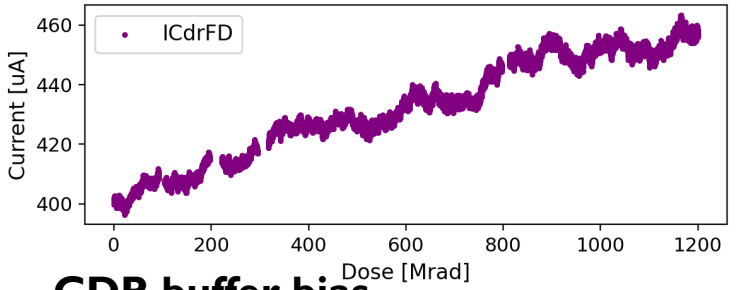
CML driver tap 2 bias



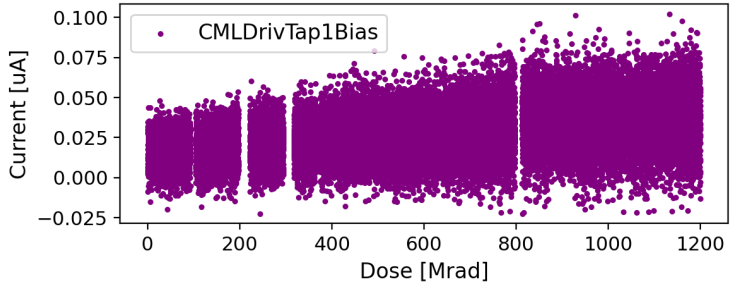
CDR VCO main bias



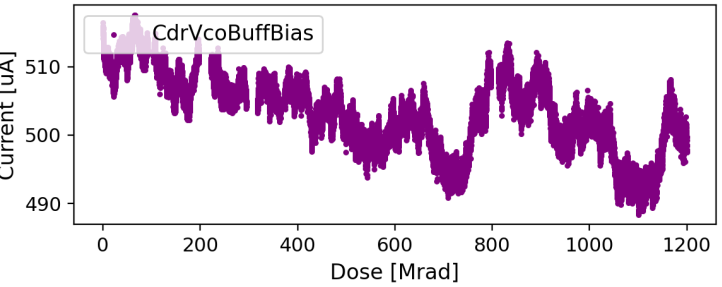
CDR FD current



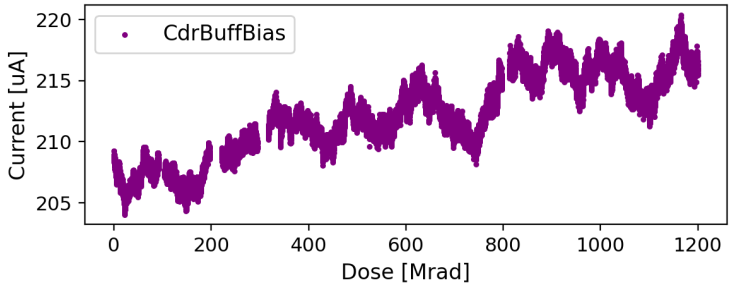
CML driver tap 1 bias



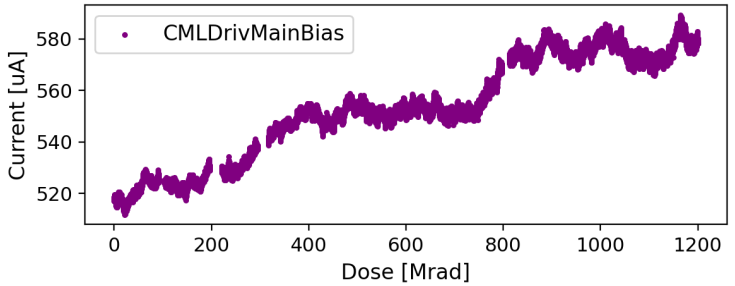
CDR VCO buffer



CDR buffer bias

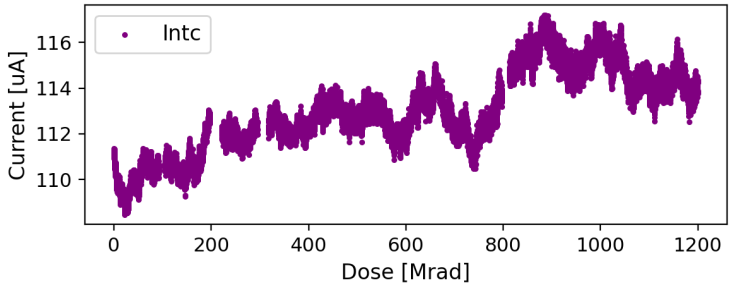


CML driver tap main bias

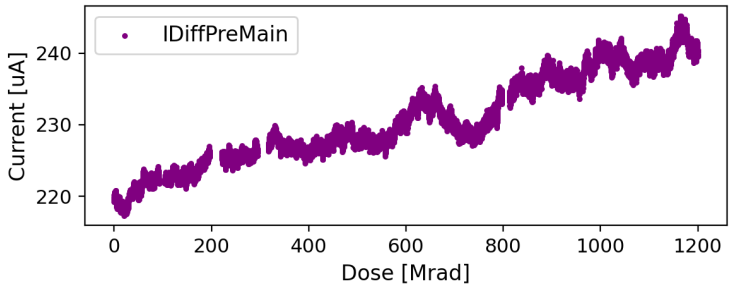


More currents…

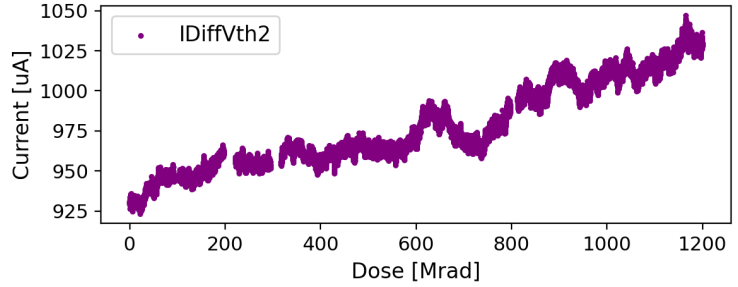
NTC pad current



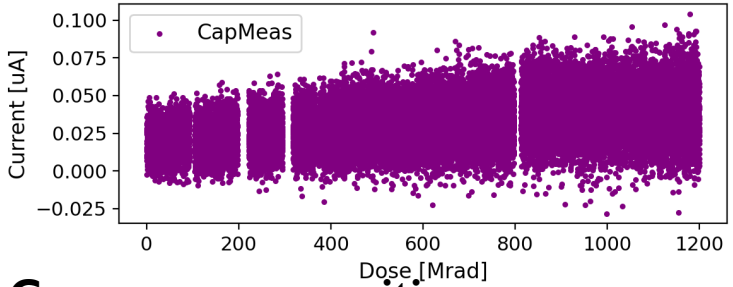
Preamp Main



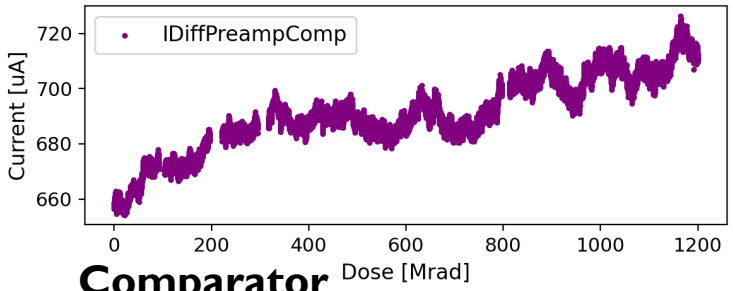
Vth2



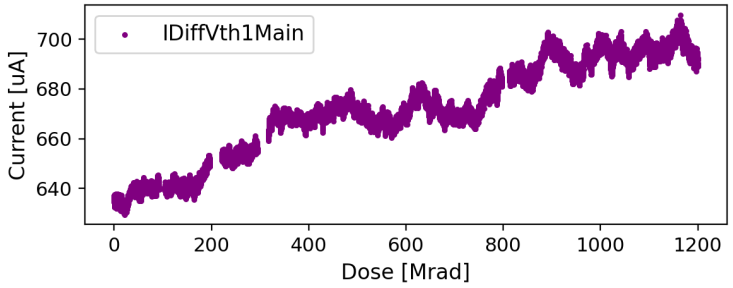
Capmeasure circuit



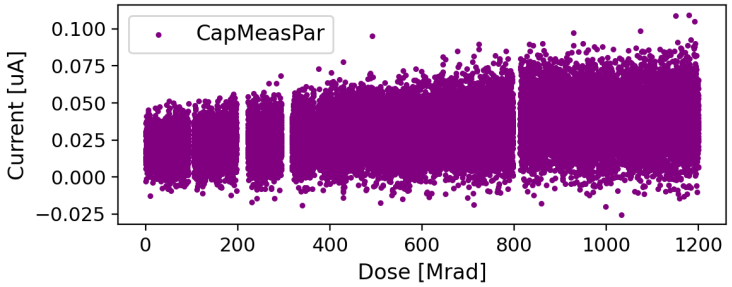
PreComp



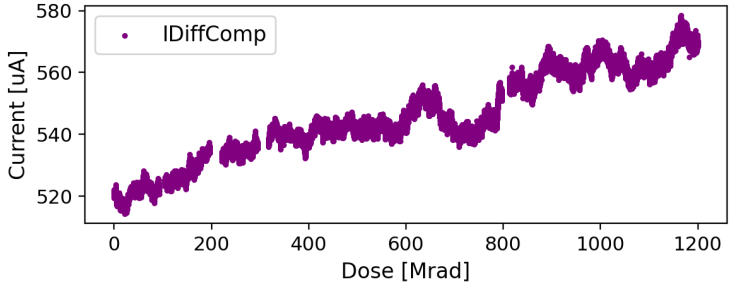
Vth1 main



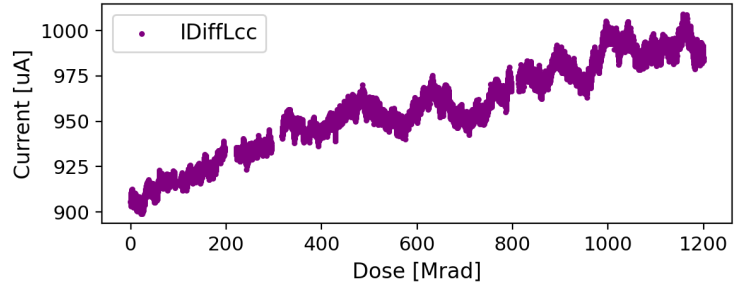
Capmeasure parasitic



Comparator

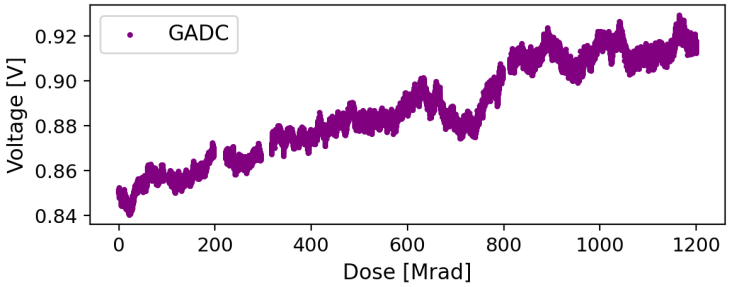


LCC

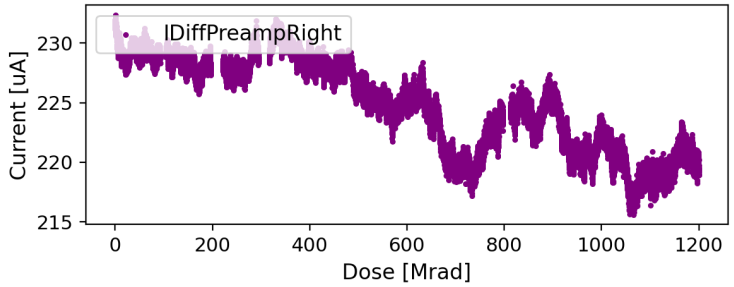


More currents…

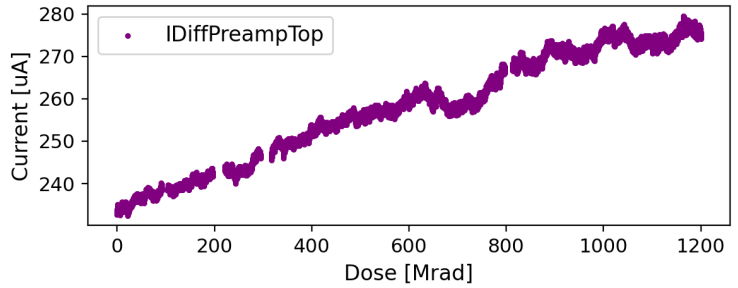
Feedback



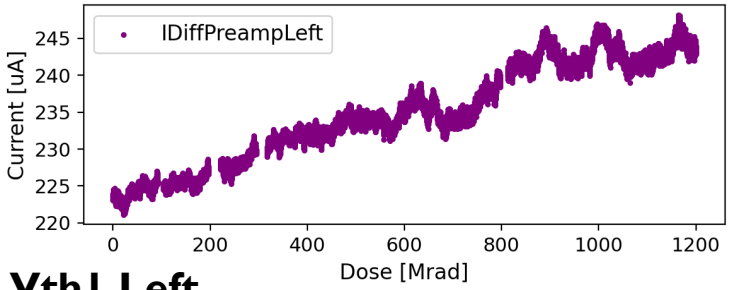
Preamp right



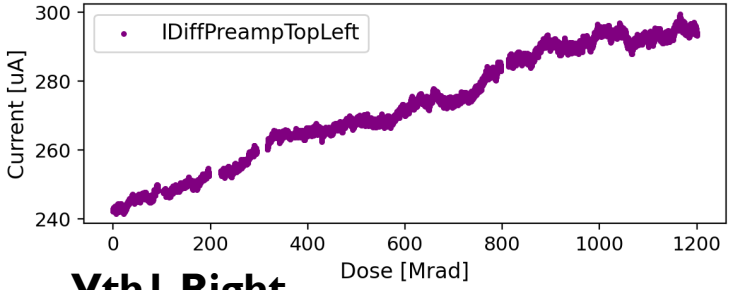
Preamp Top



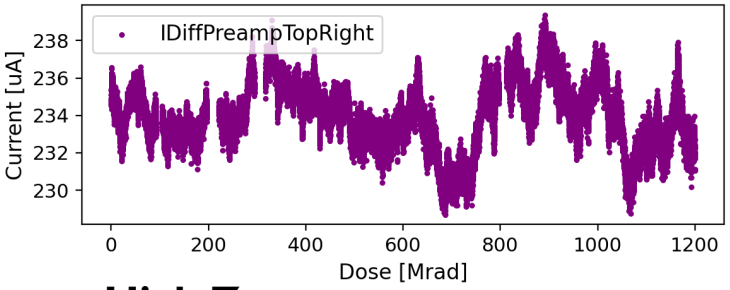
Preamp Left



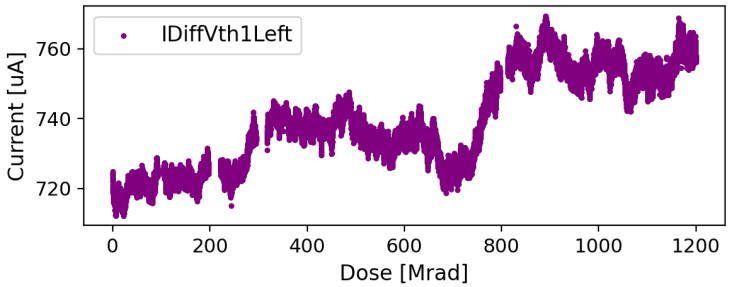
Preamp top left



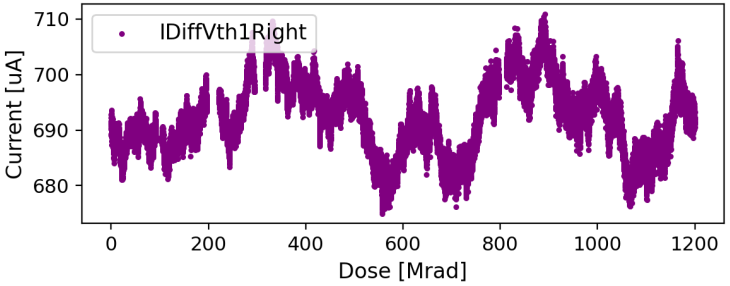
Preamp top right



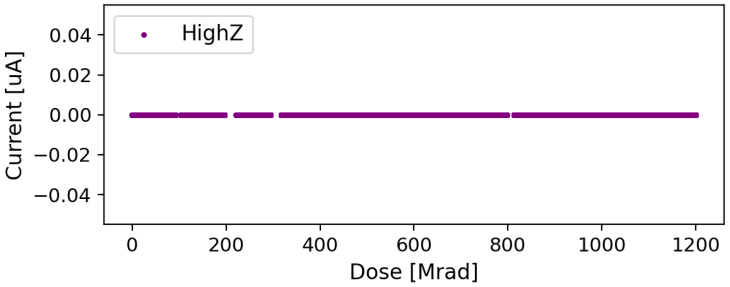
Vth1 Left



Vth1 Right

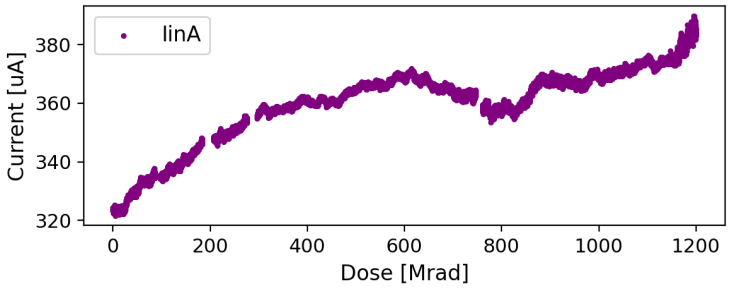


High Z

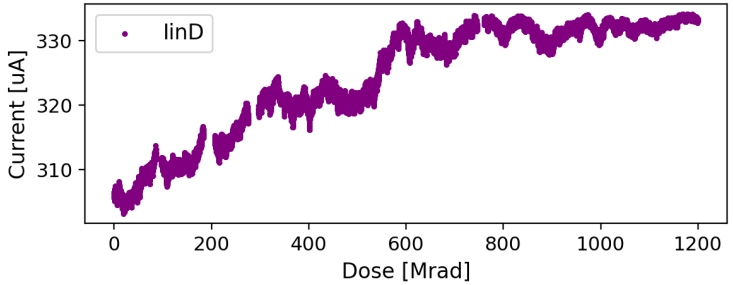


More currents…

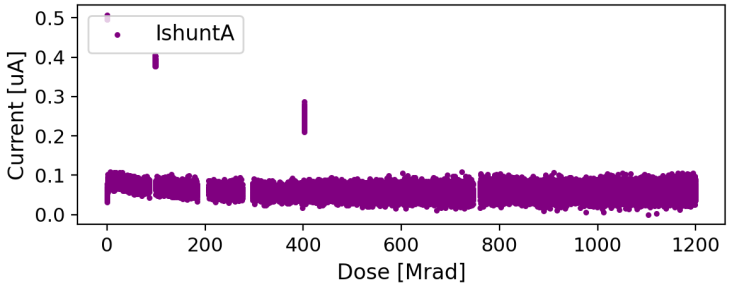
Analog input current



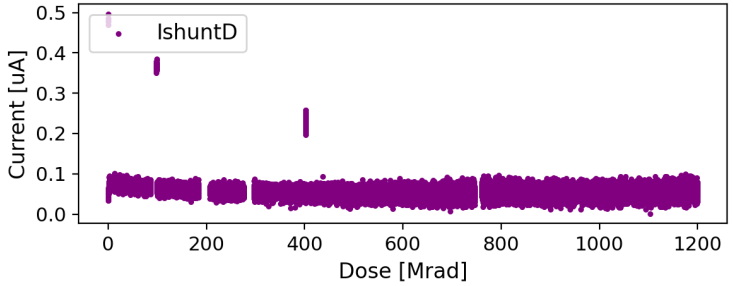
Digital input current



Analog shunt current



Digital shunt current



Conclusions

- Mostly done with analysing data from LBL X-ray irradiation and data looks mostly as expected
- Large increase in analog current is surprising

→ Plan to do follow-up irradiation with chip in SLDO mode

- Also ramping up efforts on SLIPPER V2

Thank you!

Any questions?

Table 6.5: Increase of the currents and voltages of the ITkPixV1 chip after irradiation to 1 Grad with X-rays at a dose rate of 4 Mrad/h.

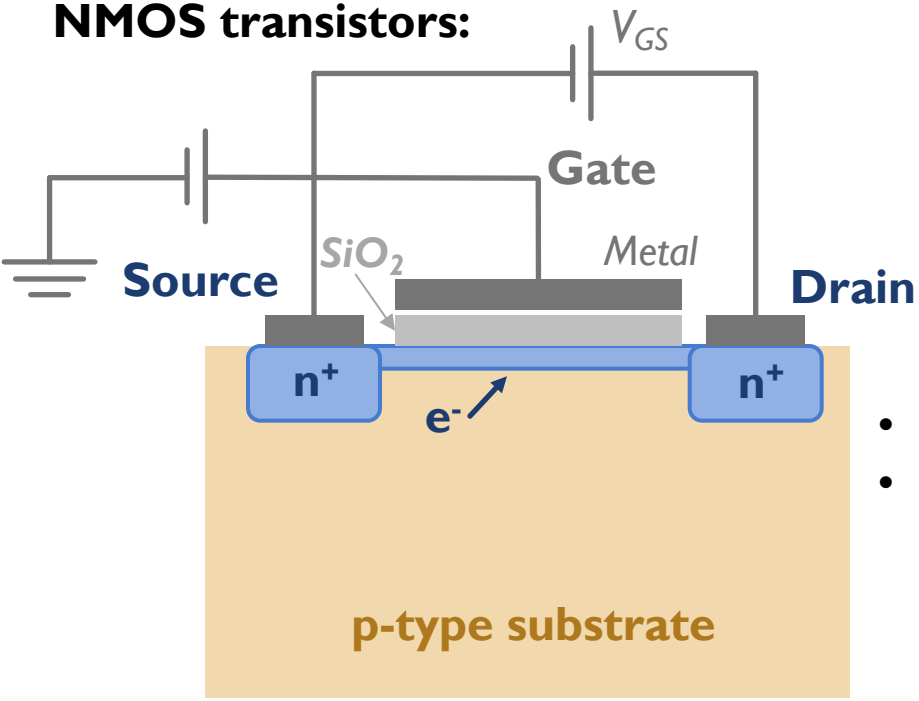
Voltage/Current	Increase
Currents	
Main reference current `Iref`	+ 4 %
Analogue input current `I_in analog`	+ 14 %
Digital input current `I_in digital`	+ 9 %
Analogue shunt current `I_shunt analog`	+ 5 %
Digital shunt current `I_shunt digital`	+ 5 %
Voltages	
Analogue input voltage `VinA`	+ 3 %
Digital input voltage `VinD`	+ 3 %
Analogue reference voltage `VrefA`	+ 12 %
Digital reference voltage `VrefD`	+ 8 %
Analogue LDO output voltage `VDDA`	+ 14 %
Digital LDO output voltage `VDDD`	+ 9 %
ADC reference voltage `VrefADC`	+ 8 %
SLDO offset voltage `V_offset`	+ 1 %

Transistors

- MOSFET transistors are the building of current (pixel detector) electronics
- Working principle:

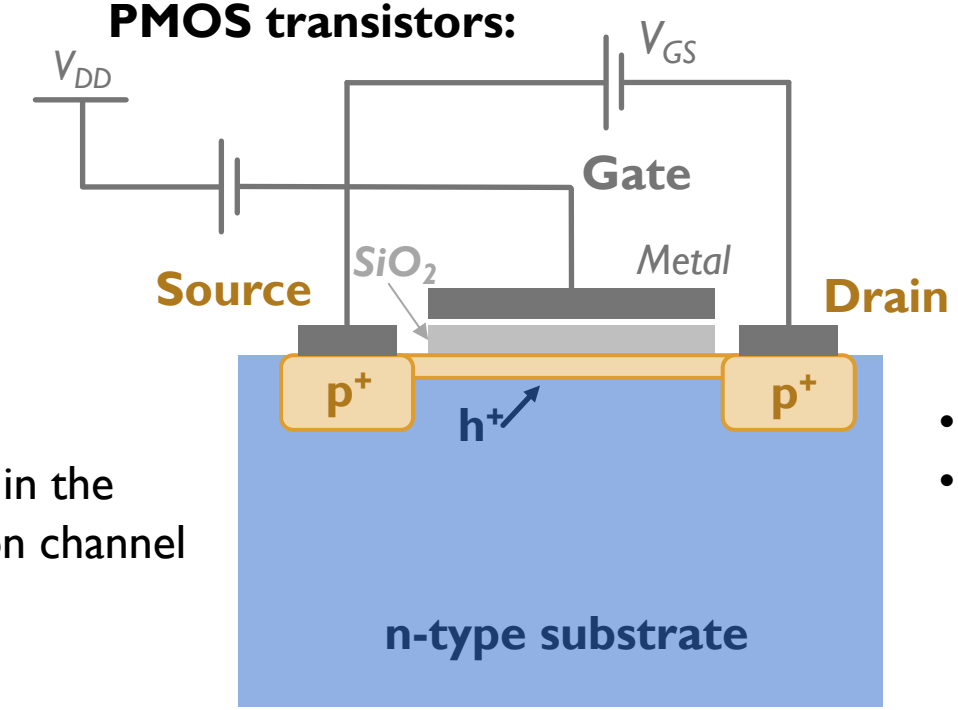
1. Voltage is applied to gate to induce a channel of free charge carriers below the Si-SiO_2 surface
2. Voltage applied between source and drain allow charge carriers to move → current

NMOS transistors:



- $V_{GS} > 0$
- Electrons in the conduction channel

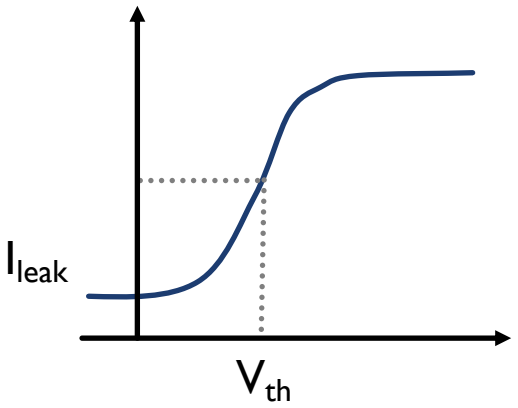
PMOS transistors:



- $V_{GS} < 0$
- Holes in the conduction channel

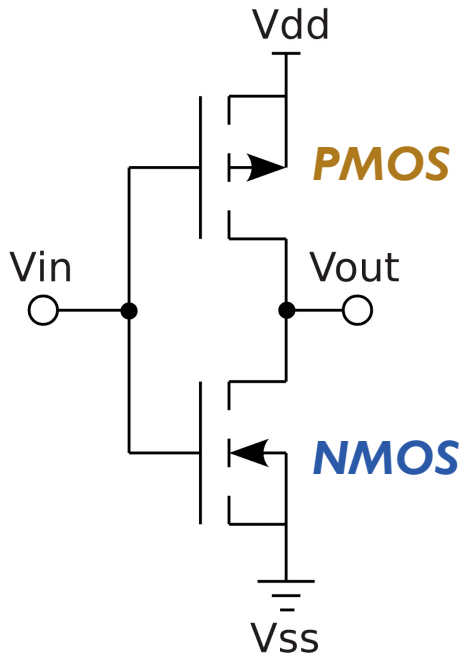
Transistors part II

Transistor turn-on curve



- Important characteristics of transistors include:
  - Transistor leakage current (I_{leak}) → current when no voltage V_{GS} is applied
  - Threshold voltage (V_{th}) → voltage at which the transistor turns on
- Various logic gates can be constructed from combinations of PMOS and NMOS gates
- E.g. Inverter gate → if you input 0, you get 1 and vice versa

CMOS Inverter

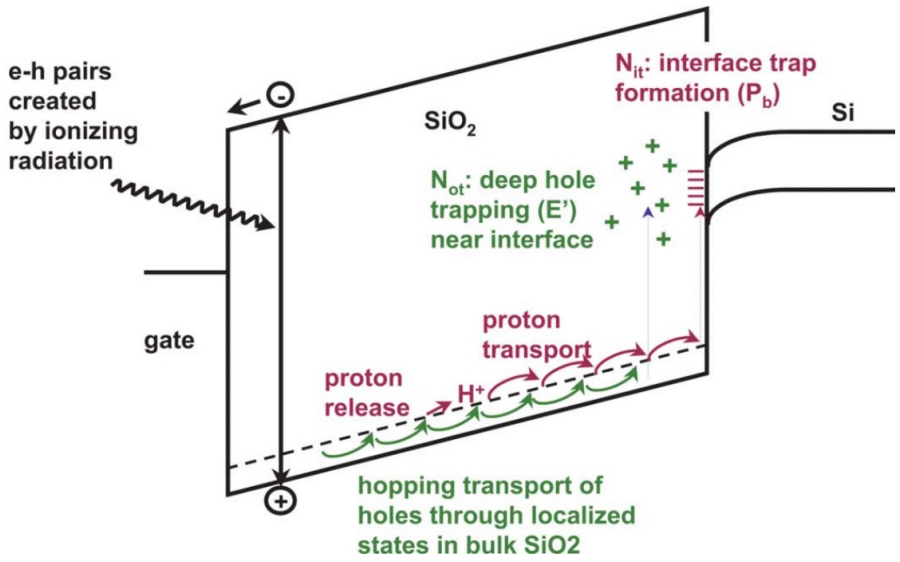


Damage to SiO_2

- In readout electronics, the damage to the SiO_2 and at the Si-SiO_2 interface are more important
- Mainly caused by ionization creating charged defect state in the oxide or at the interface → high electric fields exist in oxides, which separate the charge carriers

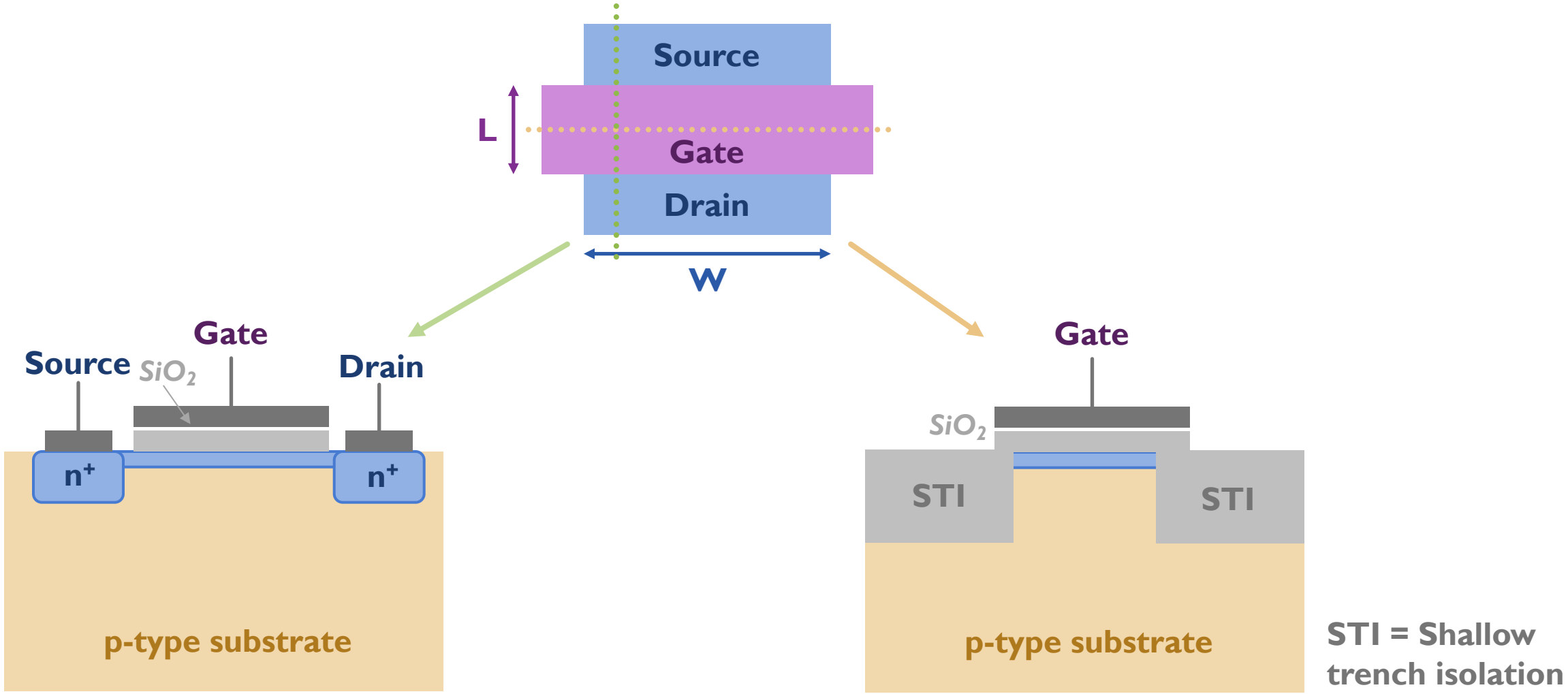
Two different effects to consider:

- Oxide charges (SiO_2) → defects in SiO_2 are always donor-like (positive), occurs relatively quickly
- Interface states (Si-SiO_2 surface)
  - → Impurity hydrogen ions released from lattice
  - → Give rise to new interface states which serve as traps
  - → Slower process due to lower mobility of hydrogen ions
  - → Can be both acceptor and donor like, depending on material
  - → Interface traps are **negatively charged in NMOS** (under positive bias) and **positively charged in PMOS** (under negative bias)



	NMOS	PMOS
Oxide charges	+	+
Interface traps	-	+

Transistors

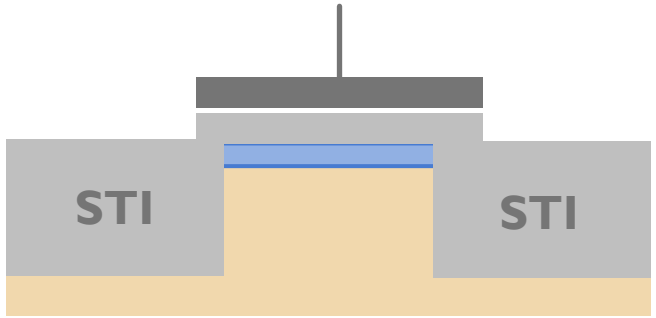


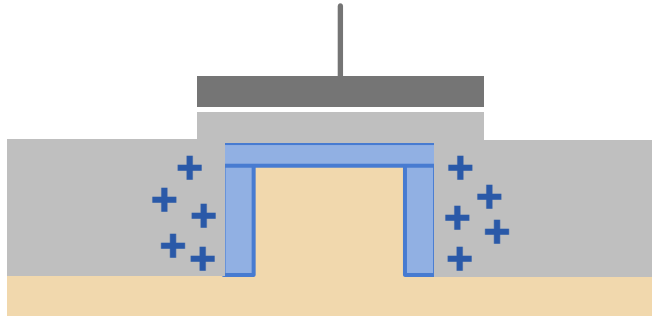
STI = Shallow trench isolation

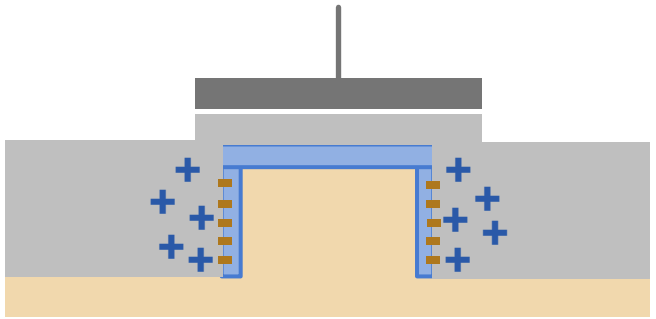
Edge effects - NMOS

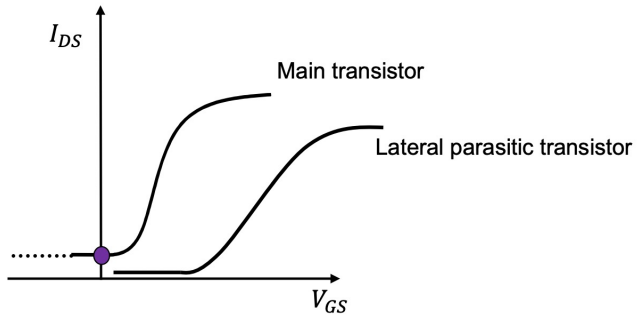
- Depending on transistor type, TID damage effects can look different
- Consider effects of radiation damage in STI
- In NMOS transistors:

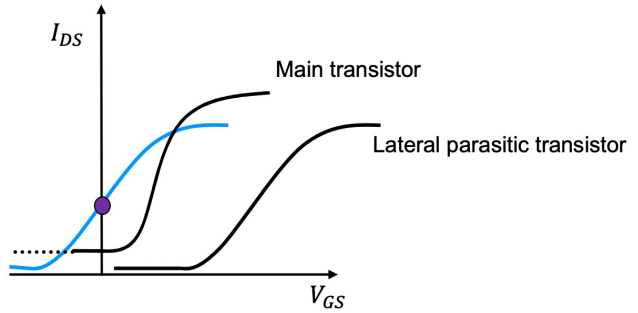
1. Fast build-up of positive oxide charges
   - → opens up another channel through which electrons can flow between source and drain
   - → Leakage current increases
   - → Threshold voltage decreases
2. Slower build-up of negative interface charges
   - → Counteracts the effect of positive oxide charges
   - → Leakage current decreases
   - → Threshold voltage increases

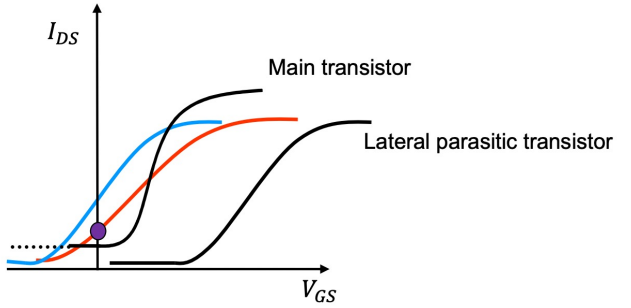












Edge effects - PMOS

- In PMOS transistors:

1. Fast build-up of positive oxide charges
   - → Holes in the conduction channel, so no additional channel opens up
   - → Leakage current does not increase
   - → Threshold voltage decreases
2. Slower build-up of positive interface charges
   - → Same effect as oxide charges
   - → Threshold voltage increases further

→ Mechanism known as Radiation Induced Narrow Channel Effect (RINCE)