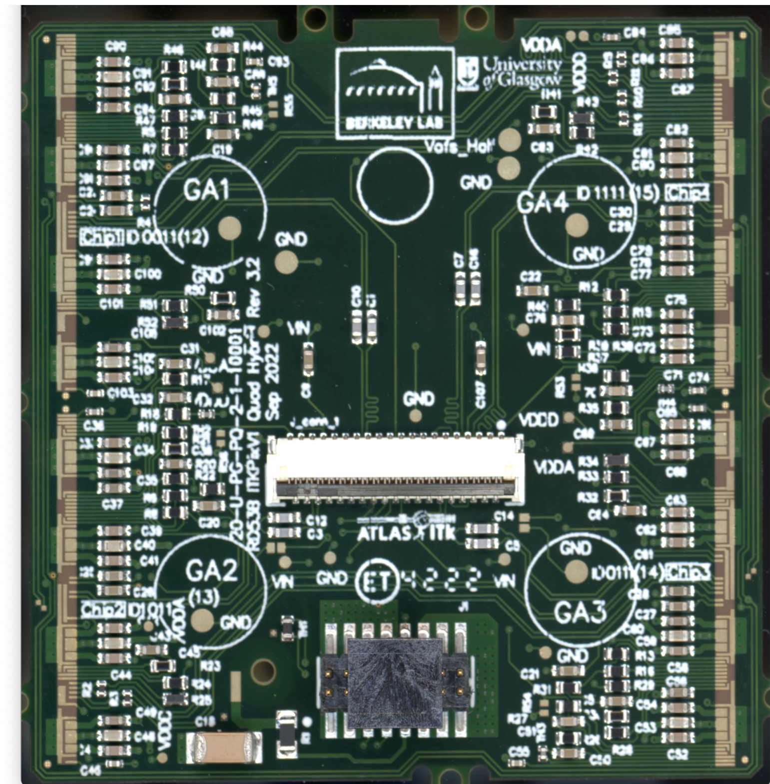
# Quad Hybrid QC Process

Marija Marjanović

# ITk Quad Pixel Hybrids

- Common design for all layers
  - Slight difference in size for L1 hybrids
- Different SMD components loaded depending on the layer
  - SLDO parameters
  - L1
  - L2-L4
- Bare flex production
  - NCAB (L1: 350 ; OS: 840)
  - Tecnomec (OS: 840)
  - Yamashita (Japan in-kind contribution)
- Population order from CERN
  - Vendor 1 – L1 + 50% OS – Order out 17/10 – Start assembly ~February 2024
  - Vendor 2 - 50% OS – Order out 11/10



Bare Panels Reception
Edinburg
Oklahoma
[+ Glasgow,Japan, OB sites]
Bare Panels Reception QC

Bare Panels Manufacturer [Vendor 2]
Glasgow

Components Population Manufacturer [Vendor 1]
Glasgow

QA Testing
Edinburg
Oklahoma
[+ Glasgow,Japan, OB sites]
Populated Boards after thermal cycling

Sampling

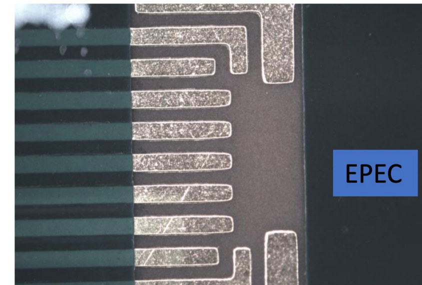
Populated Panels Reception
Edinburg
Oklahoma
[+ Glasgow,Japan, OB sites]
Populated Panels Reception QC

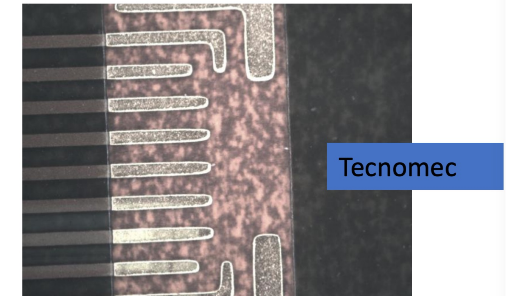
Cutting of individual Hybrids
Edinburg
Oklahoma
[+ Glasgow,Japan, OB sites]
Populated Boards QC

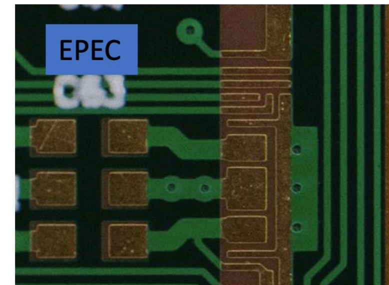
Shipping to Modules Assembly sites
Edinburg
Oklahoma
[+ Glasgow,Japan, OB sites]
Shipping Procedures

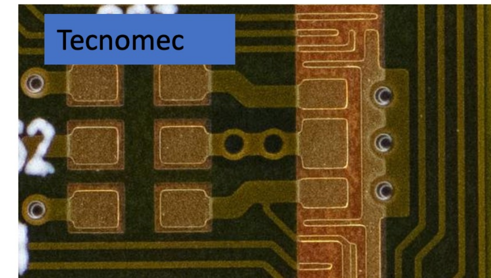
# Acceptance tests

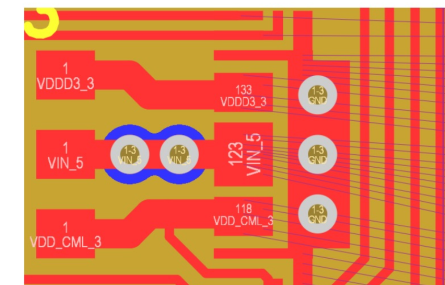
- Accept /Reject the batch on acceptance criteria set in the price inquiry document and the technical notes
  - Visual Inspection
  - Metrology – X-Y measurement
  - Dowel Hole check
  - Layer thickness
  - Via resistance
- Design Check
- Over/under etching of Cu
- Signal Transmission
- Wirebonding test
- Any other fabrication variation compared to the design



# Hybrid QC and QA measurements

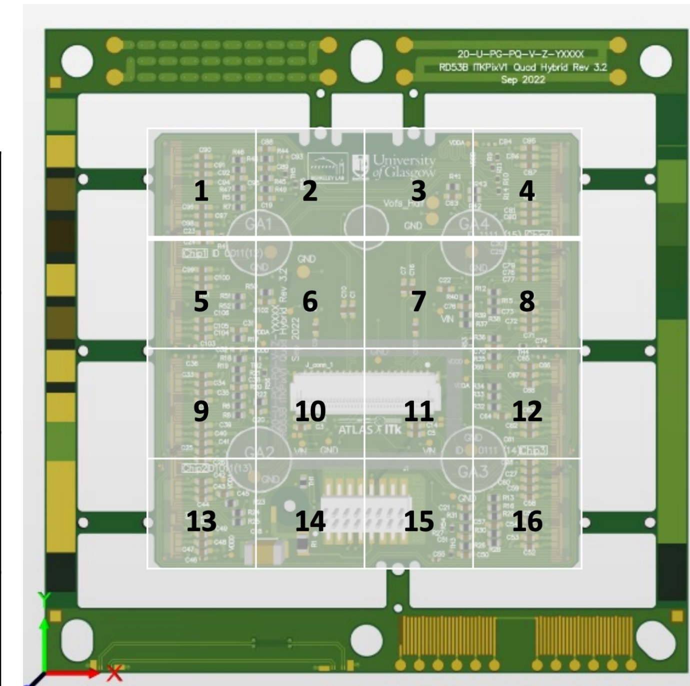
- Quality Assurance (QA) tests - performed to qualify the design
- Quality Control (QC) tests - ensure design specifications are fulfilled
  - Catch unacceptable defects as really as possible
- Both QC and QA tests are stored in production database (PDB)
  - Complete traceability of the hybrids

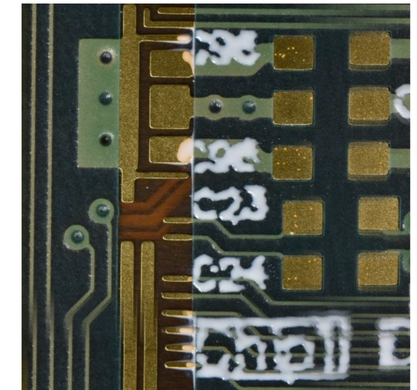
# Hybrid QC Production and QC Testing Flow

- Reception
- Population
- Tab cutting
- QA pre-thermal cycle / thermal shock
- QA post-thermal cycle / thermal shock
- QC
- QA post radiation cycle
- PCB ready for module
- PCB Reception at module site

# Bare hybrid reception stage summary

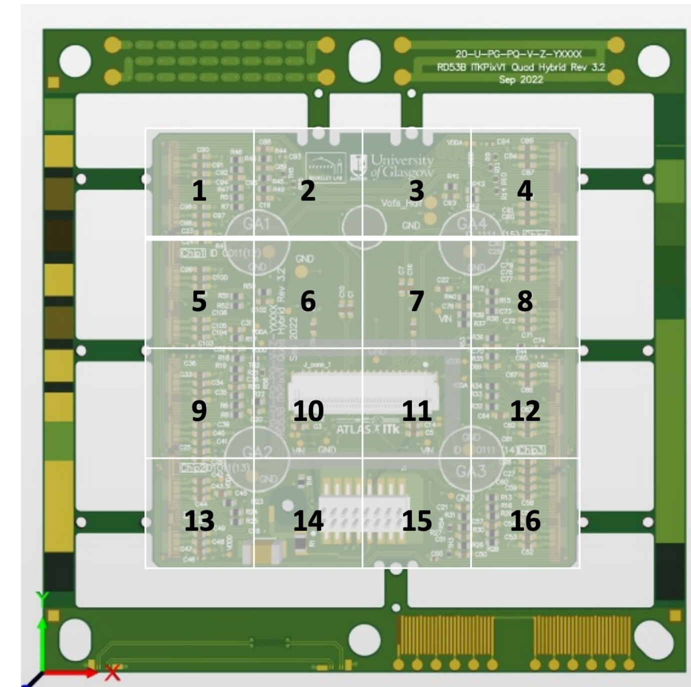
| **QC Reception tests of bare board** | Frequency | Measurements |
|---|---|---|
| Report for Bare flex PCB | Per batch | Industry report<br>Ionic contamination check |
| Bare board visual inspection | 10% of a batch | Optical high-resolution Image<br>Visual Inspection results |
| Metrology | 5% of a batch | Flex body dimensions (X, Y)<br>Diameter of dowel hole A and width of slot-B<br>Output from Jig testing(pass/fail) |
| Dowel hole tolerance check | All | Pass/fail |
| Layer thickness measurement | 25% of a batch | individual layer thickness measurements of the flex PCB stack-up |
| Via resistance test | QA - ~5flexes | Resistance |

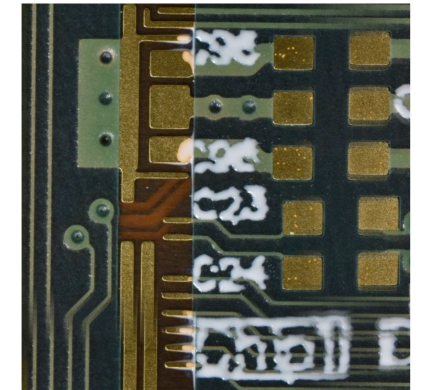


# Visual Inspection

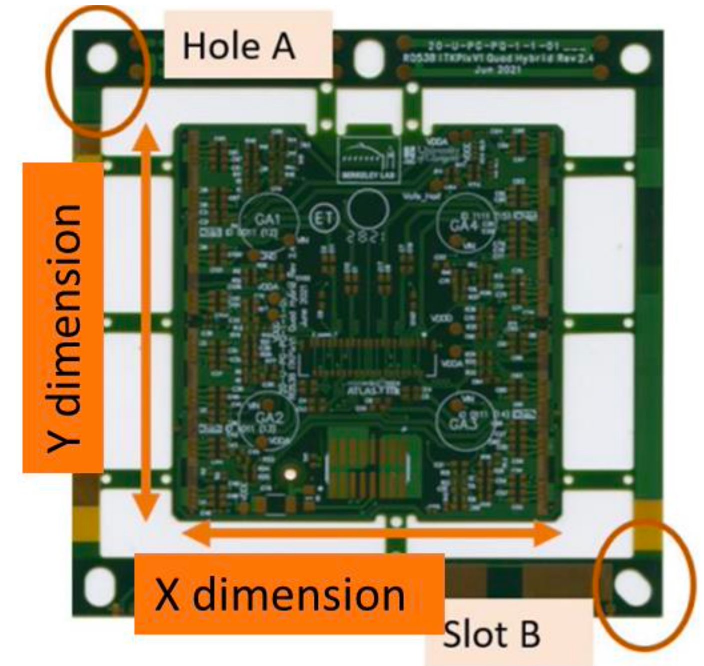
- Performed on 10% of bare hybrids
  - Back and front side
- Separated in several categories (each one assessed separately 1 - 3)
  - Wirebond pad contamination
  - Particulate contamination
  - Watermarks
  - Scratches
  - Soldermark irregularity/cracks
- Overall grading 1 (perfect) – 5 (unusable)

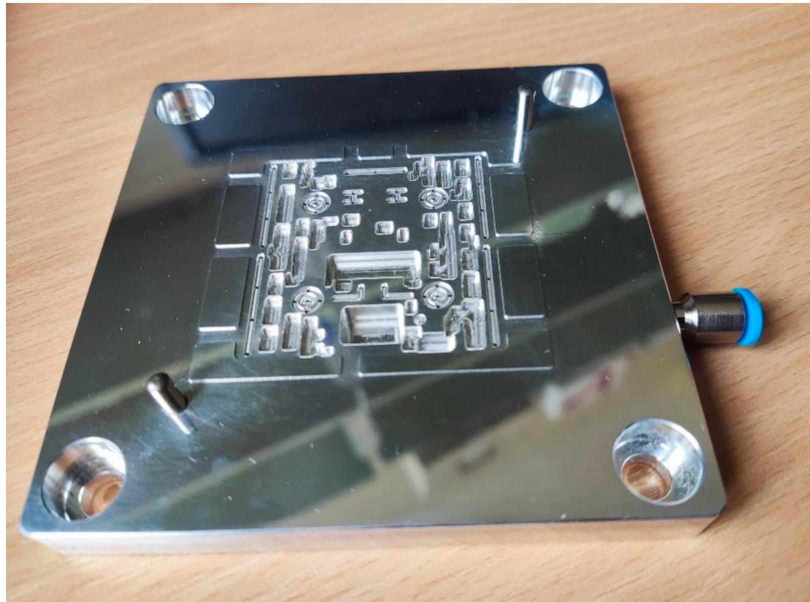


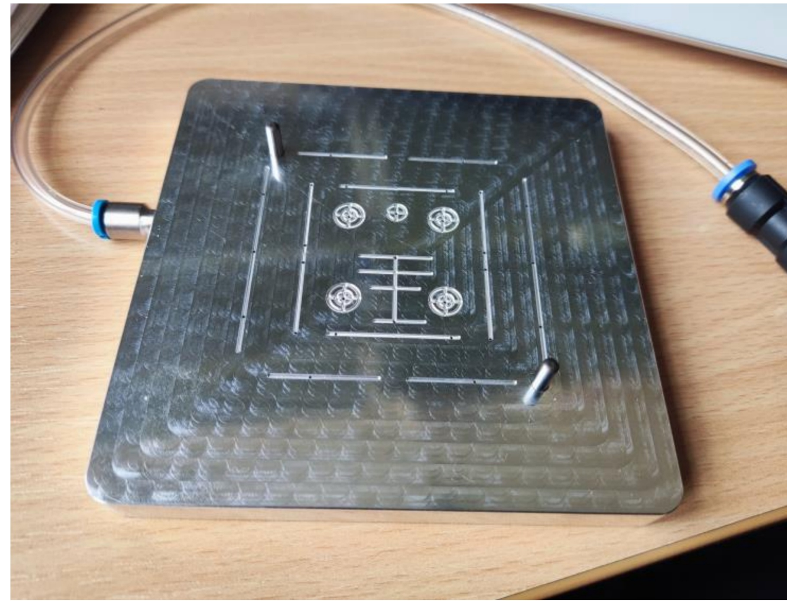



# Metrology

- Board dimensions
  - X and Y dimensions
- Average thickness of all FE chip pick-up areas
- Std deviation of thickness of all FE chip pick-up area
- Dowel hole/slot dimensions
  - Diameter of dowel hole (top left of the flex)
    - Diameter 3mm -0/+100 um
  - Width of dowel slot (bottom right of the flex)
- Performed on 5% of batch

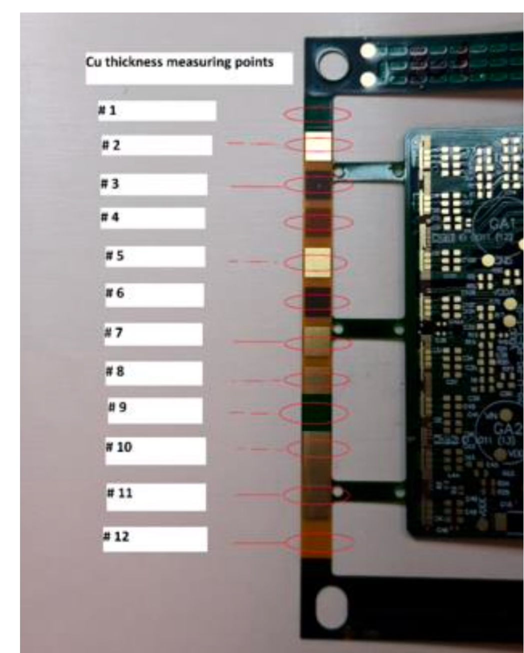


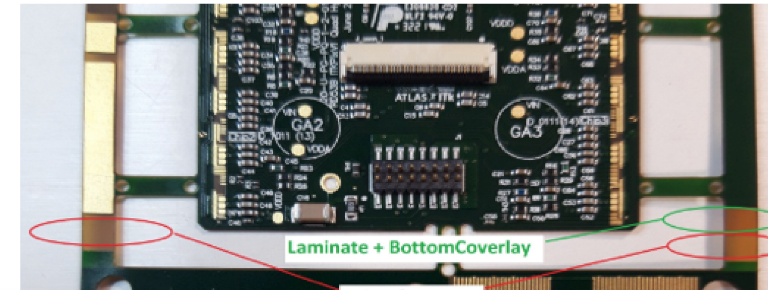





# Layer thickness measurement

- Performed on 25% of flexes (one per panel)
- Specification
  - Cu thickness of top layer 23-27 um
  - Cu thickness of inner layer 10-12 um
  - Cu thickness of bottom layer 23- 27 um
  - Dielectric thickness 5um (as per IPC)
  - Coverlay with Adhesive thickness
  - Overall thickness 250um +/-20 %




epec | build to print electronics

**Material Stack Up: Flex**

**Part Number: RD53B ITHPixV1 Quad Hybrid REV 3.1**

| Layer | Thickness | Unit | Material |
|---|---|---|---|
| | 18 | um | LPI Soldermask (Flexible) |
| Layer 1 | 24 | um | Base Copper 12 um + Plated 12 um |
| | 50 | um | Polyimide (Adhesiveless) |
| | 25 | um | Adhesive |
| Layer 2 | 12 | um | Copper |
| | 13 | um | Polyimide (Adhesiveless) |
| Layer 3 | 24 | um | Base Copper 12 um + Plated 12 um |
| | 25 | um | Coverlay Adhesive |
| | 25 | um | Coverlay |

Flex Thickness

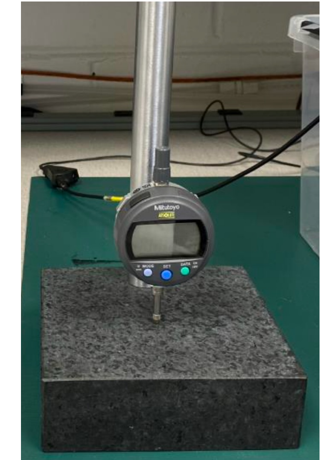
Updated to 25 um by EPEC

Flex Thickness: 216 um Spec: 200 um +/- 50 um

228 um

Cu thickness Measurements

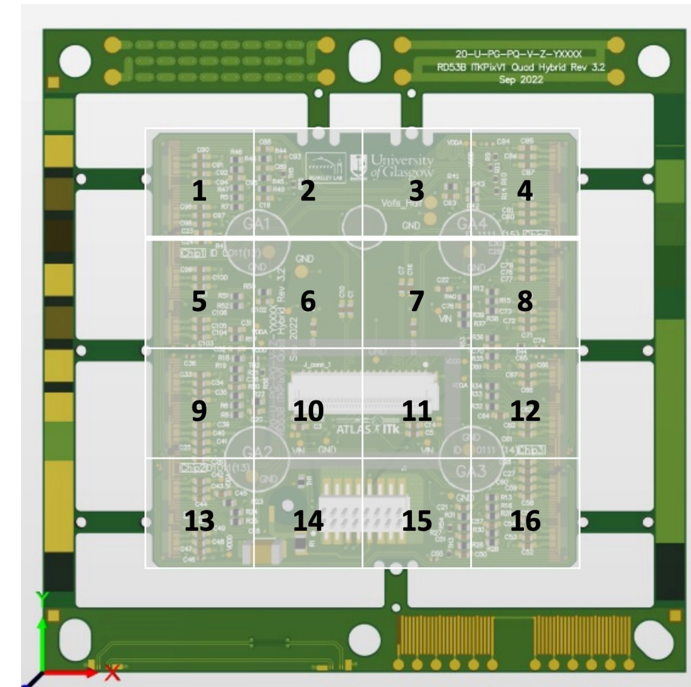
| Structure on the frame | Description |
|---|---|
| 1 | L+TCu+TSM |
| 2 | L+TCu+ENIG |
| 3 | L+MCu |
| 4 | L+BCu+ENIG |
| 5 | L+TCu+BCu+ENIG(2) |
| 6 | L+MCu+BCu+ENIG |
| 7 | L+TCu+ENIG+MCu |
| 8 | L+TCu+Mcu+Bcu+ENIG(2) |
| 9 | L+TCu+TSM+MCu+BCu+BCL |
| 10 | L+TCu+ENIG+MCu+BCu+BCL |
| 11 | L+TCu+ENIG+MCu+BCu+ENIG |
| 12 | Laminate(L) |



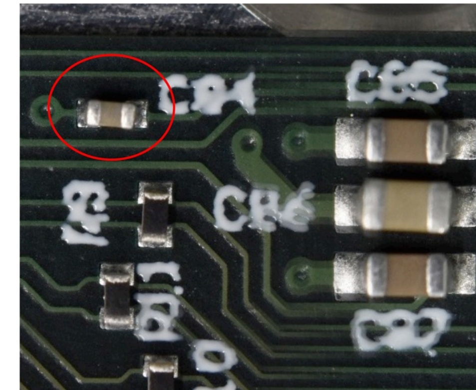
# Population stage summary

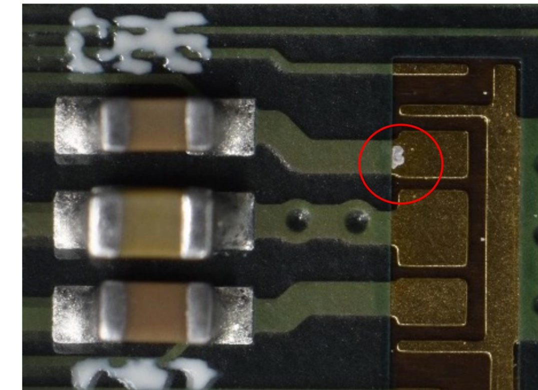
| **QC Population** | Frequency | Measurements |
|---|---|---|
| Report for population | Per batch | Industry report |
| Populated board visual inspection | 10% of a batch | Optical high-resolution Image<br>Visual Inspection results |

# Visual Inspection



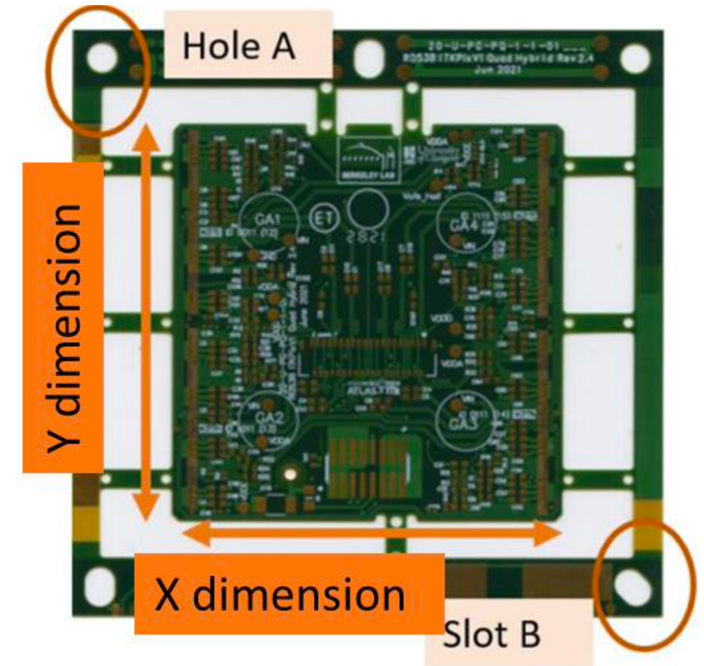

- Performed on 10% of populated hybrids
  - Only front side
- Separated in several categories (each one assessed separately 1 - 3)
  - Wirebond pad contamination
  - Particulate contamination
  - Watermarks
  - Scratches
  - Soldermark irregularity/cracks
  - HV LV connector assembly
  - Data connector assembly
  - Solder spills
  - Component misalignment
  - Shorts/close proximity of components due to misalignment
- Overall grading 1 (perfect) – 5 (unusable)





# Metrology

- HV capacitor thickness
- Thickness including the black body of power connector (excluding pins)
- Dowel hole/slot dimensions
  - Diameter of dowel hole (top left of the flex)
    - Diameter 3mm -0/+100 um
  - Width of dowel slot (bottom right of the flex)
- Performed on 5% of batch

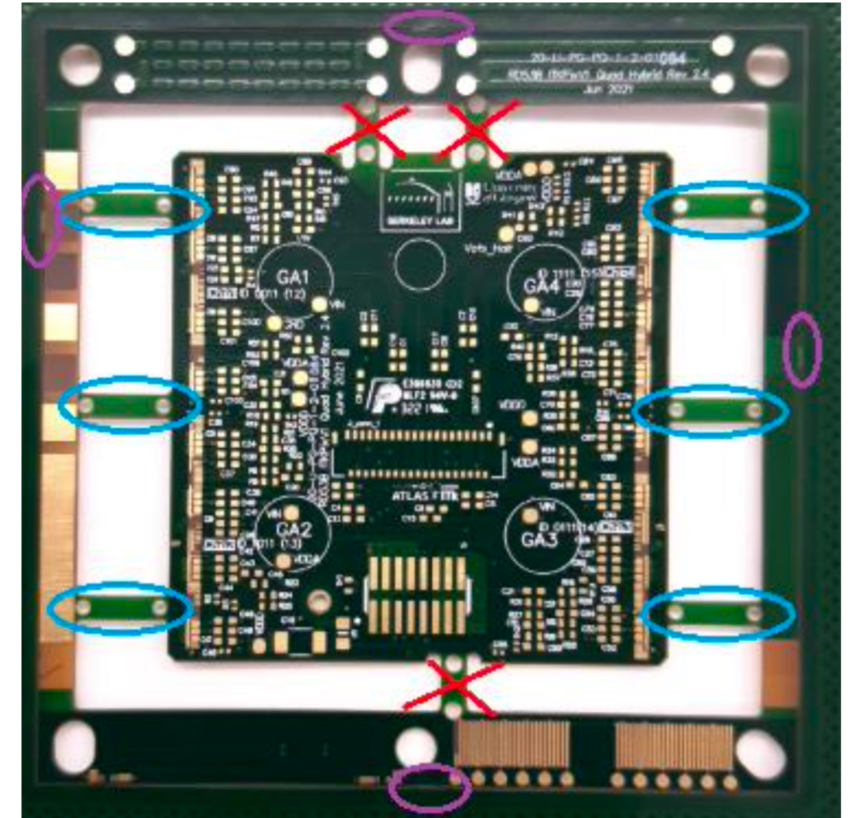


# Cutting stage summary

| **QC Cutting** | Frequency | Measurements |
|---|---|---|
| Tab cutting | All | Pass/fail |

# Hybrid QC Production and QC Testing Flow

- Reception
- Population
  - Visual Inspection
  - Component Position Check
- Tab cutting
  - Quick tab cutting inspection

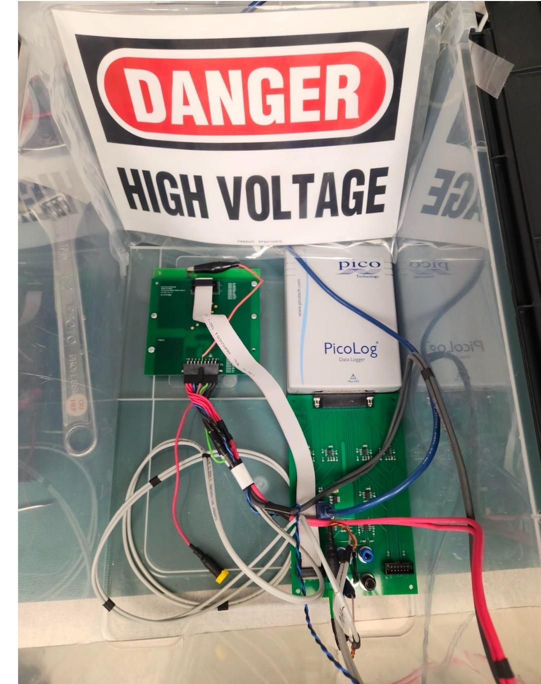


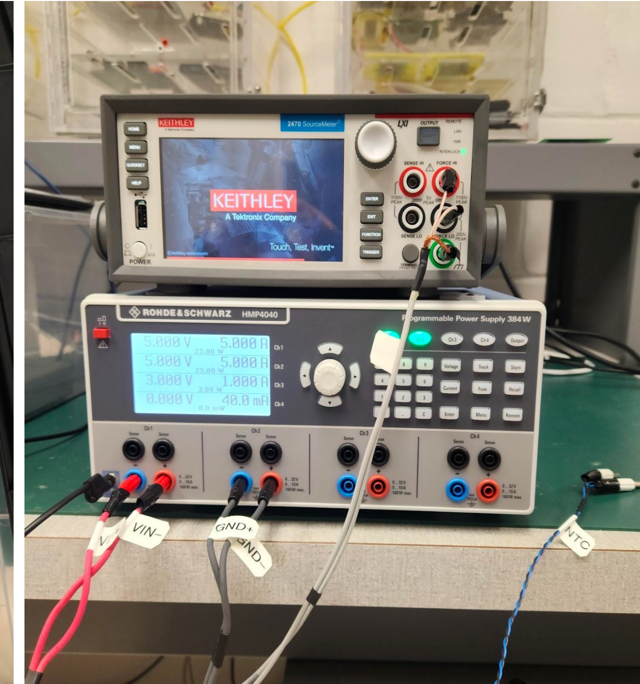
# QC stage summary

| **QC stage** | Frequency | Measurements |
|---|---|---|
| LV and HV test | All | LV and HV electrical tests including NTC measurement |
| Dowel hole tolerance check | All | Pass/fail |

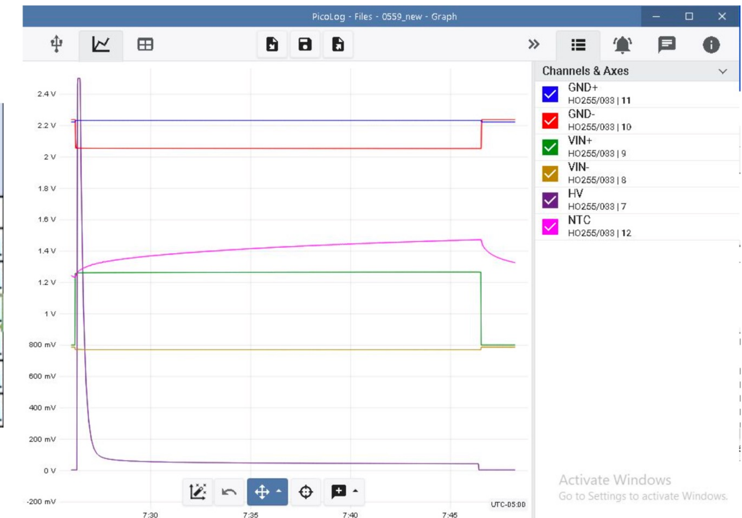
# LV – HV test

- LV test
  - GND drop, Vin drop ➔ effective resistance
  - NTC value
- HV test
  - Leakage current
- Temperature, humidity

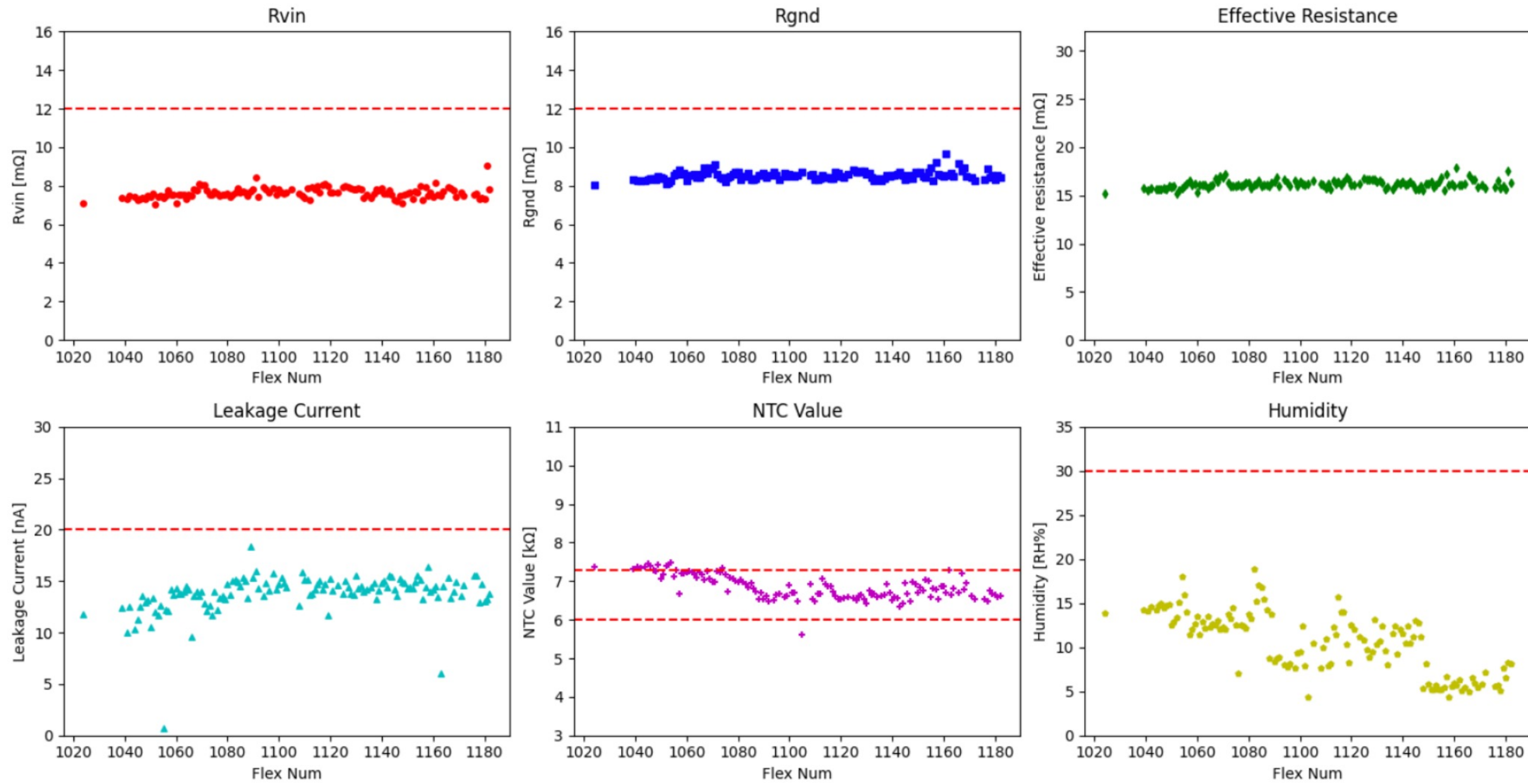



| Flex Serial number | VIN+ | VIN- | Vin Drop (V) | GND+ | GND- | GND Drop (V) | Capacitor leakage test (mV) | NTC reading (V) | Resistance Vin(Ohms) | Resistance GND(Ohms) | Total Resistance( m Ohms) | Capacitor Eqivalent leakage current(nA) | NTC Value(Kohms) | Temperature | Humidity |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 20-U-PG-PQ-2-1-1-0241 | 1.301 | 0.769 | 0.532 | 2.233 | 2.004 | 0.229 | 60 | 1.612 | 0.01064 | 0.00458 | 15.22 | 6 | 6.328 | 23 | 51 |
| 20-U-PG-PQ-2-1-1-0243 | 1.328 | 0.77 | 0.558 | 2.234 | 1.995 | 0.239 | 52 | 1.62 | 0.01116 | 0.00478 | 15.94 | 5.2 | 6.296 | 23 | 51 |
| 20-U-PG-PQ-2-1-1-0335 | 1.485 | 0.767 | 0.718 | 2.241 | 1.828 | 0.413 | 21 | 1.842 | 0.01436 | 0.00826 | 22.62 | 2.1 | 5.537 | 23 | 51 |
| 20-U-PG-PQ-2-1-1-0557 | 1.525 | 0.766 | 0.759 | 2.234 | 1.988 | 0.246 | 52 | 1.669 | 0.01518 | 0.00492 | 20.1 | 5.2 | 6.111 | 23 | 51 |
| 20-U-PG-PQ-2-1-1-0559 | 1.264 | 0.769 | 0.495 | 2.231 | 2.052 | 0.179 | 42 | 1.47 | 0.0099 | 0.00358 | 13.48 | 4.2 | 6.939 | 23 | 51 |
| 20-U-PG-PQ-2-1-1-0560 | 2.114 | 0.753 | 1.361 | 2.244 | 1.75 | 0.494 | 67 | 1.989 | 0.02722 | 0.00988 | 37.1 | 6.7 | 5.128 | 23 | 51 |



# LV– HV test



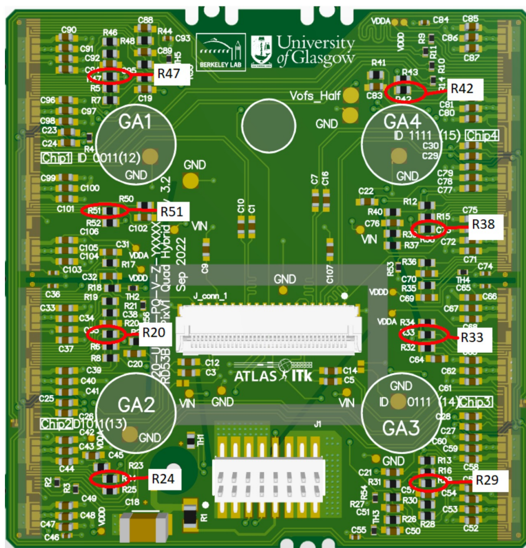

Slide borrowed from Koji

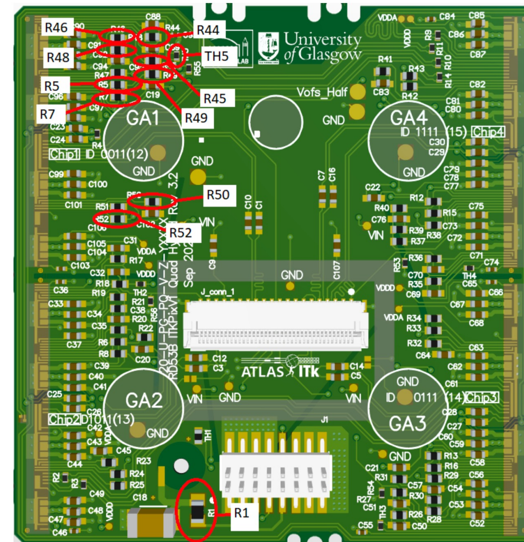
# QA pre-thermal cycle / thermal shock stage summary

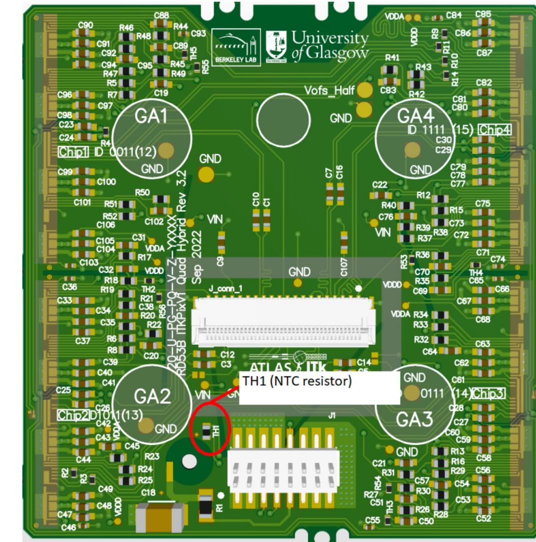
| **QA pre-thermal tests** | Frequency | Measurements |
|---|---|---|
| Metrology | | Flex body dimensions (X, Y)<br>Diameter of dowel hole A and width of slot-B<br>Output from Jig testing(pass/fail) |
| SLDO and precision resistor measurement | | Resistor values and tolerance |
| NTC Verification | | NTC value and parameters |
| Signal transmission test | | S-parameter and Impedance values and plots |
| Via resistance test | | Resistance |
| Wirebond pull test | | Strength and failure |

# QA testing

- SLDO and precision resistors
  - 5-10 flexes per batch
  - When a new reel of resistors has been loaded (information from population vendor)
- NTC verification
  - 5-10 flexes per batch
  - When a new reel of resistors has been loaded (information from population vendor)
  - +40 C, 0 C, -40 C in the environmental chamber ➔ with the soak time of 1h at each step

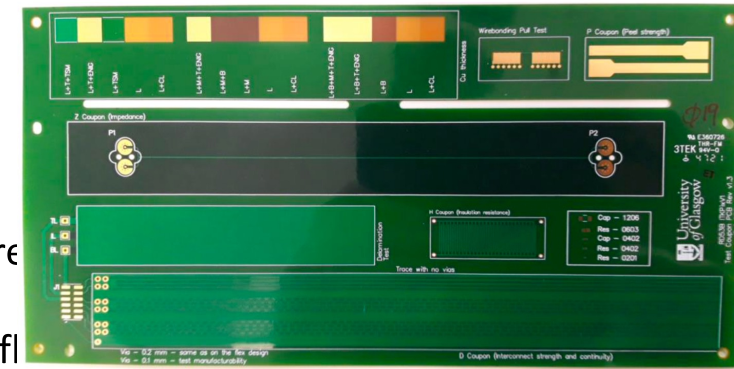


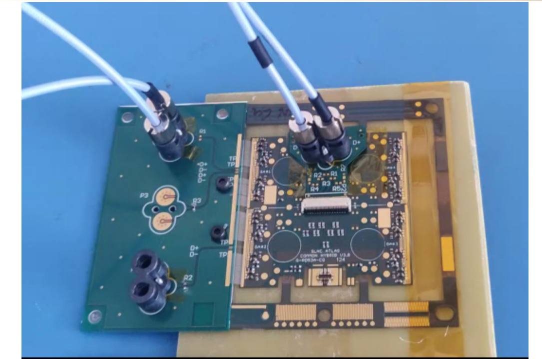



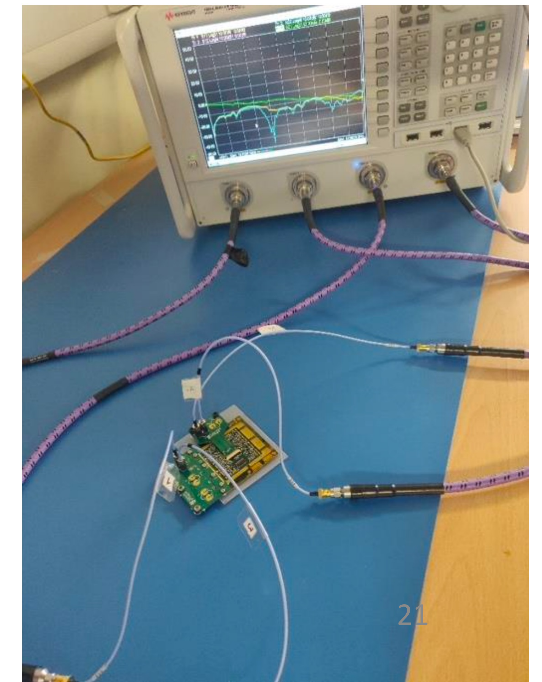



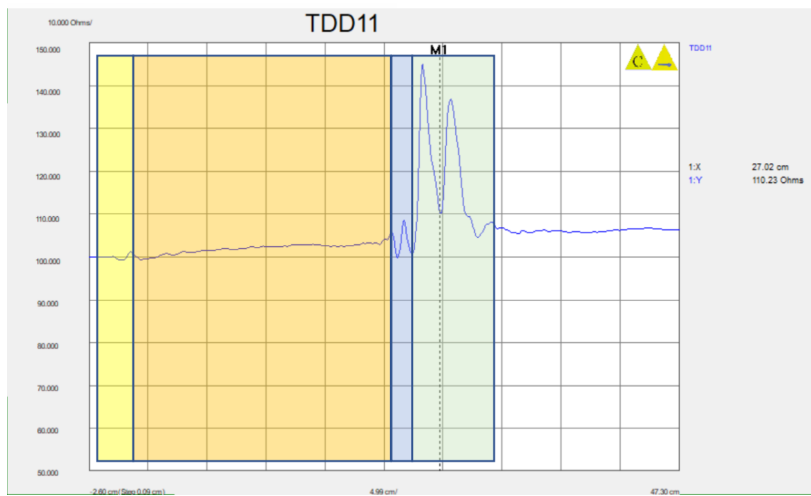
# Signal transmission

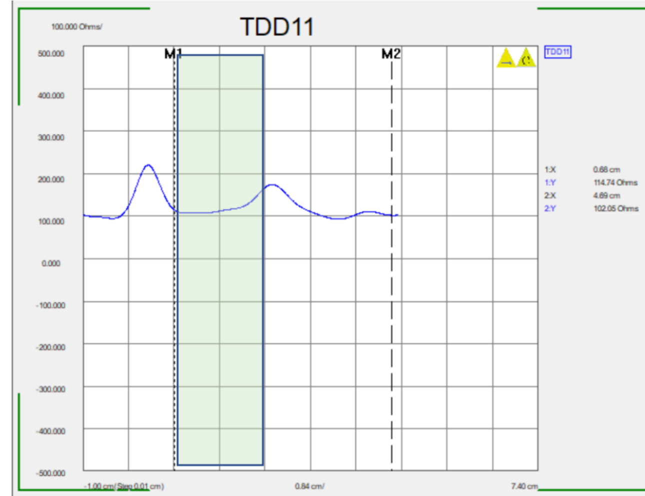
- Signal transmission test measures the S-parameters to understand the losses and to ensure these meet the specifications
- This test verifies that the correct stack-up and dielectric is used in the construction of the fl to ensure that the impedance is within specifications
- Specifications
  - Differential impedance of the transmission lines 100 Ω ± 10%
  - Attenuation of the signal, measured at 0.64 GHz, <2 dB
  - Signal transmission on the module PCB and via the connector must have a crosstalk attenuation of > 30 dB
- Procedure:
  - Measure the S-parameters for the uplink/downlink for data/cmd respectively
  - Derive the impedance from the S-parameters measurement using the pseudo-TDR measurement feature in the test system of the network analyser
  - S21 and S22 recorded at 640MHz
  - Also done on the test coupon for a differential pair structure





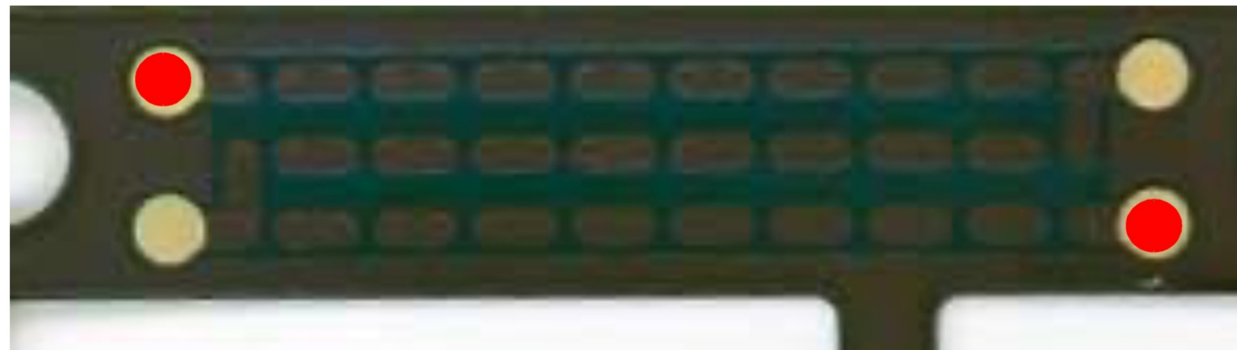




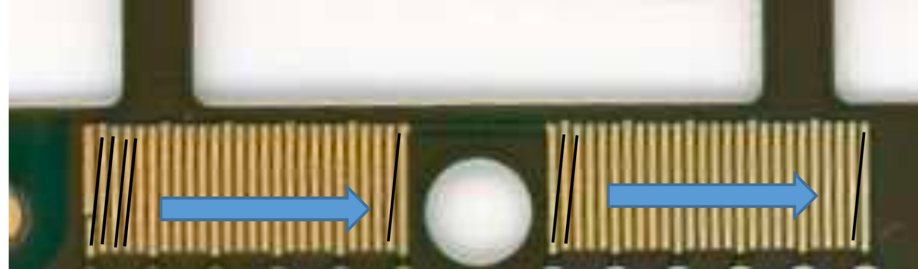
# Via chain resistance testing

- Via resistance measurements ensure that the flex substrate is not being damaged by thermal cycling
- Measurements to be repeated before and after thermal cycling (and thermal shock as a destructive test)
    - Pre-post difference in resistance of < 4 Ohms
- Check if thermal cycling causes any delamination of the flex, and therefore damaging the vias, altering their resistance
- Flexes are thermally cycled in an environmental chamber from -45°C to +60°C
- 5-10 flexes per batch and on test coupons



# QA tests –Wirebond pull test

- Check if the surface finishing is suitable for a high-quality and reliable wirebond
- Wirebonds are tested pre and post thermal cycles
- Thermal chamber from -45°C to +60°C for 1(and 100) cycle
- 5-10 flexes per batch



# QA post-thermal cycle / thermal shock stage summary

| **QA pre-thermal tests** | Frequency | Measurements |
|---|---|---|
| NTC Verification | | NTC value and parameters |
| Via resistance test | | Resistance |
| Wirebond pull test | | Strength and failure |

# QA post-radiation cycle stage summary

| | Frequency | Measurements |
|---|---|---|
| Signal transmission test | | S-parameter and Impedance values and plots |
| Via resistance test | | Resistance |

# Hybrid QC Production and QC Testing Flow

- Reception
- Population
- Tab cutting
- QA pre-thermal cycle / thermal shock
- QA post-thermal cycle / thermal shock
- QC
- QA post radiation cycle
- PCB Reception at module site
  - Visual inspection
  - Mass
  - Metrology

# Hybrid QC Production and QC Testing Flow

- Reception
- Population
- Tab cutting
- QA pre-thermal cycle / thermal shock
- QA post-thermal cycle / thermal shock
- QC
- QA post radiation cycle
- PCB Reception at module site
- Data uploaded to production DB at each stage

# Hybrid QC/QA data management

- Hybrid component type created in the PDB as well as the production stages and associated tests

**Type List**

Actions

| Name | Code | Subproject | SN |
|---|---|---|---|
| Triplet L0 Stave PCB | TRIPLET_L0_STAVE_PCB | Inner pixels | PT |
| Triplet L0 R0 PCB | TRIPLET_L0_R0_PCB | Inner pixels | P0 |
| Triplet L0 R0.5 PCB | TRIPLET_L0_R0.5_PCB | Inner pixels | P5 |
| Quad PCB | QUAD_PCB | Pixel general | PQ |

**Stage List**

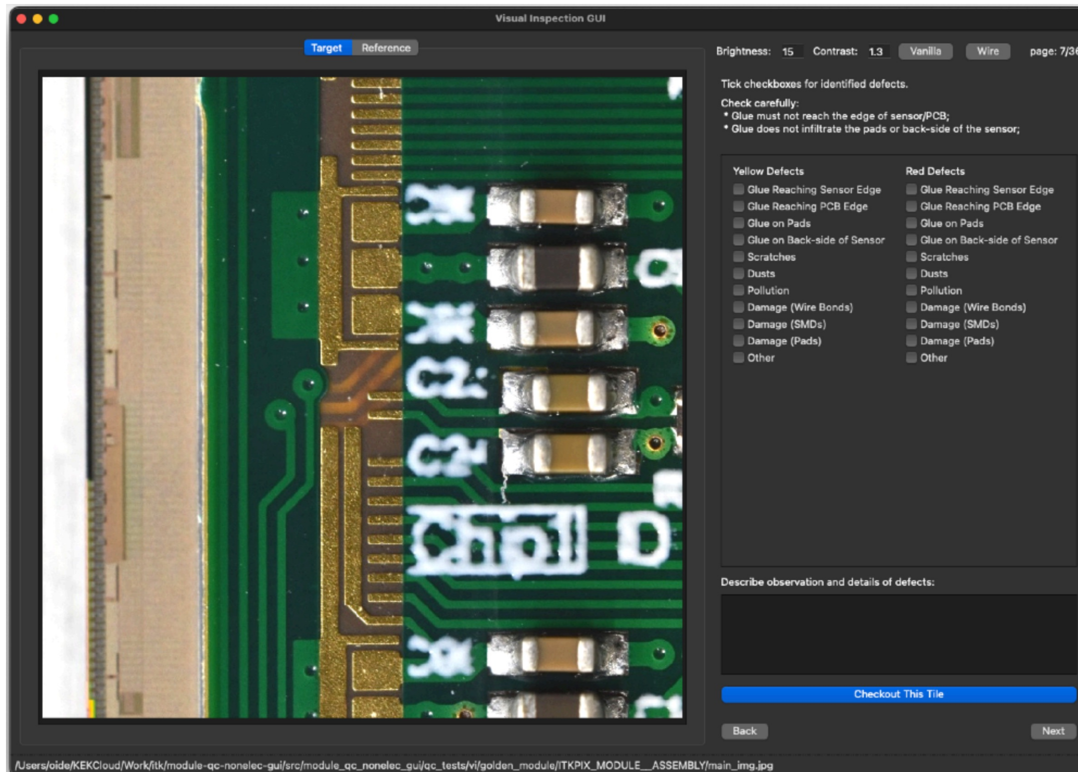
Actions — Add

| Name | Code | Type | |
|---|---|---|---|
| Reception | PCB_RECEPTION | INITIAL | Tests 6 |
| Population | PCB_POPULATION | | Tests 2 |
| Cutting | PCB_CUTTING | | Tests 1 |
| QA pre-thermal cycle / thermal shock | QA_PRE_THERMAL_CYCLE | ALTERNATIVE | Tests 7 |
| QA post-thermal cycle / thermal shock | QA_POST_THERMAL_CYCLE | ALTERNATIVE | Tests 3 |
| QC | PCB_QC | | Tests 2 |
| QA post radiation cycle | QA_POST_RADIATION_CYCLE | ALTERNATIVE | Tests 2 |
| Test failed, needs investigation | UNHAPPY | ALTERNATIVE | Tests |
| PCB ready for module | PCB_READY_FOR_MODULE | | Tests |
| PCB Reception at module site | PCB_RECEPTION_MODULE_SITE | | Tests 3 |

# Flex QC data management

- Non-electrical GUI + localDB

➔ upload to production DB




20UPGPQ2110243

Module PCB - Quad PCB

Basic Info

| | |
|---|---|
| ATLAS Serial Number | 20UPGPQ2110243 |
| Alternative Identifier | No alternative identifier |
| Component Type | Module PCB PCB |
| Type | Quad PCB |
| Current Stage | POPULATION |
| Current Location | University of Oklahoma OKLAHOMA |
| Shipment Destination | No current shipment destination |
| Home Institute | University of Edinburgh EDI |

Top | Modules | PCBs | Bare Modules | Sensors | QC Tests | YARR Scans

Top Page > Component List > 20UPGPQ1101197

20U PG PQ 11 01197

Quad-PCB/Prototype/EPEC-100um

ITkPD Component Page

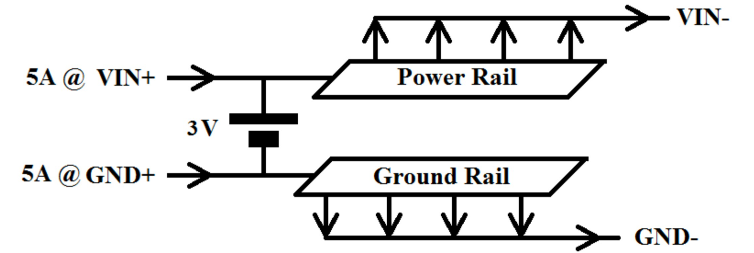
Component Information

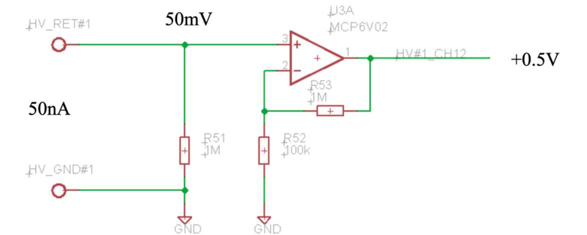
No match.

| Item | Value |
|---|---|
| Serial Number | 20UPGPQ1101197 |
| Production DB Component ID | 0551a0e5c93529ea88a7c52865cb3eca |
| LocalDB Component ID | 63e1800cb5aac100367799a5 |
| Component Type | module_pcb |
| Super-Component | 20UPGR92101197 |

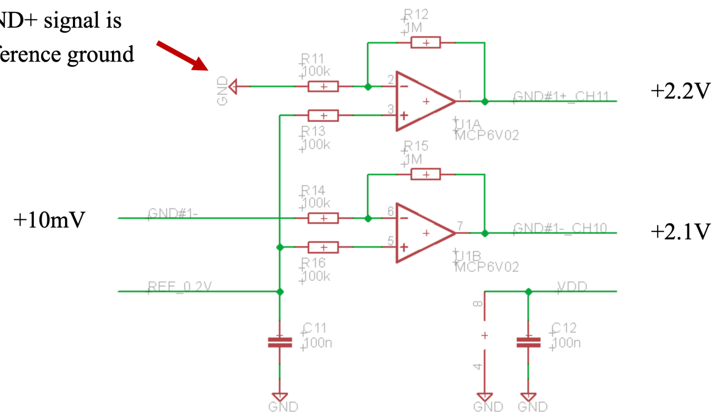
# Back up

# LV – HV test

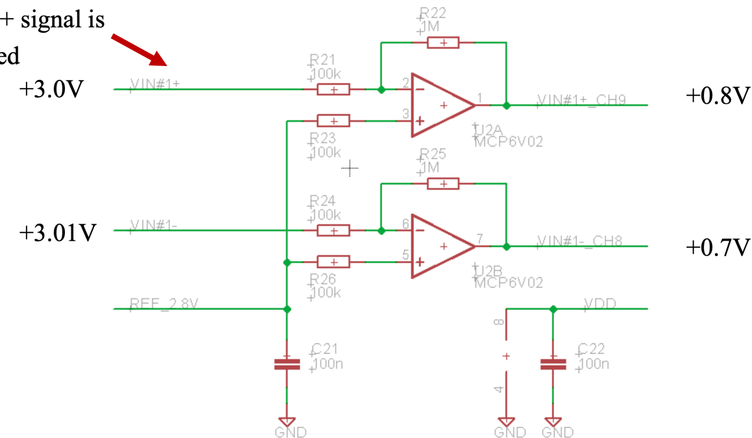


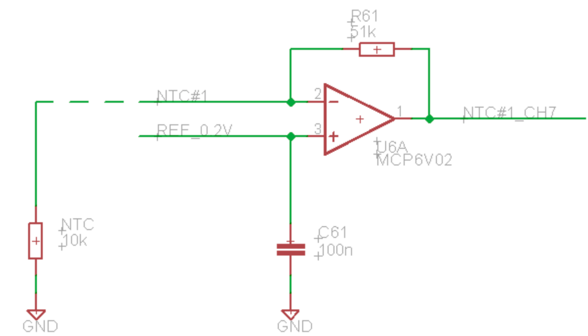




GND+ signal is reference ground




VIN+ signal is biased



# Hybrid QC/QA data management

- PCB design version
- PCB manufacturer technology
- PCB manufacturer
- SMD population vendor

# Hybrid QC/QA data management

PCBs are tracked as batches

- Batch for each set of bare PCBs received from the manufacturer
- Batch for each set of bare PCBs received from the population vendor

Bare PCB batch properties:

- PCB design stack-up total thickness
- PCB manufacturer batch number
- Date panel manufactured PCB Manufacturer
- PCB Manufacturer Ionic contamination result
- Number of panels with all good flexes
- Number of panels with one cross out
- Number of panels with more than one cross-out

Populated PCB batch properties:

- SMD population batch number
- Date SMD loaded
- SMD NTC manufacturer part number
- SMD NTC nominal value
- SMD NTC tolerance
- HV capacitor nominal value
- HV capacitor rating
- HV resistor nominal value
- HV resistor tolerance
- SLDO resistor nominal value (analogue)
- SLDO resistor tolerance (analogue)
- SLDO resistor nominal value (digital)
- SLDO resistor tolerance (digital)
- PCB Manufacturer SMD population vendor
- SMD Population Ionic Contamination result

# Site Qualification Process

- Procedure documents and requirements table are prepared by the SQ team
- Complete draft upload to EDMS
- Circulation for comment for 1 week
    - Comments addressed
- Released for SQ
    - Following feedback from the first few groups, make any changes to the documents
- Circulation for comment on EDMS
    - Comments addressed
- EDMS approval

# Site Qualification Process

## Lab infrastructure - cleanroom

- Particle concentration compatible with class 9 ISO 14644-1
- Particle count in the cleanroom should be regularly monitored, and a system should be in place to alert operators if the count has gone out of specification
- Cleanroom operators wear the following lab garments: ISO9 compatible Lab coat, hairnet, shoes/shoe covers, cleanroom gloves and face mask
- Dew point has to be below the module temperature when it is being handled
- Temperature and humidity of the testing site cleanroom should be monitored to alert operators if the conditions have gone out of specification

## Lab infrastructure – storage area

- Temperature 18C to 24C and RH 0 to 30% and ESD protection
  - Model of cabinets and how low humidity is achieved
- Notification system for out-of-spec temperature and RH that is able to report
- Storage space is sufficient for at least 4 weeks of planned production rate

## Lab infrastructure - shipping

- Shipping containers will have to maintain module cleanliness, ESD protection (refer to IEC 61340-5-1 and IEC 61340-5-2) as well as reduce and measure mechanical shock
  - Use Pelicase or equivalent for external case. Place PCB in a sealed ESD bag. List indicators and sensors planned to be used for shipments
- Shipping is performed in the database

# Site Qualification Process

- Database interaction

# Site Qualification Process for Flex QC

3.1 Visual inspection of bare flexes

3.2 Layer thickness measurement

3.3 Metrology

3.4 Visual inspection of populated flexes

3.5 LV/HV test

- Report the findings on 5 flexes

# Site Qualification Process for Flex QA

4.1 Signal transmission test on flex

4.2 Thermal cycling

4.3 Thermal shock

4.4 Extensive QA HV test (pre- and post-thermal cycling)

- HV test upto 1100V
- HV soak test to identify defects due to prolonged HV to the circuit

4.5 QA tests - Measuring SMD components values, Via resistance, delamination,insulation resistance

4.6 QA peel test

- Measure the peel strength of the Cu to the laminate (Done by the vendor)

4.7 Wirebond pull test (pre- and post- thermal cycling)

4.8 HV capacitor QA test

- Performed on a HV capacitor coupon with multiple HV capacitors to ensure the correct capacitors are loaded and also check that the capacitors work as per the rating on the datasheet

# Site Qualification Process

# Additional tests on the test coupon

- Peel test
    - Requested as a part of the PCB fabrication so will not be done as a part of flex QC
- Delamination test
    - Measure capacitance between copper planes before and after thermal cycling (and thermal shock)
    - Ensures copper planes don’t deform as a consequence of thermal cycling process
- Insulation Resistance test
    - Apply HV between one pair of conductor tracks (traces) and measure the resulting leakage current to ensure the insulation resistance is sufficiently high (example around or above 100 GOhms)

# Additional tests on the test coupon

- Repeat the LV-HV test for the extender period (soak test)
- Repeat the test by running the test for 8 hrs
- Repeat the test by running overnight

# HV capacitor QA test

Test to ensure that the correct capacitor is loaded on the flex PCBs

This PCB should be populated in the same run as the flex PCBs

- The HV capacitor PCB has 50 capacitors connected between HV and GND
- Apply HV (650Vx1.5 = -975V) for 20 mins and record the observation

Module specification document

- The HV filter surface mount capacitor will be either a "High Reliability Capacitor" having met the MIL-PRF-49467 specification rated to the maximum operational sensor bias or a standard component rated to twice the maximum operational sensor bias
- The HV capacitor chosen will be sample tested with each lot qualified by testing 5% or 200 units (whichever is the lesser number) with no failures
- Test conditions are 100$^{o}$C with a test voltage applied for 1 hour with a measured leakage current < 10 nA on all tested parts