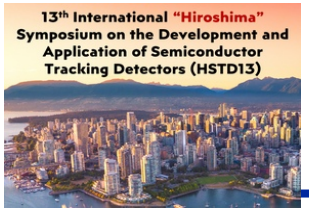
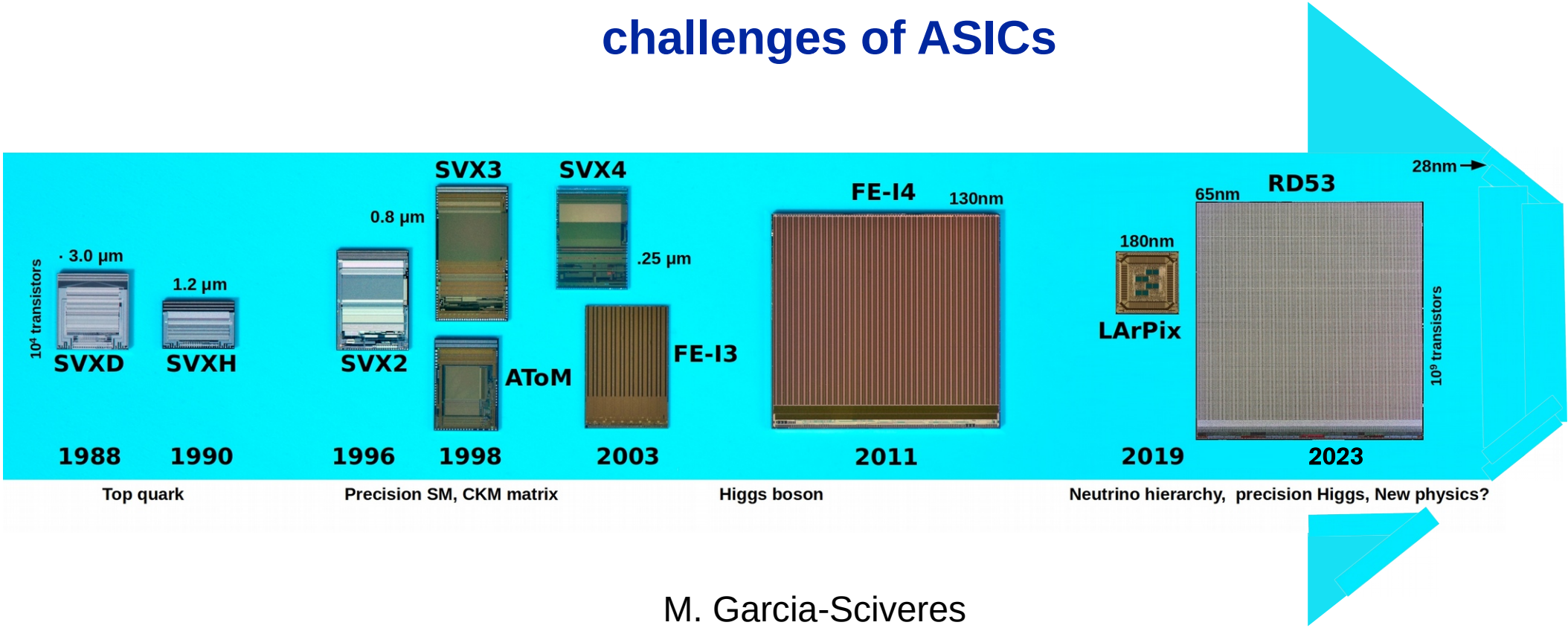


Future directions and challenges of ASICs

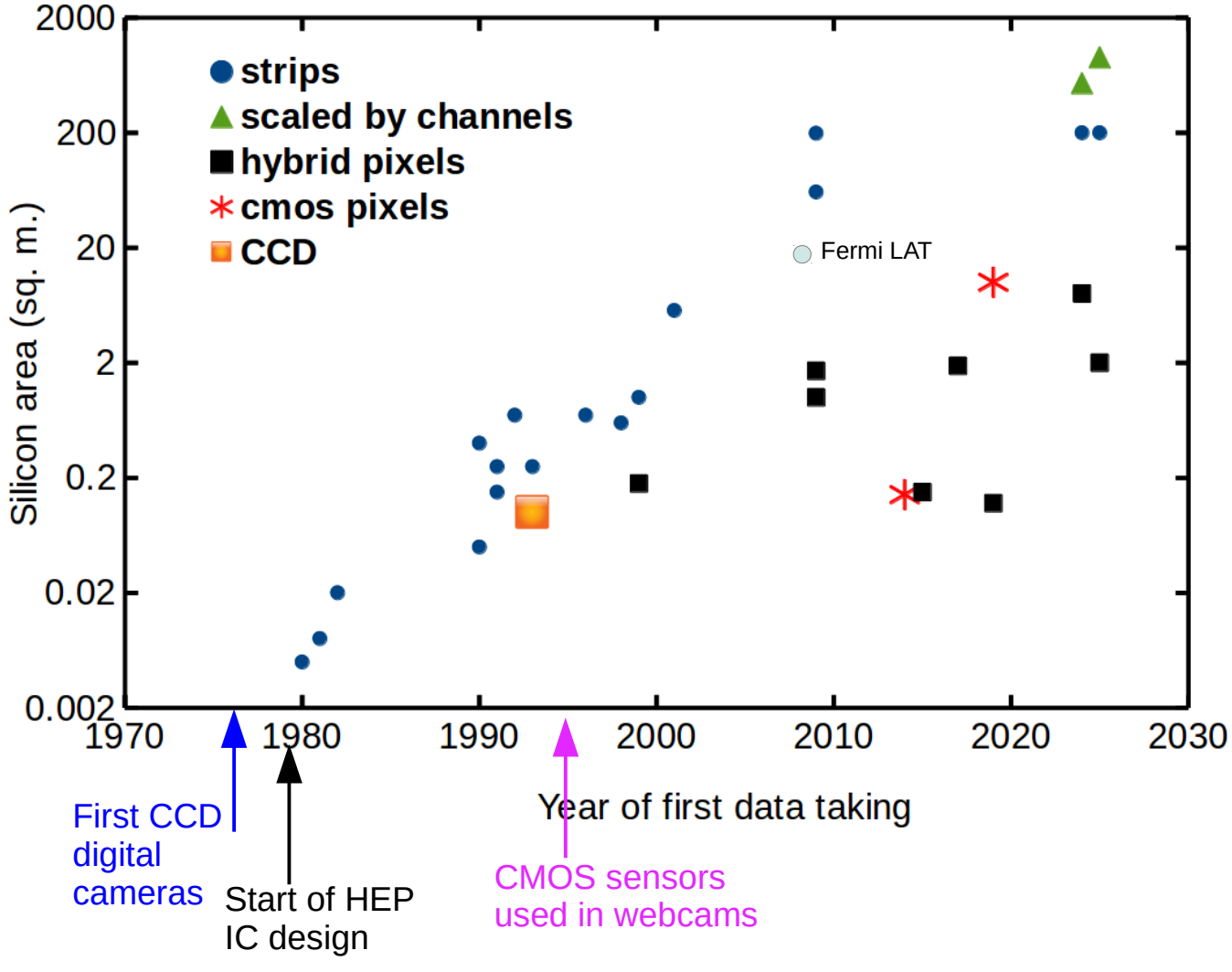


M. Garcia-Sciveres
Lawrence Berkeley National Lab

2023 HSTD13 – Vancouver

Silicon Detectors at Colliders

(and in orbit)



Strip Detectors

1980	NA1
1981	NA11
1982	NA14
1990	MarkII
1990	DELPHI
1991	ALEPH
1991	OPAL
1992	CDF SVX
1993	L3
1996	CDF SVX'
1998	CLEO III
1999	BaBar
2001	CDF SVXII+ISL
2009	ATLAS SCT
2009	CMS tracker
2025	ATLAS ITK
2025	CMS upgrade

Hybrid Pixels

1999	Delphi
2009	ATLAS
2009	CMS
2015	ATLAS IBL
2017	CMS
2019	velopix
2025	ATLAS
2025	CMS

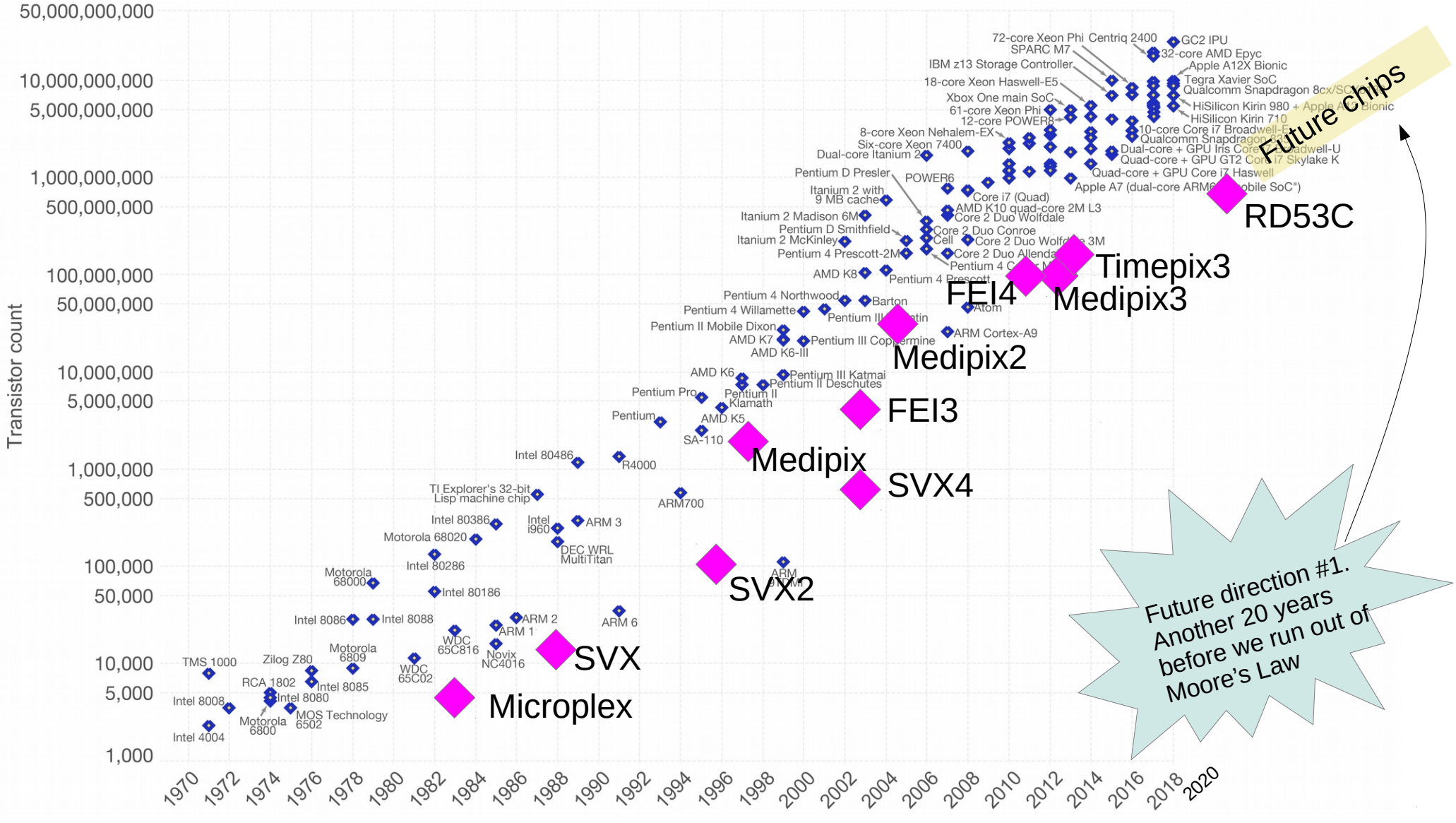
CMOS Pixels

2014	STAR
2019	ALICE

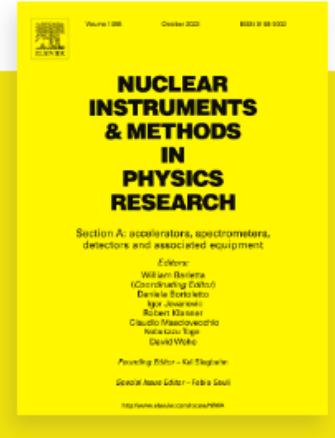
CCDs

1993	VXD

Tracker ICs vs Microprocessors



Aside: This Just Out:



Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

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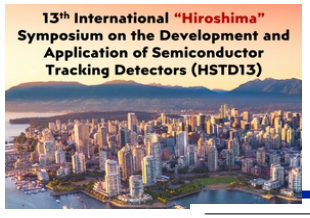
Microelectronics in High Energy Physics

Edited by

- Alessandro Marchioro Experimental Physics,CERN,Switzerland
- Philippe Farthouat Experimental Physics,CERN,Switzerland

Last update 21 August 2023



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journal homepage: www.elsevier.com/locate/nima

Particle physics experiments: From photography to integrated circuits

Erik H.M. Heijne *

IEAP/CTU, Husova 240/5, CZ 110 00 Prague 1, Czech Republic
CERN EP Dept, 1 Esplanade des Particules, CH 1211 Geneva 23, Switzerland
Nikhef, Science Park 105, 1098XG Amsterdam, Netherlands

Front-end electronics for silicon strip trackers: Architectures and evolution

Jan Kaplon

CERN, 1211 Geneva 23, Switzerland

Hybrid pixel readout integrated circuits

Maurice Garcia-Sciveres

Lawrence Berkeley National Laboratory, Berkeley, USA

Monolithic CMOS Sensors for high energy physics — Challenges and perspectives

W. Snoeys

CERN, Esplanade des Particules, CH-1211 Geneva 23, Switzerland

ASIC survival in the radiation environment of the LHC experiments: 30 years of struggle and still tantalizing

Federico Faccio

CERN, EP department, Esplanade des Particules 1, Meyrin, 1211, Switzerland

Radiation tolerant optoelectronics for high energy physics

Jan Troska [a,*], François Vasey [a], Anthony Weidberg [b]

[a] *EP Department, CERN, Esplanade des Particules, Geneva, 1211, Switzerland*
[b] *Physics Department, Oxford University, Denys Wilkinson Building, Oxford, OX1 3RH, United Kingdom*

ASICs for LHC intermediate tracking detectors

G. Hall [a,*], A.A. Grillo [b]

[a] *Blackett Laboratory, Imperial College, London SW7 2AZ, UK*
[b] *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA 95064, USA*

Cryogenic electronics for noble liquid neutrino detectors

Hucheng Chen *, Veljko Radeka

Brookhaven National Laboratory, Upton, NY, United States of America

Analog-to-digital converters and time-to-digital converters for high-energy physics experiments

Ping Gui

Southern Methodist University, Dallas, TX, USA

Radiation-hard ASICs for data transmission and clock distribution in High Energy Physics

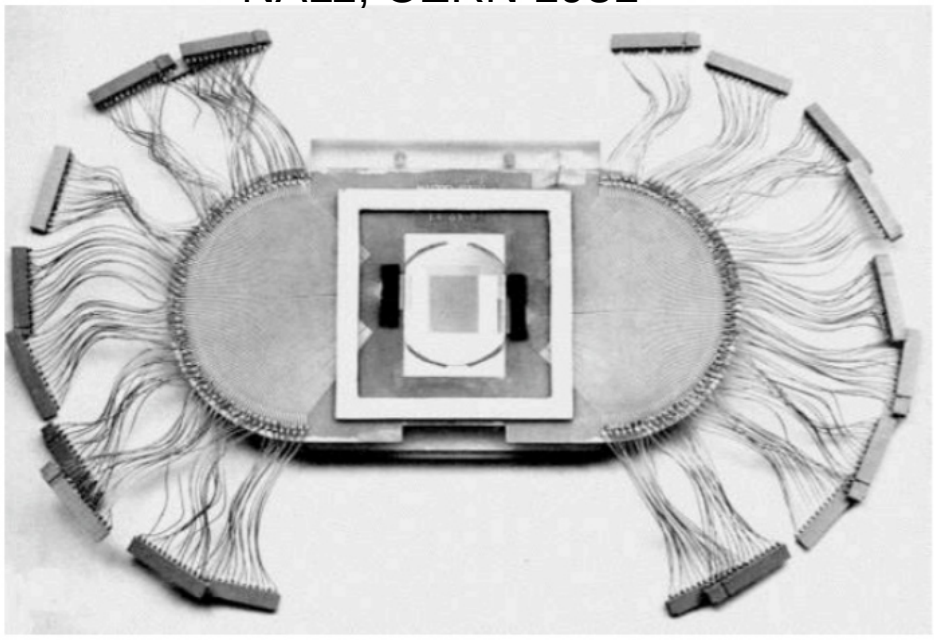
Paulo Moreira *, Szymon Kulis

CERN, European Center for Nuclear Research, Switzerland

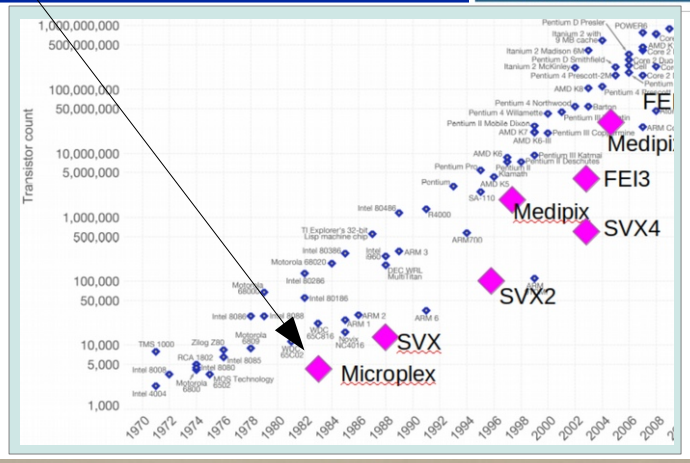
Why Microplex?

Because these were silicon strip modules before:

NA11, CERN 1981



NIM205 (1983) 99



They did not scale

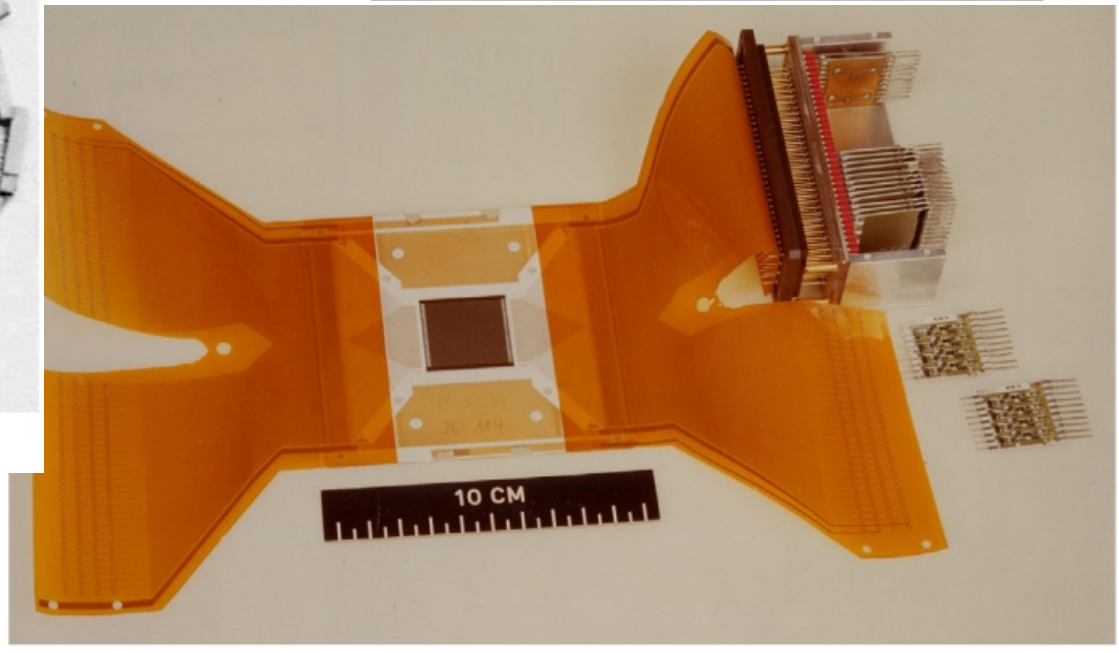
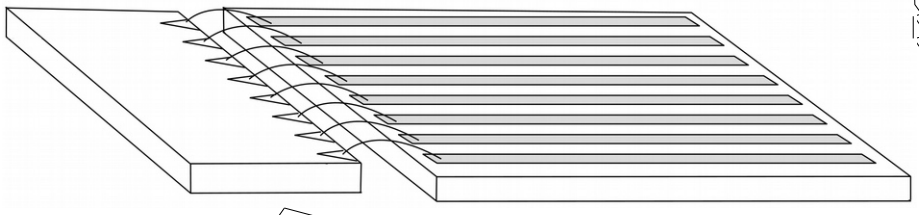
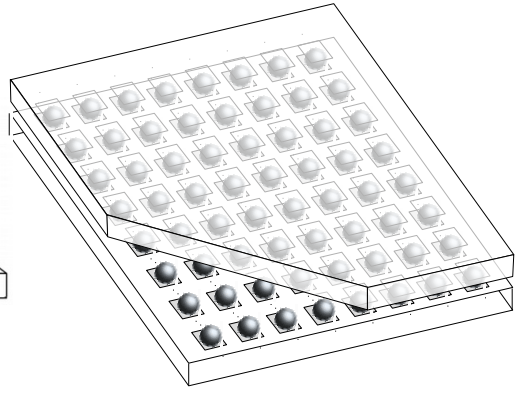


Fig. 13. Microstrip detector and the MSD2 4-channel hybrid readout circuits, providing high density signal processing in a relatively small volume (CERN photo-8310560).

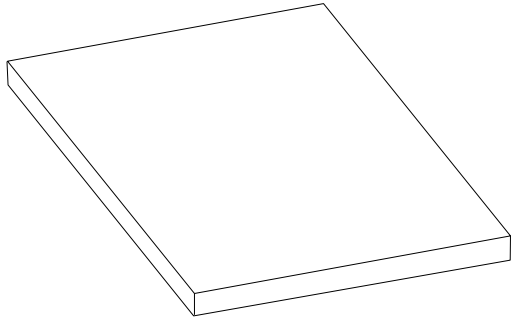
Silicon Tracker Types



Hybrid Strips

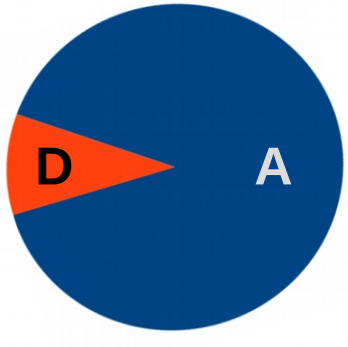


Hybrid Pixels

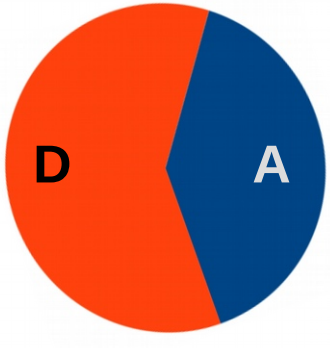


Monolithic

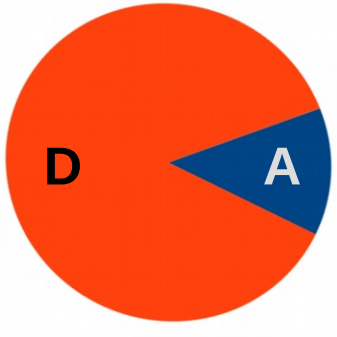
Strip IC balance of power



LEP



LHC

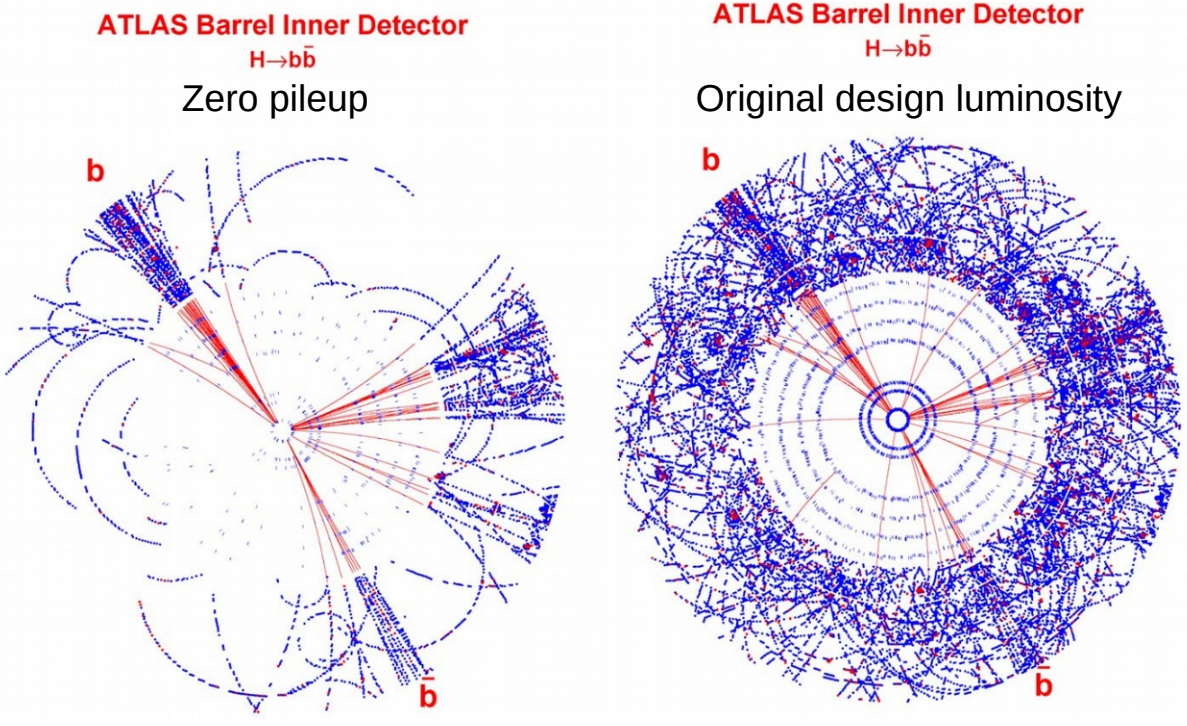


HL-LHC

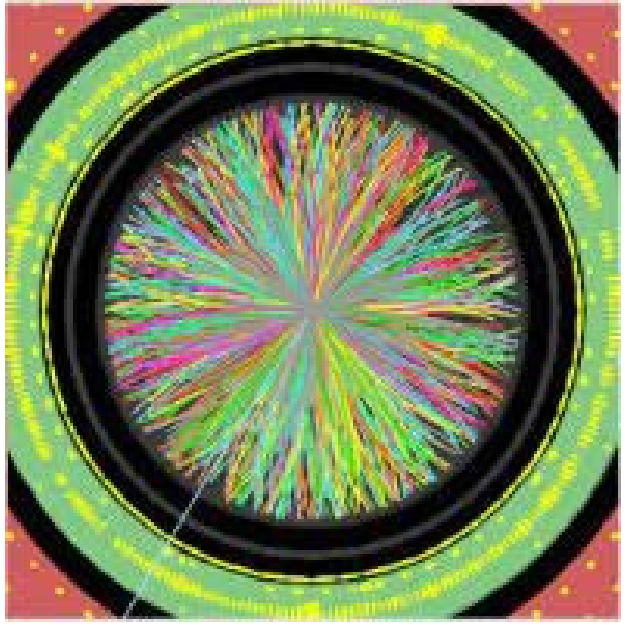
Future?

Hybrid Pixel Readout

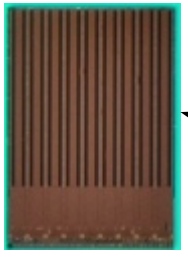
Original ATLAS motivation for pixels circa 1995



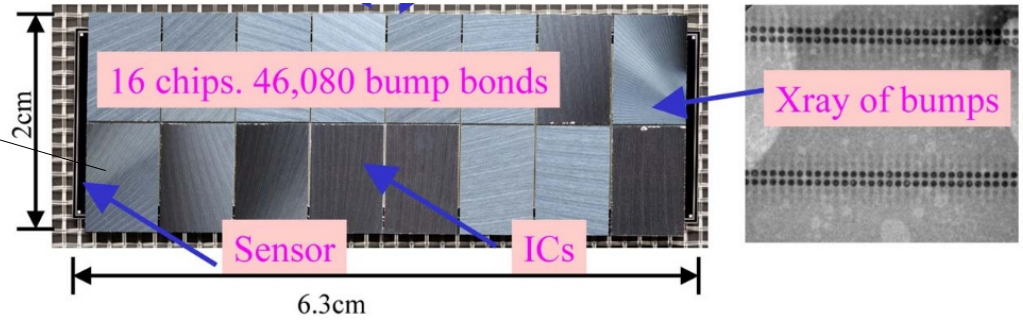
HL-LHC is far beyond



FE-I3 readout chip

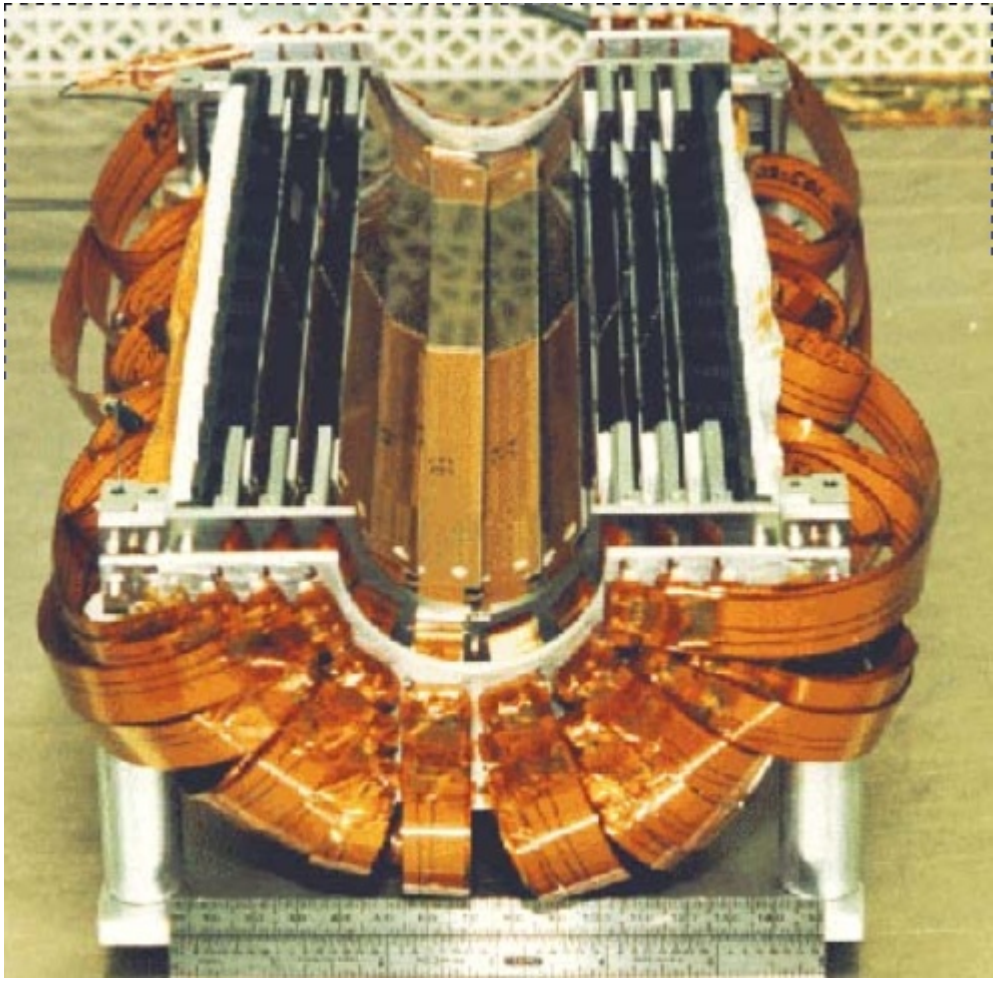


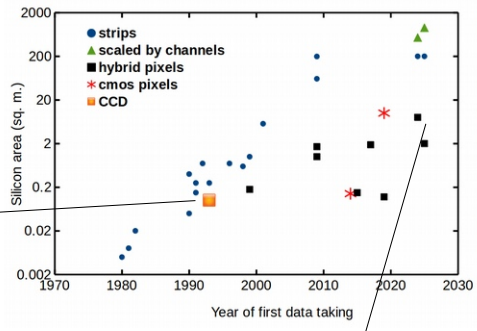
Solution:



It did not scale.
A new readout chip solution had to be developed

The Rate Extremes





SLD VXD

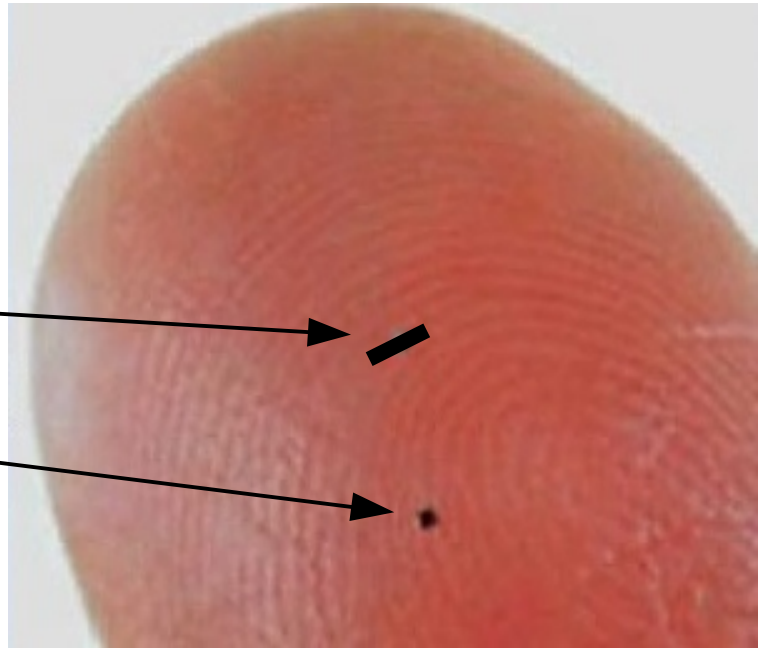
- Silicon area: 0.12 m²
- 300M pixels (20μm x 20μm)
- But only 350,000 Z decays recorded
- => most pixels were never hit by real collision particle!

HL-LHC

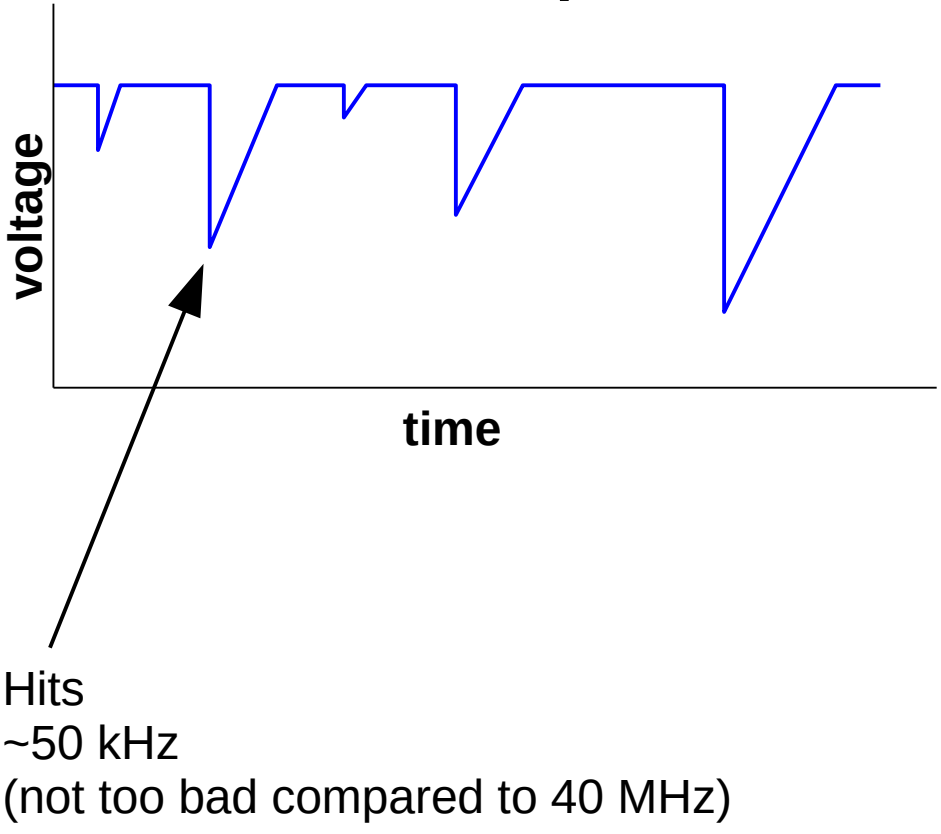
- Inner layers of ATLAS and CMS high luminosity upgrades will see 10 collision particles in every Si atom!

Single Pixel Perspective

Pixel size

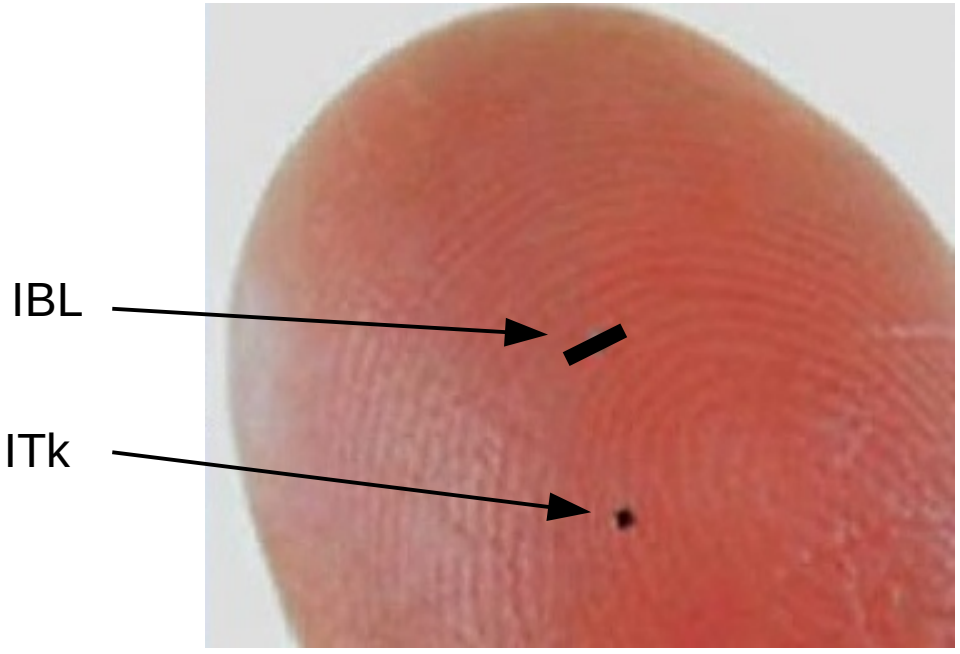


Pixel output

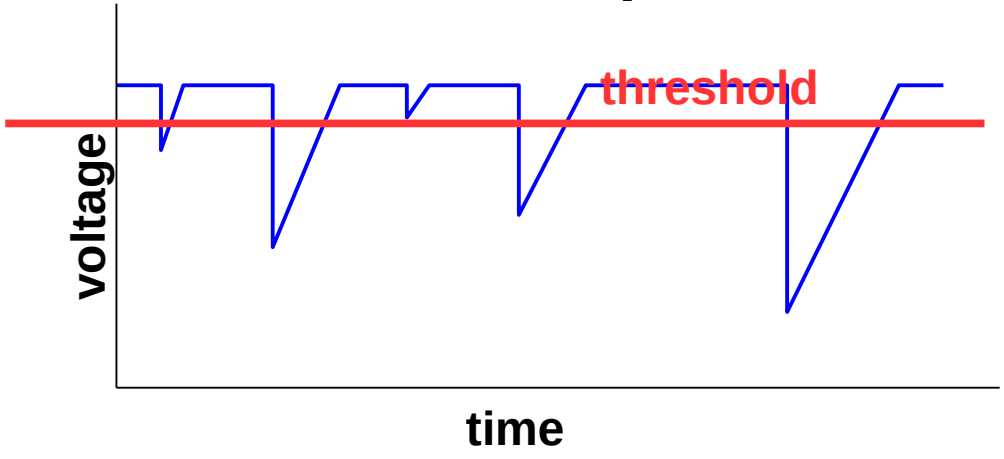


Single Pixel Perspective

Pixel size

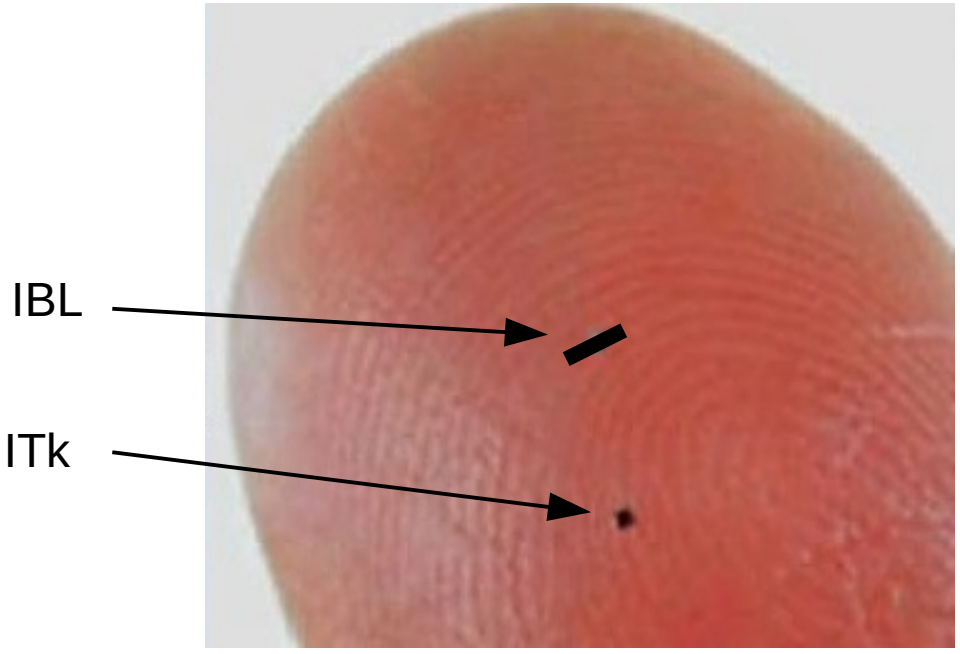


Pixel output

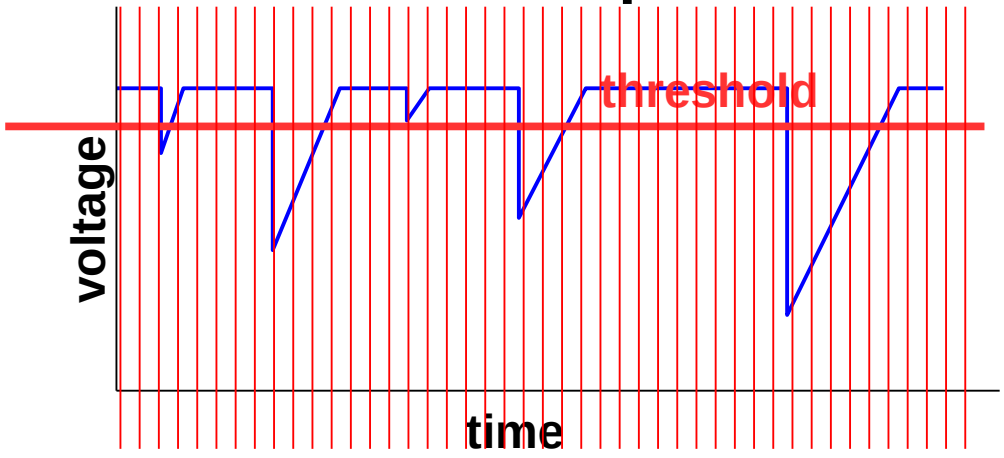


Single Pixel Perspective

Pixel size



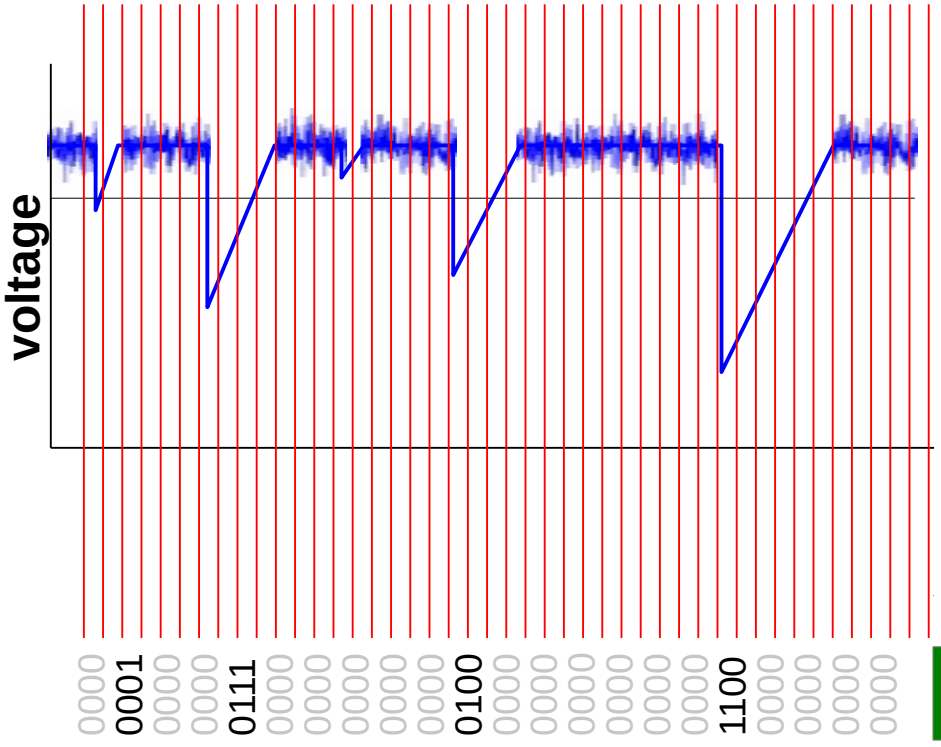
Pixel output



Bunch crossings

Digitize amplitude above threshold in each Bunch Crossing

On-Chip Storage and Trigger



On-chip memory ("FIFO")

Readout ~Gbps

Storage of all individual hits W/ ADC value (~40 Gbps for a 100Kpx chip)

Triggers (select 1/40 time slices)

Storing data at 40Gbps

High rate pixel readout chips are memories (in addition to being pixel readout chips)

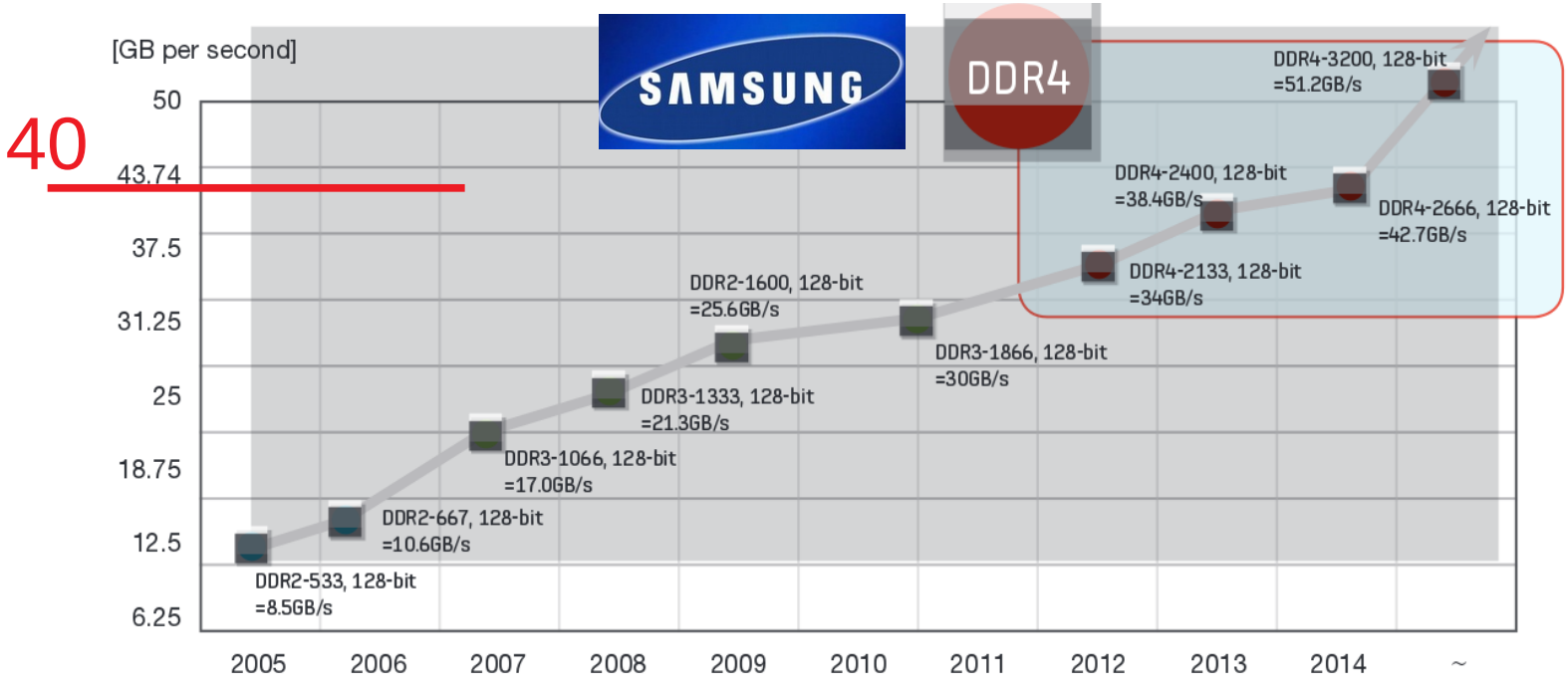
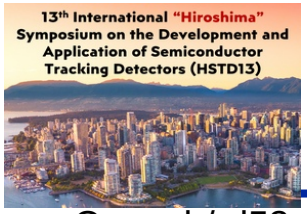


Figure 2. DDR4 higher performance compared with DDR3L and DDR2

Plot is for a memory module containing 8 silicon chips so B = b

(and this is not rad hard)

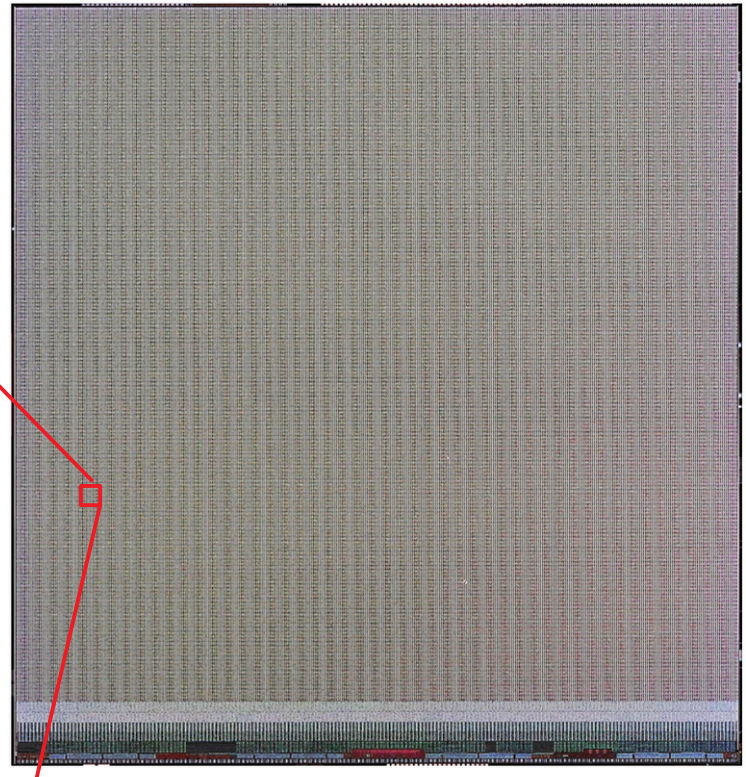


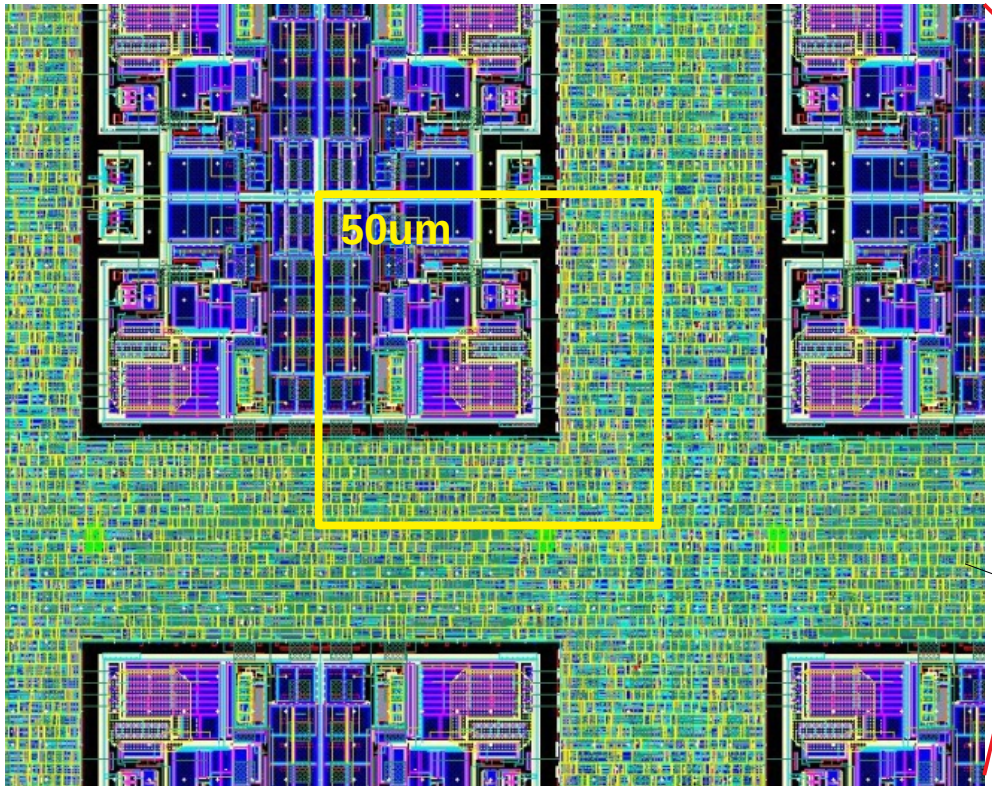
RD53 Hybrid Pixel Readout for higher rate and radiation

Cern.ch/rd53

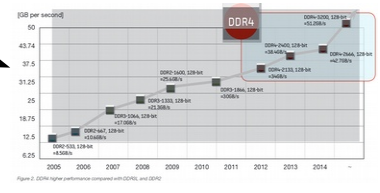
RD-53 Collaboration Home

RD-53 will design and produce the next generation of readout chips for the ATLAS and CMS pixel detector upgrades at the HL-LHC. More details can be found in the 2018 extension proposal and the original collaboration proposal.

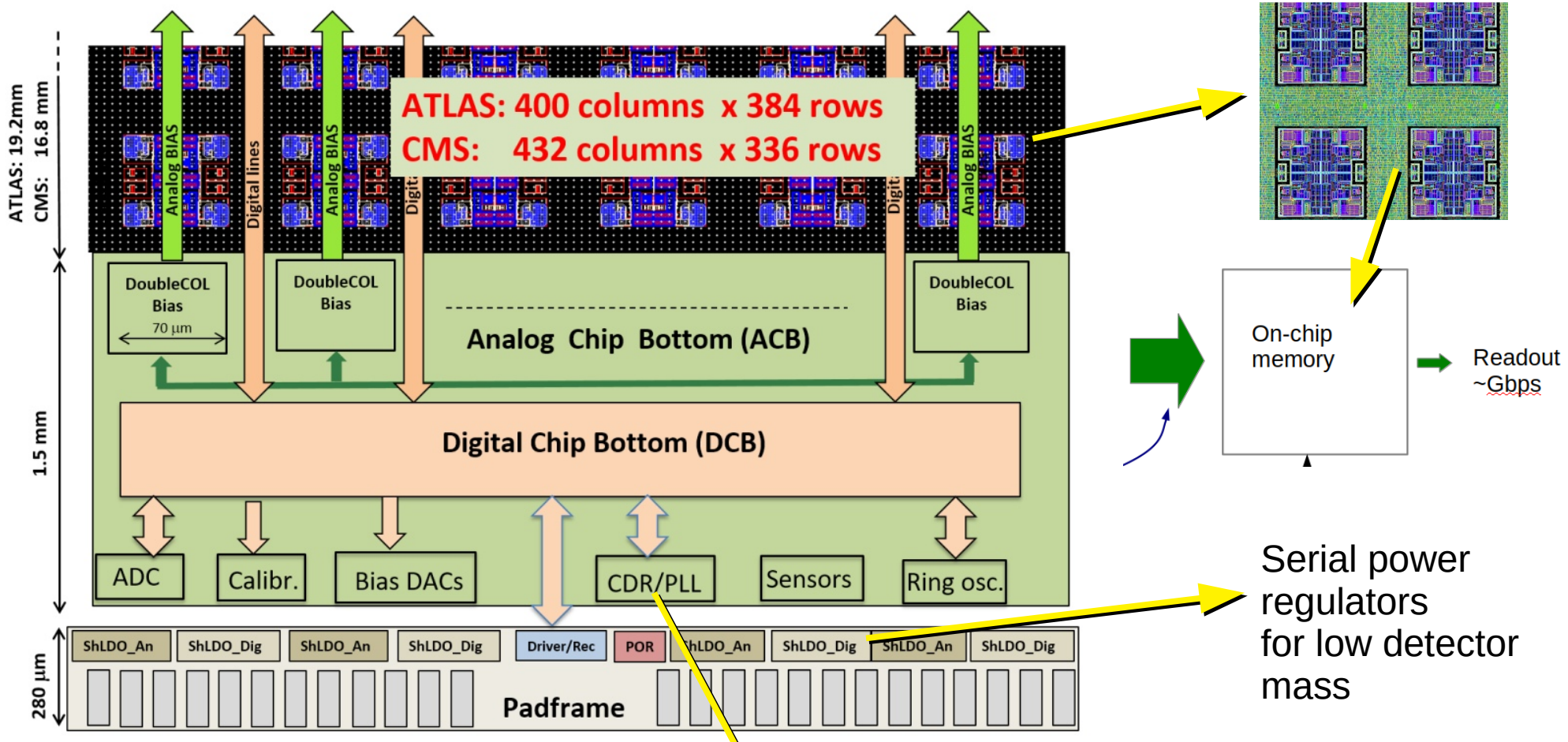




~1000 transistors



Complex system on chip

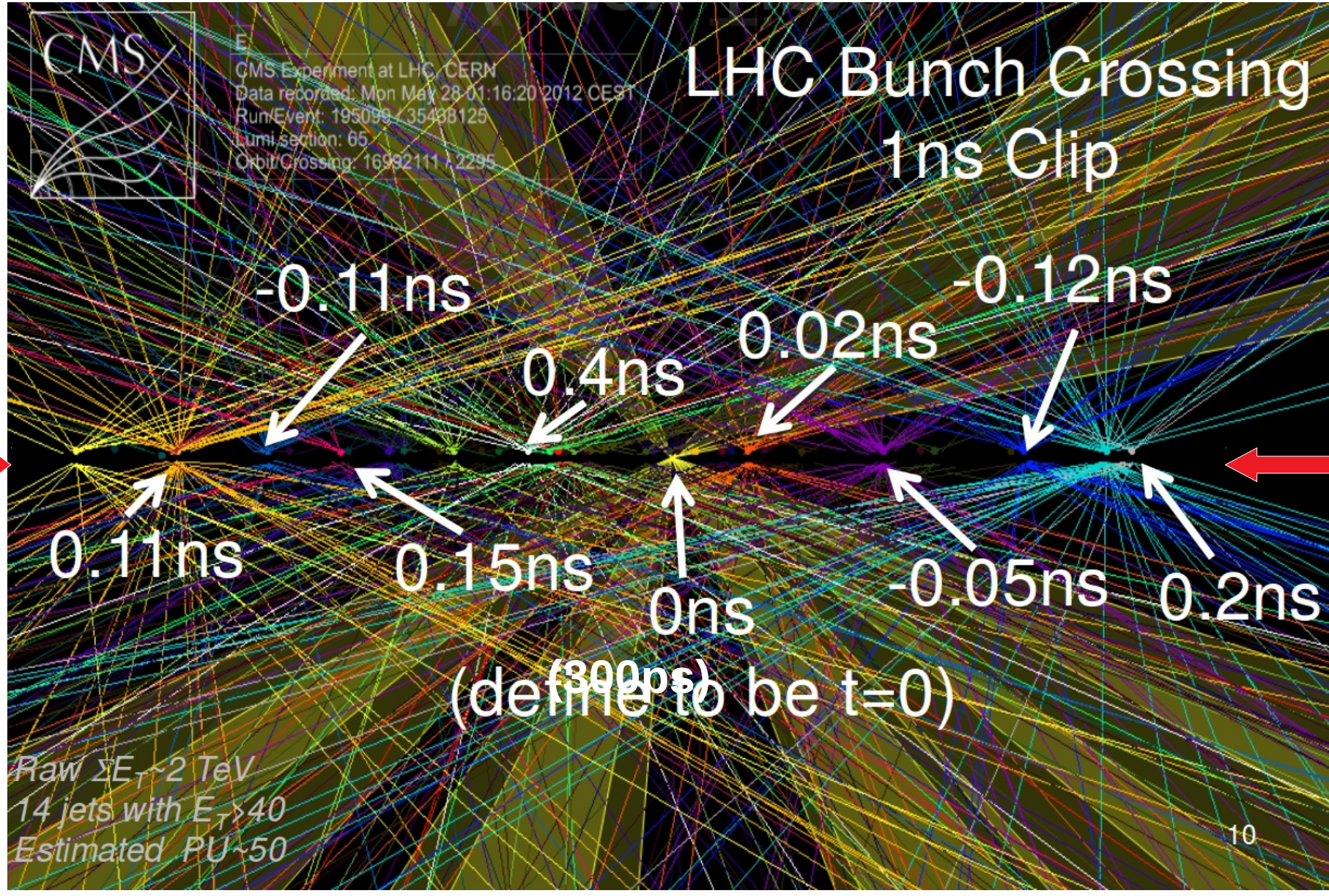


SOC trends will continue

- The more functionality the FE chip can take over the better
- Electrical communication, power distribution, environmental monitoring...
- Optical communication could be integrated in FE chip as CMOS foundries offer photonic options.
  - But many system/assembly challenges and advantage not obvious
- Wireless functionality could be included on chip
  - Significant R&D on wireless readout
  - Not s much on wireless command and control, which has a very clear use case (have to see interplay with fast timing)
- FPGA and/or AI/ML functions now straightforward to include, but use cases must be developed.
- SEU tolerance is a big challenge for on-chip functionality

What's the next scaling problem?

Future direction #2 is timing



That's a lot more data to store!

>100

40

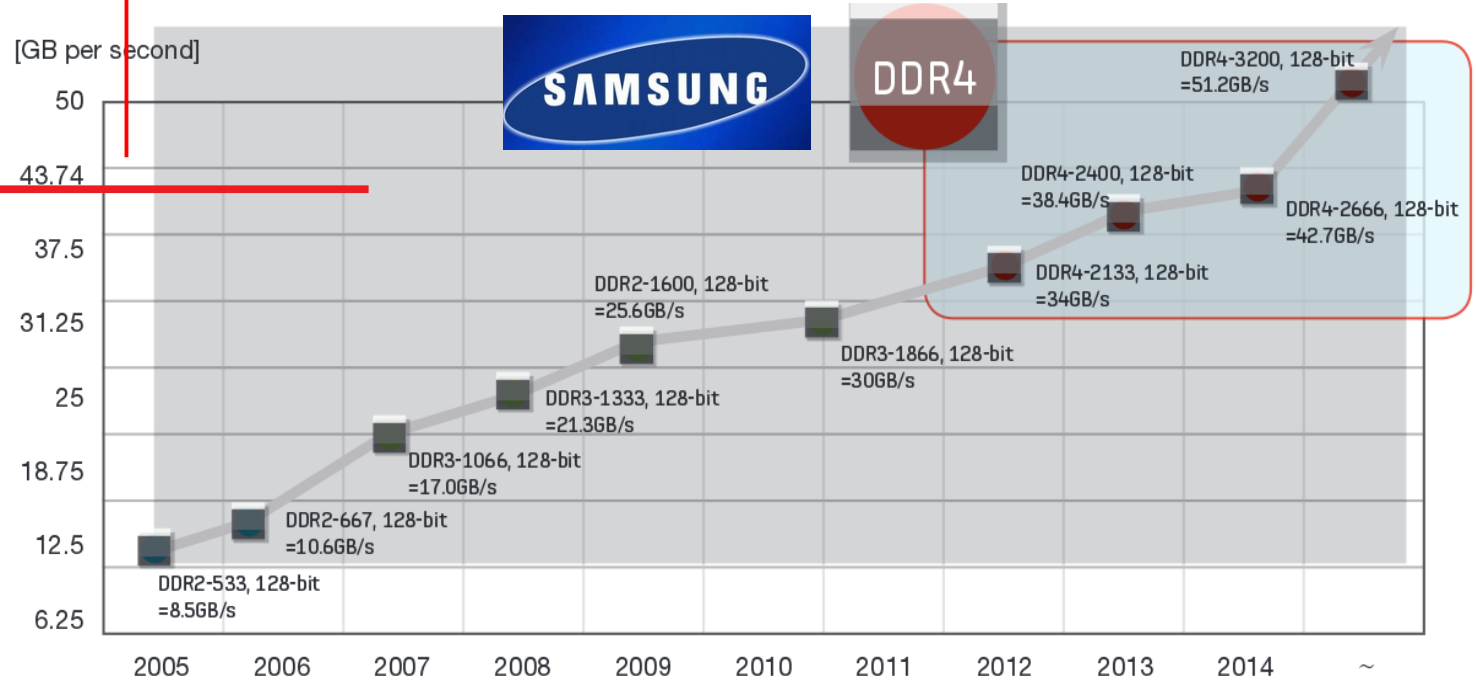
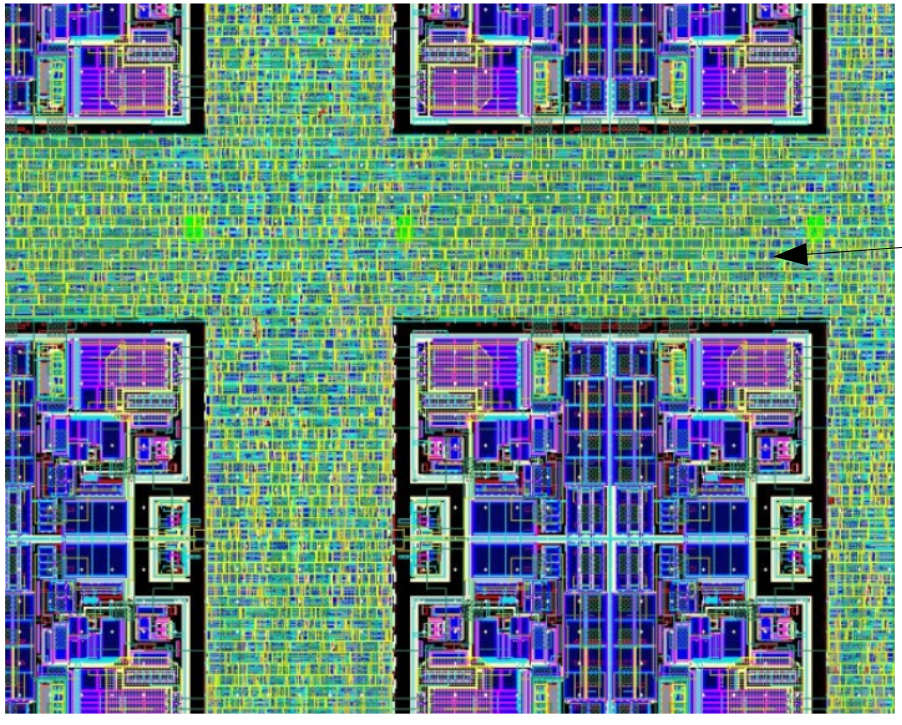


Figure 2. DDR4 higher performance compared with DDR3L and DDR2

That's a lot more data to store!

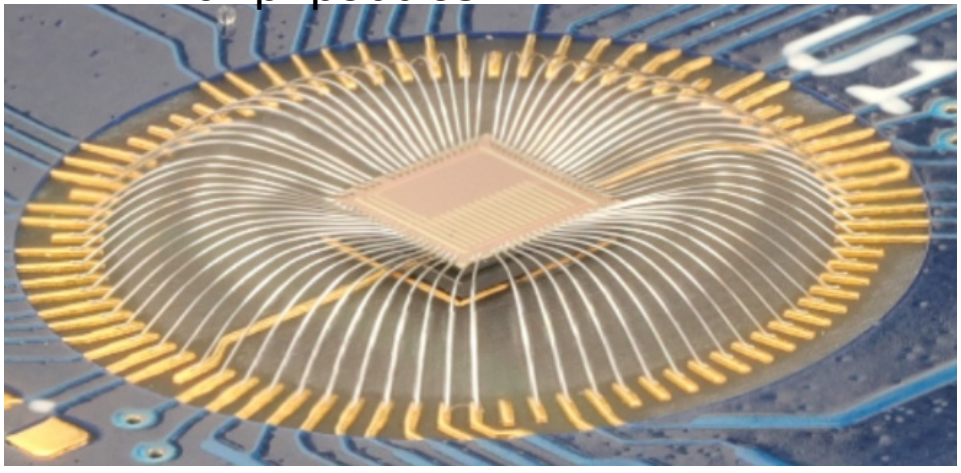


This is already full in 65nm CMOS.
But we still have 20 years of Moore's Law,
So 28nm.

Turns out that 28nm not a bad choice also for this part either
Needs to be fast with <50ps jitter
And needs a TDS with <50ps resolution

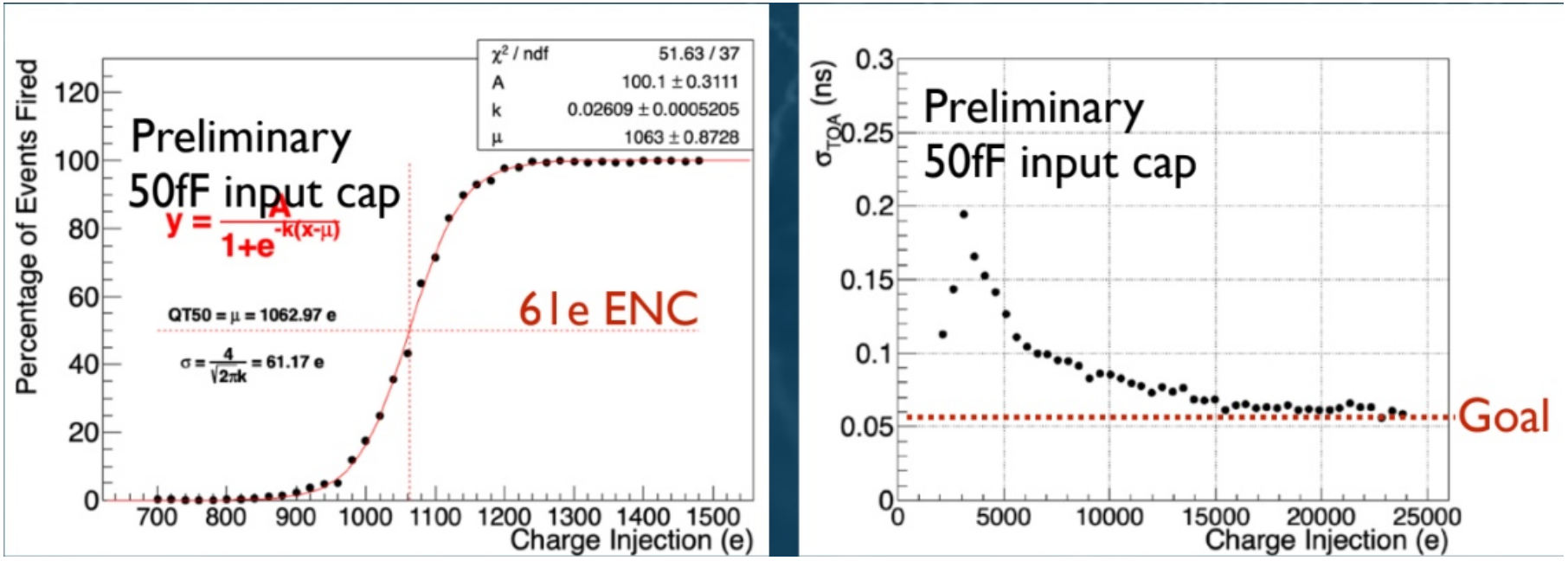
Multiple efforts to design pixels with fast timing in 28nm

LBNL chip "pebbles"



10u x30u FE, 4uW, <100e noise,
~50ps timing @ 50fF detector Cap

Next prototype already in fabrication adds:
Pixel TDC with 15u x15u , 1-2uW average power, using only 40MHz clock



Data compression and C,D transmission

- Much larger data volume due to fast timing will require significant development
- How early can data be compressed?
- ML within the pixel matrix?
  - Learned compression depending on chip location in detector?
- Advanced data transmission for x10 higher bandwidth with same power
- What about clock distribution and synchronization for fast timing?

28nm Forum

Very different situation than 10 years ago when there was competition between: 130nm possibly with 3D stacking, 90nm and 65nm for the next generation of chips.

Today everyone is immediately on board with 28nm.

Forum on 28nm CMOS

Thursday 30 Nov 2023, 14:00 → 18:30 Europe/Zurich

Kostas Kloukinas (CERN)

Videoconference — Forum on 28nm CMOS — Join

14:00 → 14:10	Welcome and Introduction	Speaker: Kostas Kloukinas (CERN)	10m
14:10 → 14:30	28nm CMOS Technology & IP blocks for HEP experiments	Speaker: Marco Andorno (CERN)	20m
14:30 → 14:45	IP Blocks in 28nm for HEP	Speaker: Franco Nahuel Bandi (CERN)	15m
14:45 → 15:05	Verification IP blocks	Speaker: Matteo Lupi (CERN)	20m
15:05 → 15:25	DART28 - The technology-related challenges of radiation-hardened transmitter	Speaker: Adam Klekotko	20m
15:25 → 15:45	DART28 - High Speed IP Design & Verification Perspective" by Stefan Biereigel	Speaker: Stefan Biereigel (CERN)	20m
16:00 → 16:20	Berkeley Lab: Fast timing analog front-end for 4D pixel detectors and other small IP blocks	Speaker: Timon Heim (Lawrence Berkeley National Lab. (US))	20m
16:20 → 16:40	Rutherford Appleton Laboratory: 28nm IP block developments	Speaker: Mark Lyndon Prydderch (Science and Technology Facilities Council STFC (GB))	20m
16:40 → 17:00	University of Bergamo: Updates on the 28nm activities	Speaker: Gianluca Traversi (Bergamo University and INFN Pavia (IT))	20m
17:00 → 17:15	AGH University: Development of fast ultra-low power 10-bit ADC Marek Idzik	Speaker: Marek Idzik (AGH University of Krakow (PL))	15m
17:15 → 17:35	NIKHEF: 28nm All Digital PLL	Speaker: Vladimir Gromov (Nikhef National institute for subatomic physics (NL))	20m
17:45 → 18:00	Open Discussion and Wrap-Up		15m

What about Strips?

- Silicon strips are still 5-10X lower power and cost than hybrid pixels
- Good solution for very large area (not covering trade-offs with MAPS)
- So what about fast timing in strips?
- HL-LHC new LGAD-based timing detectors have channel capacitance comparable to strips
- => could make LGAD strips and fast timing strips readout chips
- And maybe that opens up new possibilities...

2-sided?

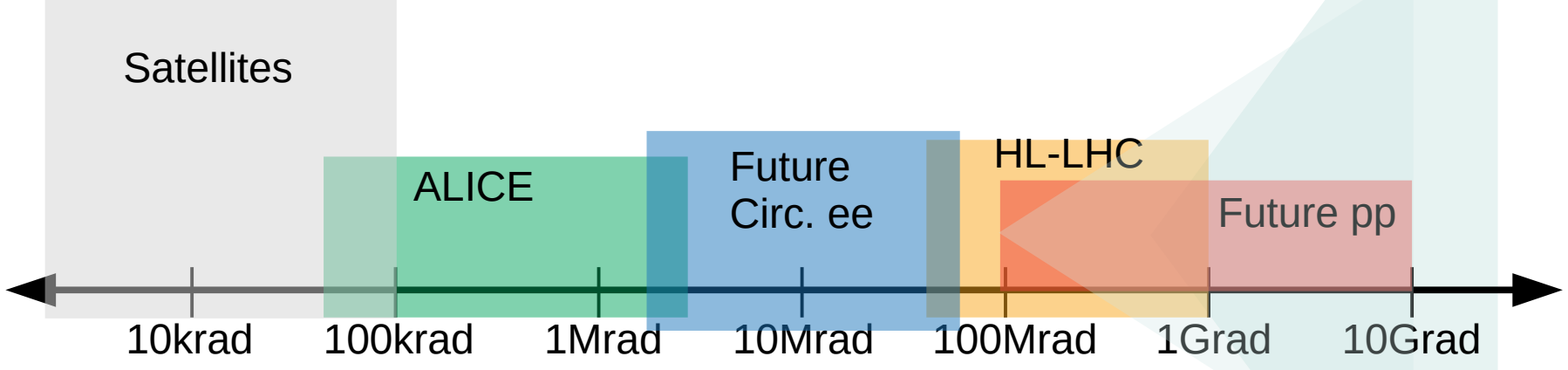
Strip as a delay line

Both z-coordinate and separation of pileup hits from timing = higher rate space-point strips

Challenge:
Modern chip design needs large effort

Typical INTEL design team

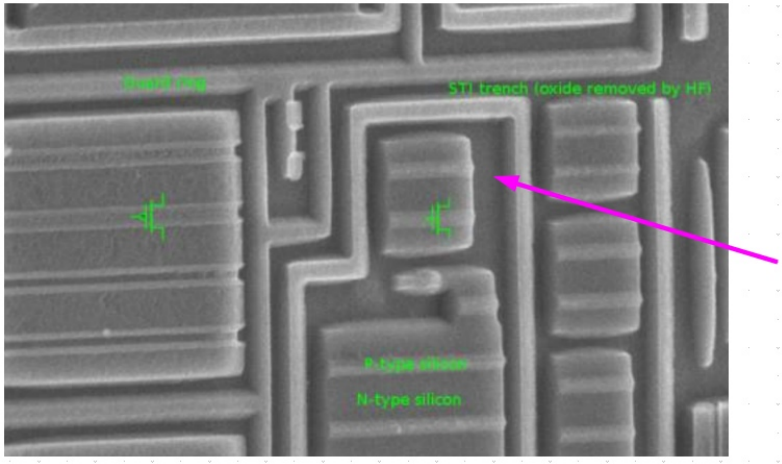
Tracker IC Radiation Challenges

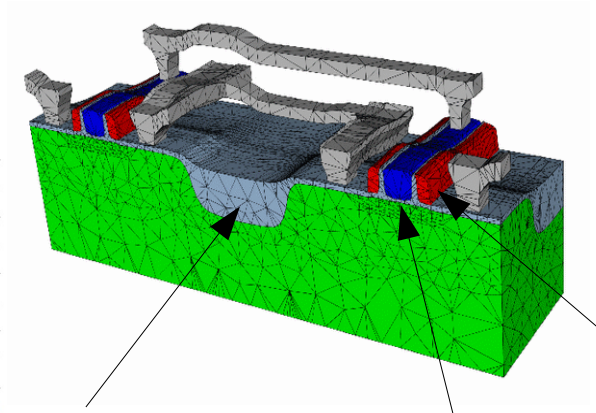


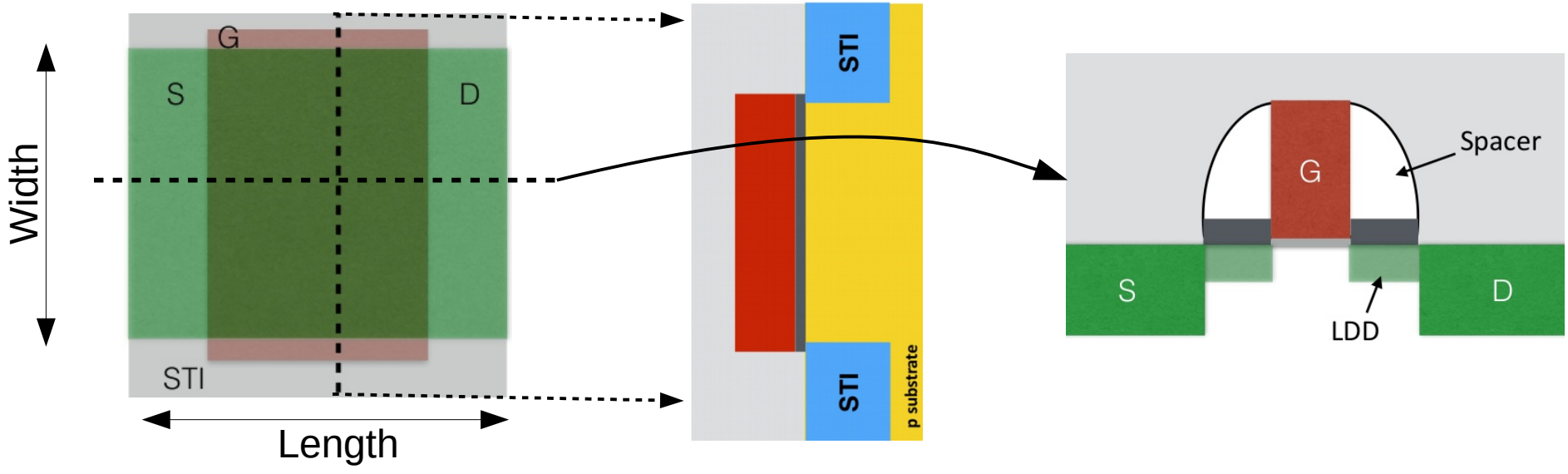
Inner Layer Dose

Temperature history
Process details
Dose rate
Dose history
Annealing
…

STI, Gate, Spacer

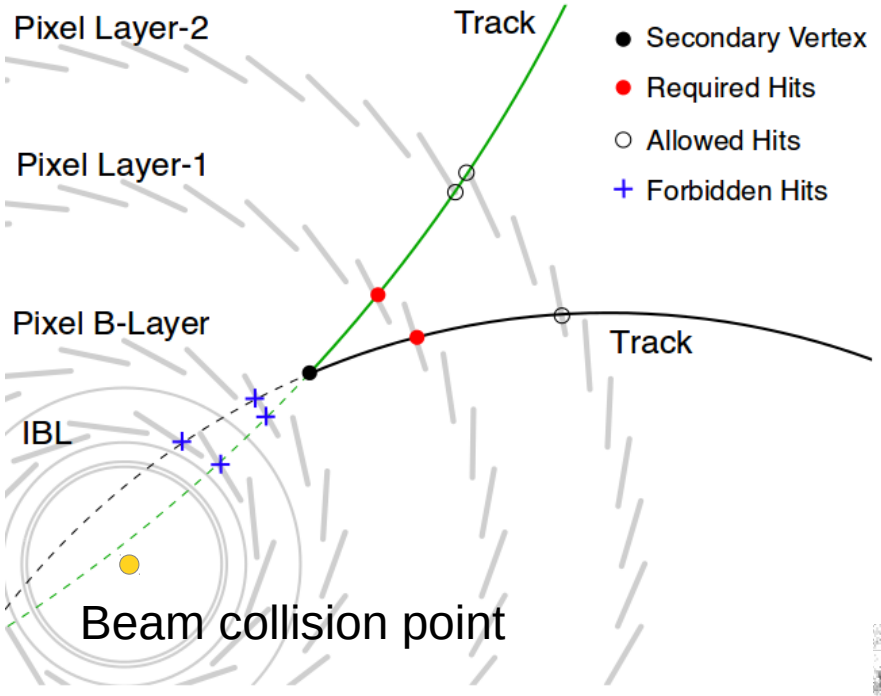


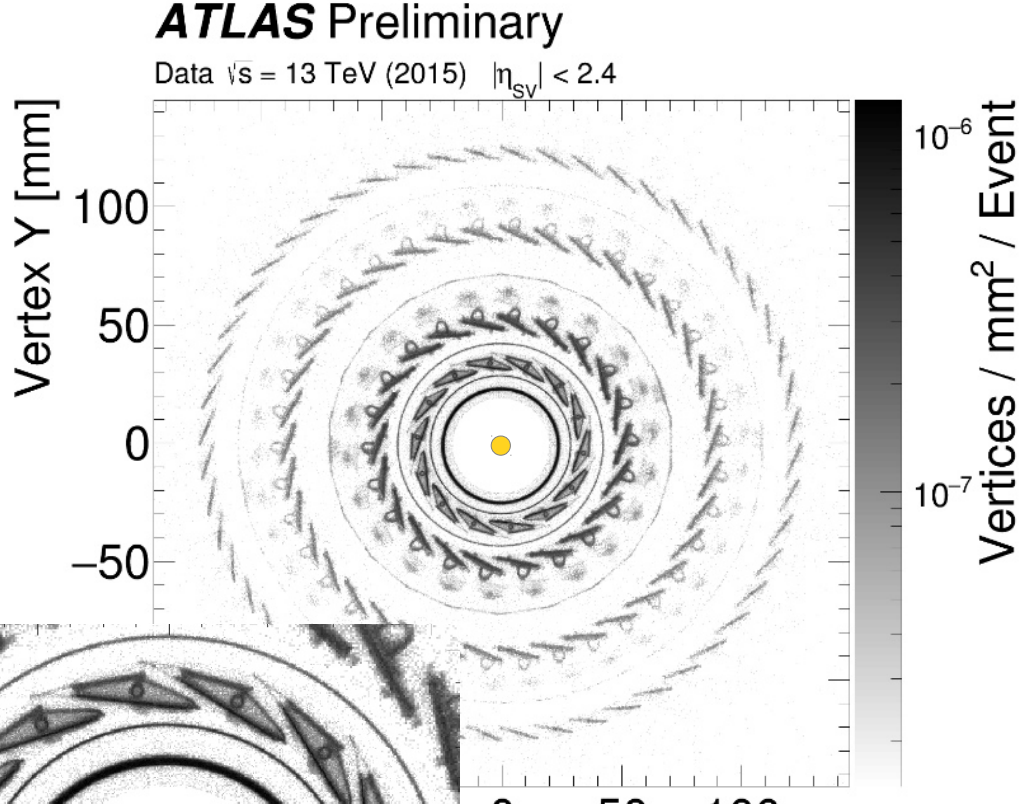


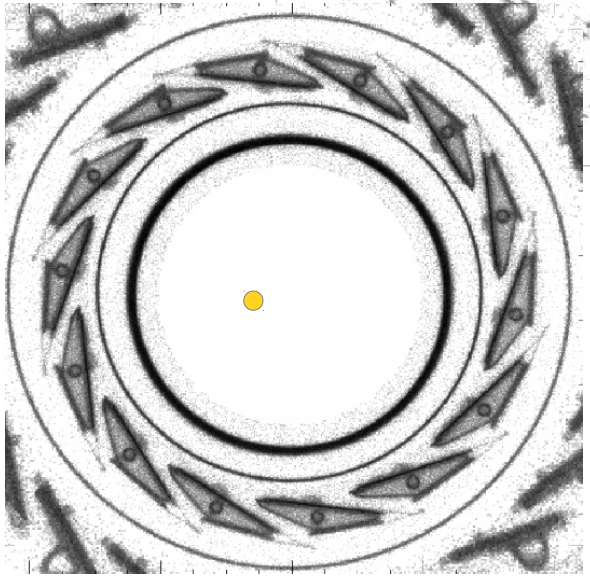


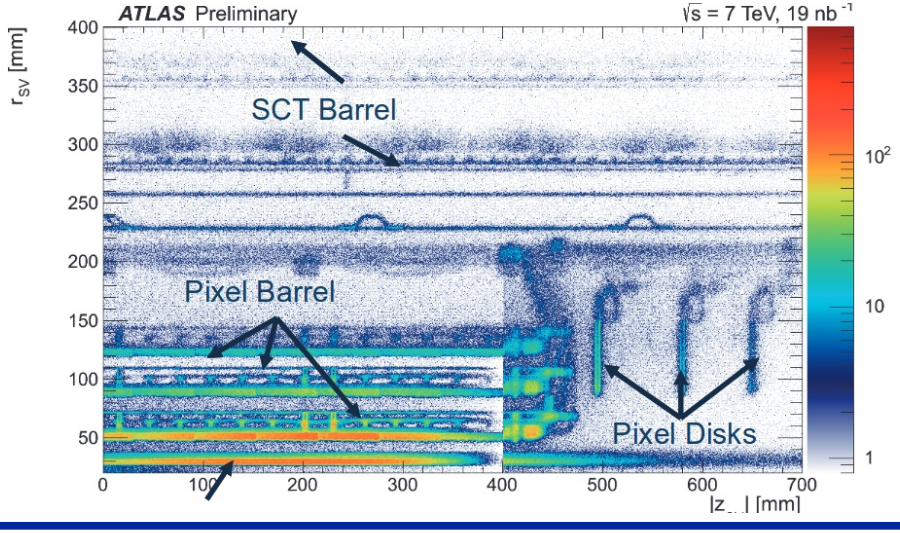
B A C K U P

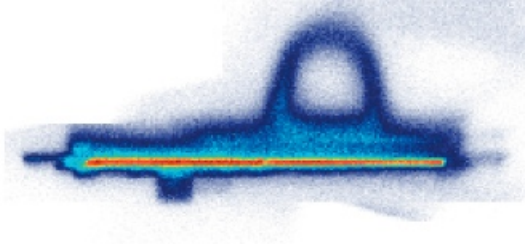
Detector can image itself in 3D



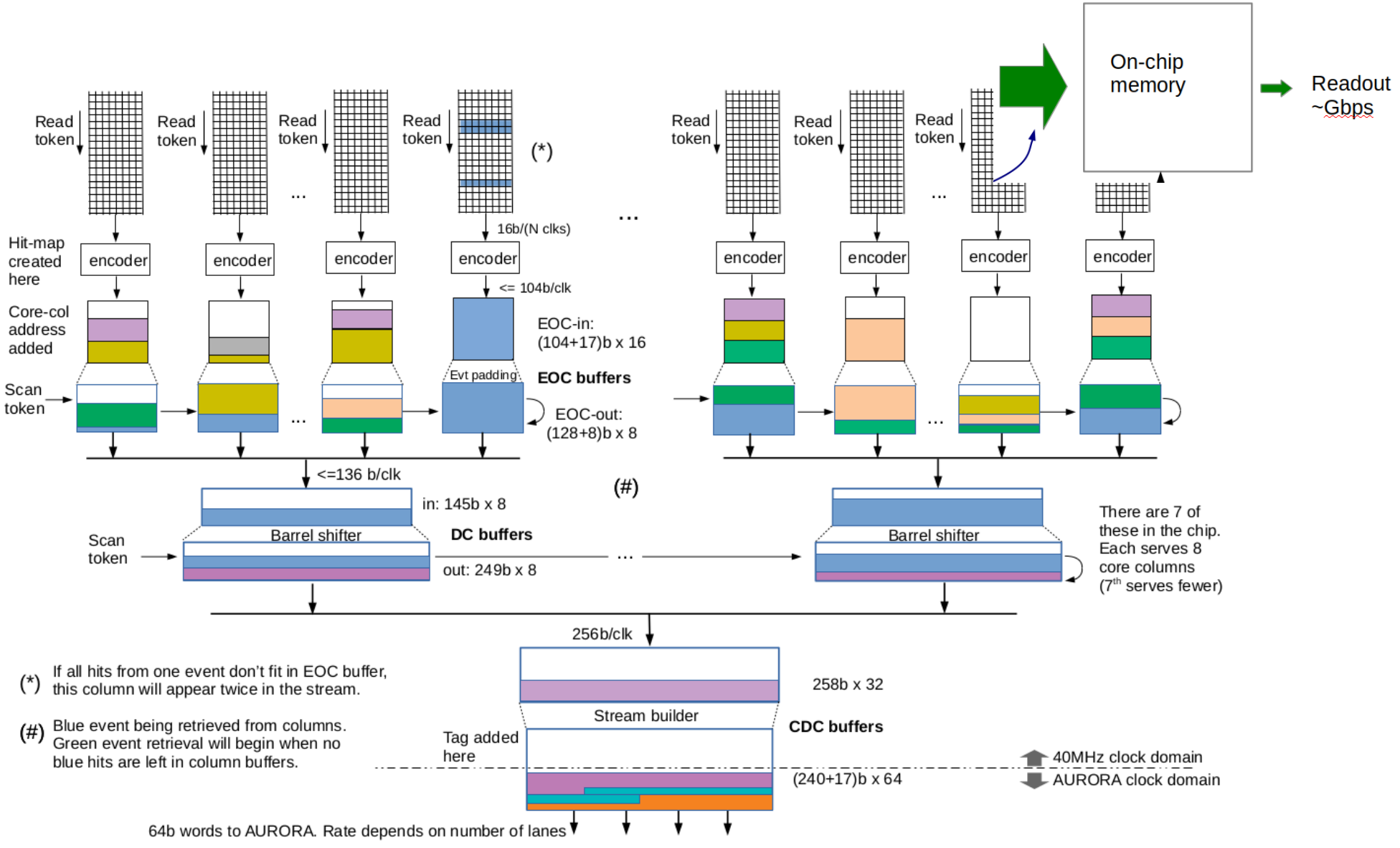




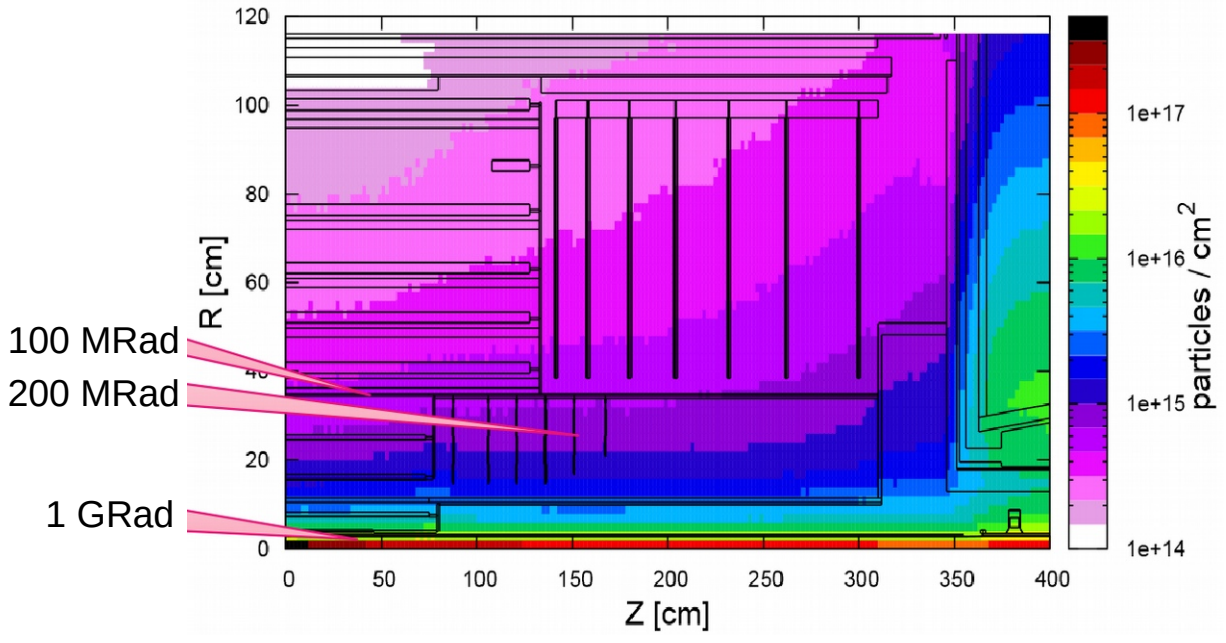




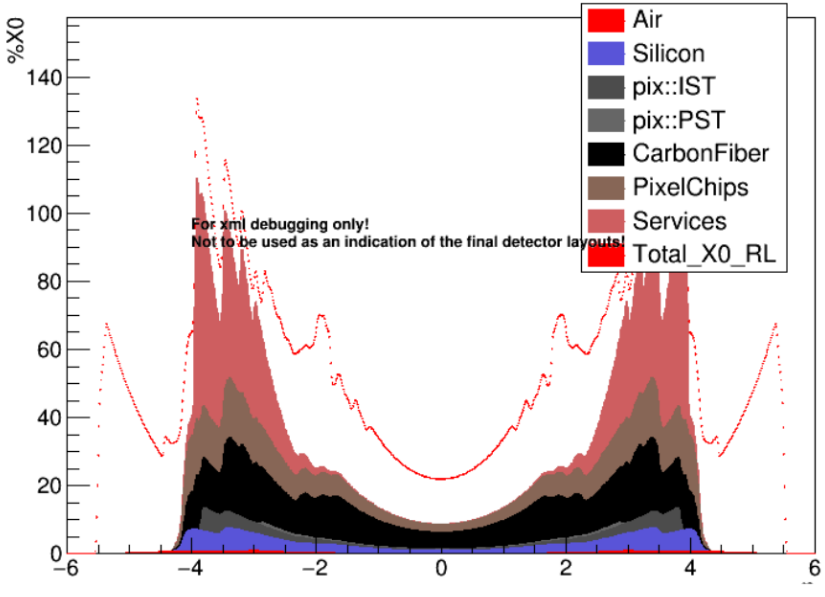
Example of non-trivial processing



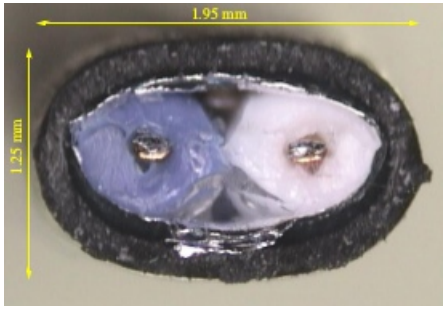
Limited Readout Bandwidth

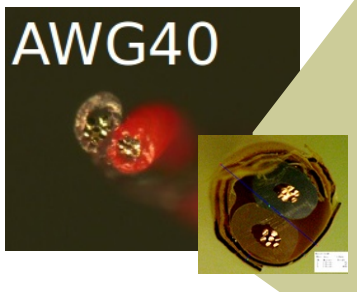


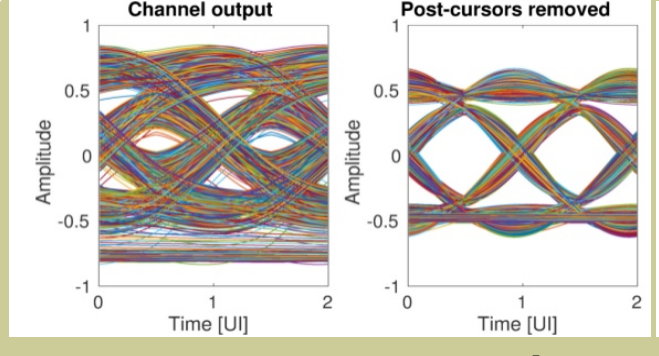
Can't use optical transmitters

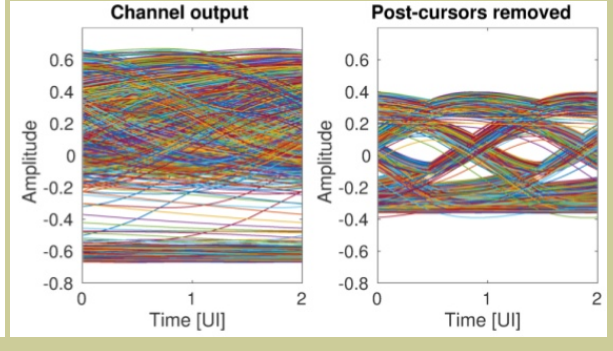


Can't use heavy shielded cables



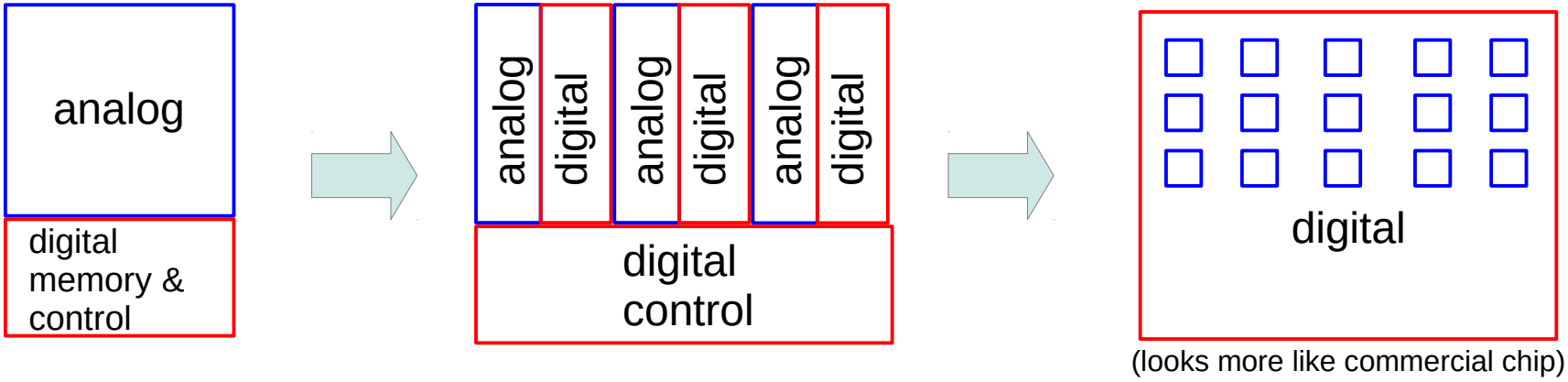






3m **5Gbps Simulation** **5m**

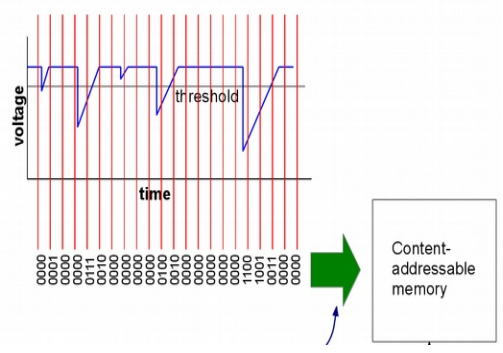
Readout Chip Evolution

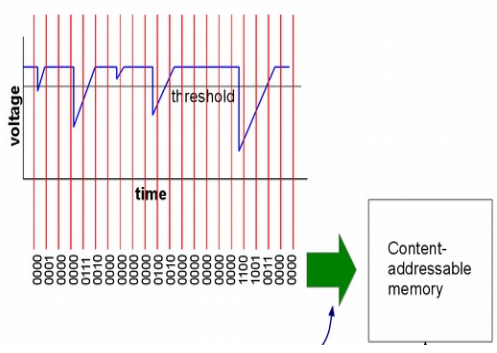


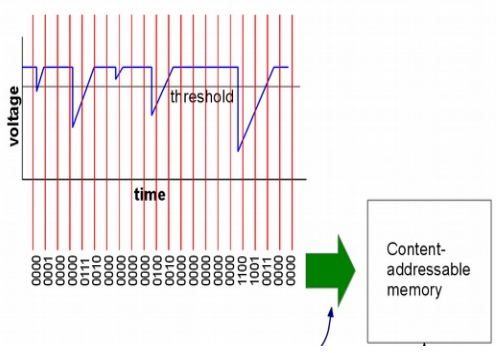
10 yrs ago

today

Future







<1Gb/s /cm^2

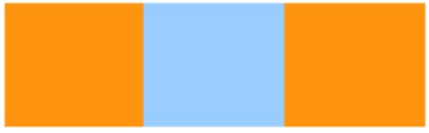
5Gb/s /cm^2

40Gb/s /cm^2

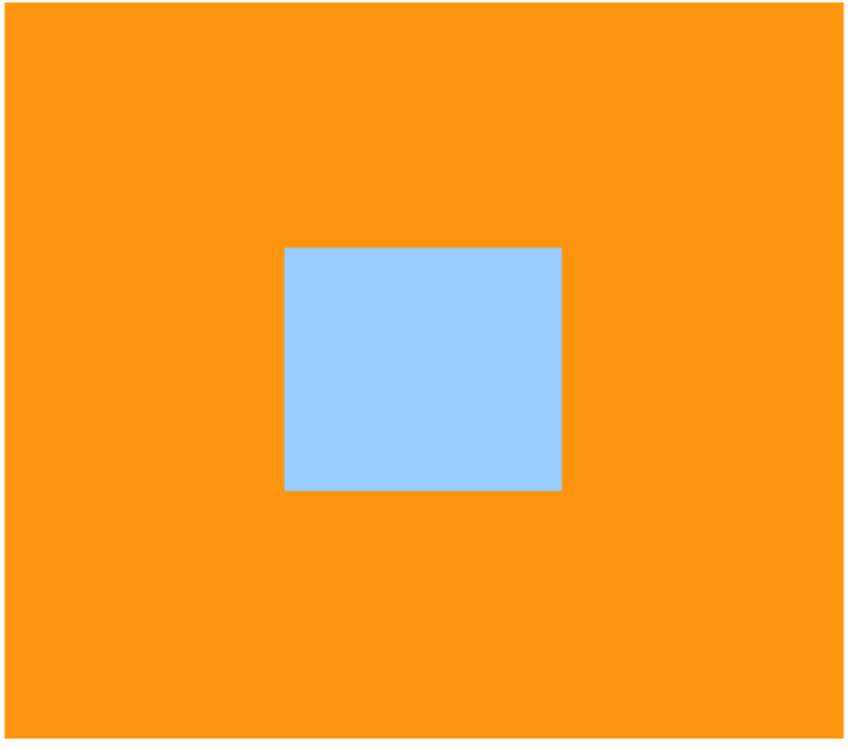
Rad Hard Logic Density Scaling

65nm

130nm

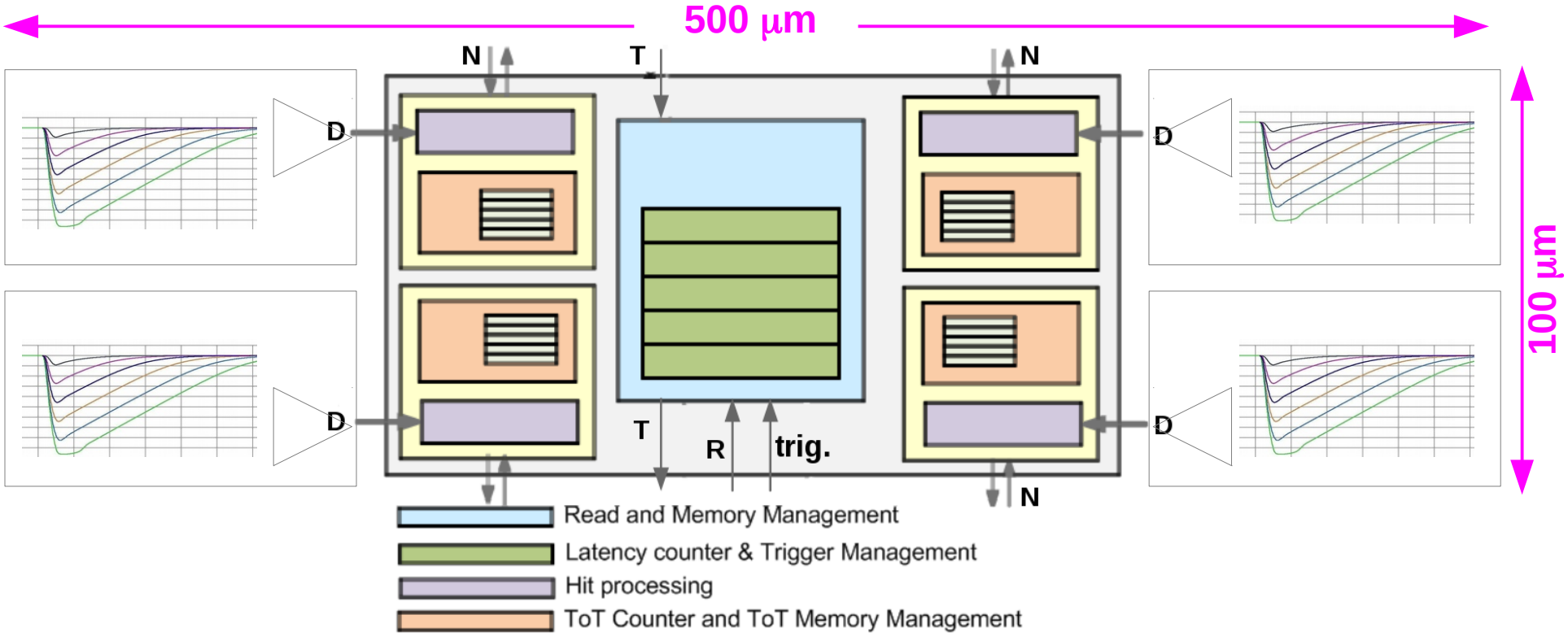


0.25um
ELT



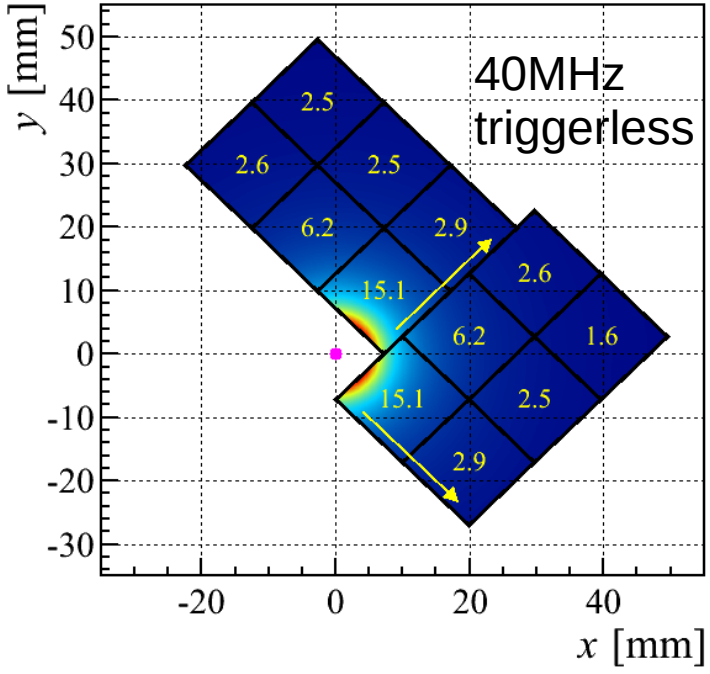
FE-I4 Digital Region

- **Digital block is shared with 4 inputs- each form an identical analog pixel.**

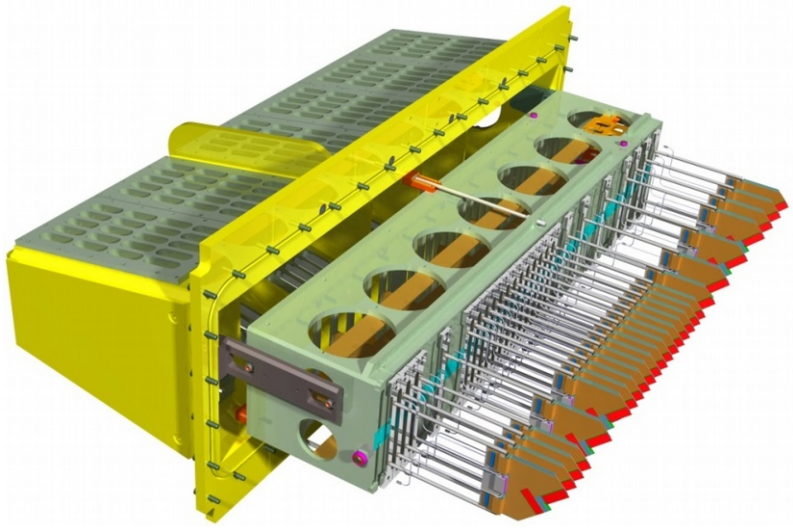


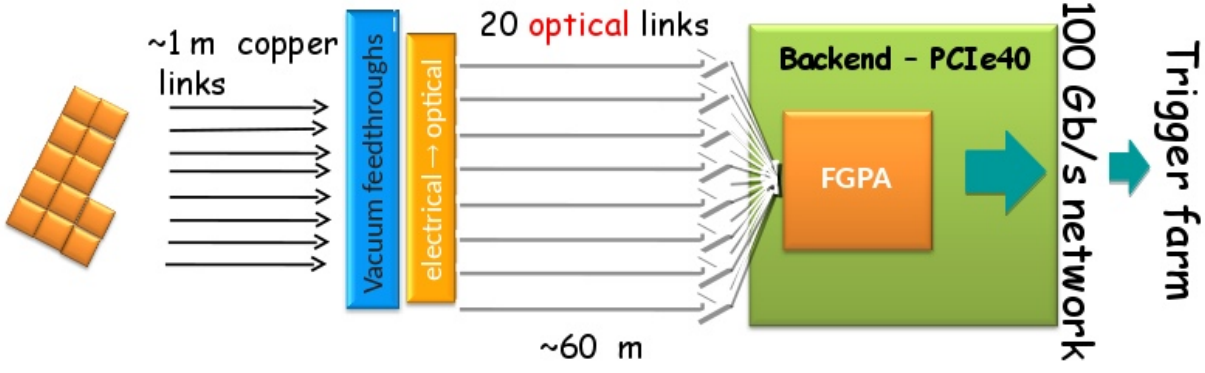
Velopix triggerless readout

Readout chips in LHCb Velopix plane
Output data rate per chip in Gbps



Velopix half with 26 planes





- Geometry looks like data flow diagram
- Lots of room outside physics acceptance
- Can have many cables out of each chip