MAPS

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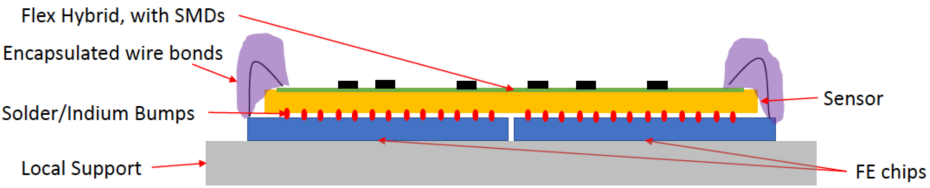
Weekly Instrumentation Meeting LBNL
03 November 2023

- Tradiational pixel detectors are **hybrid** pixel detectors, e.g. the current ATLAS Inner Detector or Inner Tracker upgrade
- Sensor: high resistivity silicon wafer, single-sided (ITk) or double-sided (IBL) process
- Frontend: low resistivity CMOS readout chip using commercial process, e.g. RD53 chips with TSMC 65 nm
- Hybridisation process: flip-chip and DC-couple sensor pixels to FE pixels
- Need 3 – 4 vendors incl. subcontractors: sensor, FE chip, hybridisation (dicing, bump deposition, flip-chipping)



Hybrid Pixel Detector - Pros and Cons

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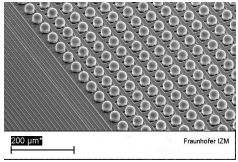
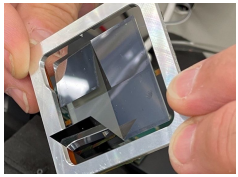
Pros

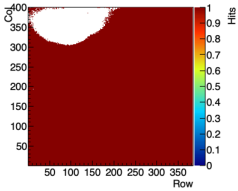
- High resistive sensors are radiation hard, at least up to 5e15 and 2e16 1 MeV n_{eq}/cm^2 for planar and 3D
- Independent vendor choices for each component, e.g. 3 different planar sensor vendors for ITk, several hybridisation vendors - eggs in baskets

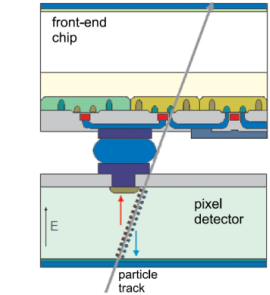


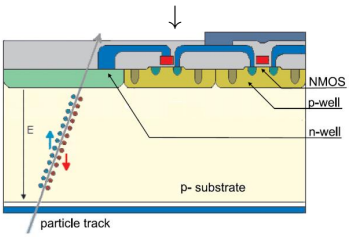


Cons

- Generally expensive due to a high number of components and vendors, high resistivity wafers manufacturered with the float-zone method
- Hybridisation is a big limitation and risk for failure
  - Physical limitations on the pixel size due to physical dimensions of the bump bonds
  - Places extra requirements on sensor and FE chip planarity
  - Flip-chip process: alignment, compression, oxidation, surface condition, solder condition
  - Thermal stress acting on bump bonds during handling and operation
  - → Novel bonding techniques being explored, e.g. Anisotropic Conductive Films (ACF), nano-wires



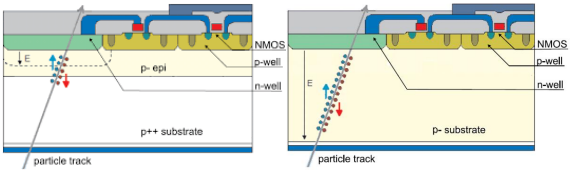




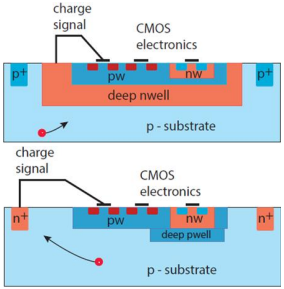
- Combine charge collection and FE electronics onto the same piece of silicon $\rightarrow$ Monolithic Active Pixel Sensor (MAPS)
- Using commercial HV-CMOS process on low-resistivity ($\sim$10–100 Ωcm) Czochralski wafers - inexpensive "as cheap as chips", ideal to cover large areas with high resolution tracking detectors
- CMOS process is one of the most popular processes to manufacture analog and digital integrated circuits in silicon devices
- HV-CMOS allows the application of a relatively high voltage of $\sim$100 V, used in power devices
- Electronics are shielded by (nested) deep wells, can also act as collection electrode

Types of (HV)-CMOS Sensors

- Terms like MAPS, HV-/CMOS sensors often used interchangeably
- MAPS: a general term, but sometimes indicates the standard process: usually on low resistivity wafers using a epitaxial layer for structures, slow charge collection, smaller pixels (e.g. 18 μm$\times$18 μm)
- DMAPS: (fully) Depleted MAPS, thinned so that breakdown voltage $>$ depletion voltage, high electric field throughout the bulk, fast charge collection (drift)
- HR-CMOS with high resistivity substrate behaves better but usually requires non-standard wafers

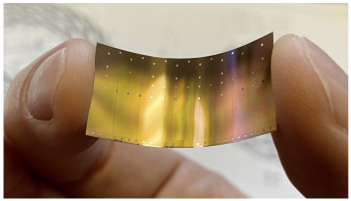


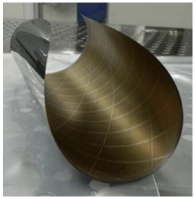
- Large fill factor
  - Usually large sensor capacitance
  - No/little low-field regions $\rightarrow$ fast
  - Radiation tolerant
- Small fill factor
  - Usually use HR substrates
  - Large low-field regions $\rightarrow$ slow
  - Less radiation tolerant



A Couple of Examples

- Mimosa-26 (2009), used in EUDET-type beam telescopes
  - CMOS sensor in ams 350 nm technology
  - 18.4 μm$\times$18.4 μm pixel pitch, rolling shutter readout
  - Slow: 115.2 μs integration time





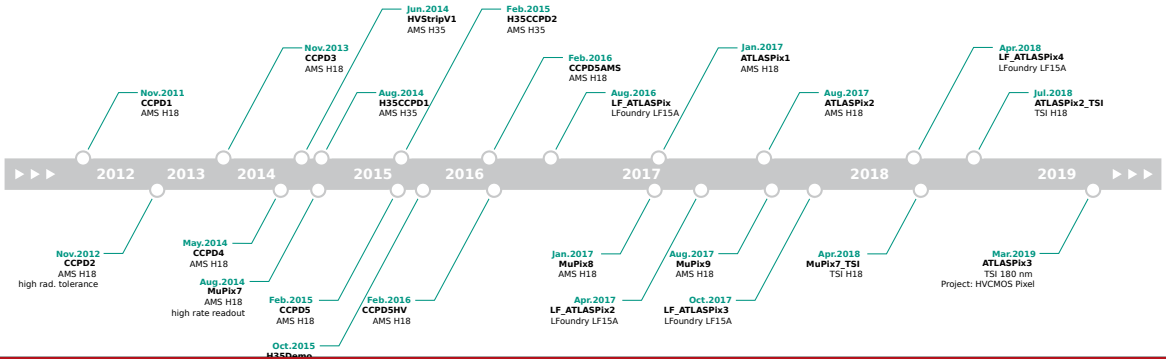
- ALPIDE, will be used in ALICE ITS3 (2029)
  - 65 nm TowerJazz technology
  - Thinned down to 20–40 μm to be bent!
  - Radiation tolerant up to 1e13 1MeV n_{eq}/cm^2

ATLASPix + Family

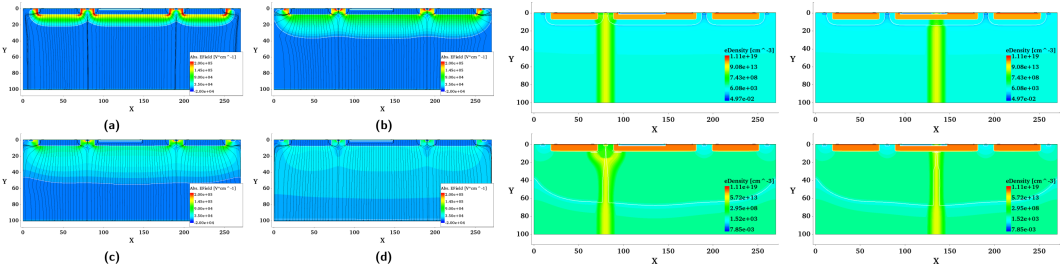
- ATLASPix3, proposed tracker for CEPC, same family as MuPix (Mu3e experiment), MightyPix (LHCb MightyTracker Upgrade)
- Name bears historical reasons: once a candidate for ATLAS ITk outer pixel layers!

→ Output protocol Aurora 64b66b or 8b10b

- Mature DMAPS with large fill factor in ams/TSI 180 nm technology on $\sim 200\,\Omega$cm wafers
- Radiation hardness ~2e15 1 MeV n_{eq}/cm^2

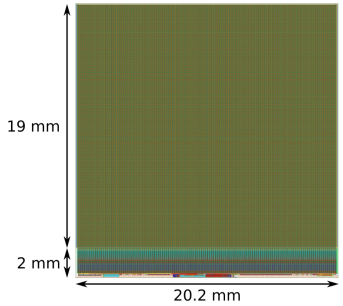


TCAD Simulations



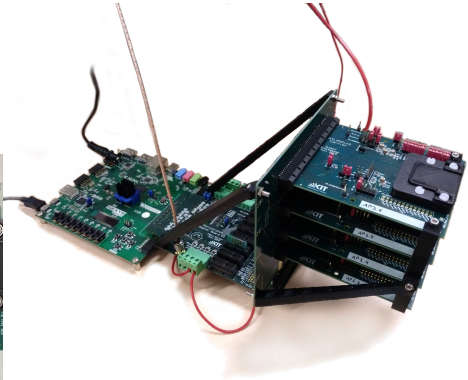
- Design process with help of TCAD (finite element) simulations
- Simulations of the fabrication process: details can be provided directly from the foundry, or using educated guess
- Faster simulations of the device structure only - more suited for HEP uses due to rather large structures (pixel vs transistor)
- Left: simulation of the electric field with different substrate resistivities with bias applied from the back
- Right: simulation of a MIP passing through at different positions for 20 Ωcm and 1000 Ωcm substrates

- Version 3 is the first full reticle-sized sensor for construction of multi-chip modules
- $20.2 \times 21\,\text{mm}^2$ reticle size, 132 columns $\times$ 372 rows, $150 \times 50\,\mu\text{m}^2$
- 3-bit threshold TDAC, 8-bit ToT, 10-bit time stamp
- Voltage regulators for shunt-LDO operation in serial power chains
- Column-drain readout with and without trigger (triggered and hit-driven)
- Configurable through serial, SPI bus or command line like RD53
- Data link 1.28 Gbit/s (64b66b) or up to 1.6 Gbit/s (8b10b)
- Low power $\rightarrow$ less requirement on cooling: $160\,\text{mW/cm}^2$ (of which $120\,\text{mW/cm}^2$ is analog) - compared to $500\,\text{mW/cm}^2$ for ITk Pixel
- Low threshold: down to 400 e
- Low material budget: thinned to 150 μm
- v3.1 with improvements (bias structure, time-walk) and trade-offs (shielding in signal injection) with minimal changes in the metal layers



Single and Multi-Chip Lab Setups

- Readout using GECCO (GEneric Configuration and COntrol) system (developed by KIT, Germany) for single chip, quad and telescope
- Diligent Nexys Video FPGA board + firmware
- Custom GECCO board (FMC–PCIe) with function card slots and power connection
- Single chip cards are PCIe cards
- Telescope-adapter card for up to 4 SCCs, all planes share the same HV and LV
- Qt-based software GUI



Single Chip Measurements

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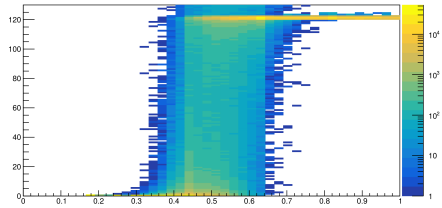
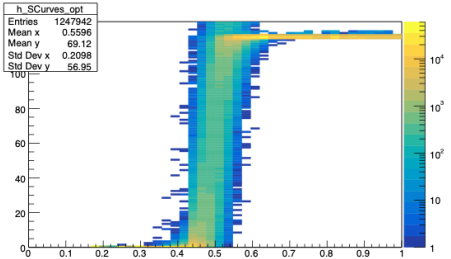
Threshold tuning

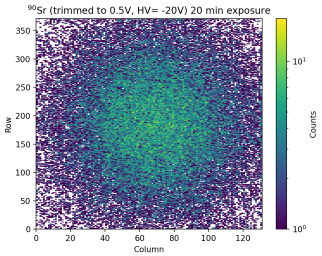


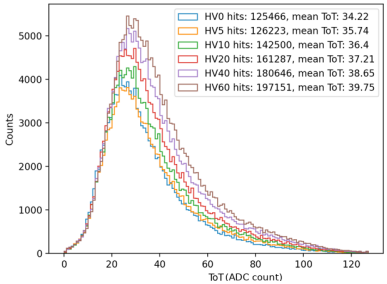
Untuned S-curves at TDAC=5 for row 40, $\sigma = 47$ mV



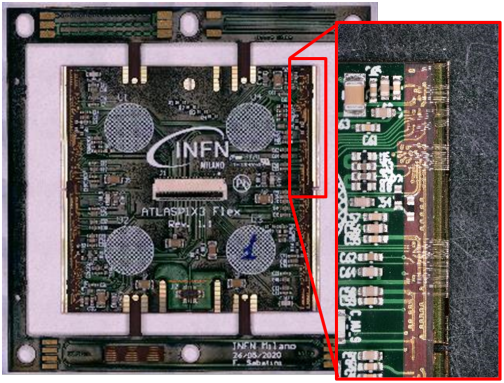
Tuned S-curves for row 40, $\sigma = 18$ mV

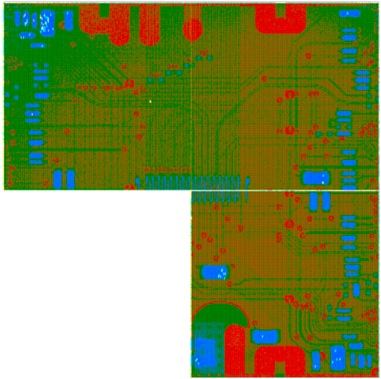
Source scan with Sr90





Quad Module





- Quad flex design inspired by ATLAS ITk Pixel
- Quad module assembly by hand and being tested in Milan
- Source measurement with x-ray (5 min with 15k–34k hits/s, untuned threshold)
- First quad in testbeam (display shows one chip in a quad)

Testbeam at DESY

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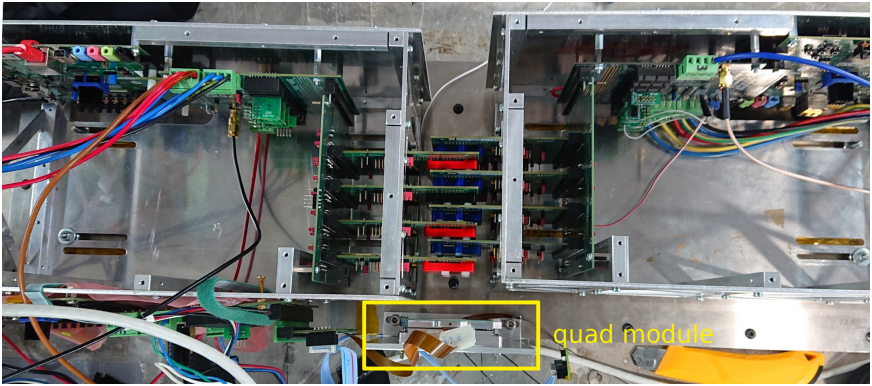
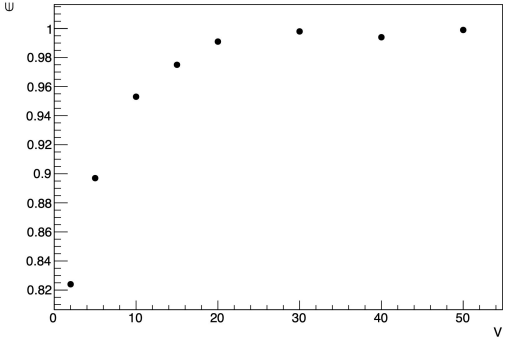
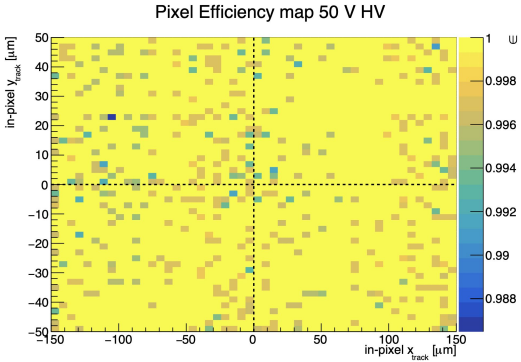
- Testbeam at DESY in 2022 using 6 GeV electron beam
- 2 arms in 2 standalone systems, biased at $\sim$ 50 V (breakdown at $\sim$ 60 V)
- Synchronisation provided by the primary system sending sync signal to the secondary
- Using hit-driven (untriggered) readout
- Interleaved arms with 1.27 cm distance between planes
- Quad module in the beam (bottom, in the pixel module carrier)

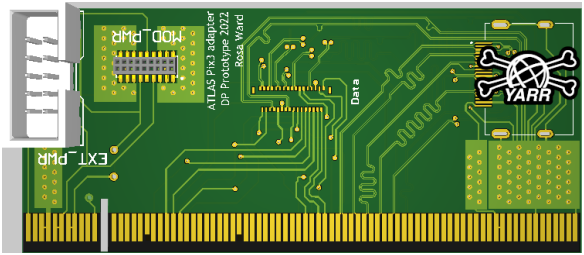


- Reconstruction and analysis with Corryvreckan (of one arm - synchronisation didn't work out)
- Not that straight-forward and required intensive debugging: crosstalk events, data corruption in hitwords (discarded)
- Total efficiency at 50 V is 99.56%





- Long journey of the ATLASPix chip family
- Mature and well-tested design for CEPC silicon tracker
- First experience with quad modules!
- Modified readout adapter card design exists with an additional DisplayPort - idea is to integrate into YARR



The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

References

- Recent update on a hybridisation vendor
- CERN first module building experience
- On novel interconnections
- Performance of the EUDET-type beam telescopes
- High-Voltage CMOS Active Pixel Sensor
- Development of CMOS Sensors for High-Luminosity ATLAS Detectors
- ATLASPix3 Testbeam Results
- ATLASPix3 TB repo
- ATLASPix3 Manual
- R. Schimassek, Test results of ATLASPIX3 — A reticle size HVCMOS pixel sensor designed for construction of multi chip modules
- Telescope public wiki: https://git.scc.kit.edu/adl_publicsoftware/atlaspix3_public/-/wikis/Telescope-Revision-2-Wiki-Main-Page
- Corryvreckan