Pebbles: paving the way towards 4D Tracking detectors

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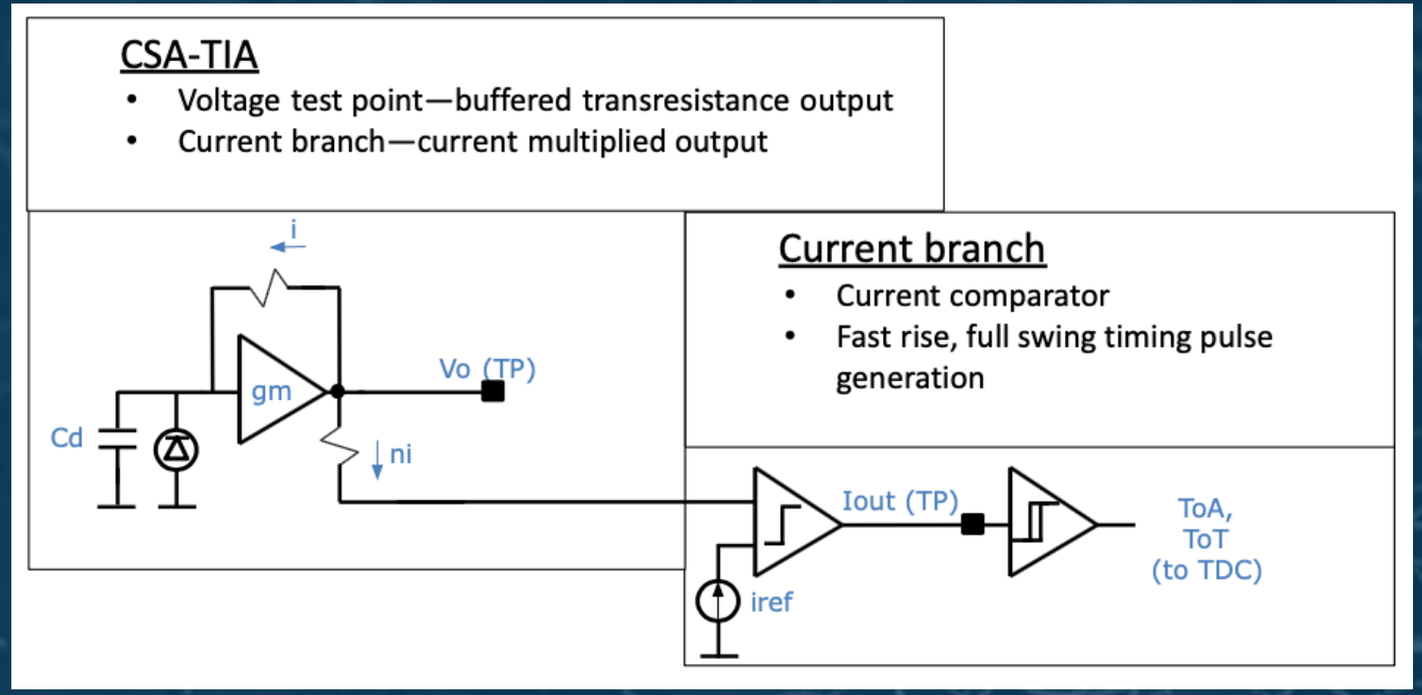
Motivation

- ATLAS ITk Pixel inner system designed for half of the original HL-LHC run time → planned to be replaced half-way through HL-LHC era
- Final opportunity for more than a decade to test and operate a real 4D tracker in the flesh, but have to set achievable specs
  - Maintain current ITk specs:
    - 50um by 50um pixel pitch
    - Analog front-end: <100e noise, <1000e threshold, <5uW, 30um x 30um
  - Add:
    - ~50ps timing resolution (AFE, TDC, readout logic) (3D sensor technology)
- 65nm technology fully exploited with current needs (>90% routing density in ITkPix pixel)
- Any additional logic requires miniaturization → 28nm CMOS
  - LBNL has started effort in 28nm CMOS chip design with focus on analog front-end and time-to-digital converter

Big Rock AFE

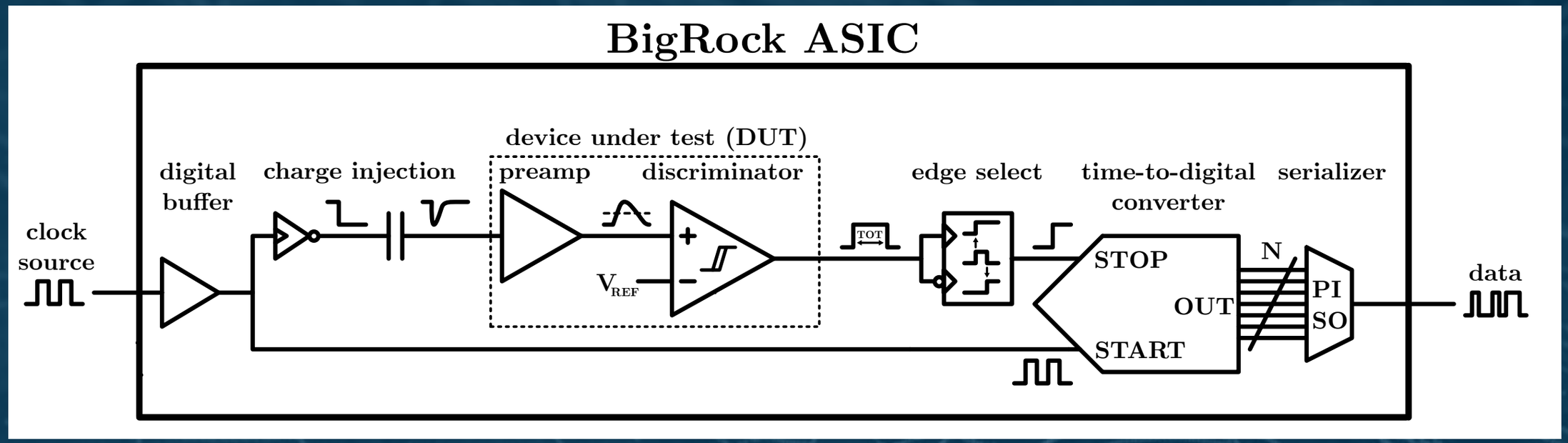


- Typical cascade CSA design
  - “Pseudo TIA” with fast peaking time (3-10ns) to optimize for low jitter
- Input current charge pulse mirrored to current comparator
- Mirror factor controllable through biases

	Specs
Idc	4uA
sigma(ToA)	~50ps
Threshold	<1000e
ENC	<100e
Area	10x30um2
Cin	50fF

Based on: Pierre Jarron, et. al, A transimpedance amplifier using a novel current mode feedback loop, 1996

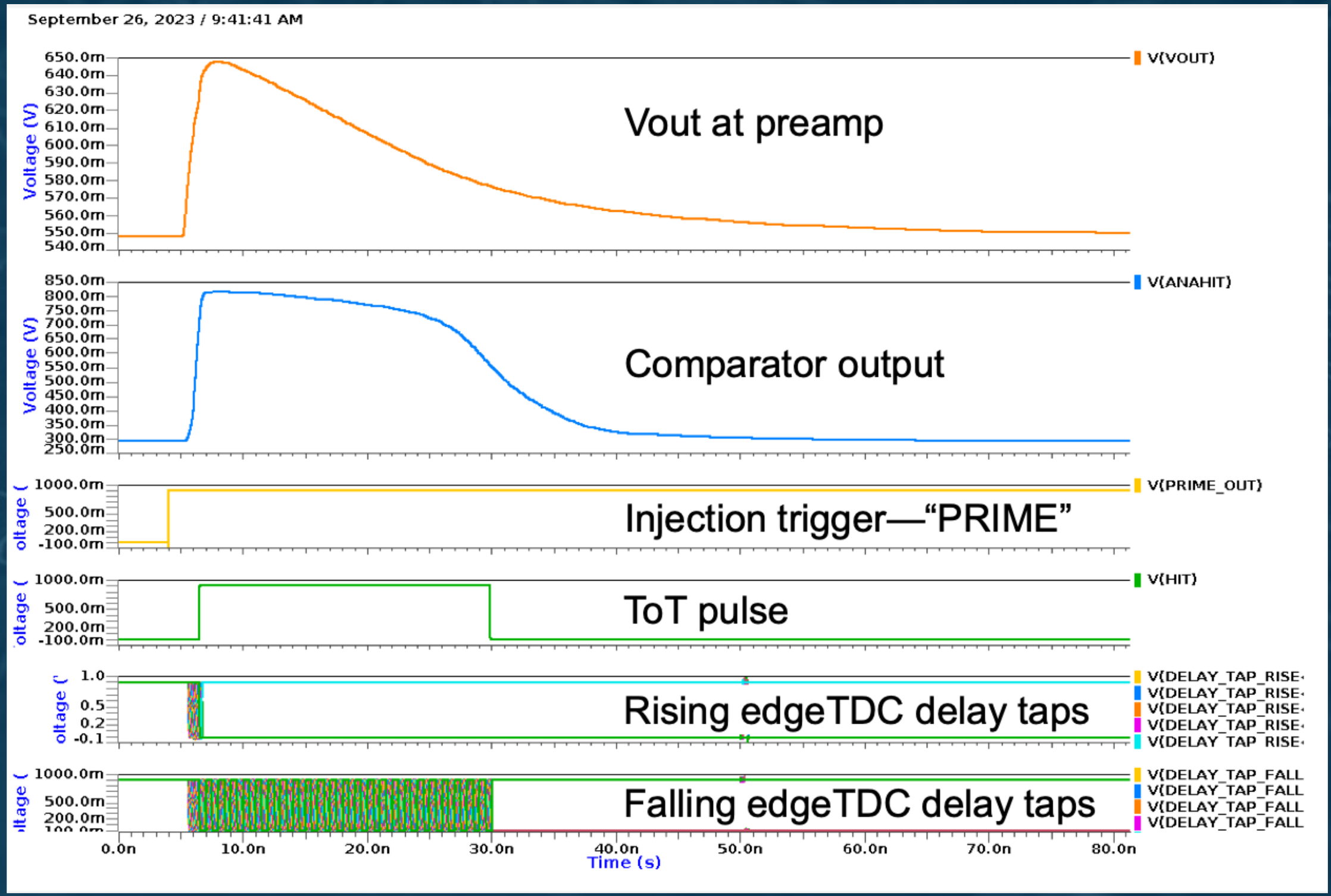
On-Chip Testbench



TDC concept:

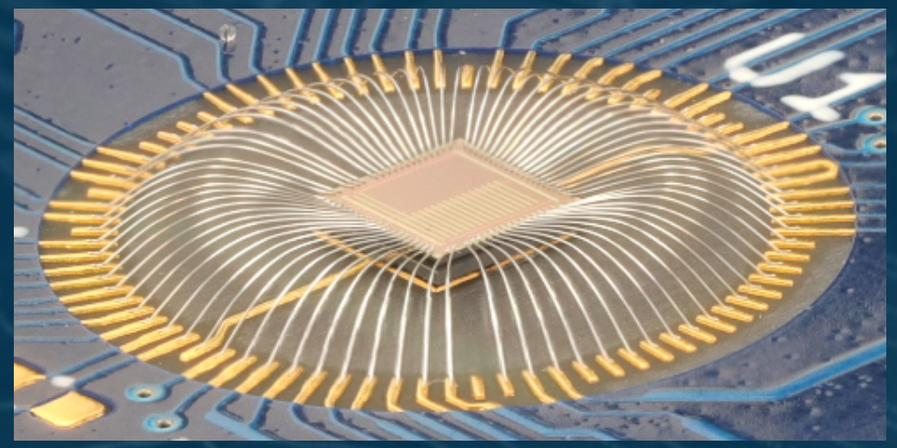
- Only meant for characterization not for usage in real pixel chip (too large, too much power)
- Differential delay-element chain
  - ~10ps resolution
- External precision 1GHz clock issues injection and simultaneously ripples through delay chain
  - Coarse counter at output of delay chain (Clock period resolution, 1ns)
- Stop signal from front-end freezes delay chain
  - Readout as fine count (~10ps resolution)
- By making delay chain slightly longer than one clock period have intrinsic calibration for each each measurement
- Two TDCs per front-end, one to measure rising edge, the other for falling edge -> very precise ToT measurement

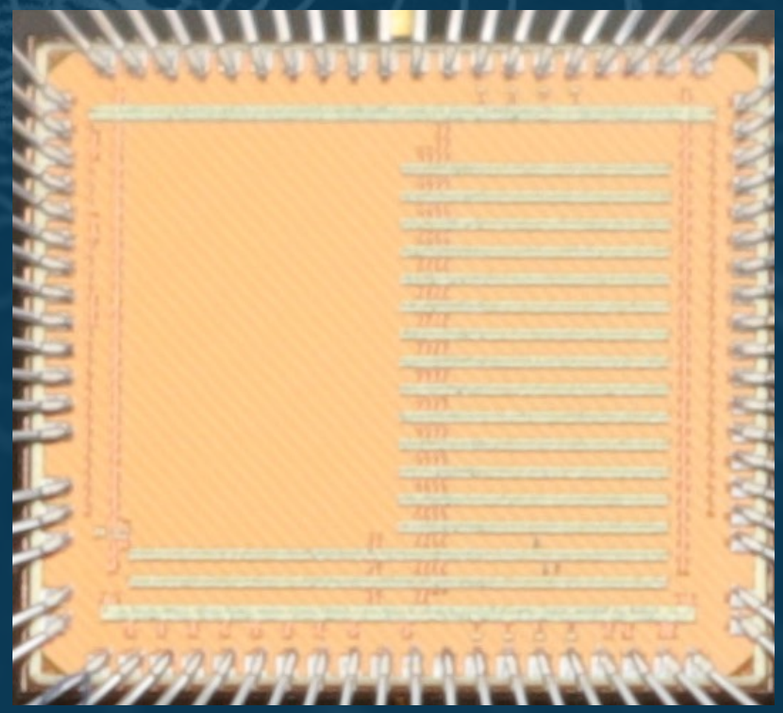
Simulation


September 26, 2023 / 9:41:41 AM
Voltage (V)
650.0m
640.0m
630.0m
620.0m
610.0m
600.0m
590.0m
580.0m
570.0m
560.0m
550.0m
540.0m
V(VOUT)
Vout at preamp
850.0m
800.0m
750.0m
700.0m
650.0m
600.0m
550.0m
500.0m
450.0m
400.0m
350.0m
300.0m
250.0m
V(ANAHIT)
Comparator output
1000.0m
500.0m
200.0m
-100.0m
V(PRIME_OUT)
Injection trigger—“PRIME”
V(HIT)
ToT pulse
1.0
0.5
0.2
-0.1
V(DELAY_TAP_RISE
Rising edgeTDC delay taps
V(DELAY_TAP_FALL
Falling edgeTDC delay taps
0.0n
10.0n
20.0n
30.0n
40.0n
50.0n
60.0n
70.0n
80.0n
Time (s)

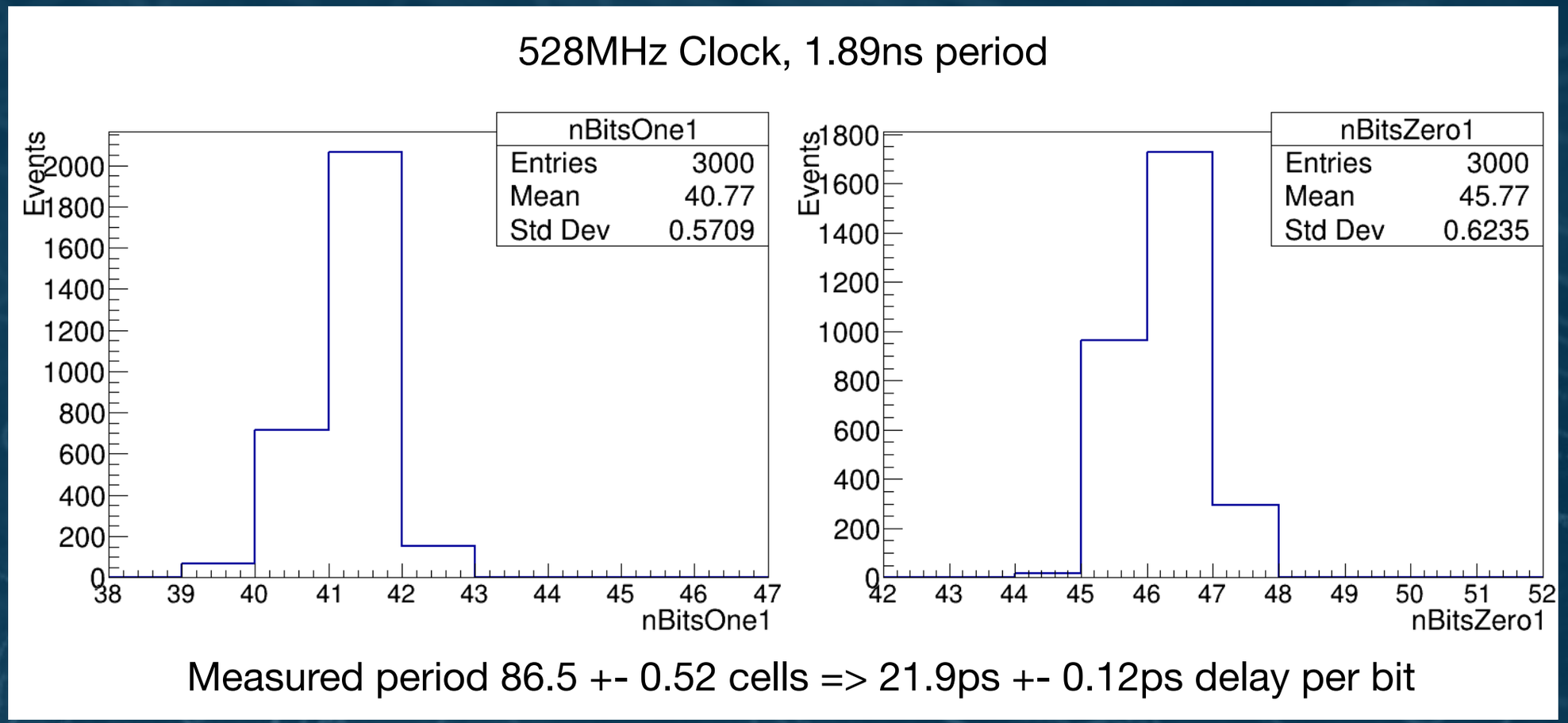
Submissions

- 2mm x 2mm mini-ASIC submissions
- Pebbles (submitted May 2022)
  - 17 Big Rock AFE channels (4 different Cin 0fF, 25fF, 50fF, 100fF)
  - High speed CML output driver (10Ghz)
  - LVDS clock receiver
- Metarock (submitted Jul 2023)
  - Improved Big Rock AFE (same channel setup)
  - Added realistic pixel TDC (small area, low power, 40MHz driven) in parallel to characterization TDC
  - PAM-4 driver





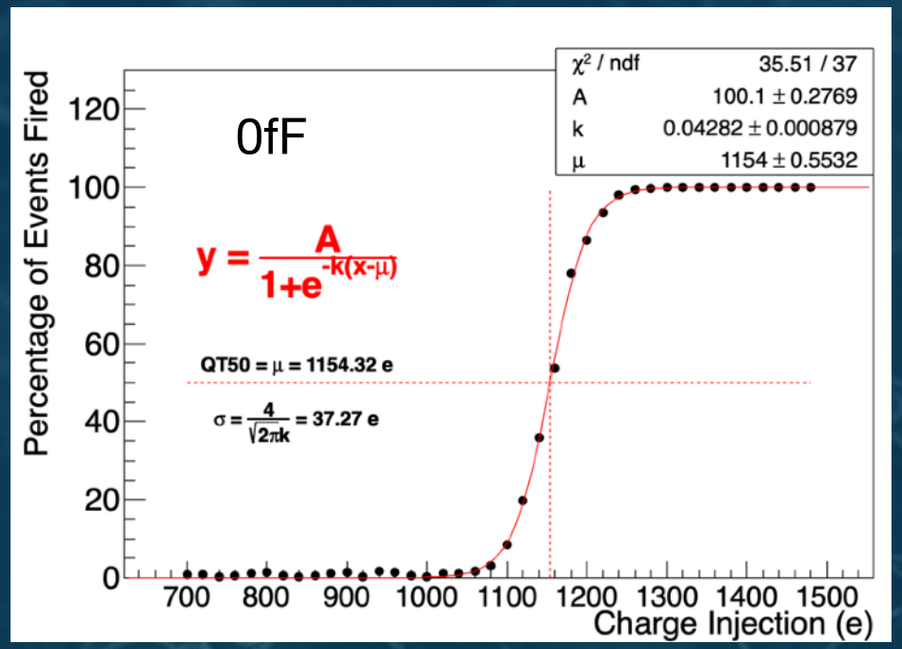
On-Chip TDC

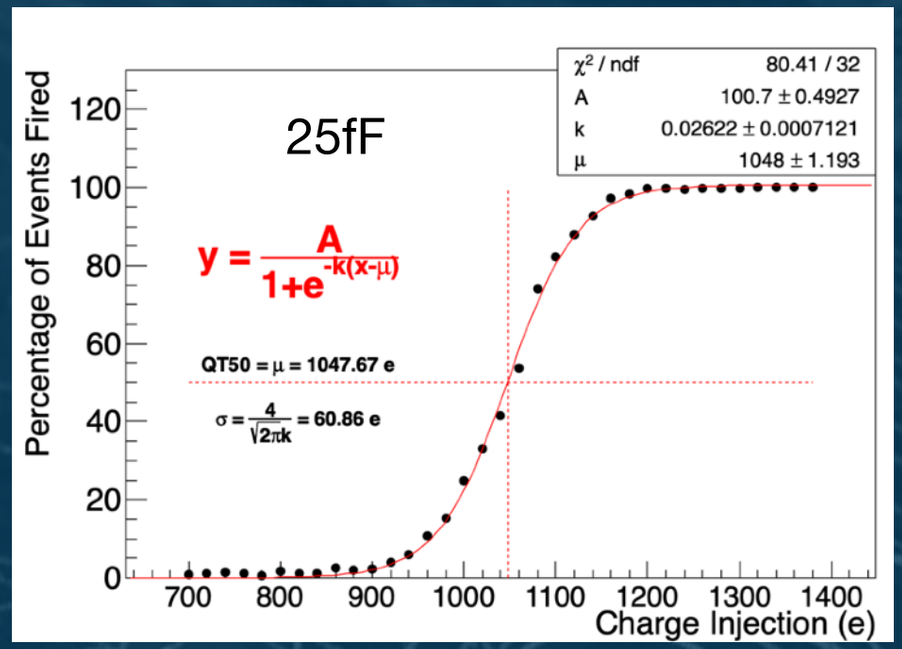


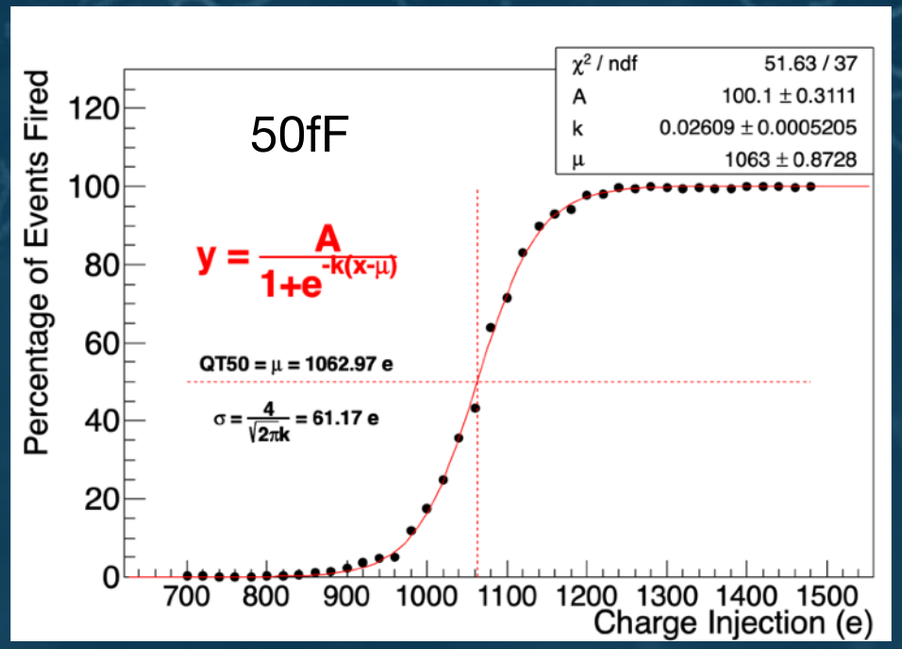
Measured period 86.5 +- 0.52 cells => 21.9ps +- 0.12ps delay per bit

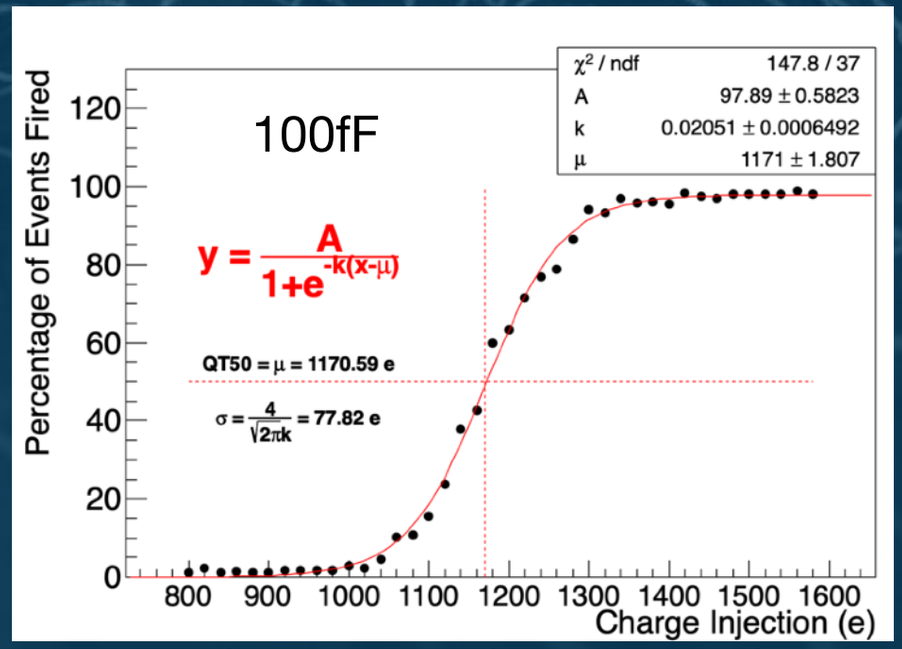
- 128-bit deep delay chain
- 6-bit coarse counter (driven by external clock)
- Rising/Falling edge from AFE freeze delay chain
- If delay chain longer than clock period can calibrate time resolution of TDC

ENC



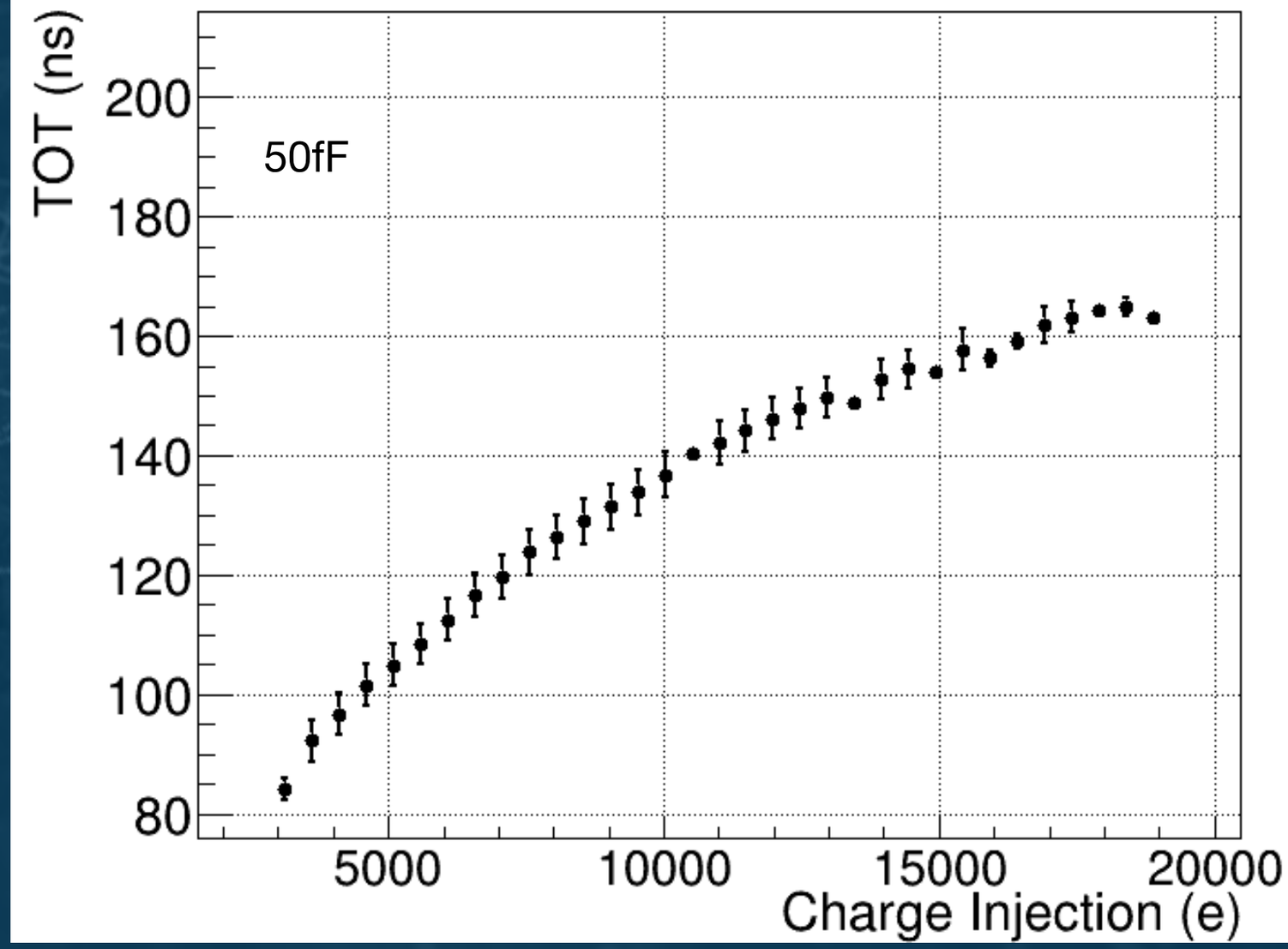






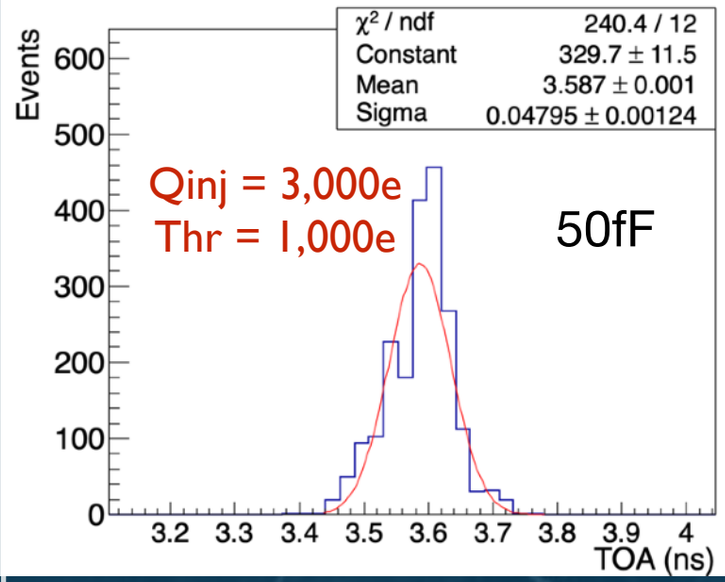
Input Cap (fF)	0	25	50	100
ENC (e)	37	61	61	78

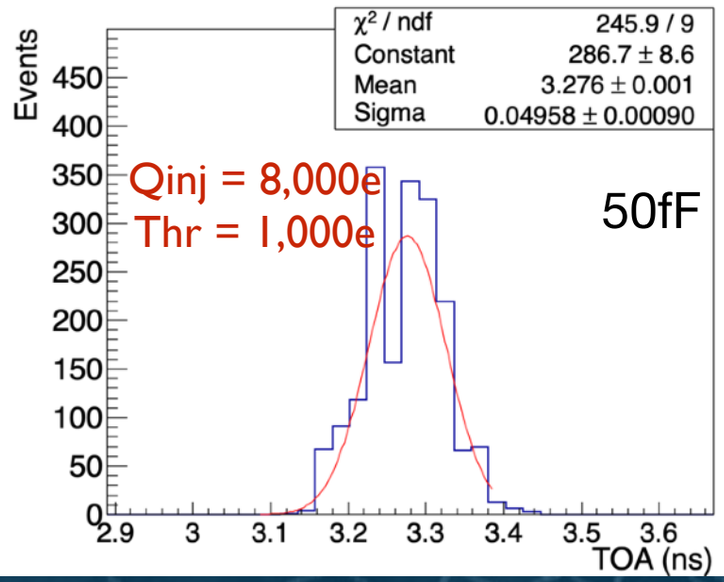
ToT

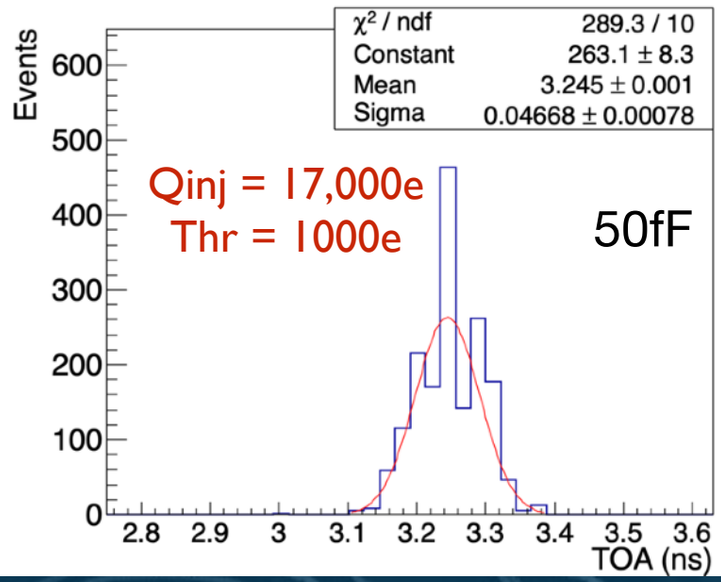


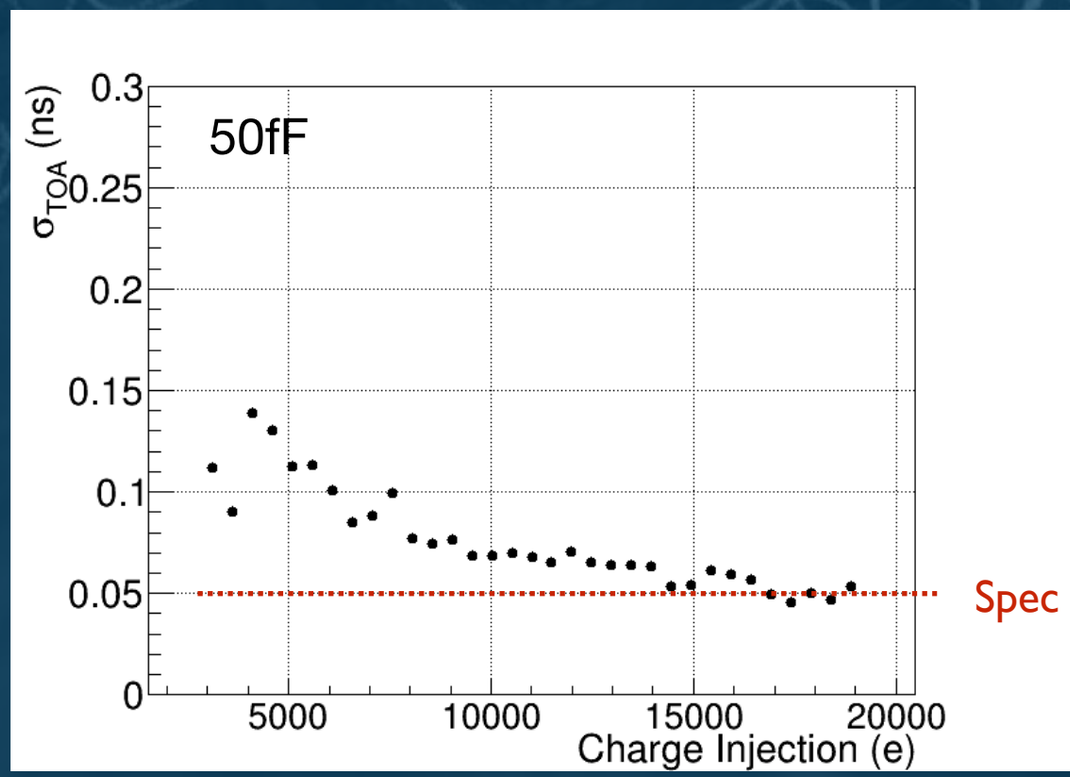
Tunable via CSA feedback current

TOA



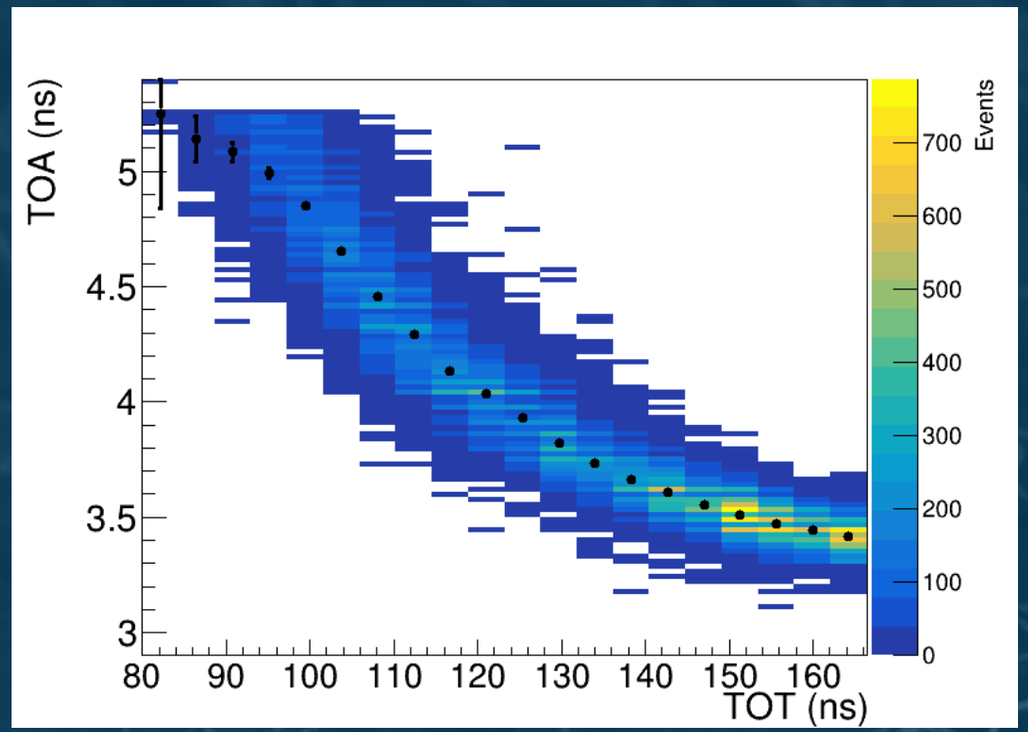


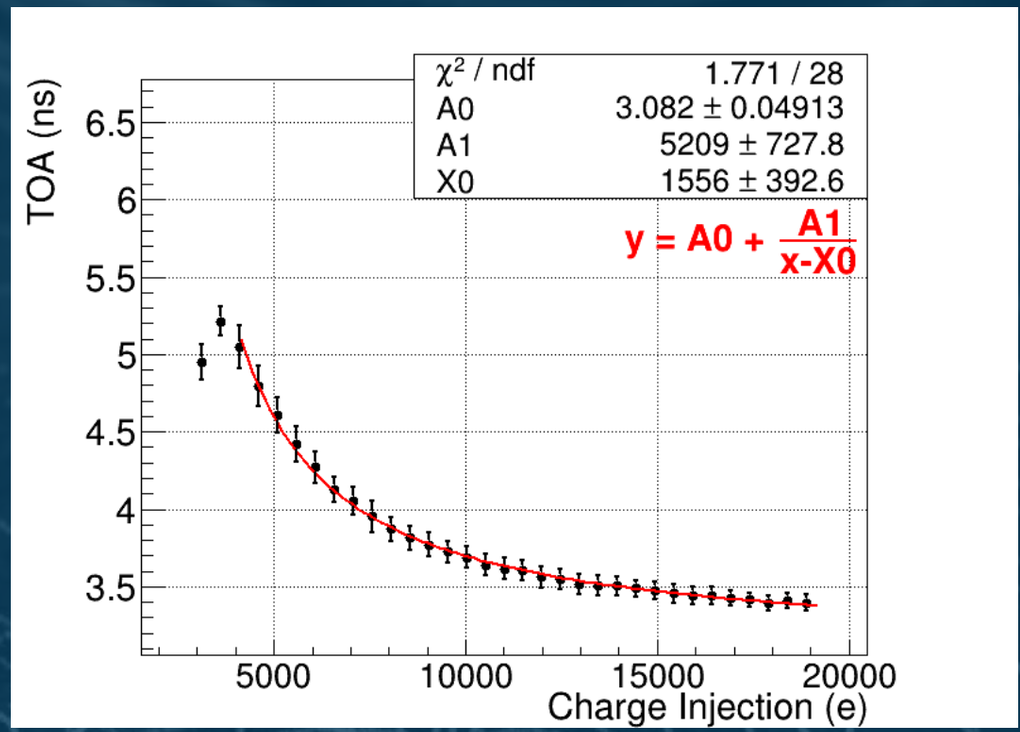


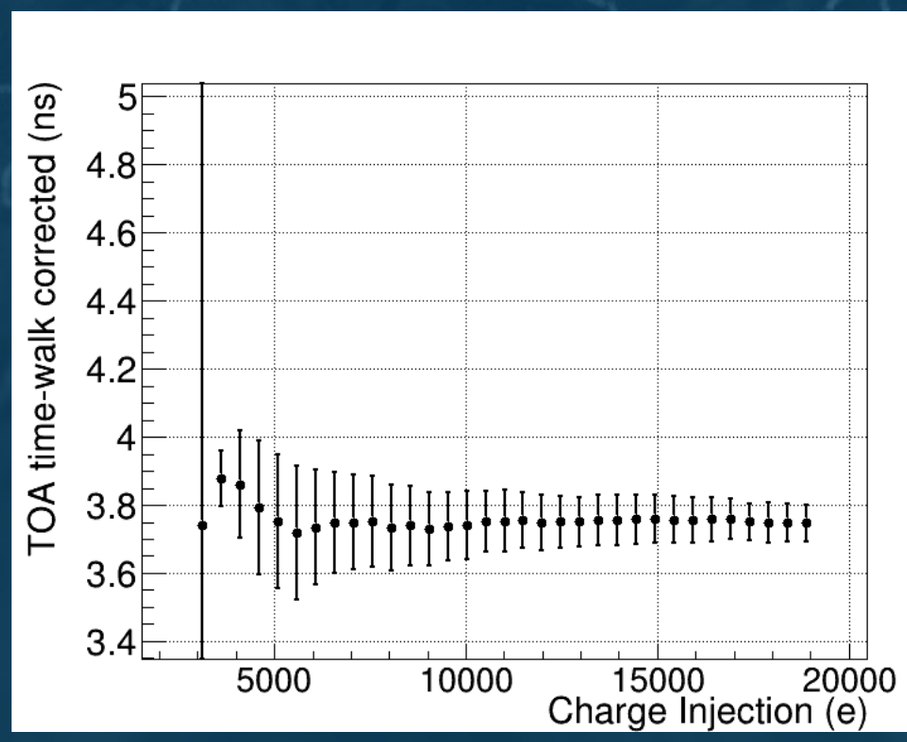


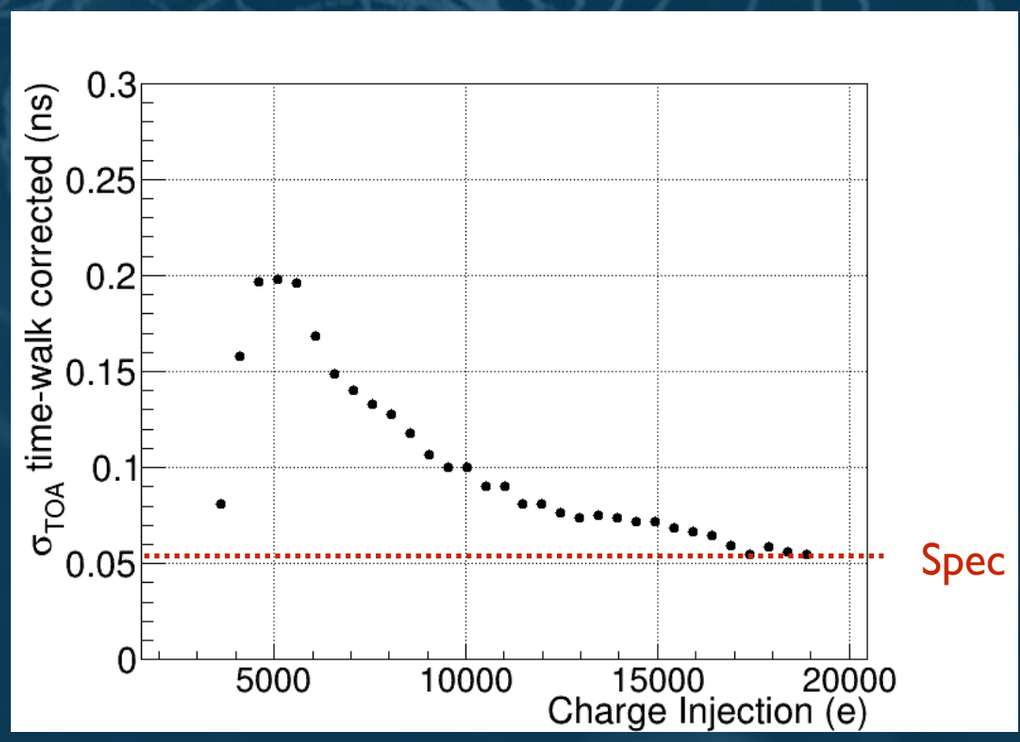
- Room temperature
- Default parameters, not further optimized
- Not corrected for timewalk!
- Meet spec with 0fF Cin

Timewalk


TOA (ns)
TOT (ns)
Events
80 90 100 110 120 130 140 150 160
3 3.5 4 4.5 5
0 100 200 300 400 500 600 700


χ² / ndf 1.771 / 28
A0 3.082 ± 0.04913
A1 5209 ± 727.8
X0 1556 ± 392.6
y = A0 + A1/(x-X0)
TOA (ns)
Charge Injection (e)
3.5 4 4.5 5 5.5 6 6.5
5000 10000 15000 20000


TOA time-walk corrected (ns)
Charge Injection (e)
3.4 3.6 3.8 4 4.2 4.4 4.6 4.8 5
5000 10000 15000 20000

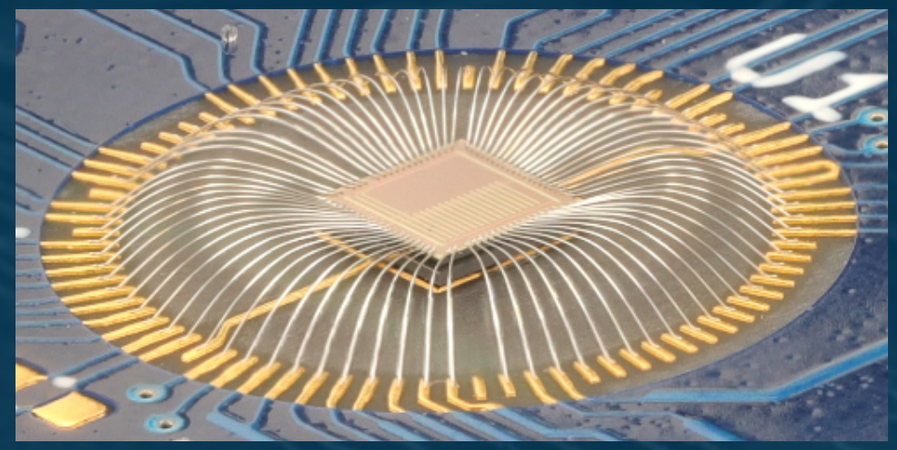

σTOA time-walk corrected (ns)
Charge Injection (e)
Spec
0 0.05 0.1 0.15 0.2 0.25 0.3
5000 10000 15000 20000

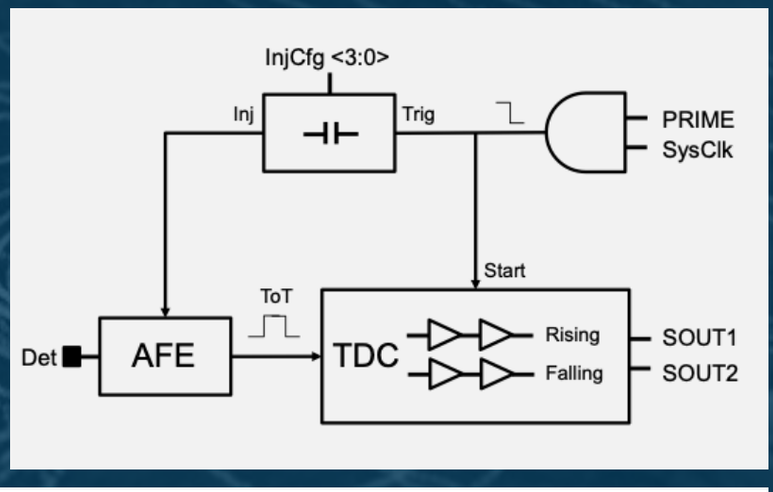
Summary

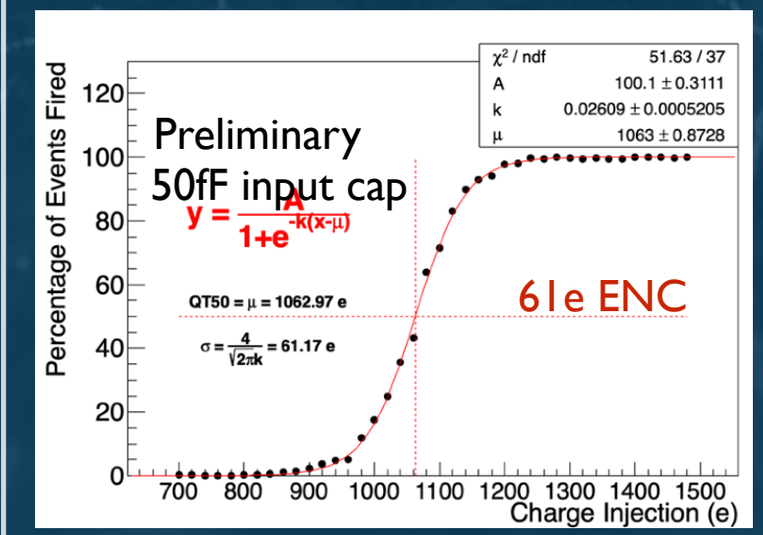
- Received first 28nm chip, Pebbles, that implements analog front-end, Big Rock, suitable for a 4D Pixel detector
- Pebbles has on-chip test bench with characterization TDC measured to have ~20ps resolution
- Test results high encouraging, close to meeting spec with out of the box settings
  - Achieved on average 75ps RMS timing resolution with 50fF Cin
  - Big Rock AFE has been improved for next submission in Metarock chip
- Excited to see performance of new pixel TDC based on time-stretching once we receive Metarock back from fabrication
  - New pixel TDC is ultra low power (~1uW) and small <15um x 15um and driven with 40MHz clock

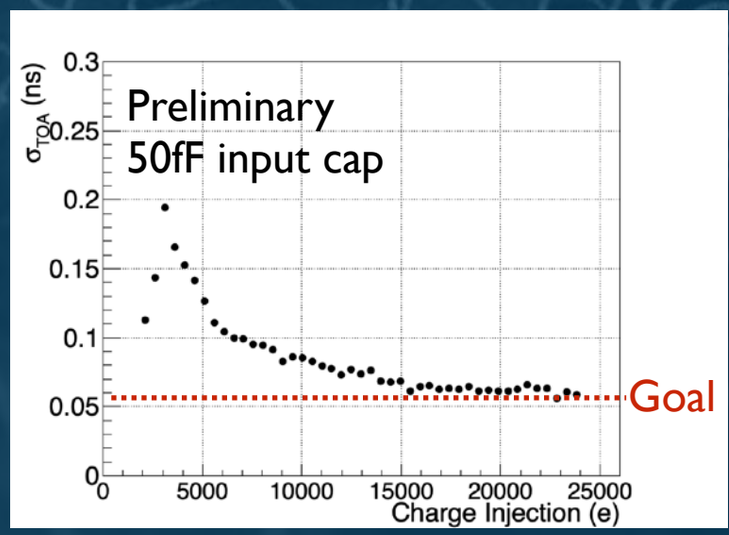
Pebbles & Metarock

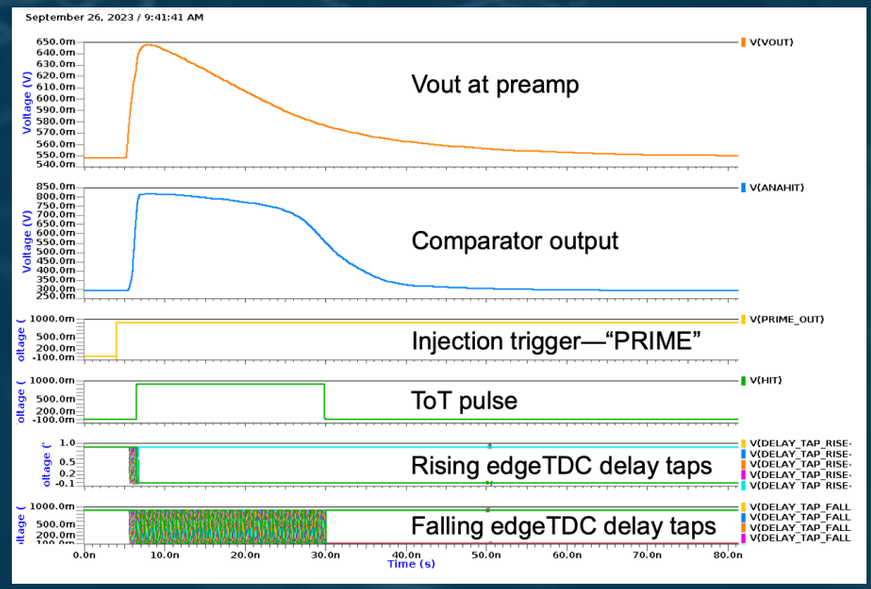
- Submitted two 28nm mini-ASICS:
  - Pebbles: implements Big-Rock AFE with on-chip test bench (received Oct 2022)
  - Metarock: improved Big-Rock AFE with realistic TDC (currently being manufactures)
- Big-Rock AFE: 10x30um2, 4uW, <100e noise, ~50ps timing @ 50fF detector capacitance
- Pixel TDC: 15x15um2, 1-2uW average, 40MHz clock











Also aiming to test 28nm for operation at cryogenic conditions,
Pebbles includes cryo-suitable reference voltage circuits,
Metarock includes single transistor test circuits.