Pixel ASIC development for ATLAS and CMS

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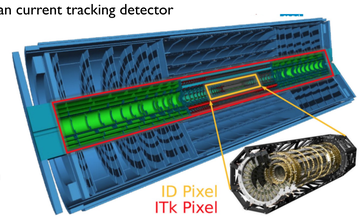
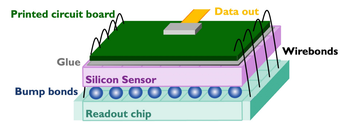
ATLAS Inner Tracker Upgrate

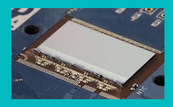
- All-silicon **upgraded tracking detector (ITk)** for HL-LHC to cope with increased instantaneous luminosity and pile-up
- Upgraded pixel detector:
- Larger silicon area → 6x larger than current tracking detector
- ~13 m2 of active area
- 9400 pixel modules
- 5.1 billion pixels
- Extended η coverage to $|\eta| \leq 4$
- Smaller pixel pitch:
  $400 \times 50\ \mu m^2 \rightarrow 50 \times 50\ \mu m^2$
- **New readout chip** to cope with higher data rates and increased radiation



ITk Pixel Module



RD53A



- Pixel chips for ATLAS and CMS upgrades have been jointly developed by the RD53 collaboration
- First joint prototype was RD53A, submitted in August 2017

→ Half-sized demonstrator chip with three different analog front-end architectures (linear, differential and synchronous)

Digital Logic & Radiation tolerance

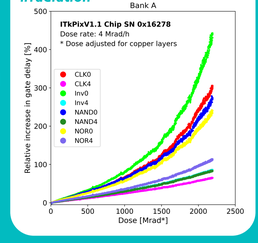
- Radiation tolerance requirement for HL-LHC: 1 Grad
- Digital logic gates particularly susceptible to radiation damage
- Chip includes ring oscillators for radiation testing → maximum allowed gate delay increase after 1 Grad is 200%
- Smallest transistors (strength 0) found to fail this requirement

→ Not used in the final chip

- Additionally, dose rate affects damage

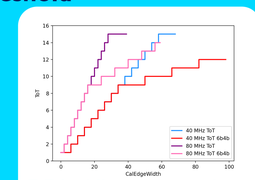
→ Factor 2 more damage at low dose rates

Digital gate delay increase with irradiation



Time over Threshold

- ToT is main chip data output during operations
- Several modes of ToT implemented for flexibility
- ToT bug fixed for ITkPixV2



ToT for different injection charges

Single-Event Upset

ITkPixV2

- **ATLAS ITkPixV2** chip submitted in April 2023
- Many small changes to improve:
  - Stability against single-event transients
  - Startup and powering stability
  - Improvements and additional monitoring sensors for temperature and radiation
- Received back engineering run wafers
- Validated most chip functionality to work as expected

→ **ATLAS Pixel ASIC ready for ITk production**

ITK TDR (Apr 2017)

RD53 Collaboration LOI (Feb 2013)

RD53A chip submission (Nov 2017)

RD53B design finished (Nov 2019)

CROC V1 submission (Jun 2021)

ITkPixV2 submission (03/2023)

CROC V2 submission (Oct 2023)

2013 | 2017 Proto IP | 2018 | 2019 RD53A | 2020 | 2021 RD53B | 2022 | 2023 RD53C | 2024

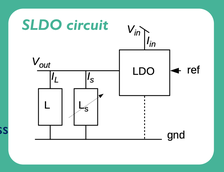
FE65-P2 and CHIPX prototype chips (Dec 2015)

Serial Powering: SLDO

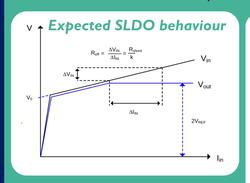
- ITkPixV1 modules will be operated in a **serial power configuration**, suppying a constant current
- Motivation: reduce the number of cables and material in the detector
- Solution: **SLDO circuit**, which powers the main load (the chip) and the internal load (shunt element)
- Shunt element is designed such that it achieves the required input current, regardless of what the chip does

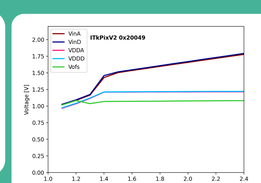
→ First introduced in FE-I4 chips and refined in RD53A & RD53B

SLDO circuit

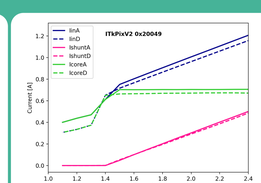


Expected SLDO behaviour





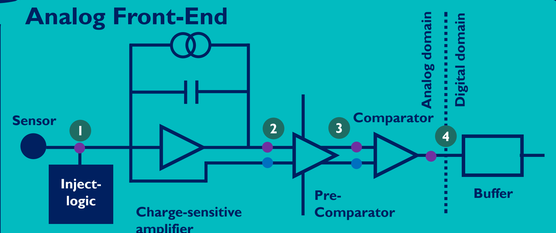
Measured SLDO voltages



Measured SLDO currents

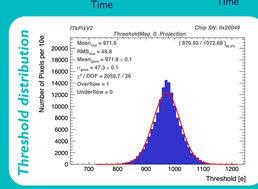
RD53A AFE review & design validation finished (12/2018)

Analog Front-End



- Differential analog front-end chosen for the ATLAS pixel readout chip
- Time-over-threshold determined by comparator and digitized
- Threshold adjustable globally and per pixel

Threshold distribution

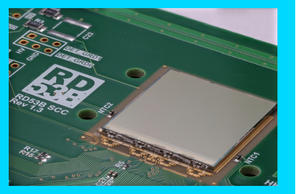


ITkPixV1 submission (03/2020)

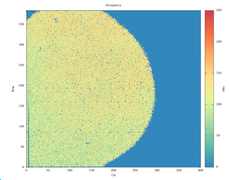
ITkPixV1.1 submission (10/2020)

ITkPixV1

- **ATLAS ITkPixV1** chip submitted in March 2020
- Found a serious issue in the time-over-threshold (ToT) memory
  - Large current for particular configurations of ToT
  - Wrong ToT storage and hit loss
- Fix to the mask on the remaining FE wafers, fixing the issue of large leakage current in ITkPixV1.1 (but ToT still not useable), submitted in October 2020



Hit map in pixel module using radioactive source



- ITkPixV1 characterised over two years in testbench setups, pixel modules (including sensors) and testbeam measurements

→ No major issues found

- ITkPixV1.1 will be used as the **ITk pre-production readout chip**