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Charge waveform digitization by counting pulses and charge neutralization

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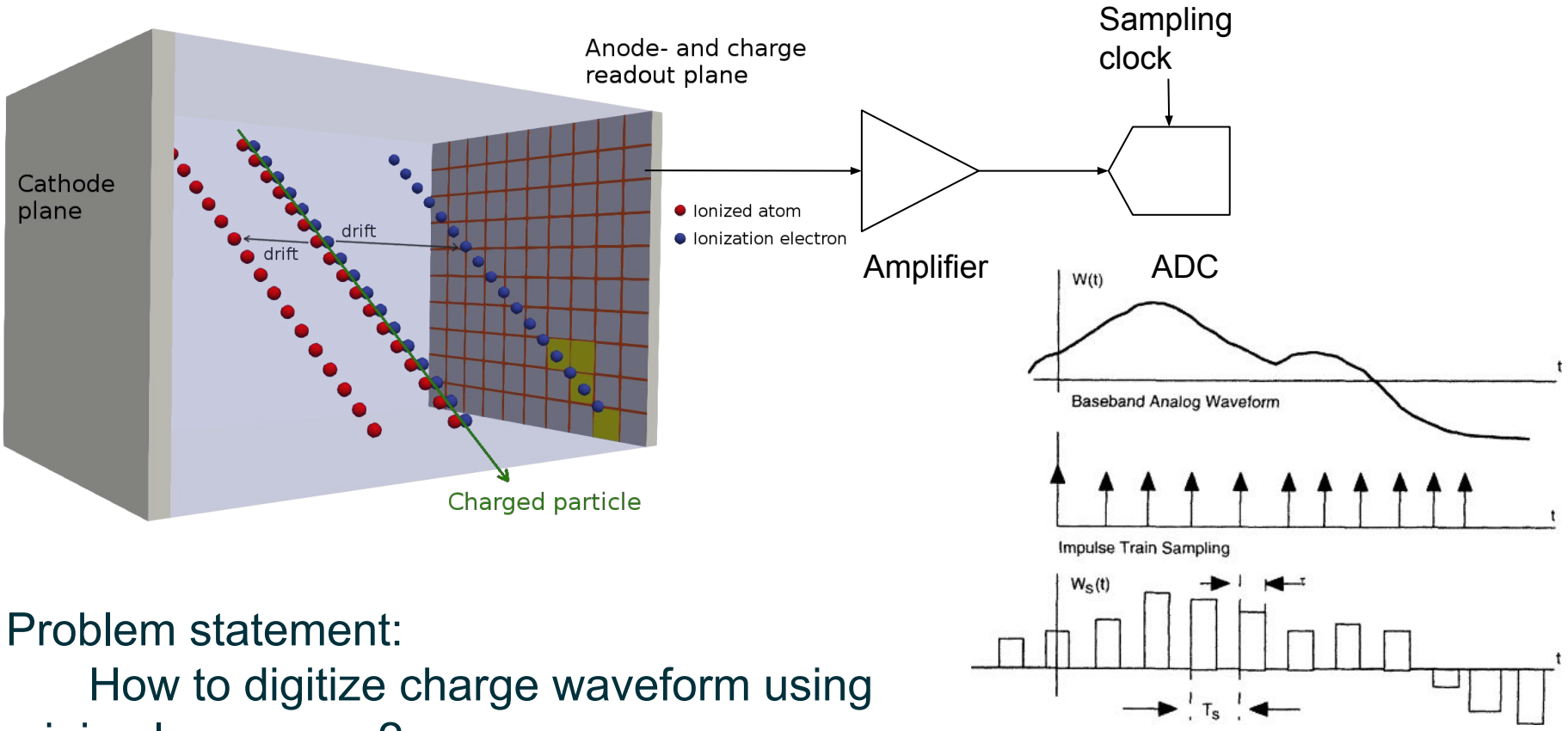
October 2023

Digitizing TPC charge waveform

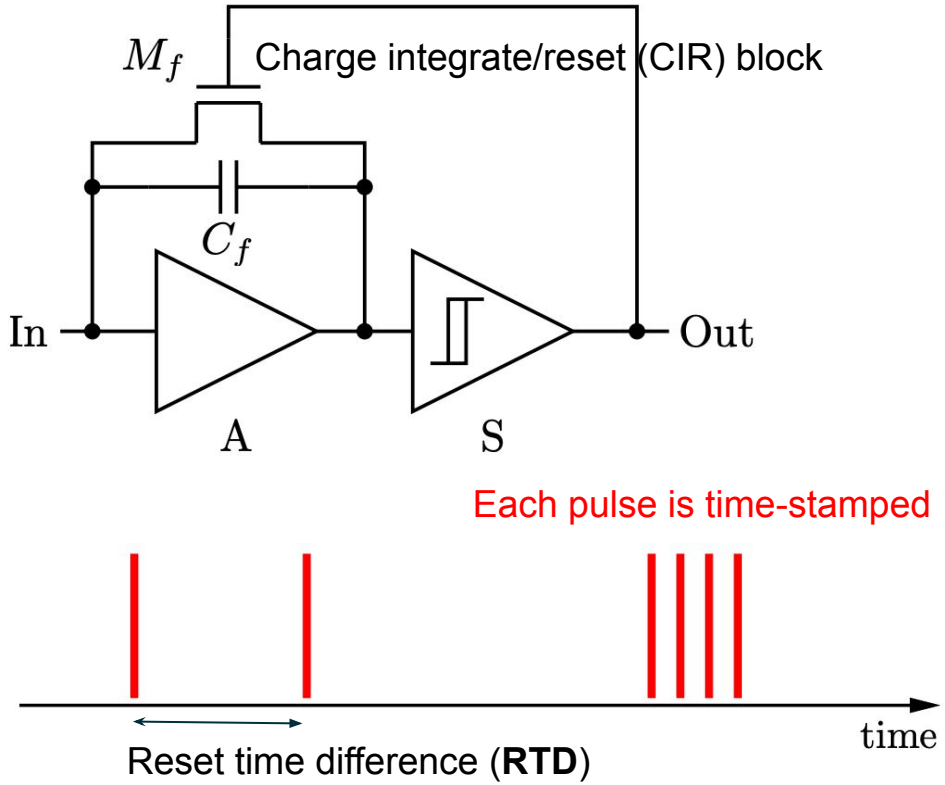


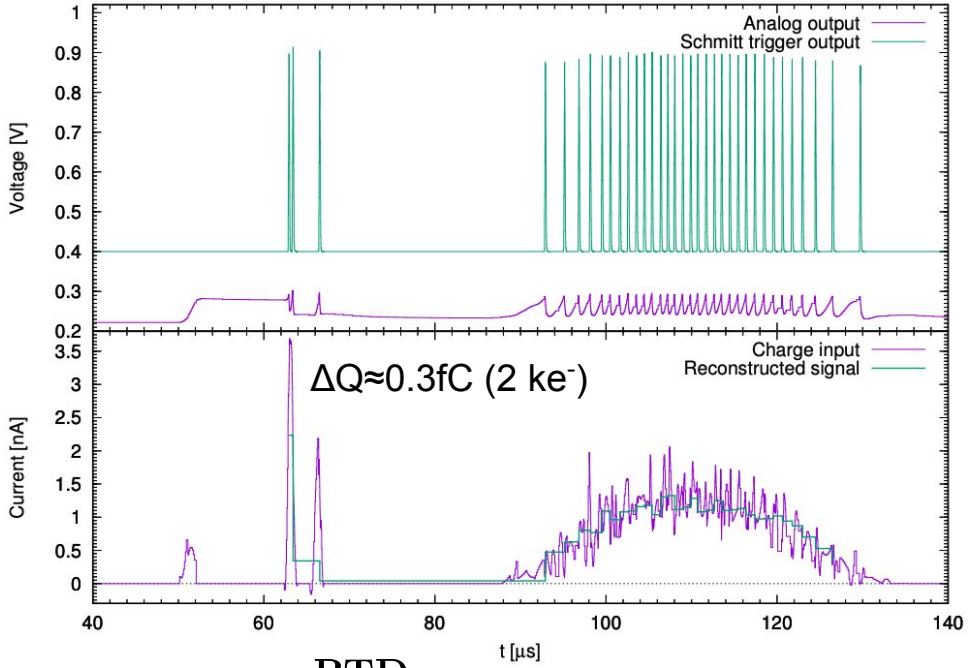
Problem statement:

How to digitize charge waveform using minimal resources?

Pulse code modulation (PCM)

TPC charge waveform and Q-Pix RTD

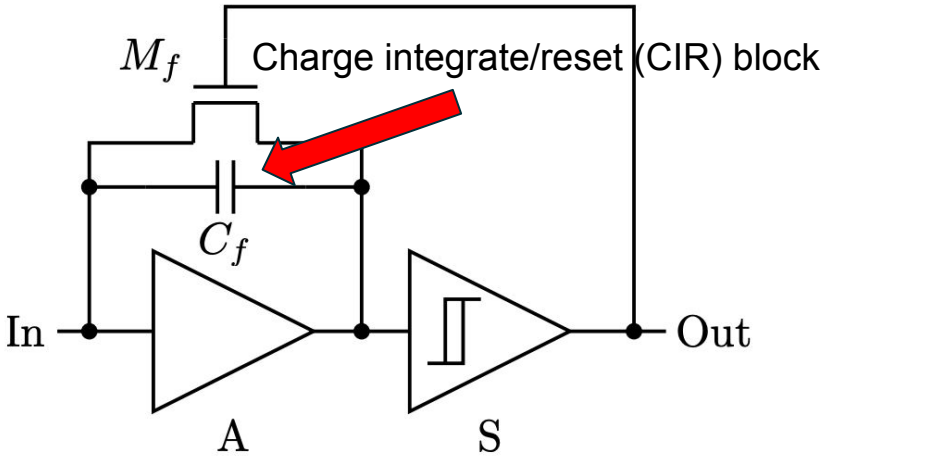


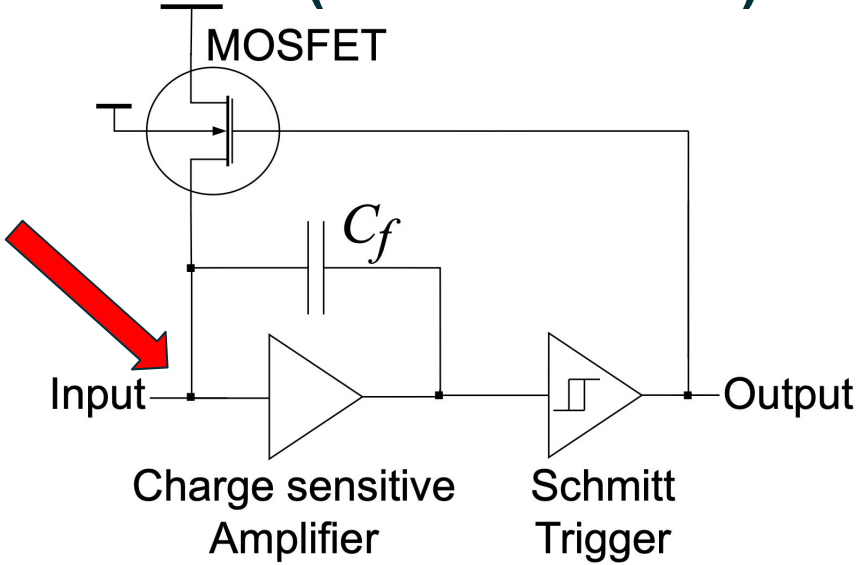


$$\Delta Q = \int_0^{\mathbf{RTD}} I(t)dt$$

Q-Pix: Pixel-scale Signal Capture for Kiloton Liquid Argon TPC Detectors: Time-to-Charge Waveform Capture, Local Clocks, Dynamic Networks, Nygren and Mei arXiv:1809.10213

Charge reset vs. charge replenishment (neutralization)



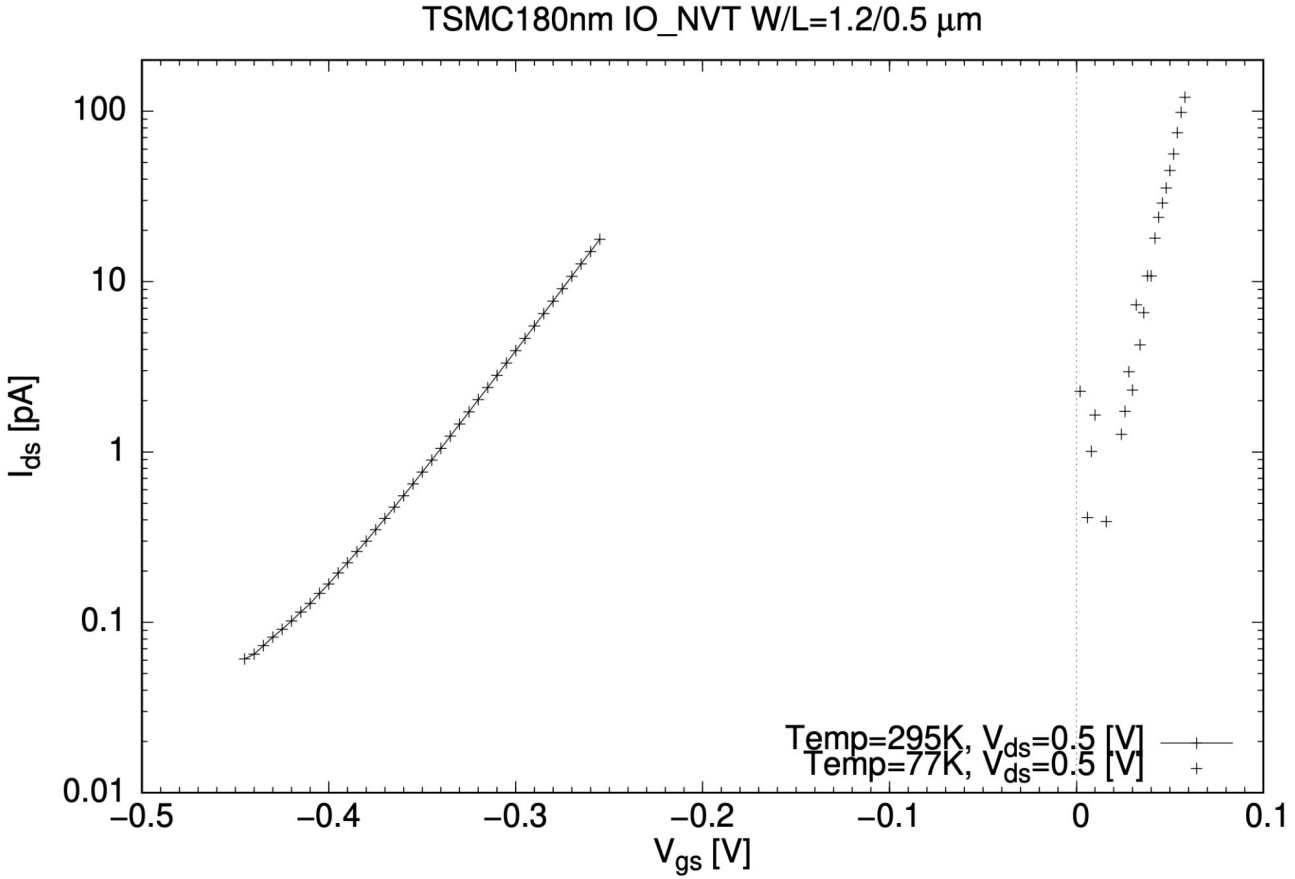


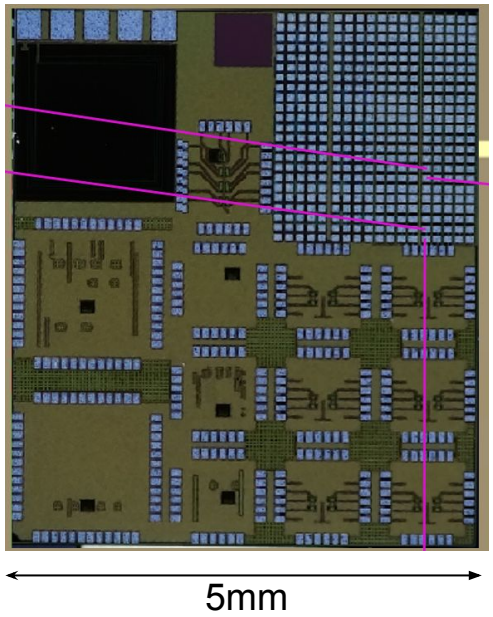
Reset time difference (**RTD**)

$$\Delta Q = \int_0^{\mathbf{RTD}} I(t)dt$$

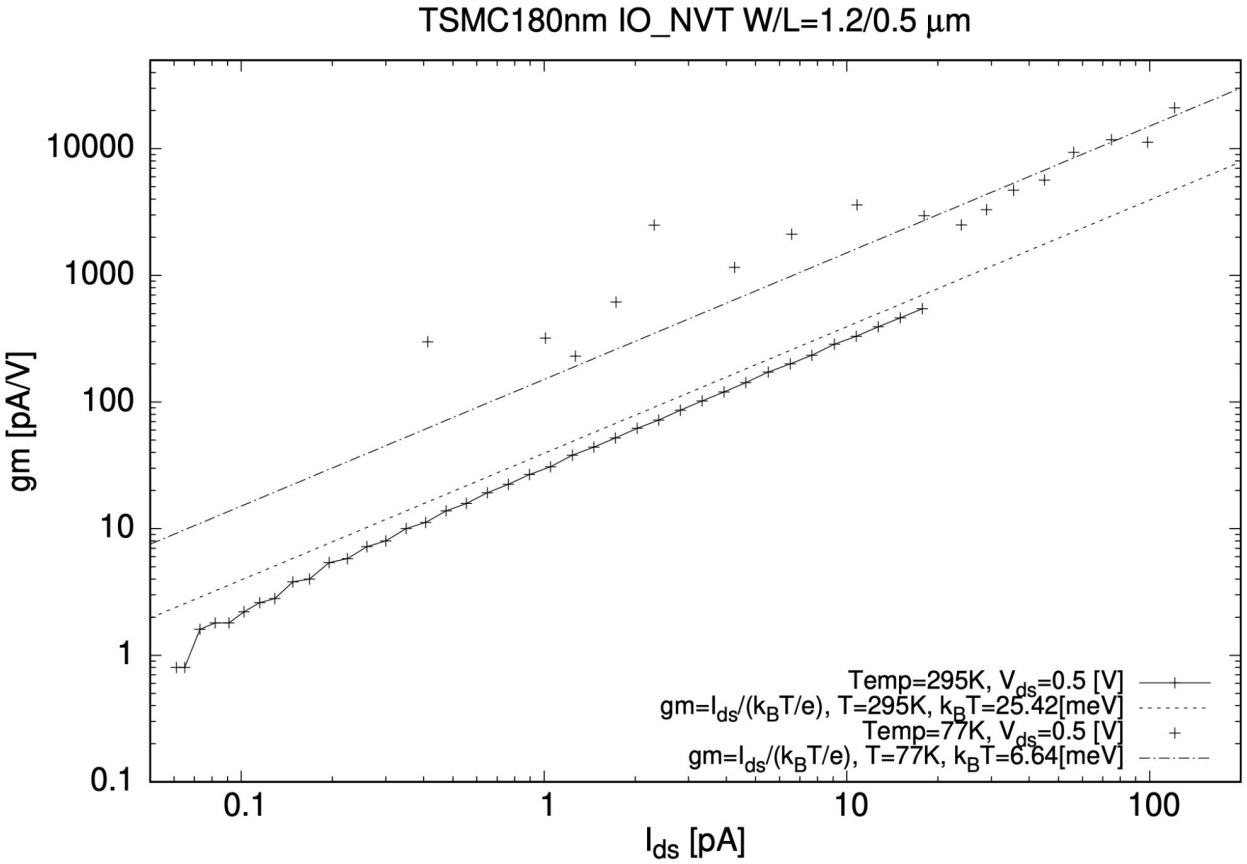
Q-Pix: Pixel-scale Signal Capture for Kiloton Liquid Argon TPC Detectors: Time-to-Charge Waveform Capture, Local Clocks, Dynamic Networks, Nygren and Mei arXiv:1809.10213

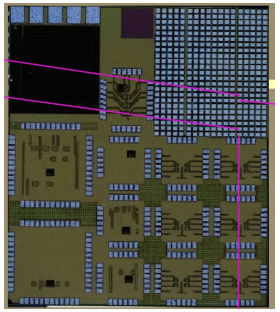
Tiny current control with NMOS in ASIC





Tiny current control with NMOS in ASIC



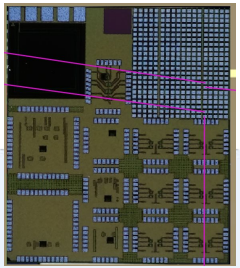


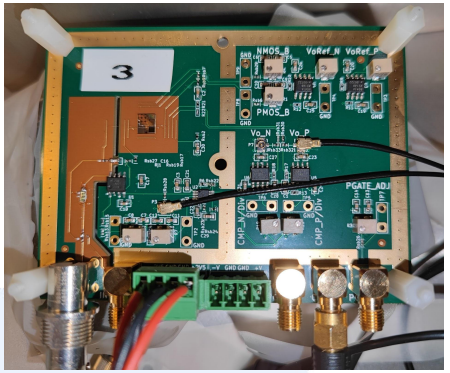
Deep sub-threshold operation
Transconductance

$$\frac{\partial I_{ds}}{\partial V_{gs}} = g_m = \frac{I_{ds}}{n \cdot k_B T/e}$$

4-terminal NMOS in chip + discrete OpAmp & CMP

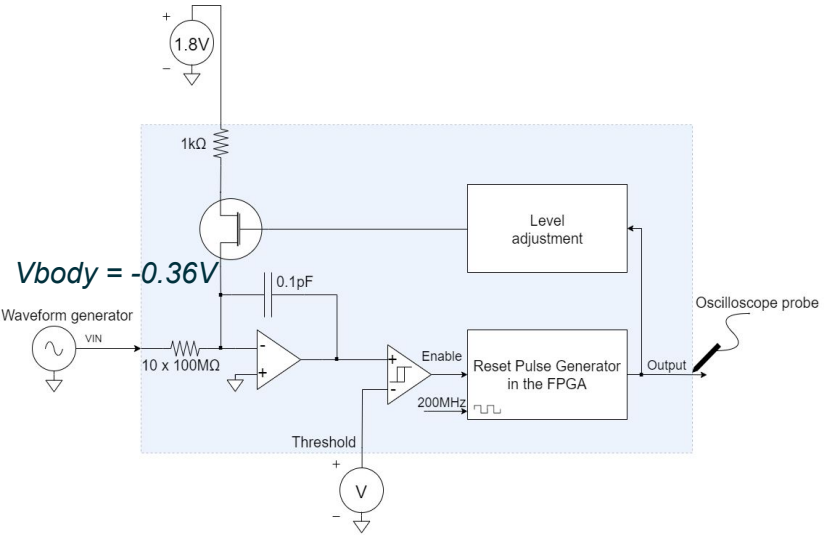
- Input: V source + 1~10 GOhm
- Charge replenishment: single NMOS current source
- Level adjustment for NMOS current control
- Low leakage current (~pA level)

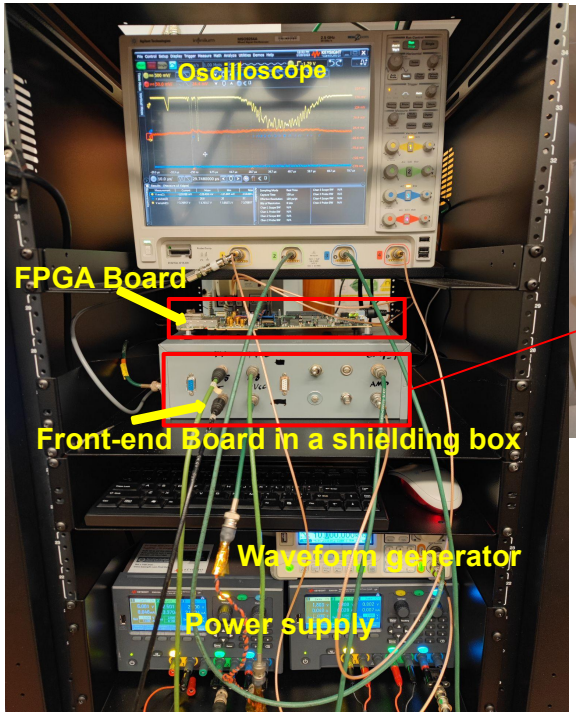


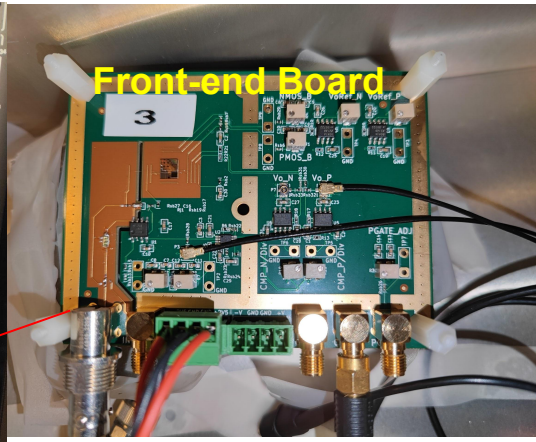


Demo with discrete OpAmp & CMP + NMOS in ASIC

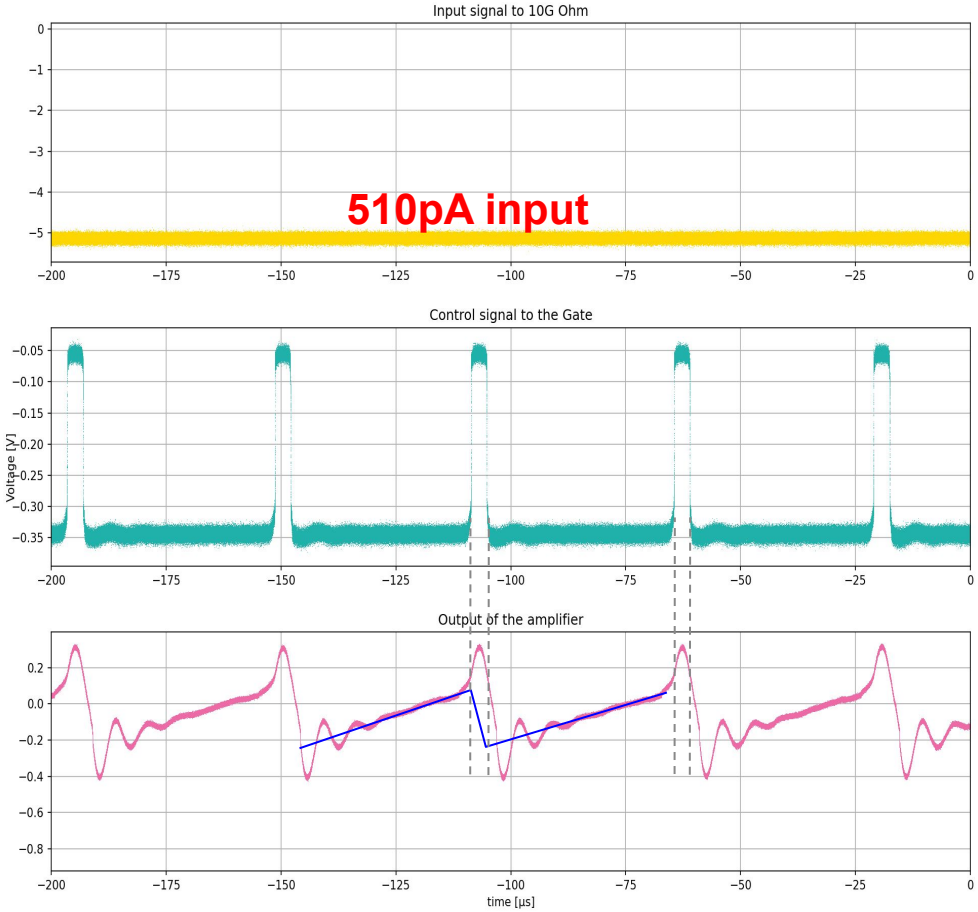
- Charge (current) waveform: Signal generator [V] through 10 x 100M Ohm
- Charge replenishment: NMOS in ASIC, wire-bonded on PCB
- Level adjustment circuits for precise NMOS gate level control. NMOS in sub-threshold
- NMOS body voltage adjusted for V_{th} and leakage through B-S junction



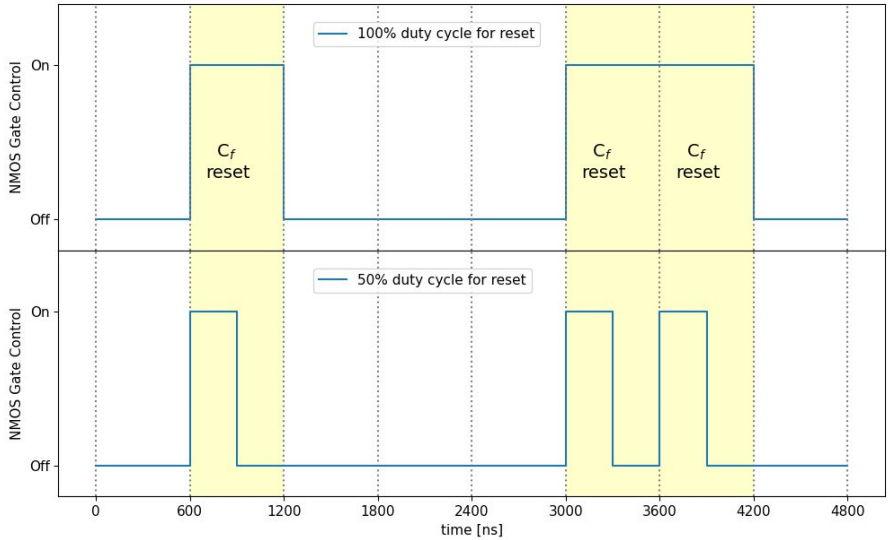




Reset pulse shape and level control

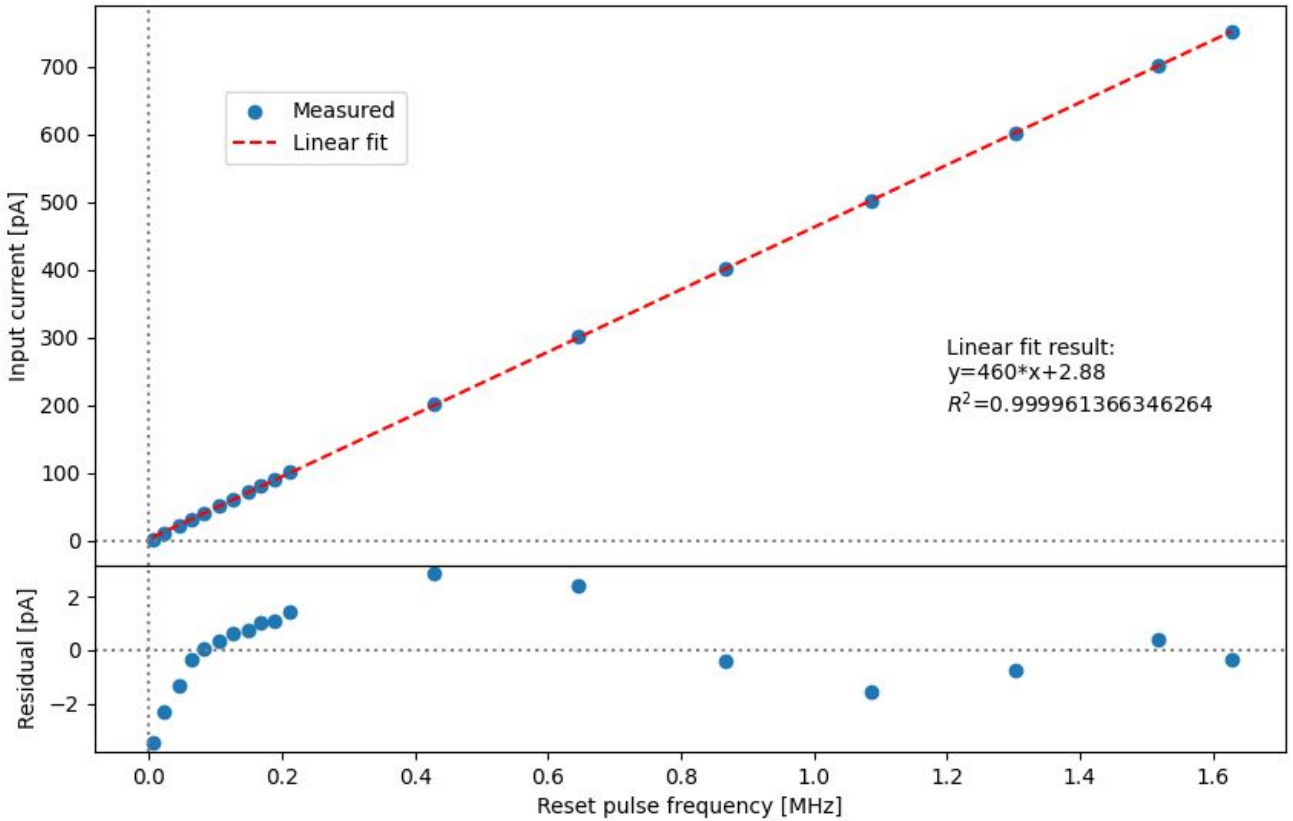


- Gate voltage must be negative to precisely control I_{ds} at low level
- In a clock cycle, the gate is on 50% of the time to allow output settling
- Output bouncing largely mitigated by better decoupling of the comparator



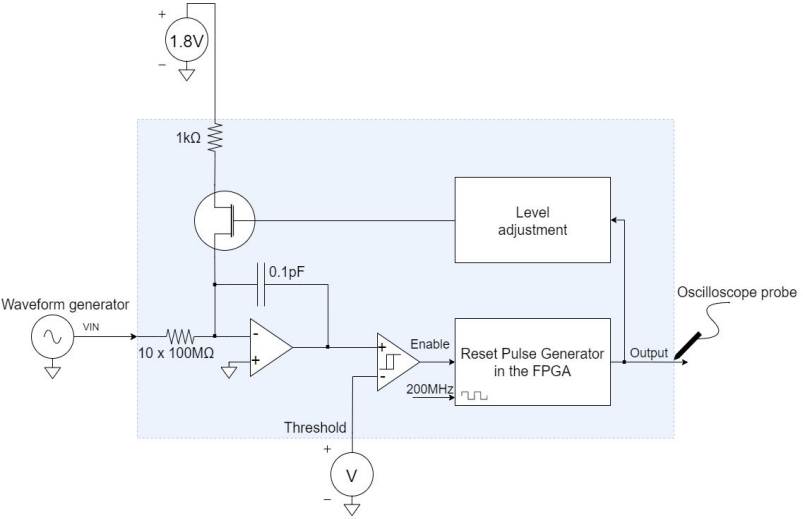
Linearity

- Reset Pulse width=300ns High + 300ns Low
- Slope is the charge during each replenishment period: ΔQ
- I = ΔQ * f + Io, ΔQ = 0.46 fC, Io=2.9pA (leakage current)

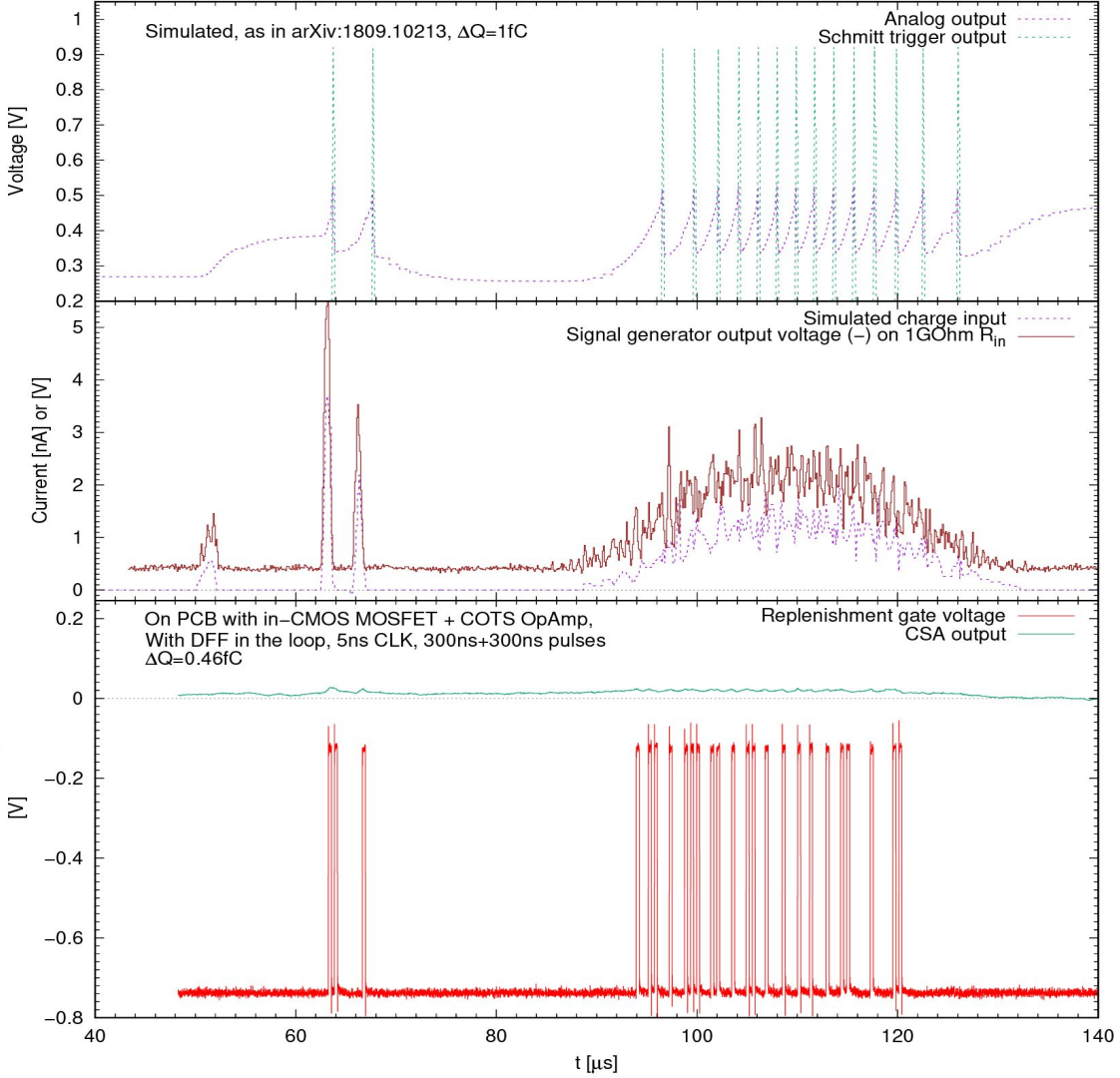


Q-Pix RTD waveform:
Simulation *vs.* Real circuit

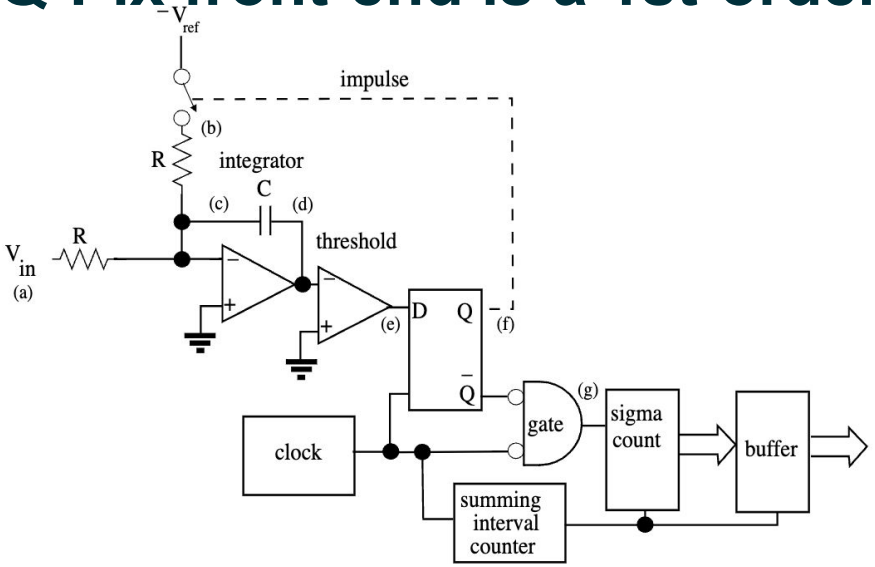
- Expected waveform as the simulation in arXiv:1809.10213
- Reset Pulse width is constant: 300ns High + 300ns Low
- ΔQ = 0.46 fC

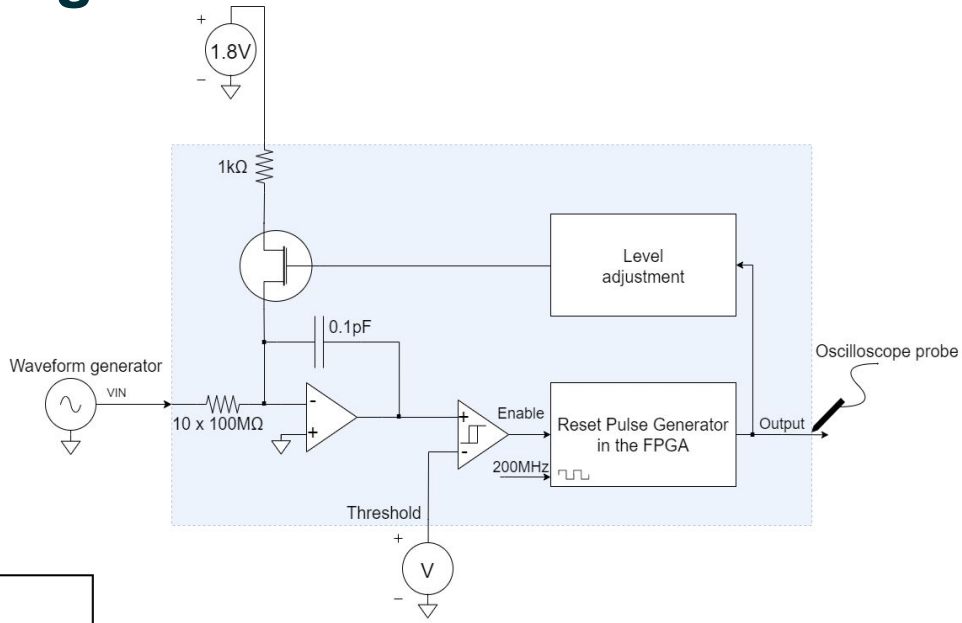


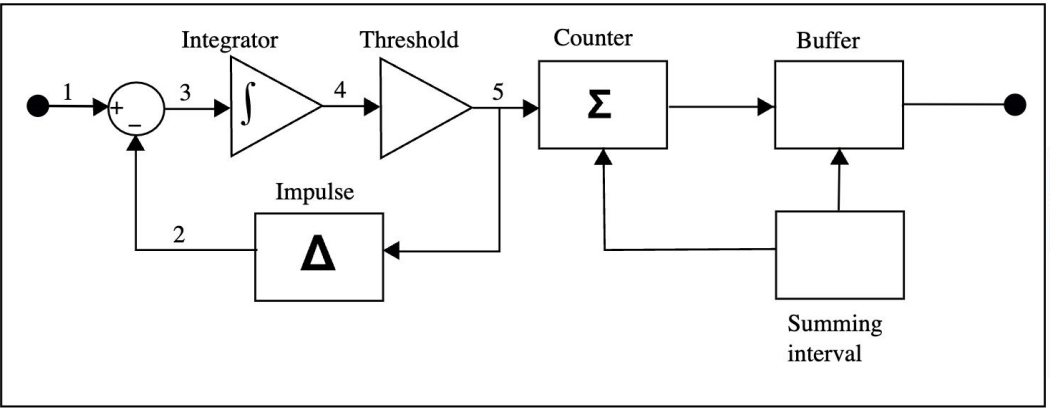
How best to reconstruct the waveform?



Q-Pix front-end is a 1st-order Sigma-Delta modulator







RTD is a zero-suppression data reduction scheme

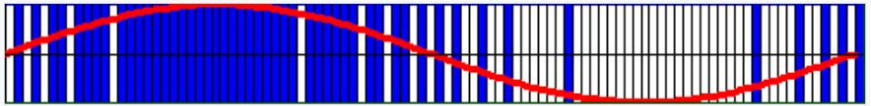
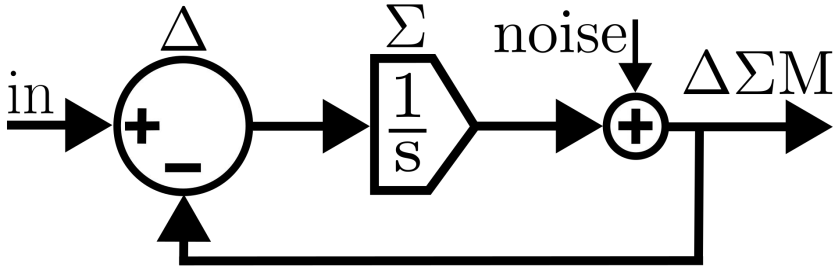


Figure 4: An example of delta-sigma modulation of 100 samples of one period of a sine wave. 1-bit samples (e.g., comparator output) overlaid with the sine wave. Logic high (e.g., V_{CC}) of the samples is represented by blue and logic low (e.g., $-V_{CC}$) is represented by white.

https://en.wikipedia.org/wiki/Delta-sigma_modulation

1st-order Sigma-Delta modulator



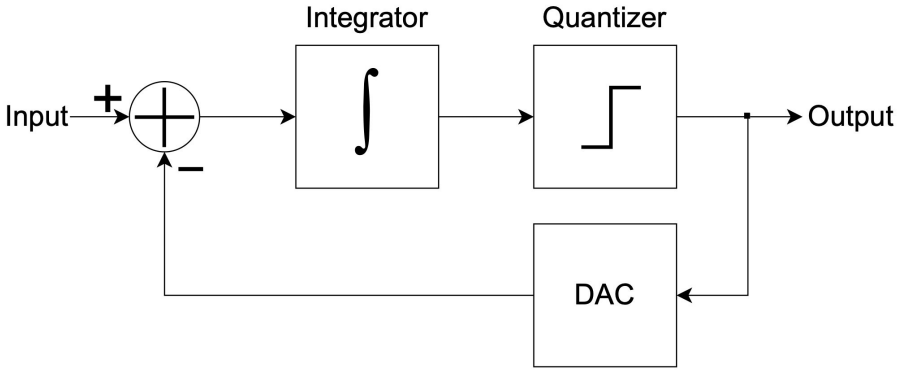
Laplace transform $s = \sigma + j\omega$

$$[in(s) - out_{\text{total}}(s)]\frac{1}{s} + noise(s) = out_{\text{total}}(s)$$

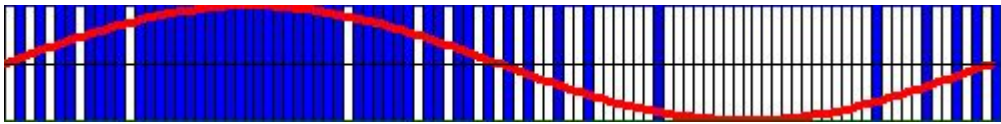
$$out_{\text{total}}(s) = out_{\text{signal}}(s) + out_{\text{noise}}(s)$$

$$\frac{out_{\text{signal}}(s)}{in(s)} = \frac{1}{s+1}$$

$$\frac{out_{\text{noise}}(s)}{in(s)} = \frac{s}{s+1}$$



1's and 0's are digital sample values at each time point
Oversample the signal by a large factor N



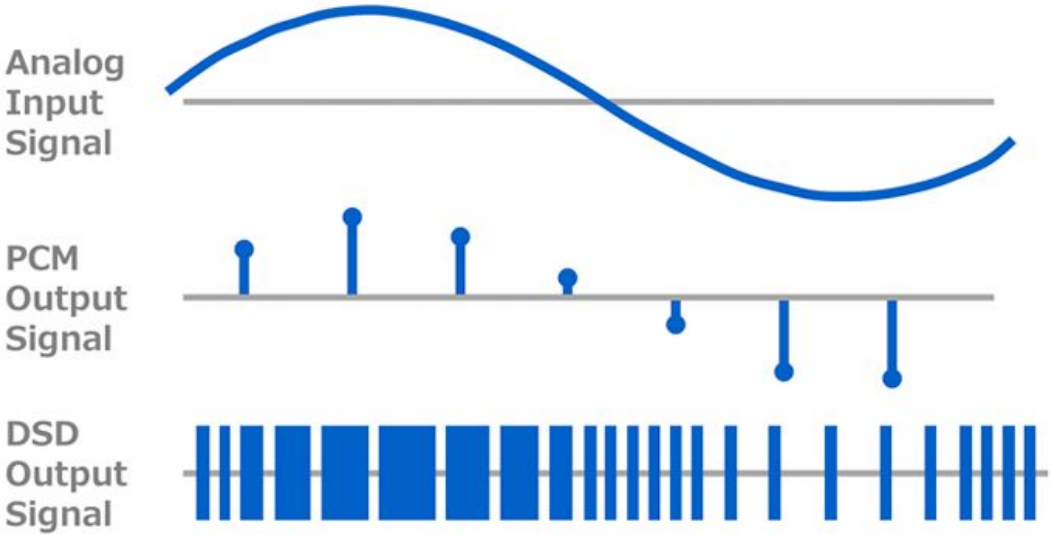
https://en.wikipedia.org/wiki/Delta-sigma_modulation

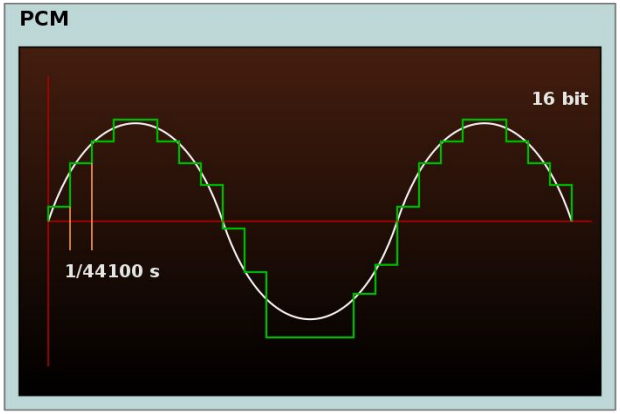
Pulse Code modulation vs Sigma-Delta modulation

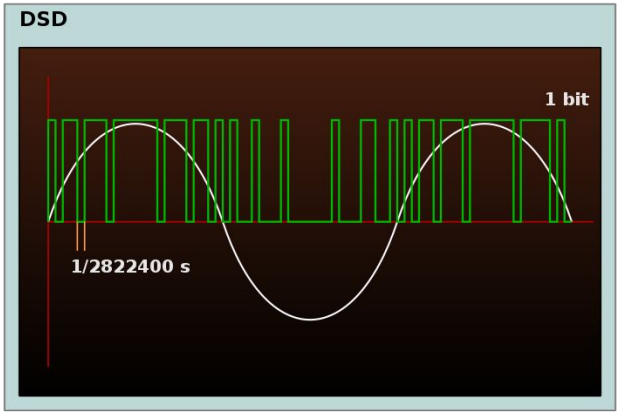
DSD

Direct Stream Digital

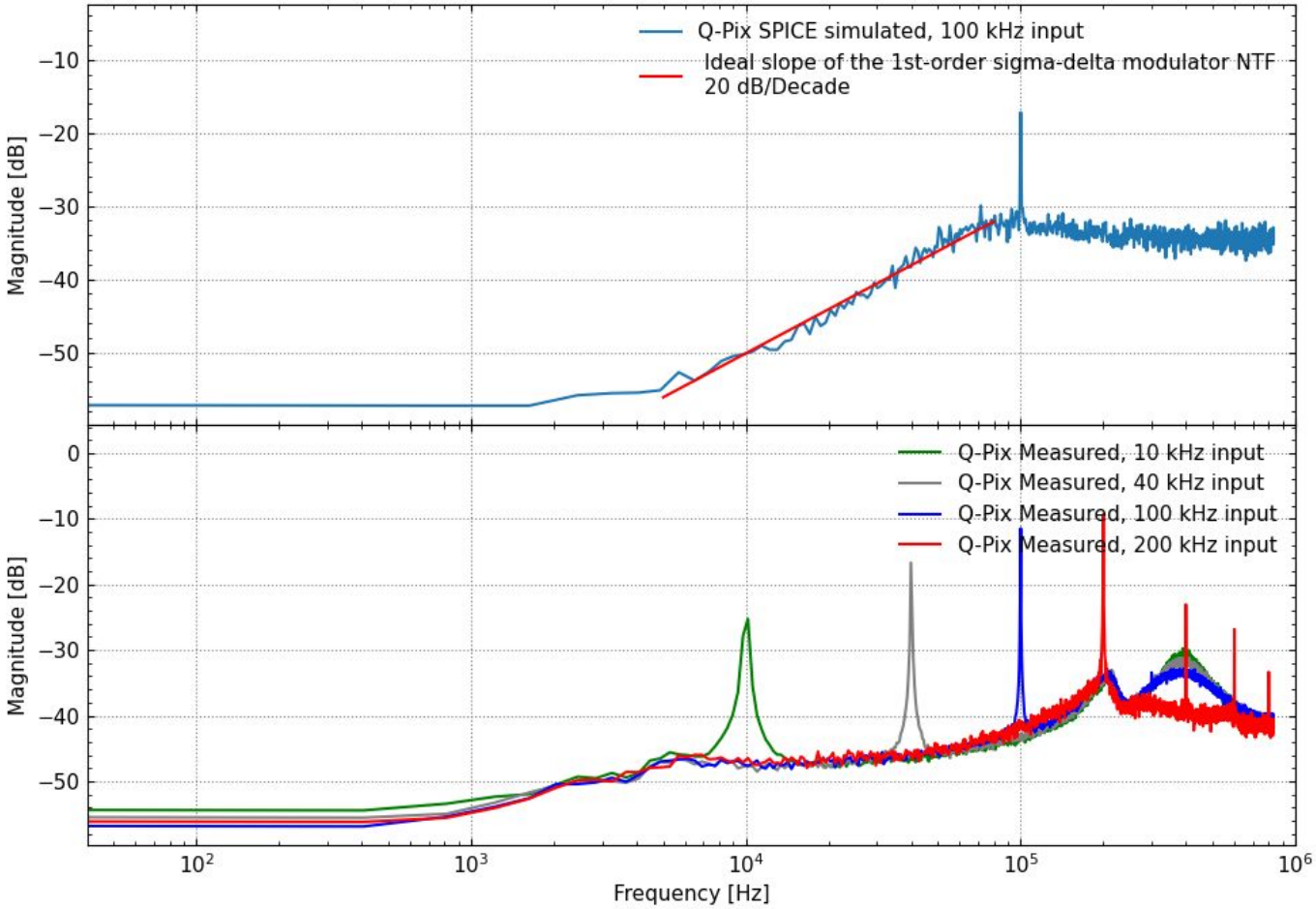
By SONY/PHILIPS
2.8224MHz clock
64x oversampled
(44.1kHz * 64 = 2.8224MHz)





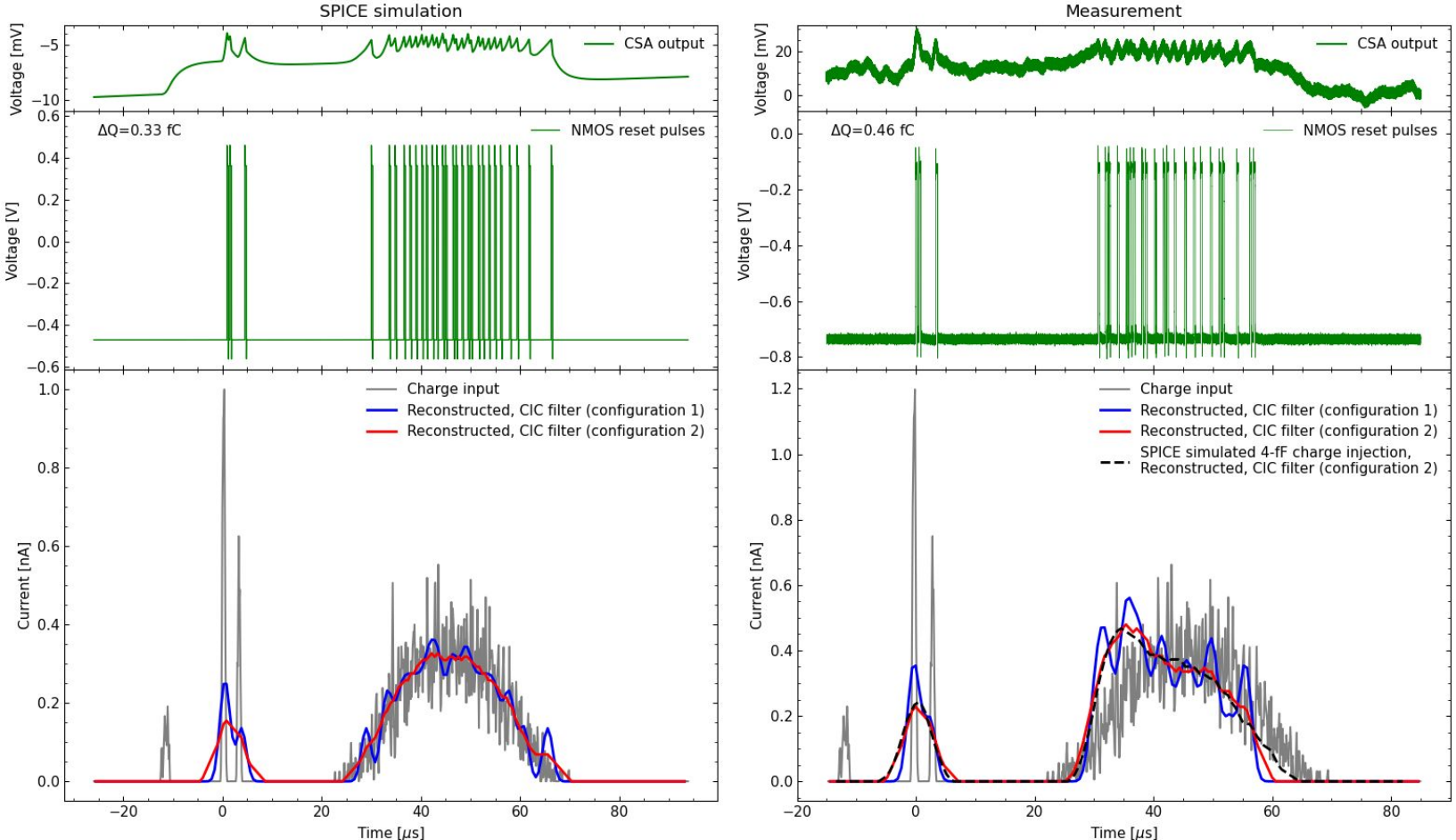


Simulated and measured Sigma-Delta spectral response



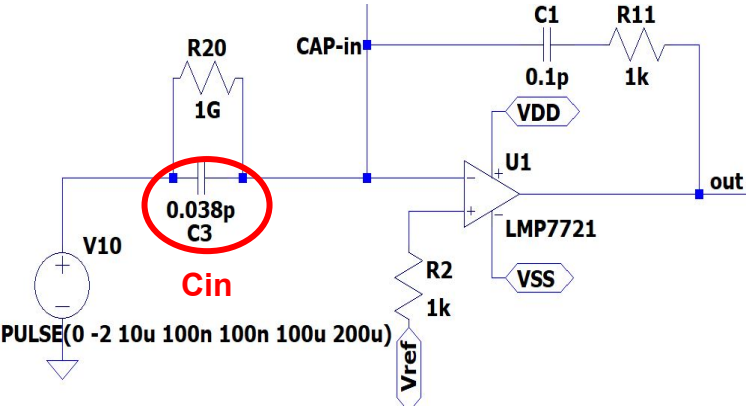
Reconstruct waveform with low-pass filter (CIC)

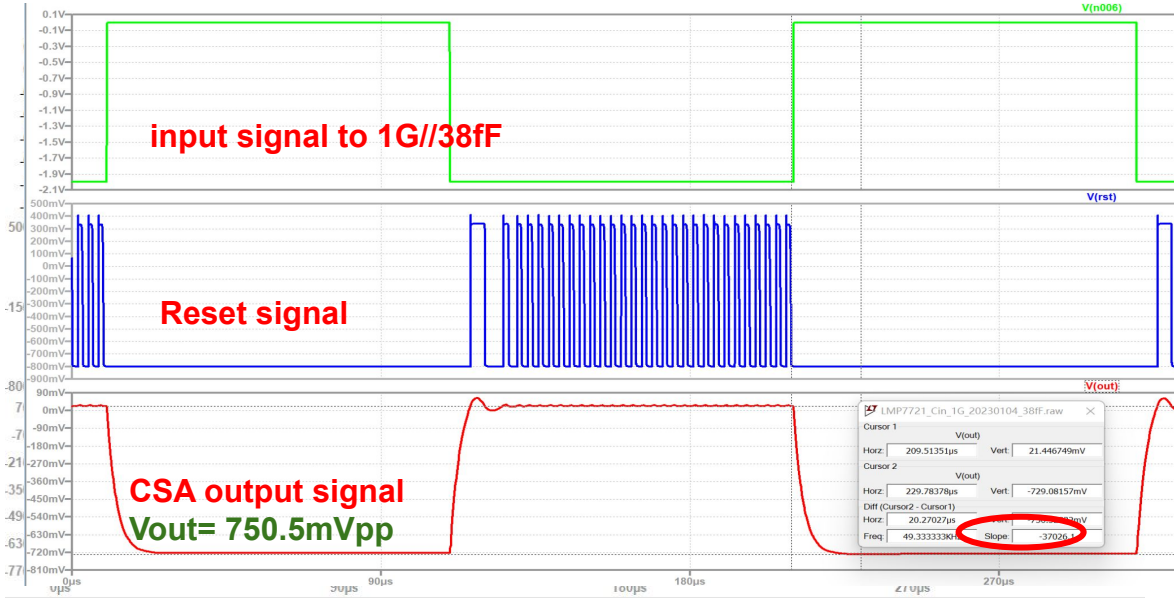
RTD is a zero-suppression data reduction scheme



Parasitic capacitance at input

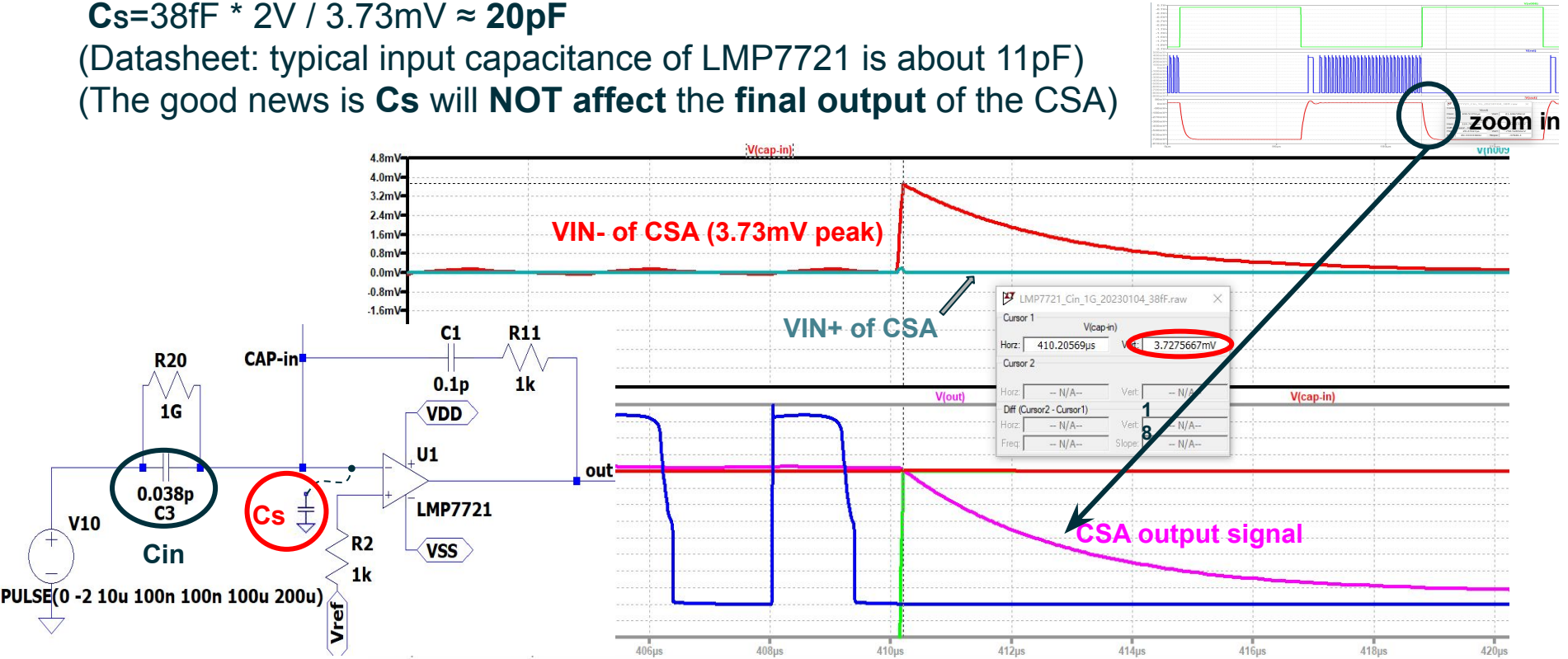
- Charge injection through the input parasitic capacitance (**Cin**) is **NOT** negligible
- Cin mainly comes from the 1G **input resistor**
- Using **square wave** to measure the Cin
- When **Cin=38fF** (Cf=0.1pF) Vin=2Vpp, **Vout=760mVpp**
- **Simulation** results:
  Vout=750.5mVpp





Parasitic capacitance at input

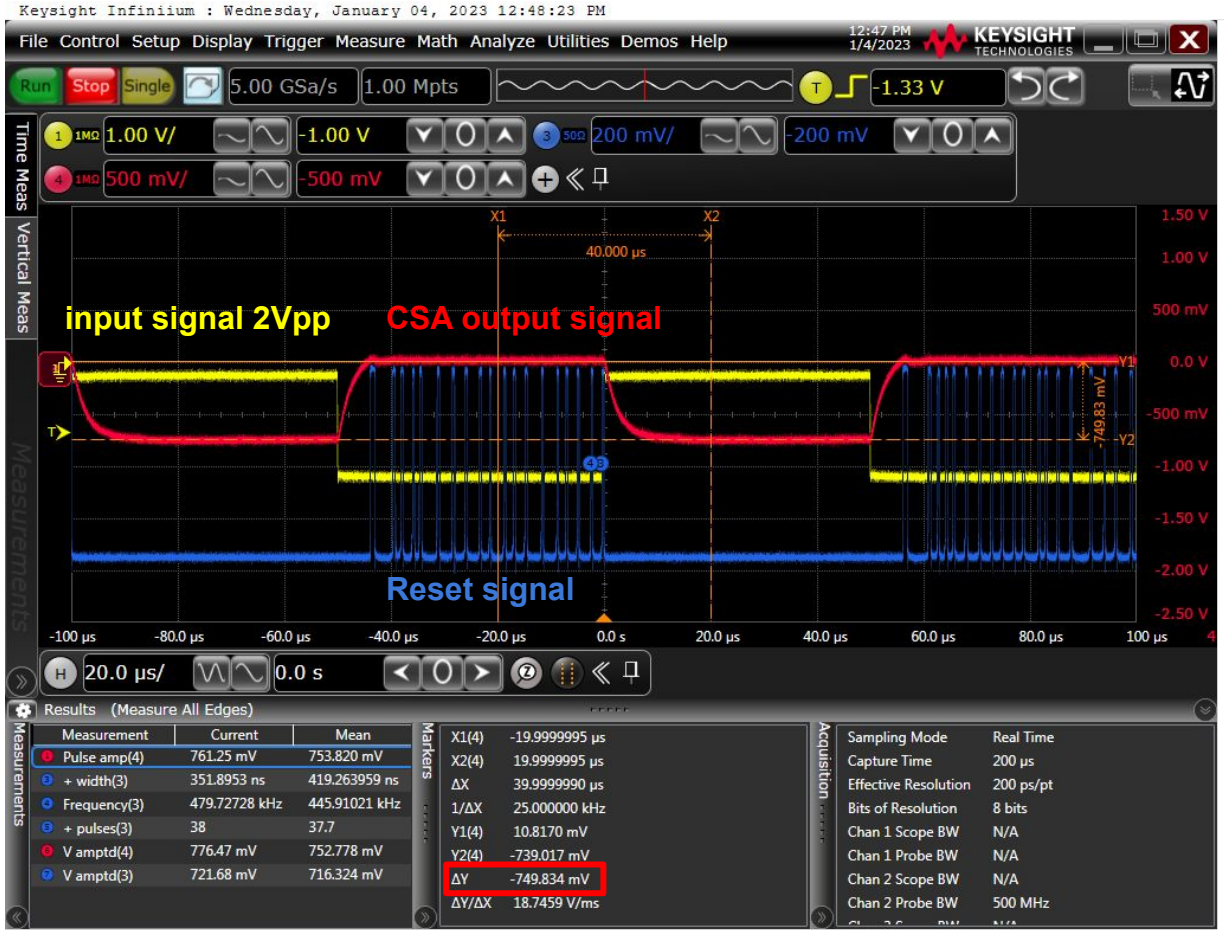
- According to the **simulation** results, the **total** parasitic capacitor of **CSA's input** is:
  Cs=38fF * 2V / 3.73mV ≈ **20pF**
  (Datasheet: typical input capacitance of LMP7721 is about 11pF)
  (The good news is **Cs** will **NOT affect** the **final output** of the CSA)



Parasitic capacitance at input

- Test results:
- Cf = 0.1pF
- Vin = 2Vpp
- Vout= 749.834mVpp
- **=> Cin≈38fF**

- Output signals and Vout value consistent with the simulations



Summary

- Demonstrated Q-Pix front-end with commercial discrete OpAmp and ASIC MOS transistors
- At the relevant current, voltage, and frequency* levels
- Fully match circuit simulation with measurement
- The only fidelity-compromising factor is the parasitic capacitance on injection resistor
- Q-Pix front-end in the charge replenishment configuration is a first-order Sigma-Delta modulator
- The noise shaping nature allows lower frequency (bitrate) operation at the same SNR after digital filter compared to naive RTD waveform reconstruction