In-silicon testing results of the AFE on the 28 nm LDRD chip (PEBBLES)

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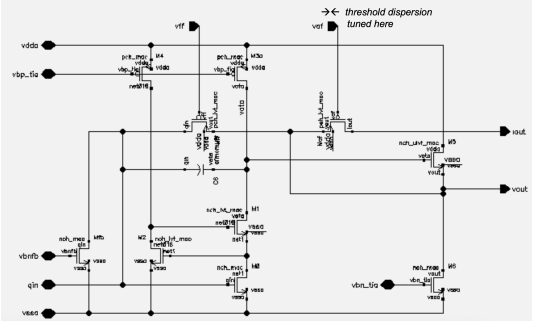
Lawrence Berkeley National Laboratory

Sep 29, 2023
Weekly Instrumentation Meeting

LBNL 28 nm LDRD

- 28 nm CMOS is a strong node for HEP in the near and long future:
  - Smaller size (compared to 65 nm and above): higher density, lower power, higher speed
  - Radiation hardness of 28 nm is also better than other nodes (130, 65, 40 and 22 nm)
- LBNL 28 nm LDRD goals: develop expertise in TSMC 28nm technology, and develop building blocks that are useful for multiple divisions (physics, nuclear ...)
  - Main goal: design and test a fast AFE with low noise and low power, plus a high precision and low power in-pixel TDC, for future 4D pixel applications
- We have two submissions in 2022 and one submission in 2023:
  - "BigRock": submitted in Feb 2022
    - 32 channels of AFE + testbed TDC, CML receiver + driver
  - "PEBBLES": submitted in May 2022, chip received Oct 2022
    - Added new blocks: voltage reference, MUX
    - "Alive" tests done Feb 2023, full tests done Sep 2023
  - "METAROCK": submitted in July 2023
    - Added the in-pixel TDC in the chip (+ other blocks)

The Analog Front End

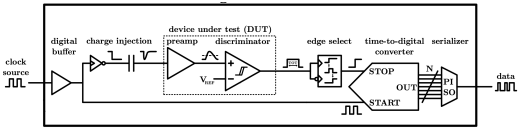


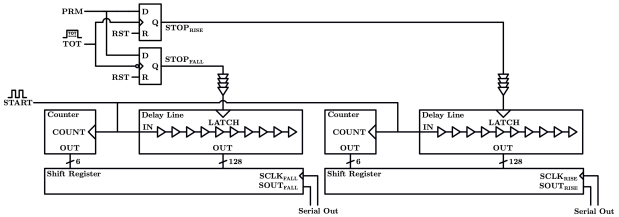
1. Pierre Jarron, et. al, *A transimpedance amplifier using a novel current mode feedback loop, 1996*

- We want a low noise and high speed amplifier
- Traditional charge sensitive amplifier (CSA, $Q \rightarrow V$): noise low, but not very fast rise time
- Transimpedance amplifier (TIA, $I \rightarrow V$): very fast pulse, but noise is also high (mainly from thermal noise of R_f)
- TIA with active feedback: use MOS devices on feedback to avoid thermal noise (not an actual resistor)
- In our amplifier design, a supplementary current output (with current amplification) is also provided (and actually used)
- Specs: $\sigma_t \sim 50$ ps , ENC$<$ 100 e, 10x30 μm, $\sim 5\mu$W

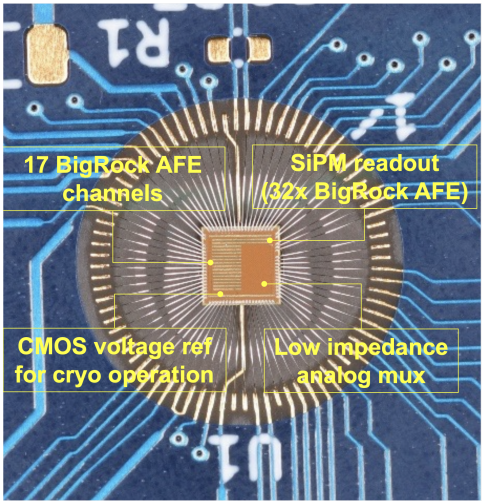
On-chip testbench for the AFE

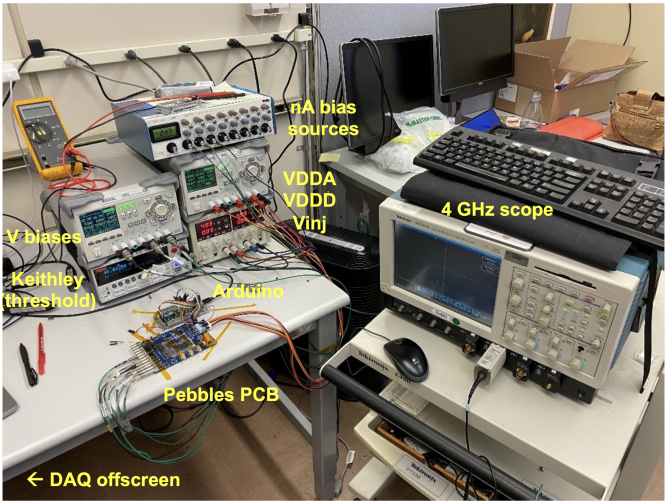
- We want to test the noise and timing performance of the AFE with testbench inside the chip (without using fast scope)
- The noise measurement is achieved by using the in-chip charge injection circuits
  - Apply a step voltage on capacitor with known capacitance ($\pm 25\%$)
- The timestamp is measured by delay-line based TDCs placed in the chip
  - Two delay lines, one for rising edge timestamp, one for falling edge timestamp
  - The TDC precision is dominated by the LSB, which is the delay time of one delay cell
  - Specs: $\sigma_t \sim 10$ ps, 50x475 μm, ~ 35 mW



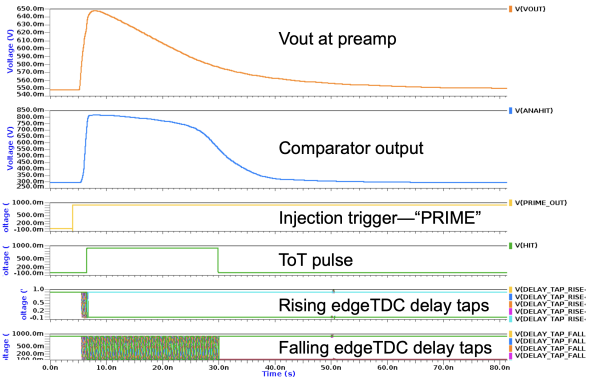


Test setup

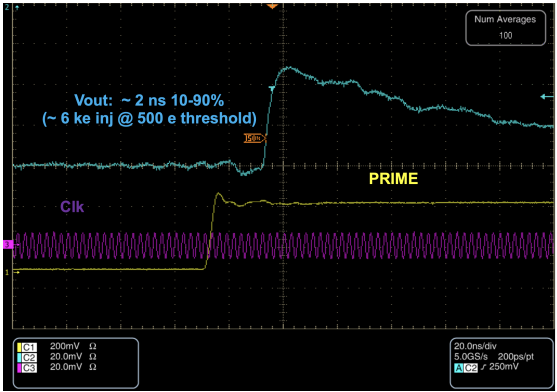

17 BigRock AFE channels
SiPM readout (32x BigRock AFE)
CMOS voltage ref for cryo operation
Low impedance analog mux


nA bias sources
VDDA
VDDD
Vinj
4 GHz scope
V biases
Keithley (threshold)
Arduino
Pebbles PCB
← DAQ offscreen

AFE output signals

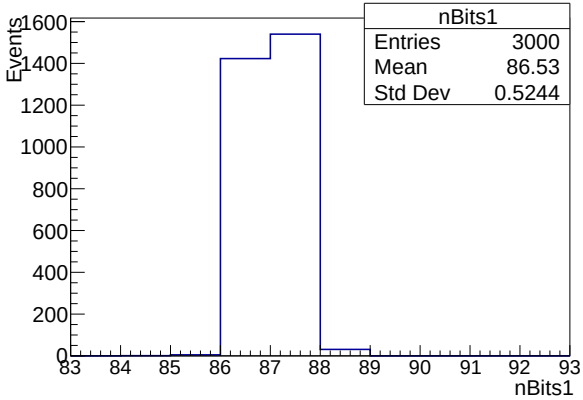


Simulation



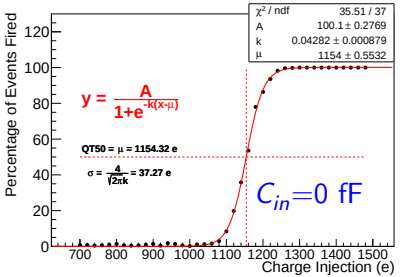
In-silicon

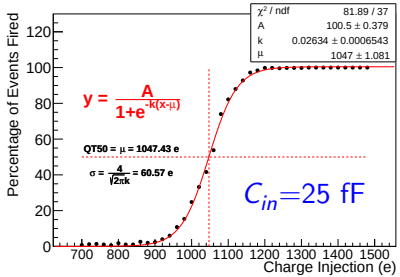
Testbench TDC performance

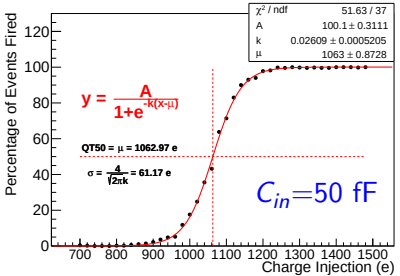


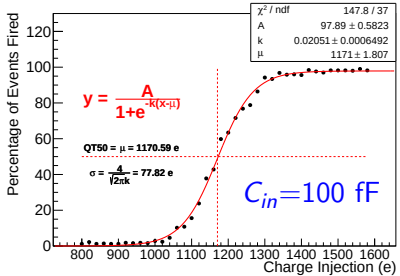
- With 528 MHz clock ($T_c = 1.89$ ns), measure the number of 1s and 0s in the delay line in a complete clock cycle: 86.53
- This gives us the TDC LSB = $T_c/86.53$ =21.89 ps

Noise measurements

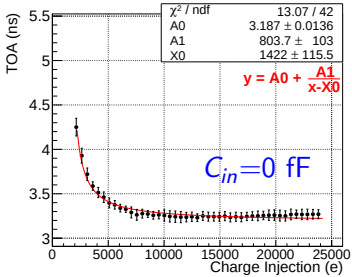


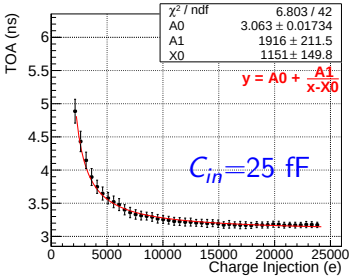


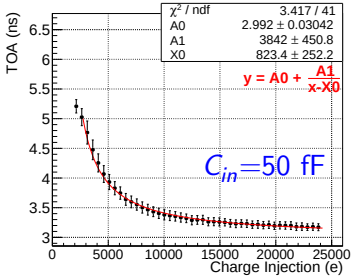


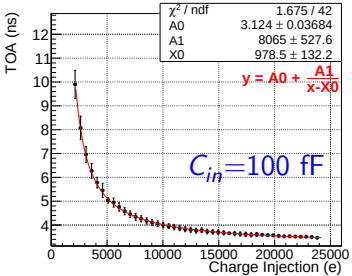


TOA vs. Charge Injection

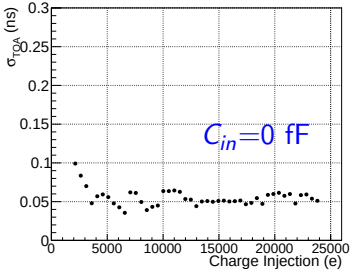


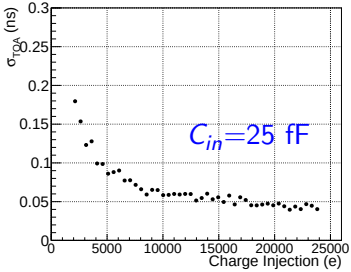


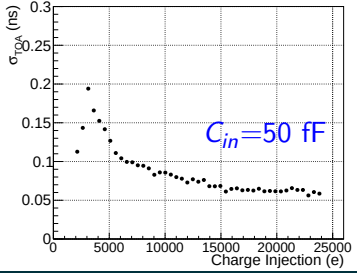


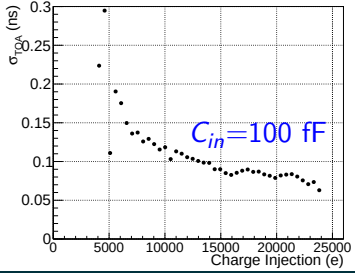


TOA resolution vs. Charge Injection

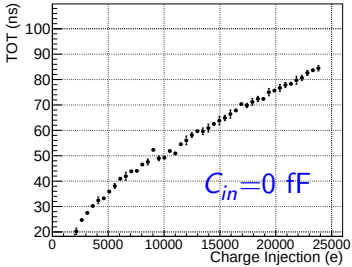


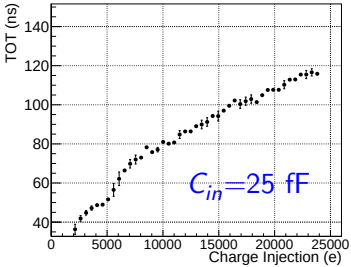


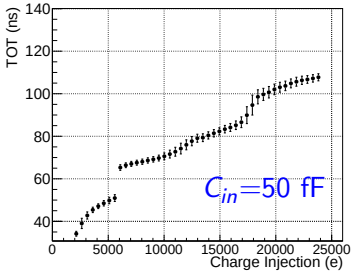


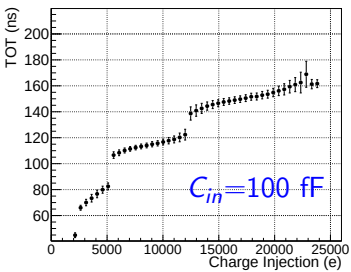


TOT vs. Charge Injection

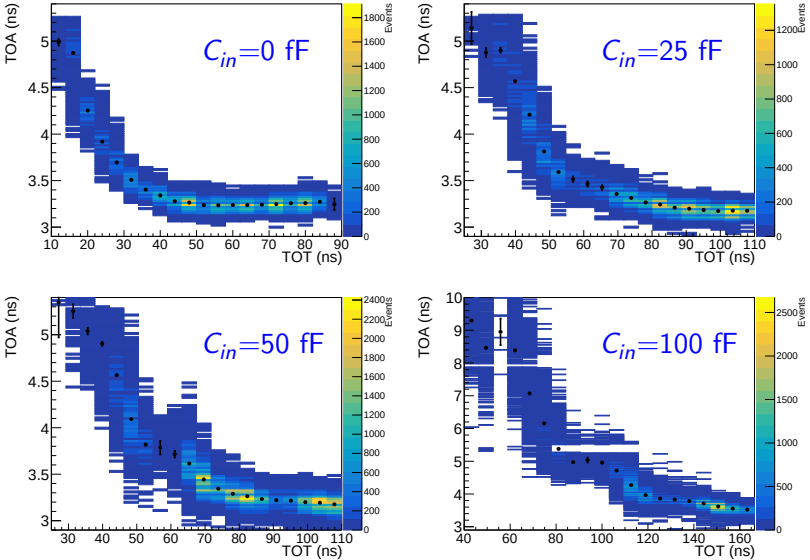




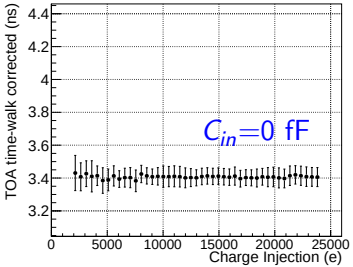


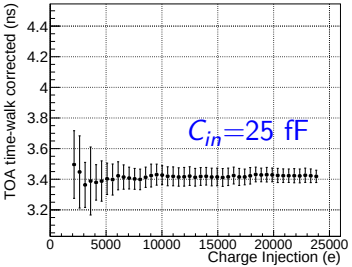


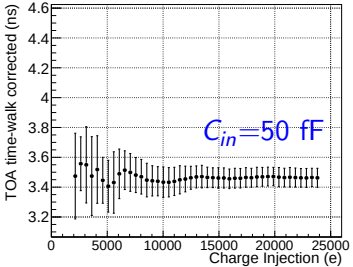
TOA vs. TOT: time-walk correction

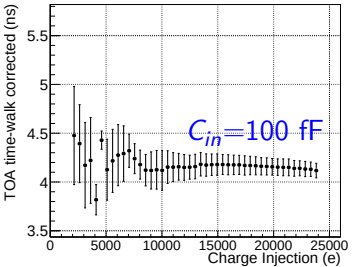


TOA vs. Charge Injection after time-walk









Summary

- First-ever AFE with $<$100 e ENC and $<$100 ps time resolution and $\sim 5\mu$W power consumption
- In-silicon test results look promising, for 50 fF input capacitor:
  - ENC$\sim$ 60 e
  - $\sigma_t \sim 50 - 100$ ps for $>$ 5000 e charge injection
  - About 2 ns time-walk from 2k to 25k charge injection
- Results will be presented in TWEPP 2023 next week
- Stay tuned for our next submission (METAROCK), in which an in-pixel TDC with $<$100 ps time resolution and $< 5\mu$W power consumption is implemented!

Backup slides