Disconnected bump analysis in Module-QC tools

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LBNL Instrumentation meeting

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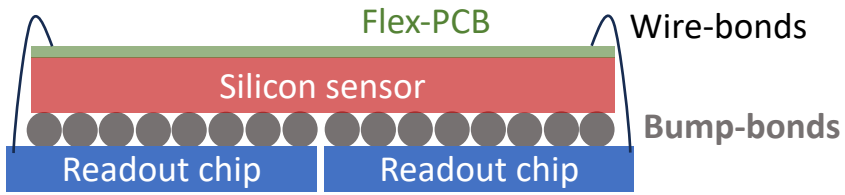
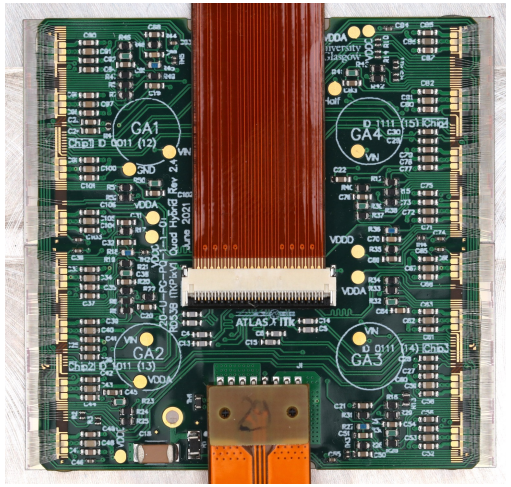
Context

- In Module QC we have a **pixel failure analysis**, which checks the electrical functionality of each pixel on the readout chip.

- We are expanding the pixel failure analysis **(full pixel failure test)** to check also for disconnected bumps



(Not to scale)



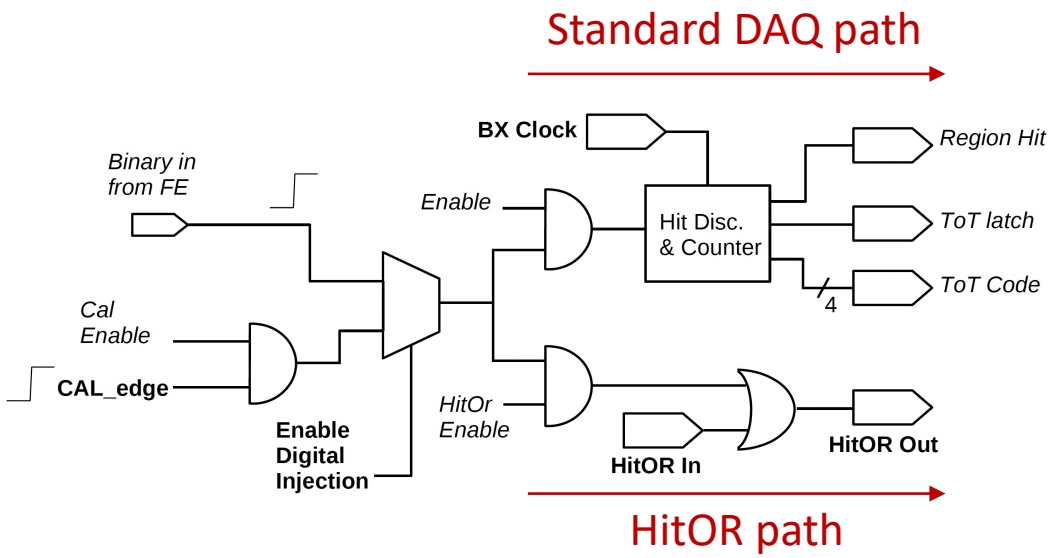
- We have 153600 pixels in each chip, and we expect chips to have less than 0.4% of disconnected bumps (600) after thermal cycling

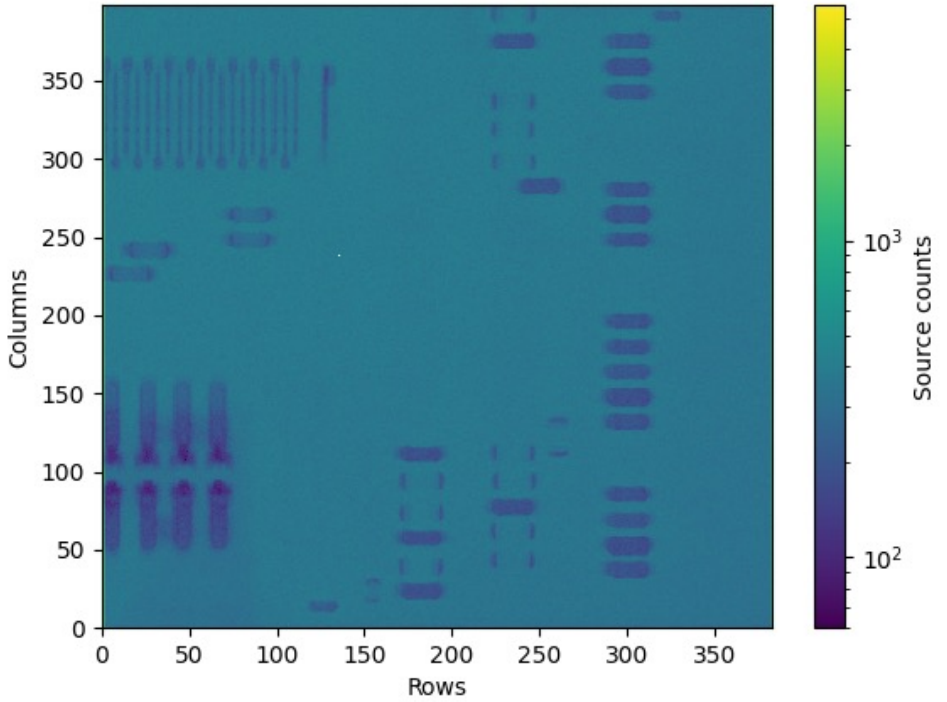
Methods

How to identify disconnected bumps?

1) **Source scan**

- Place module in front of source – we expect connected pixels to detect particles from source
- Complication #1: It takes time (depending on source and material on flex) and complicates setup
- Complication #2: Source scan uses HitOR path → separate from DAQ path (used for data-taking) and prone to its own problems



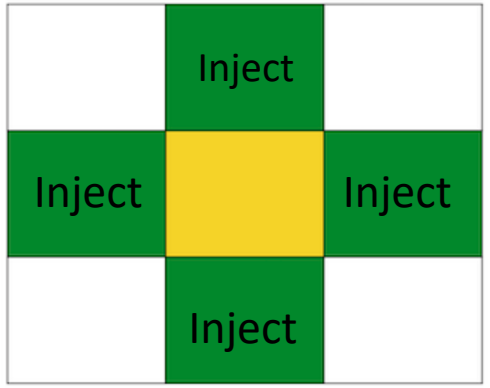


Methods

How to identify disconnected bumps?

2) Disconnected bump scan

- Connected pixels should have cross-talk with neighboring pixels
- Inject large charge in neighboring pixels – check for hits in central pixel
- Complication #1: Some sensor / pixel types of low cross-talk → difficult to inject enough charge to see hits on central pixel
- Complication #2: Edge pixels or pixels with broken neighbors have fewer neighboring pixels which we can inject charge into



3) Zero-bias scan

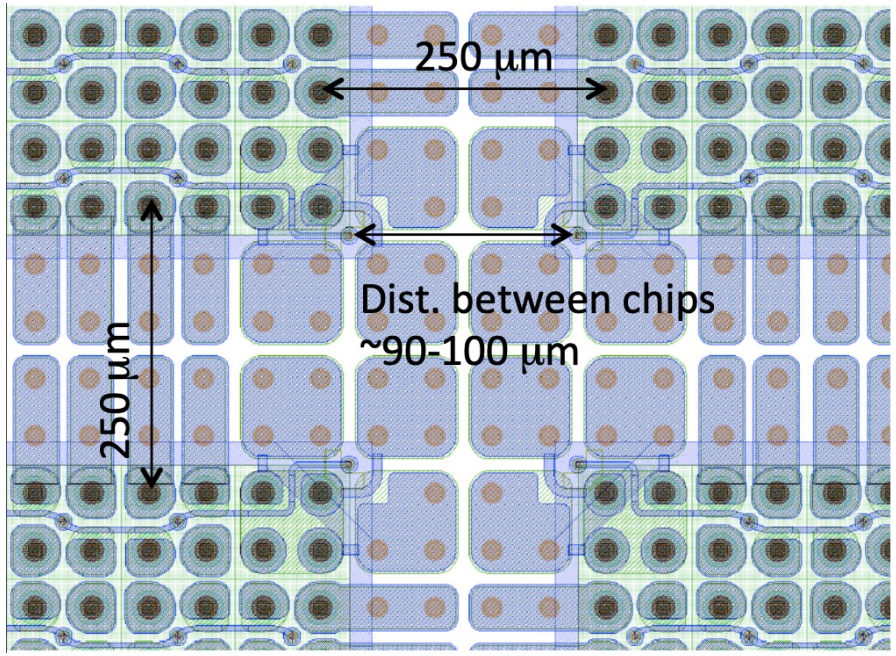
- Connected pixels should have larger noise difference when HV is applied / not applied
- Complication #1: Separation in noise difference is not clear between connected and disconnected pixels

Module and sensor types

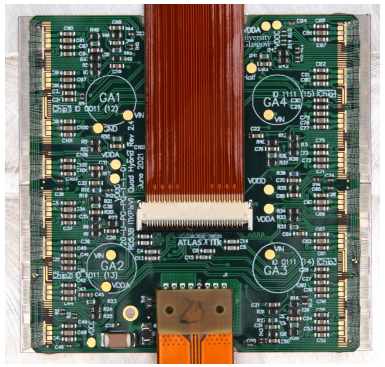
Goal is to make a procedure which takes into account all three methods, and can be used with or without source scan

We have several variations in module types, which may impact optimal algorithm:

1. Quads vs. triplets
2. Sensor type (planar vs. 3D, vendor)
3. Location of pixel on the module (edge vs. matrix)
4. Pixel size (50 x 50 µm vs. 25 x 100 µm)

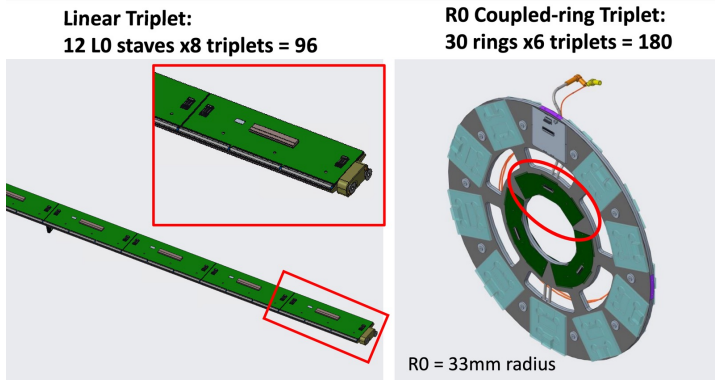


In quad modules, we expect inner-edge and outer-edge pixels to behave differently, because size of silicon pixels differ



Quad module – 4 chips bump-bonded to single sensor

Triplet module – 3 chips bump-bonded to 3 sensors



The plan

Ideally we would have one of each module type available to study. We don't have that.
We have:

1. **Advacam Micron Planar** (quad module) (20UPGM22001172)
2. **HPK planar** (quad module) (20UPGM21301089)
3. IZM Sintef 3D (single chip card)
4. FBK 3D (single chip card)

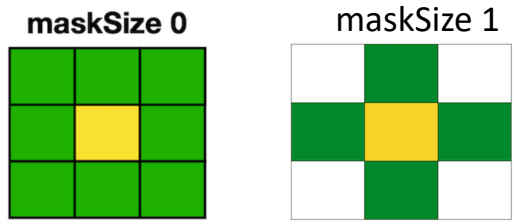
These modules do not provide enough data to come up with fancy algorithm to identify disconnected bumps.

Instead I implemented a **basic disconnected bump analysis in module-qc-tools**, so that we can crowd-source collection of data and use this to make a better-informed algorithm.

We also want to understand how well the non-source scans alone can identify disconnected bumps – if possible we could run source scans batch-wise in production.

Procedure

Baseline procedure:



B.10.3.2 Full Pixel Failure Test

- Disconnected bump scan
- Merged bump scan @ 1000e (L0) or @1500e (L1/L2)
- Threshold scan with no bias
  - Turn off HV
  - Re-tune chips to 1000e (L0) or 1500e (L1/L2)
  - Threshold scan (high def, low range)
  - Turn on HV
  - Re-tune chips to 1000e (L0) or 1500e (L1/L2)
- Source scan
  - Obtain at least 10 hits on connected pixels (setup dependent)

Several small changes to YARR scans MR666:

- Change default mask size (0) and don't mask pixels after disconnected bump scan
- Add two merged bump scans:
  - One for 1000e and 1500e tuning
  - Similar to disconnected bump scan but injecting less charge

Re-tuning for 0-bias scan is a pain. Consider dropping? Need to check impact on results…

Details on my setup in a bit

Procedure

User needs to supply the following scans to run a pixel failure analysis:

1. Digital scan
2. Analog scan
3. Threshold scan (high-def)
4. Noise scan
5. Disconnected bump scan
6. Merged bump scan
7. Threshold scan (0-bias, high-def)
8. Source scan

If any of these scans are missing, the analysis will still run but the module will fail QC

→ Module may pass QC is this test is missing

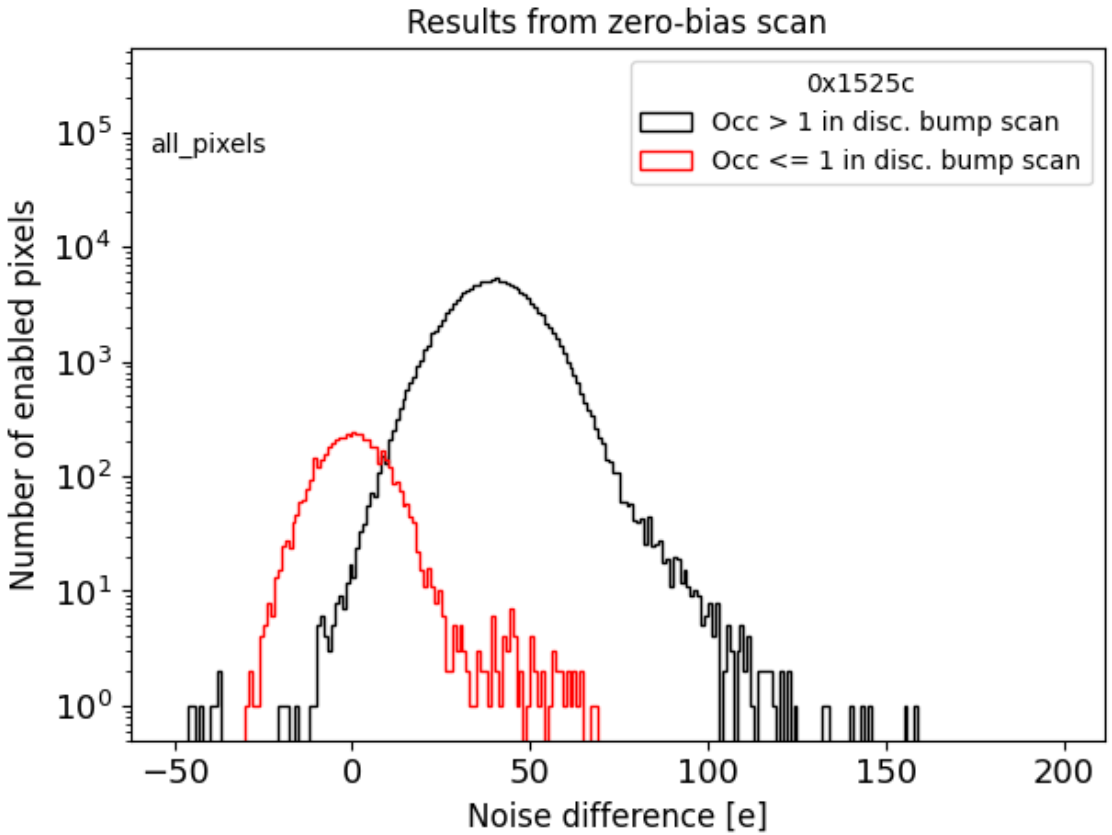
QC selection

These selection are applied on each pixel, and the number of pixels failing each are stored in the output file

Selection name (prodDB)	
MERGED_BUMPS	Pixel fails if more than 50 hits / 100 injections, and is paired next to another failing pixel
DISCONNECTED_BUMPS_ZERO_BIAS_SCAN	No selection, just diagnostic plots
DISCONNECTED_BUMPS_XTALK_SCAN	Pixel fails if occupancy <= 1
DISCONNECTED_BUMPS_SOURCE_SCAN	Pixel fails if occupancy <= 10
DISCONNECTED_PIXELS	Pixel fails if it fails x-talk **or** source requirements

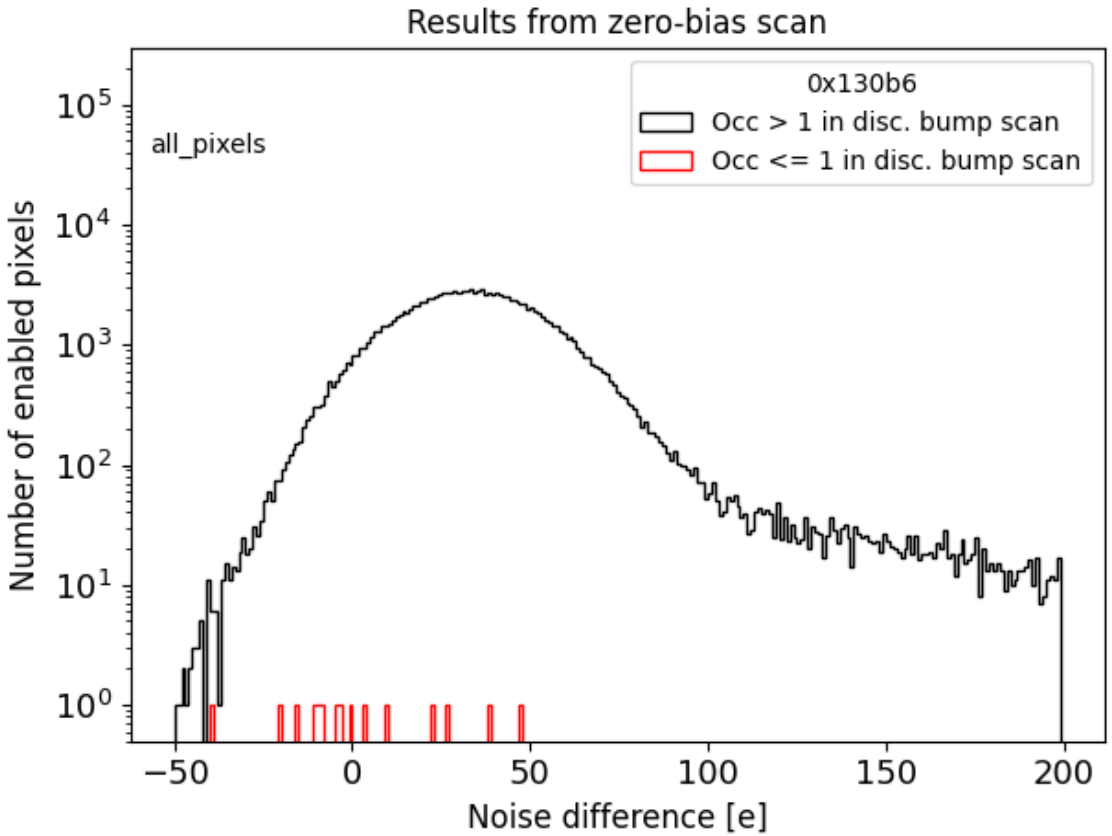
Results – zero-bias scan

One chip from Advacam micron:



Some correlation of the noise difference with the disconnection; however separation is not clear

One chip from HPK:

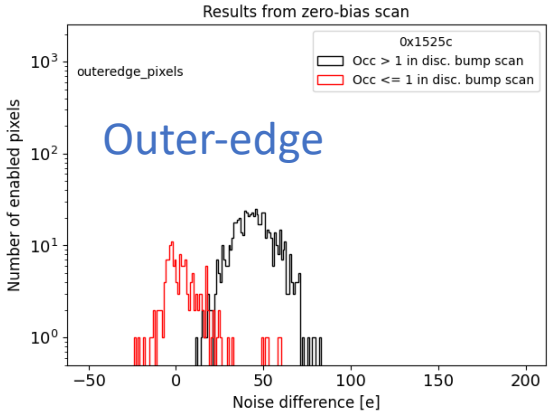


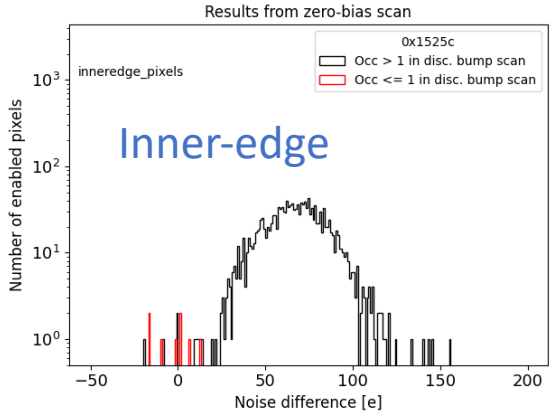
HPK has higher noise; Noise-difference of connected pixels not far enough away from 0

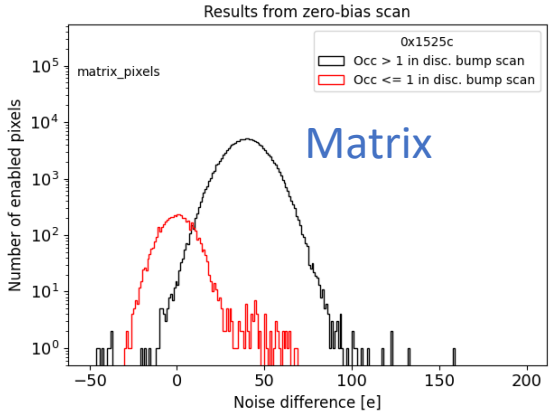
Results – zero-bias scan

* Module SN and chip ID used to distinguish between inner and outer edge pixels

One chip from Advacam micron:

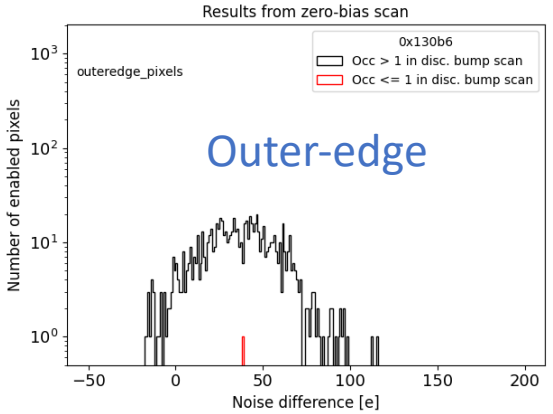


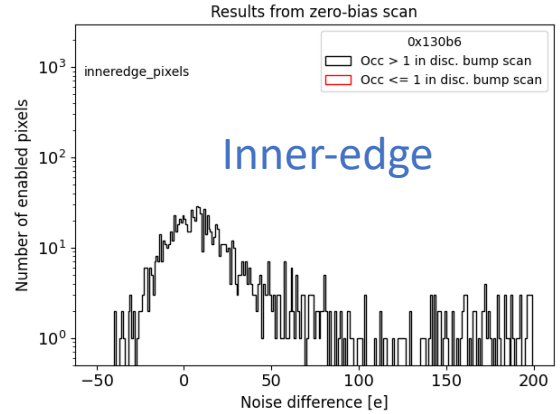


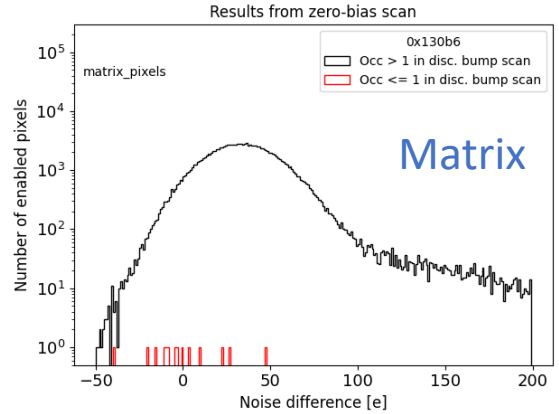


Noise difference slightly higher for inner-edge pixels

One chip from HPK:







Noise difference slightly higher for outer-edge pixels

Source scan setup

My procedure for running source scan is:

- Digital scan with clean mask
- Analog scan
- Noise scan (1 minute)
- Source scan for 1 hour

} Not needed if running source scan immediately after other electrical pixel failure scans (these are included)

Using Americium-241 and ”default” source-scan parameters:

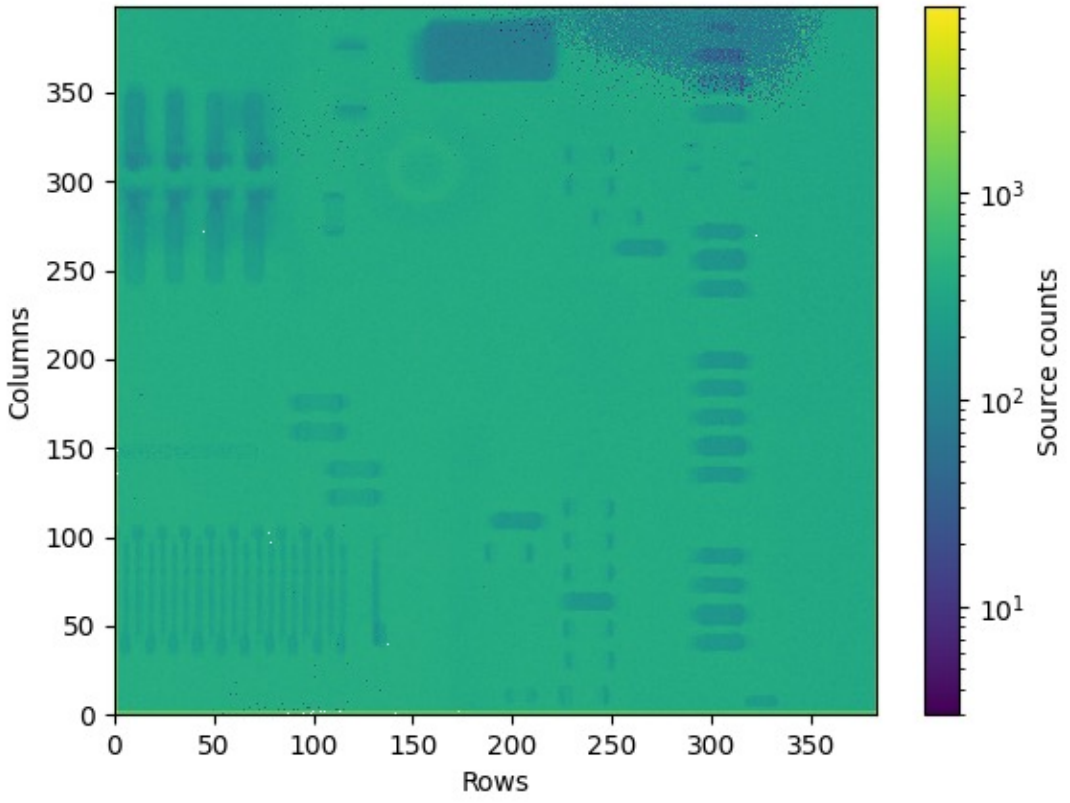
```
{
  "config": {
    "count": 0,
    "delay": 56,
    "extTrigger": false,
    "frequency": 0,
    "noInject": true,
    "time": 300,
    "edgeMode": false
  },
  "loopAction": "Rd53bTriggerLoop"
```

```
  "name": "Selftrigger",
  "prescan": {
      "InjVcalDiff": 0,
      "InjDigEn": 0,
      "Latency": 57,
      "SelfTrigEn": 1,
      "SelfTrigDigThrEn": 1,
      "SelfTrigDigThr": 1,
      "SelfTrigMulti": 4,
      "SelfTrigDelay": 45
  }
```

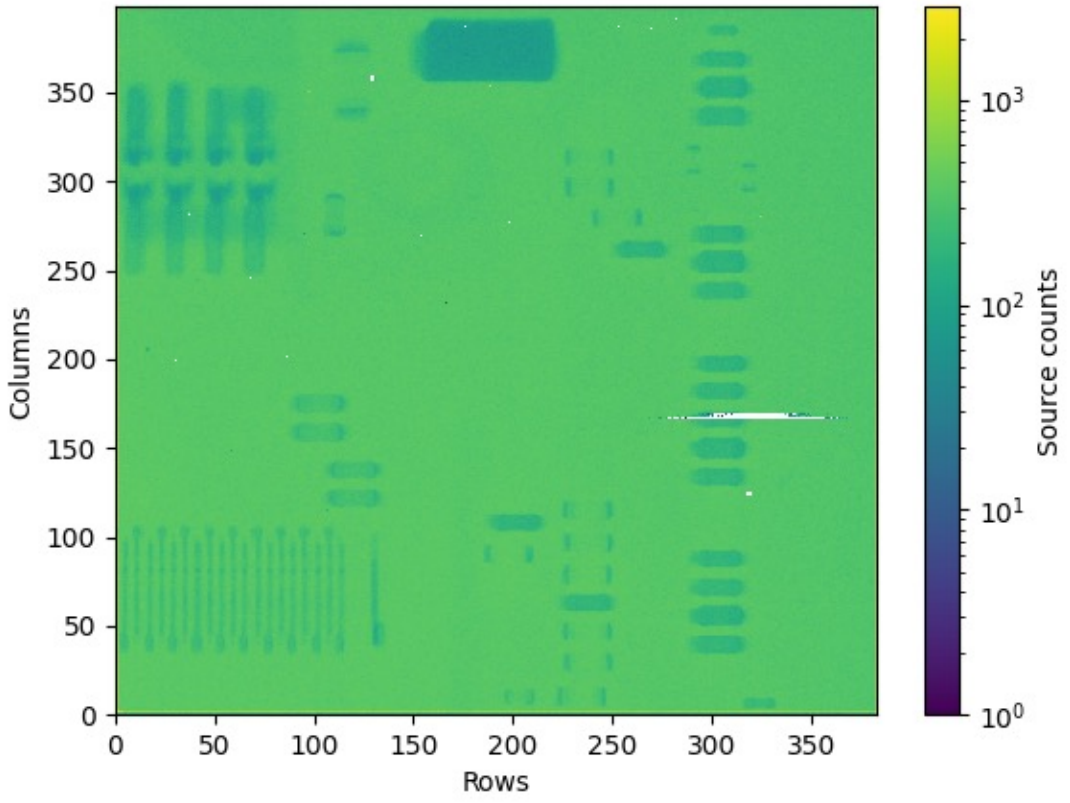
Mask applied during source scan is checked for consistency with electrical failures

Results – source scan

One chip from Advacam micron:

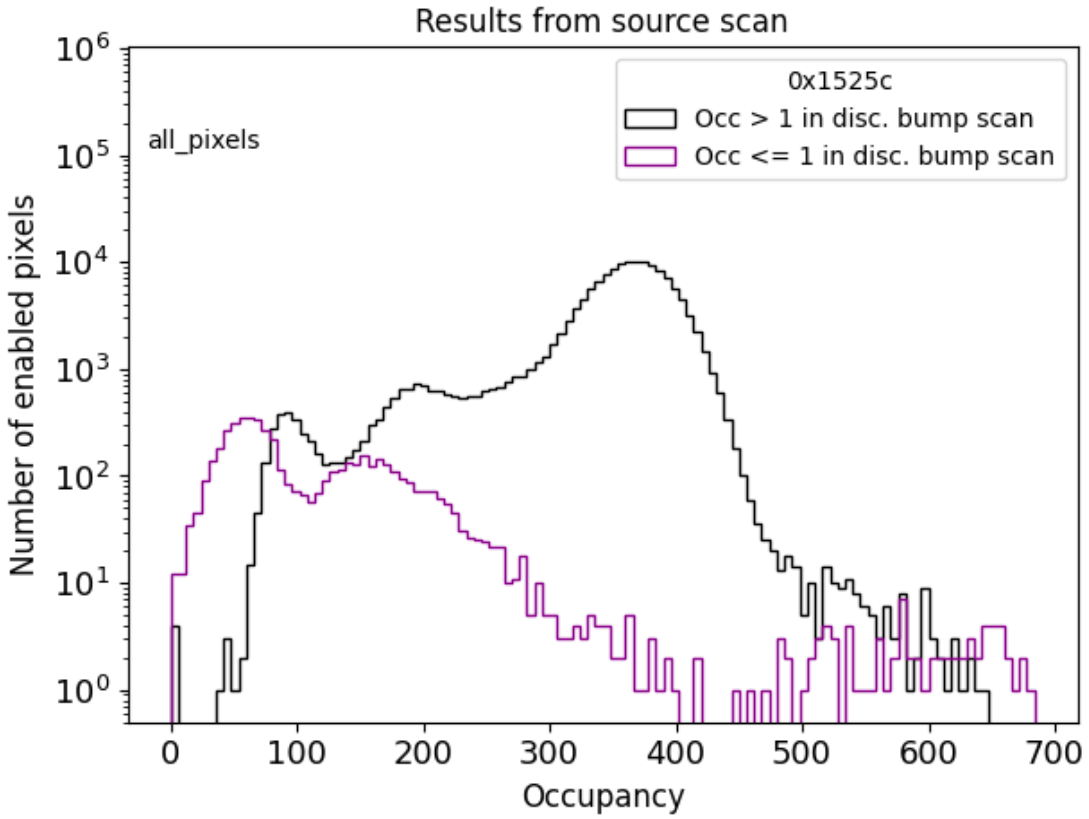


One chip from HPK:

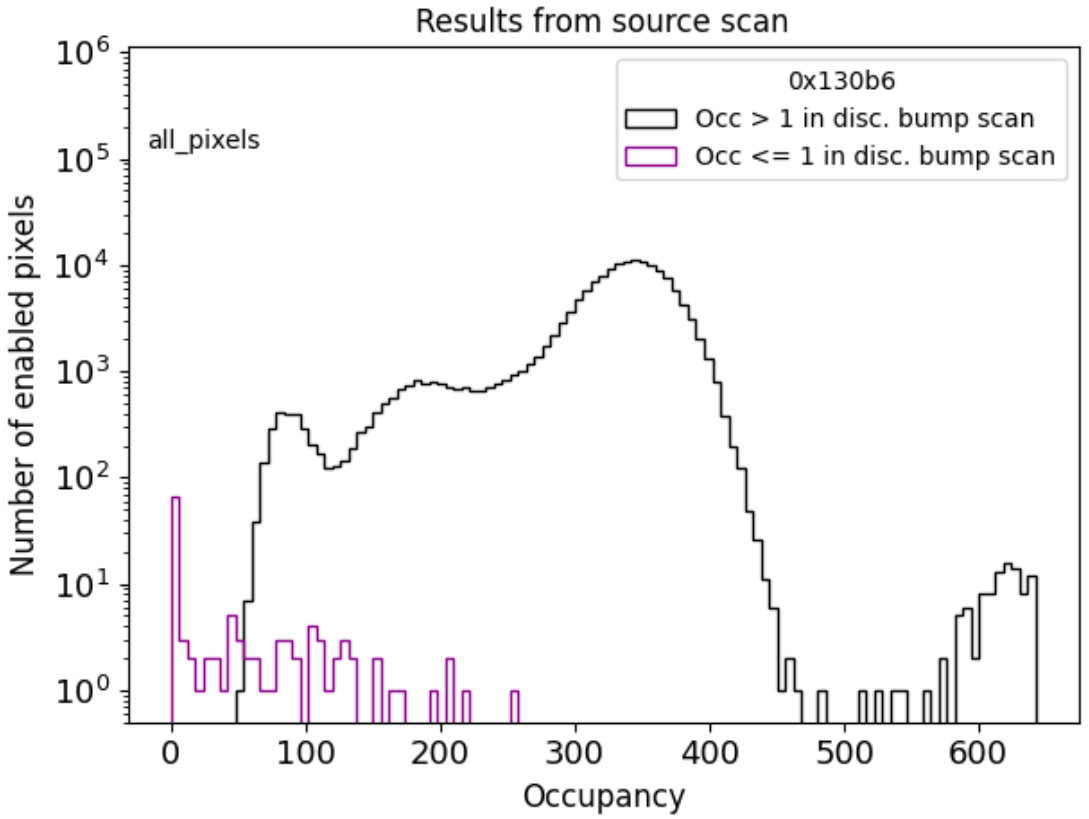


Results – source scan

One chip from Advacam micron:

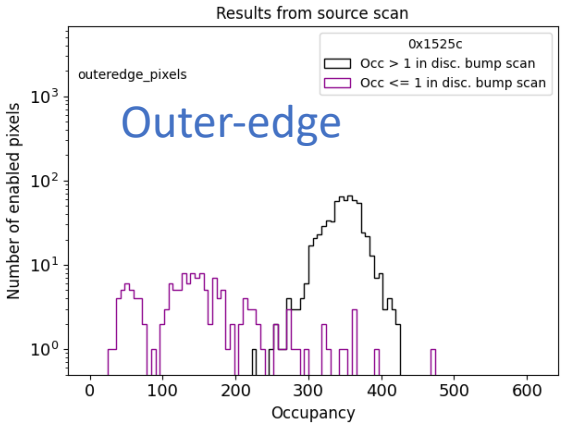


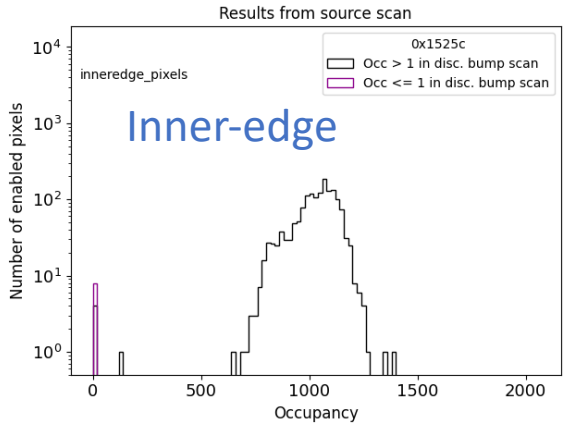
One chip from HPK:

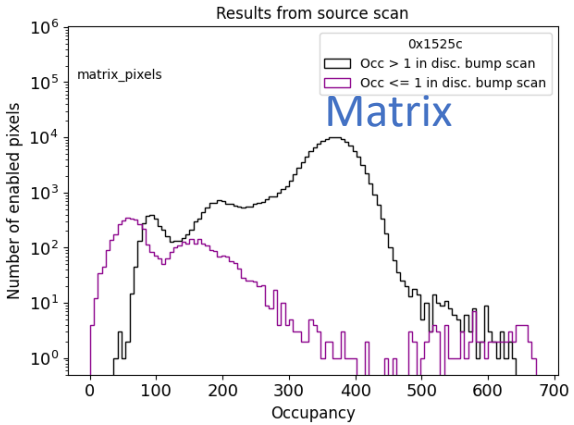


Results – source scan

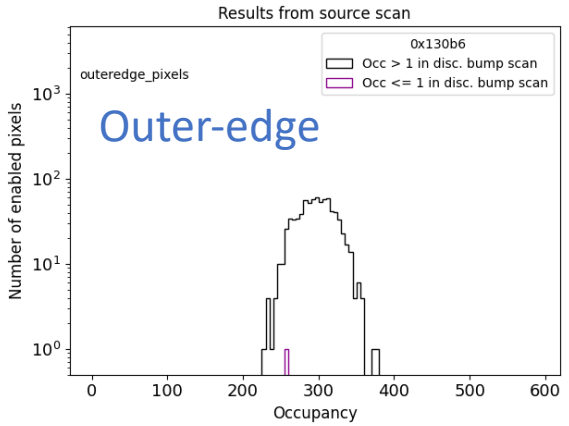
One chip from Advacam micron:

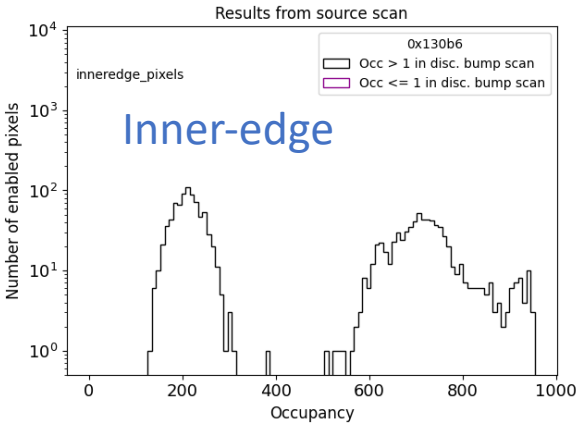


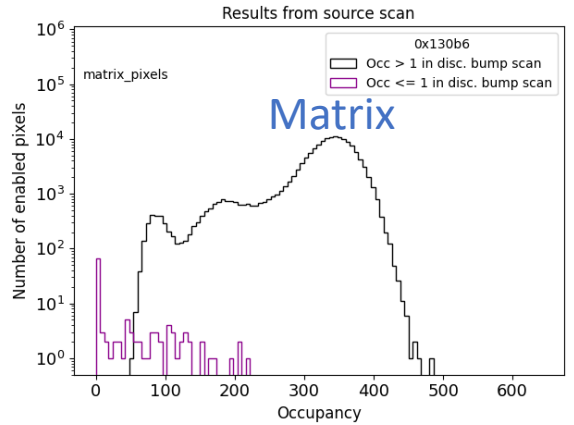




One chip from HPK:



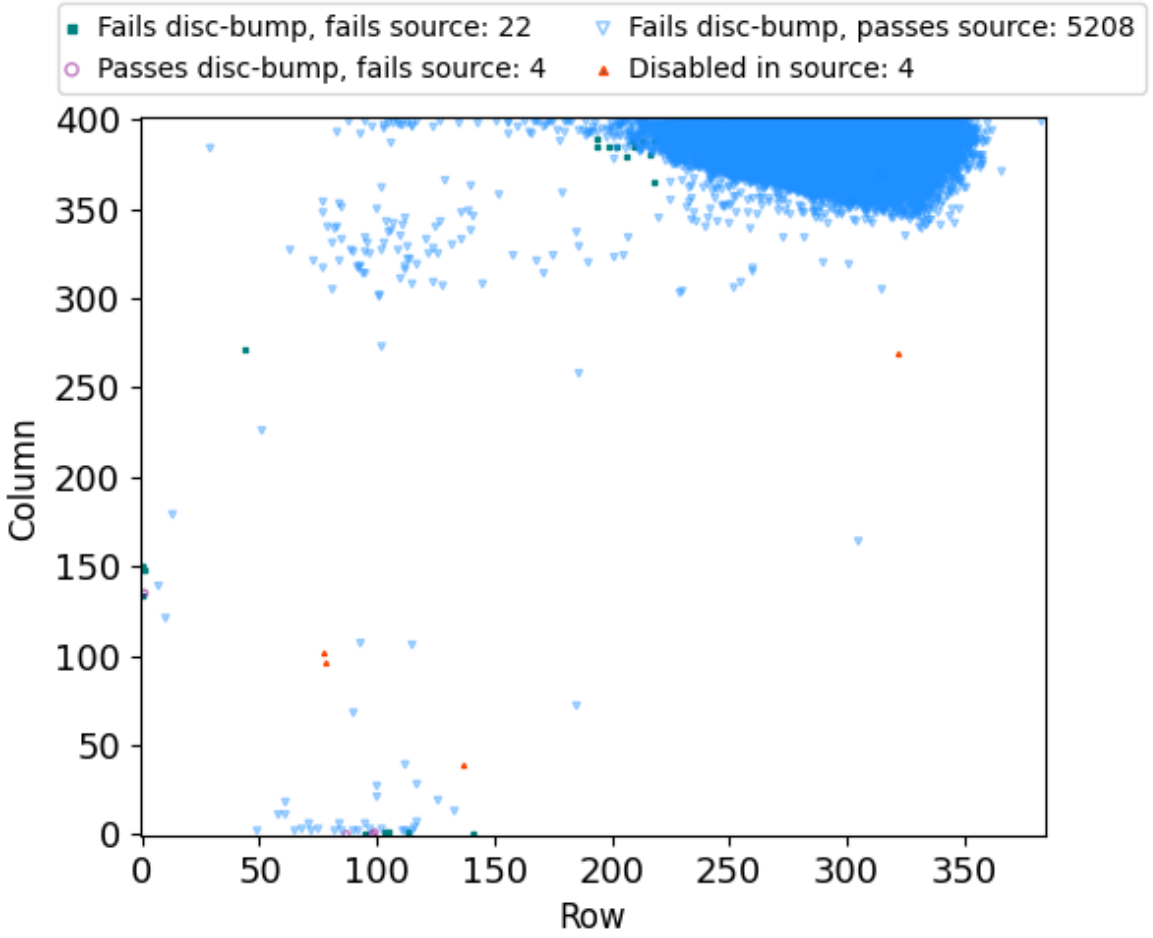




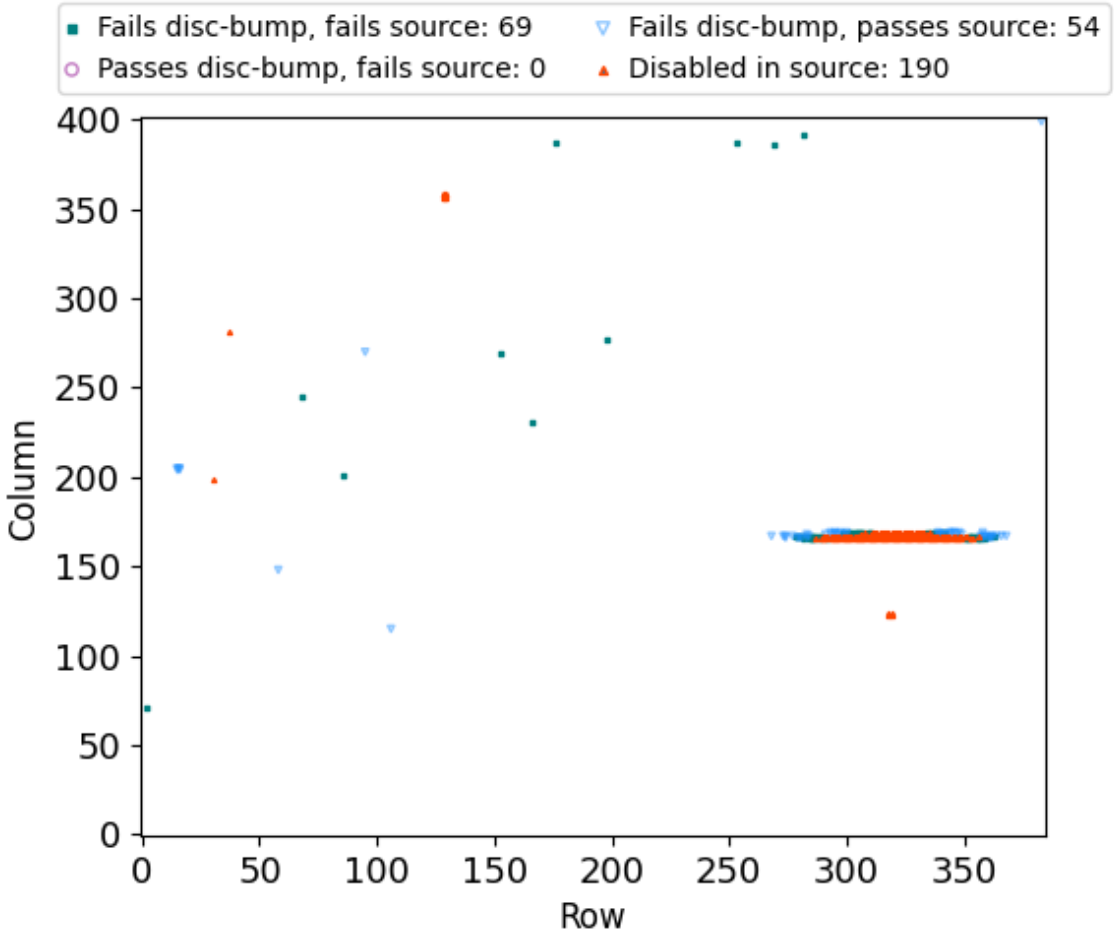
I am surprised by the difference in # of source scan counts between inner-edge pixels – is pixel sensor geometry is different in Advacam and HPK?

Results – source scan vs. disconnected bumps

One chip from Advacam micron:

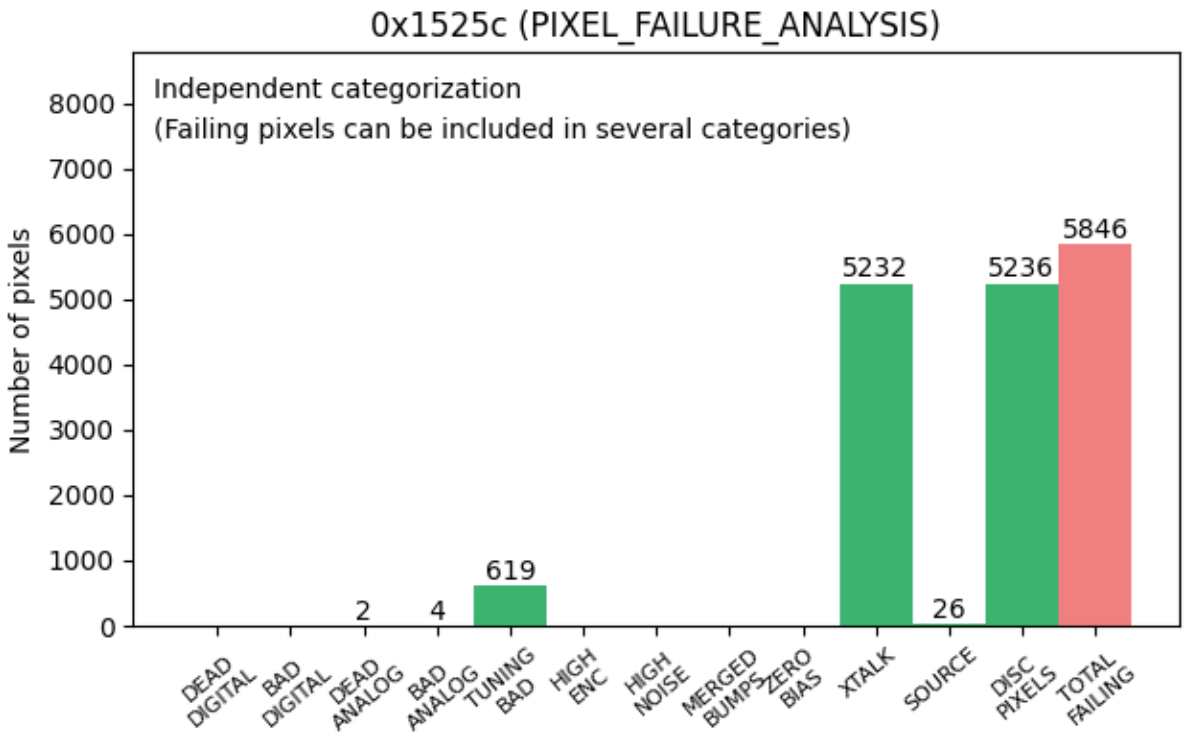


One chip from HPK:

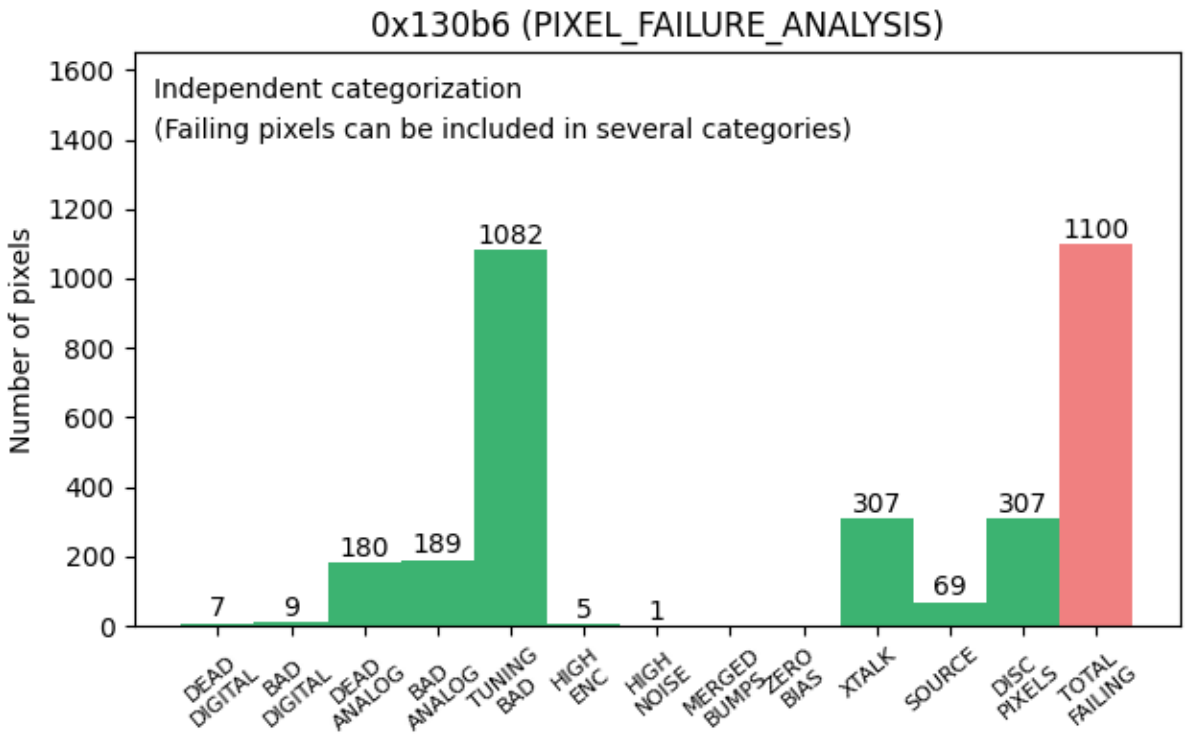


QC-results

One chip from Advacam micron:

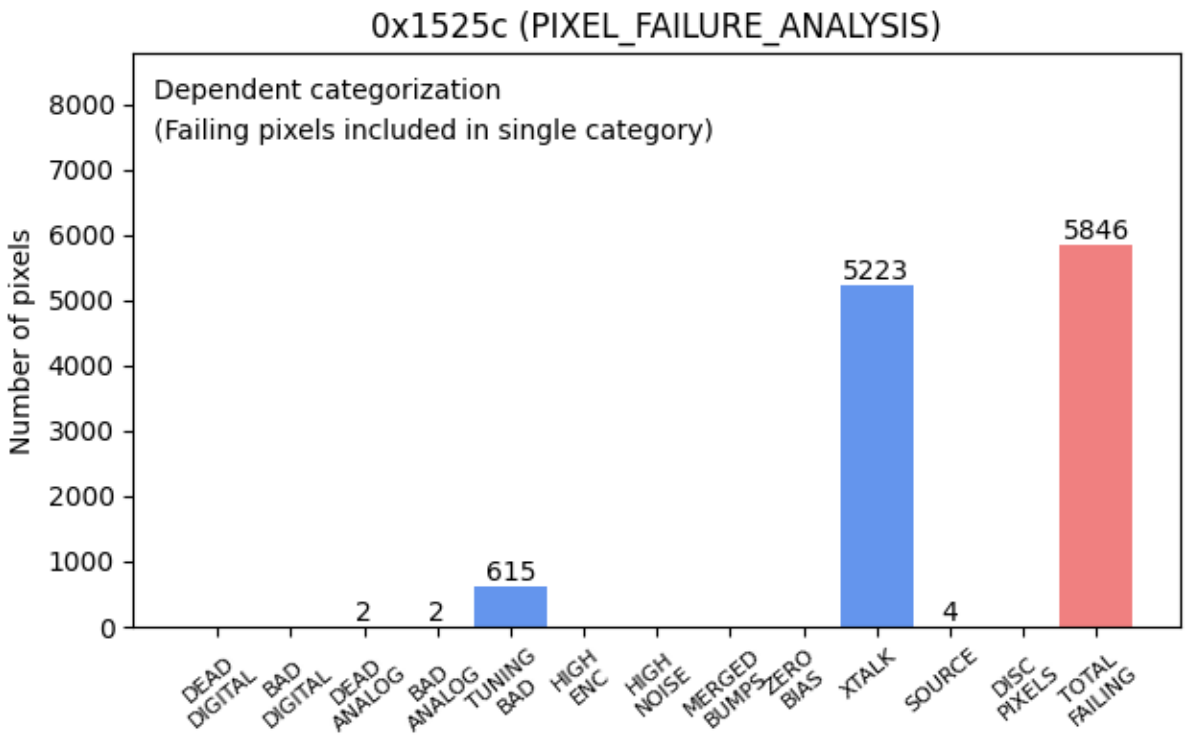


One chip from HPK:

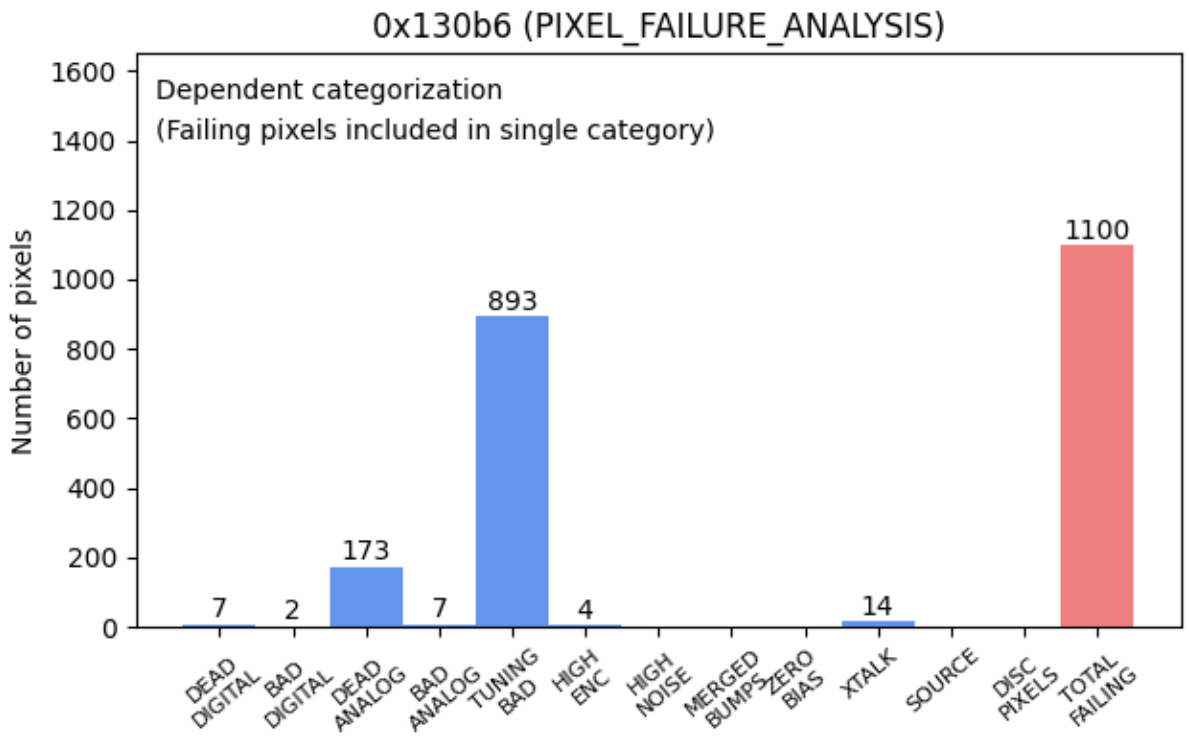


QC-results

One chip from Advacam micron:



One chip from HPK:



QC-results

One chip from Advacam micron:

PIXEL_FAILURE_ANALYSIS for 0x1525c

Parameter	Analysis result	QC criteria	Pass
ELECTRICALLY_FAILED	619	[0, 154]	False
DISCONNECTED_PIXELS	5236	[0, 600]	False
FAILING_PIXELS	5846	[0, 600]	False

One chip from HPK:

PIXEL_FAILURE_ANALYSIS for 0x130b6

Parameter	Analysis result	QC criteria	Pass
ELECTRICALLY_FAILED	1086	[0, 154]	False
DISCONNECTED_PIXELS	-1	[0, 600]	False
FAILING_PIXELS	-1	[0, 600]	False

(Missing scan → automatically fails (-1))

These both look really bad because of the poor tuning

DISCONNECTED_PIXELS includes merged bump analysis

FAILING_PIXELS = ELECTRICALLY_FAILED or DISCONNECTED_PIXELS

The QC document we have now states that:

- Number of electrical failures after module assembly is < 0.1 % (154 pixels)
- Number of disconnected bumps after thermal cycling is < 600
- Right now chip will fail QC if it has more than 154 electrical failures, but less than 600 total failing pixels…

Output file

These are the variables stored in the output file:

"PIXEL_FAILURE_DEAD_DIGITAL": 0,
"PIXEL_FAILURE_BAD_DIGITAL": 0,
"PIXEL_FAILURE_DEAD_ANALOG": 2,
"PIXEL_FAILURE_BAD_ANALOG": 2,
"PIXEL_FAILURE_TUNING_BAD": 615,
"PIXEL_FAILURE_HIGH_ENC": 0,
"PIXEL_FAILURE_HIGH_NOISE": 0,

Dependent categorization (each pixel only categorized with single failure)

"PIXEL_FAILURE_ELECTRICALLY_FAILED": 619, All electrical failures

"PIXEL_FAILURE_SOURCE_SCAN_DONE": 1, Flag if source scan was provided

"PIXEL_FAILURE_MERGED_BUMPS": 0,
"PIXEL_FAILURE_DISCONNECTED_BUMPS_ZERO_BIAS_SCAN": 0,
"PIXEL_FAILURE_DISCONNECTED_BUMPS_XTALK_SCAN": 5232,
"PIXEL_FAILURE_DISCONNECTED_BUMPS_SOURCE_SCAN": 4,

Independent categorization (each pixel could be in multiple categories)

"PIXEL_FAILURE_DISCONNECTED_PIXELS": 5236, → Results from fancy algorithm (for now just OR of XTALK_SCAN or SOURCE_SCAN

"PIXEL_FAILURE_FAILING_PIXELS": 5846 → Number of pixels failing electrically or are disconnected

Other details / new features

- For 4 chips, analysis takes ~30 seconds to run

- Pixel maps store pass/fail criteria of each pixel for every pixel selection criteria. These maps will be used to visualize data on LocalDB and compare results from different tests. Data is stored as 2D (384 x 400) numpy arrays of booleans in a single pickle file. Size of file containing 24 pixel maps is 3.6 MB.

Next few days

- Update documentation on procedure and specs
- Complete changes to YARR scans (MR666)
- Polish pixel failure analysis (MR79) and release QC v2 (v2)

After release:

- Calculate largest cluster of pixel failures
- Allow for multiple source scan results to be combined
- Analyze if source scan was run long enough
- Collect data from 3D single chip cards
- Analyze data collected from various groups and adjust procedures / specifications
- Make fancy disconnected bump algorithm

Backup

Backup: Electrical pixel failure test

Procedure:

B.10.3 Pixel Failure Test

B.10.3.1 Electrical Pixel Failure Test

- Digital Scan with clear mask
- Analog Scan
- Threshold Scan (high res, low range)
- Noise Scan (10M trigger)
- ToT Memory Scan (Release 3: not ready)

Pixel failure categories:

Failure	Scan type	Criteria
Digital Dead	Digital Scan	Occupancy<1% of injections
Digital Bad	Digital Scan	Occupancy<98% or>102% of injections
Analog Dead	Analog Scan	Occupancy<1% of injections
Analog Bad	Analog Scan	Occupancy<98% or>102% of injections
Tuning Bad	Threshold Scan	|Pixel threshold - Mean threshold distribution| > 5×40e^*
High ENC	Threshold Scan	Mean pixel noise < 200e (L0) or < 300e (L1/L2)
Noisy	Noise Scan	Occupancy> 10^{-6} hits per BC
ToT Memory Failure	ToT Memory test	Occupancy <100% of injections

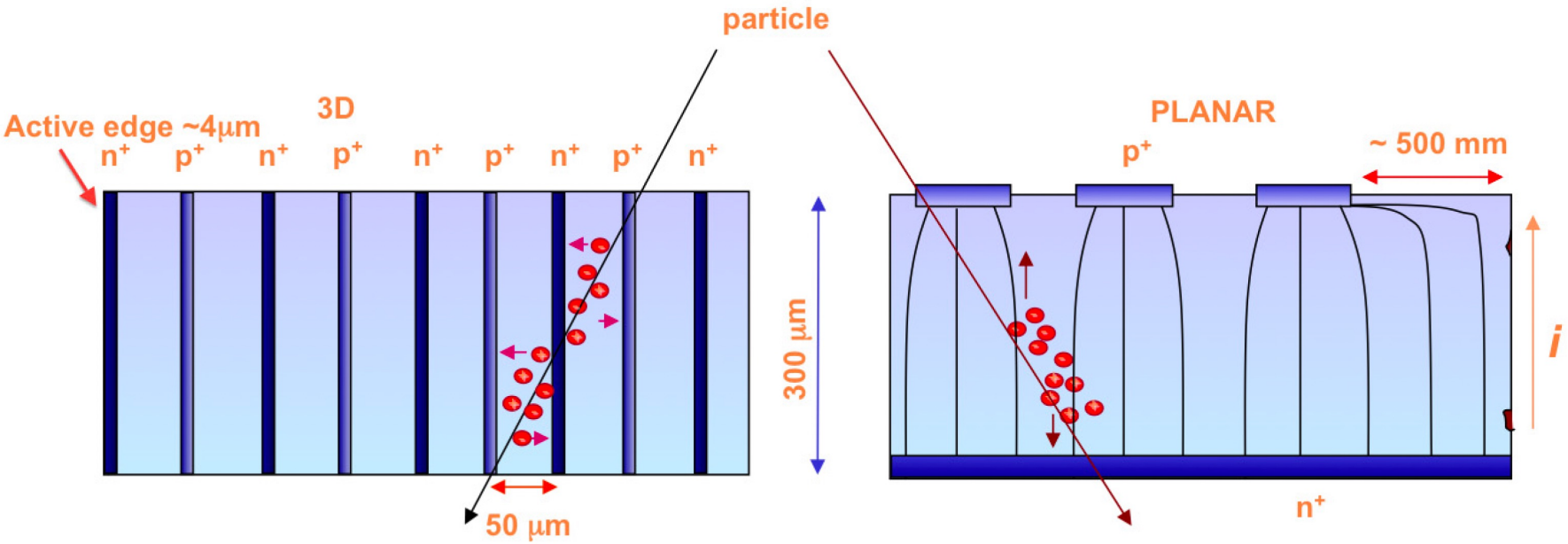
Modules are required to have less than 0.1% of electrically failing pixels after module assembly.

(Quads only)

Hybridization PRR Modules

Flip-chip	Sensor	Type	Done	Groups	# more to assemble	Bare Module reception
HPK	HPK	20 proto + 129 pre-		KEK	20 + many reception	
IZM	HPK	20 proto + 61 pre- + more	5	Germany	15 Prototypes @ 3/wk	
				CERN	10 Production	30
				Paris		30
				Oxford		25
Advacam	Micron – 100um	22 + 3 returned proto	20 + 3	USA	2 now - 10 from next batch	
	Micron - 150um	60 pre-	10	Paris	18 (inc. started) @ 4/wk	
				UK	18	8
				USA	6	
	HPK	20 proto	5	Italy	15	
LND	FBK	10 proto - trashed		Italy	-	
	HPK			Italy/USA/MPI		

Backup

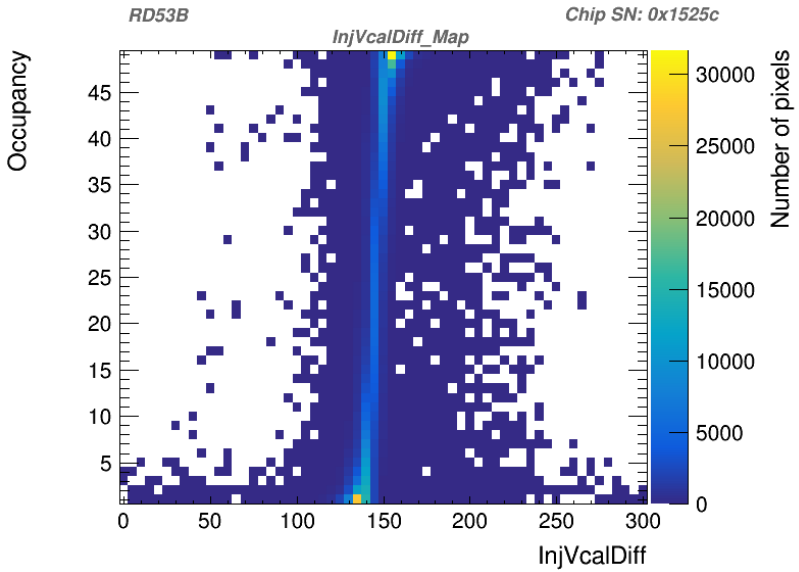

particle
Active edge ~4μm
3D
n+ p+ n+ p+ n+ p+ n+ p+ n+
300 μm
50 μm
PLANAR
p+
~ 500 mm
n+
i

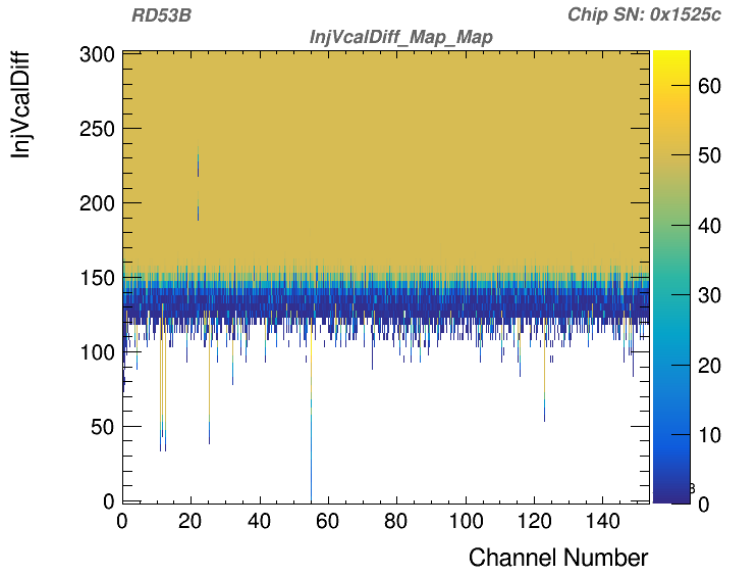
B.10.2 Tuning performance

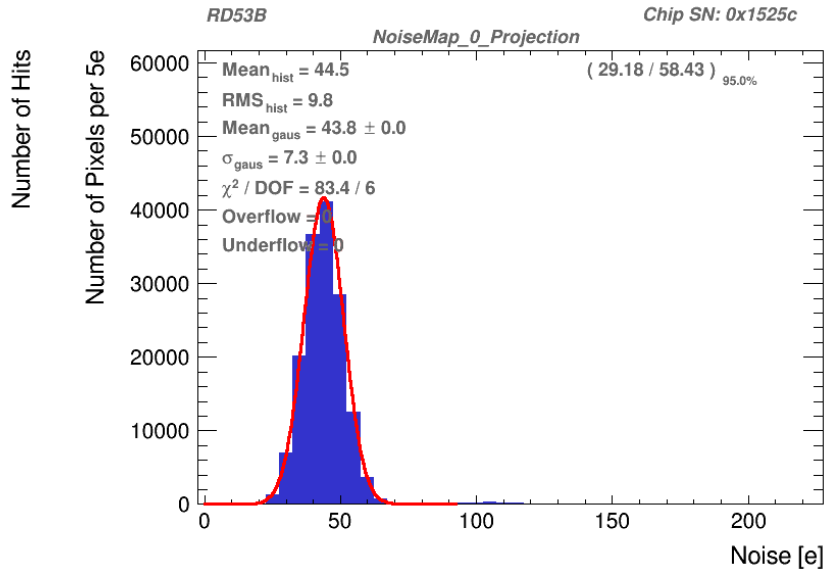
Please note that ToT scans or tunings are not available for ITkPixV1.1.

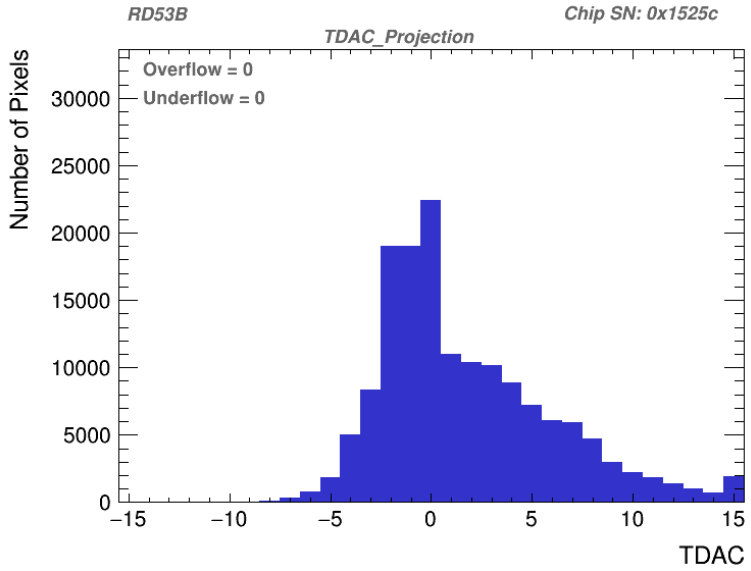
- Tuning:
  - Global threshold tune @2000e
  - Threshold Scan (high range, low def)
  - ToT scan, 6000e injection charge
  - ToT tune 8bc @ 6000e
  - Global threshold tune @2000e
  - Pixel threshold tune @2000e
  - Global threshold re-tune @1000e (L0) or @1500e (L1/L2)
  - Pixel threshold re-tune @1000e (L0) or @1500e (L1/L2)
  - Injection delay tuning
- Post-tuning:
  - Threshold Scan (high def, low range)
  - In-time threshold measurement
  - ToT scan, 6000e injection charge

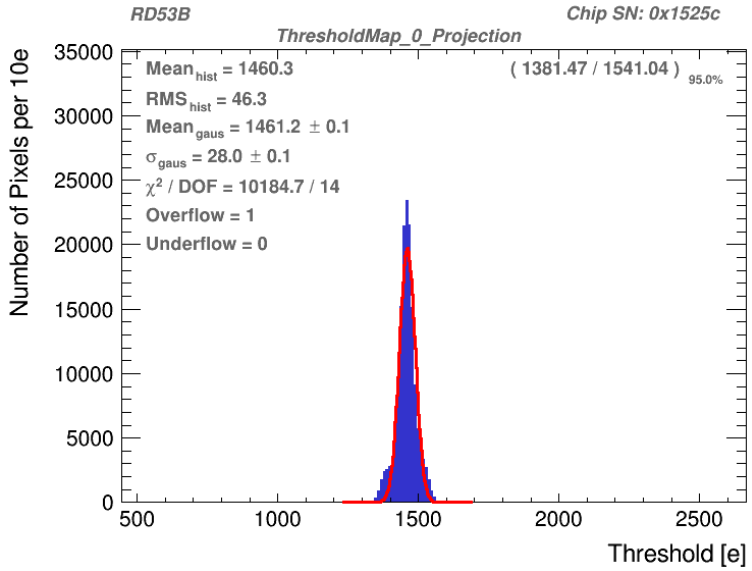
Tuning


RD53B
Chip SN: 0x1525c
InjVcalDiff_Map
Occupancy
InjVcalDiff
Number of pixels


RD53B
Chip SN: 0x1525c
InjVcalDiff_Map_Map
InjVcalDiff
Channel Number


RD53B
Chip SN: 0x1525c
NoiseMap_0_Projection
Number of Hits
Number of Pixels per 5e
Mean hist = 44.5
RMS hist = 9.8
Mean gaus = 43.8 ± 0.0
σ gaus = 7.3 ± 0.0
χ² / DOF = 83.4 / 6
(29.18 / 58.43) 95.0%
Noise [e]


RD53B
Chip SN: 0x1525c
TDAC_Projection
Number of Pixels
Overflow = 0
Underflow = 0
TDAC


RD53B
Chip SN: 0x1525c
ThresholdMap_0_Projection
Number of Pixels per 10e
Mean hist = 1460.3
RMS hist = 46.3
Mean gaus = 1461.2 ± 0.1
σ gaus = 28.0 ± 0.1
χ² / DOF = 10184.7 / 14
Overflow = 1
Underflow = 0
(1381.47 / 1541.04) 95.0%
Threshold [e]