X-ray irradiation update

Maurice Garcia-Sciveres, Maria Mironova, Timon Heim

Weekly student instrumentation meetin

20 September 2023

BERKELEY LAB

ATLAS EXPERIMENT

Intro to radiation damage

Two types of radiation damage relevant to pixel sensors:

- **Bulk damage**
  - Non-ionising energy dose (NIEL) effects
  - In units of 1MeV neutron equivalent does (n/cm^2)
  - E.g. causes crystal defects (displaced atom and vacancy) → **Most important for pixel sensor**
- **Surface damage:**
  - Total ionising dose (TID) effects
  - In units of X-ray equivalent Rad
  - Affects electronics in CMOS through charge build-up → **Most important for readout chip**

In ITk:

- 10^{16} n/cm^2 fluence and 1 Grad dose for the inner layers
- Possibility to replace innermost two pixel layers, due to expected radiation damage

Intro to radiation damage

- Transistor properties:
  - Technology used (130 nm, 65nm, 25nm CMOS etc) → minimum possible feature size
  - Production process and foundry used
  - Transistor geometry and size (W and L of transistor, or W/L, also referred to as transistor strength)
  - Exact transistor layout → modifications possible to increase radiation tolerance (e.g. enclosed transistor layout)
- Operational parameters:
  - **Temperature** and Supplied voltage
- Irradiation properties:
  - Type and energy of incoming particles (mainly for calculating TID)
  - **Dose rate**
- Annealing:
  - After irradiation, created defects do not stay the same, but can recombine, or create more damage, depending on operational parameters

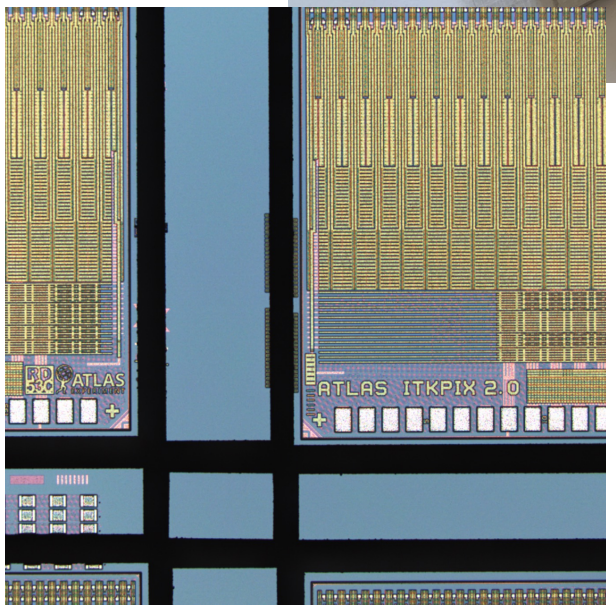
  → generally, annealing at high temperatures and unpowered, can reverse TID damage

ITkPixV2 irradiation studies

- Understanding the radiation tolerance of the pixel readout chip is very important

→ Expect a total dose of 1 Grad over the lifetime of ITk

- Design validated in simulation up to 500 Mrad, taking into account different transistor settings (e.g. voltages and radiation effects)
- But radiation damage is complicated and we need to test in detail on the chip
- We characterised the radiation tolerance of ITkPixV1 in a lot of detail (PRR talk)
- Received back ITkPixV2 chips a few months ago, and need to repeat the main measurements we performed on ITkPixV1



ITkPixV2 ring oscillators

- ITkPixV2 chip includes ring oscillator for radiation testing of digital logic (located at chip bottom)
- 42 ring oscillators made with different logic cells and different transistor sizes (strength 0, 1 and 4)
- Oscillator drives a 12-bit counter, enabled for a given period of time

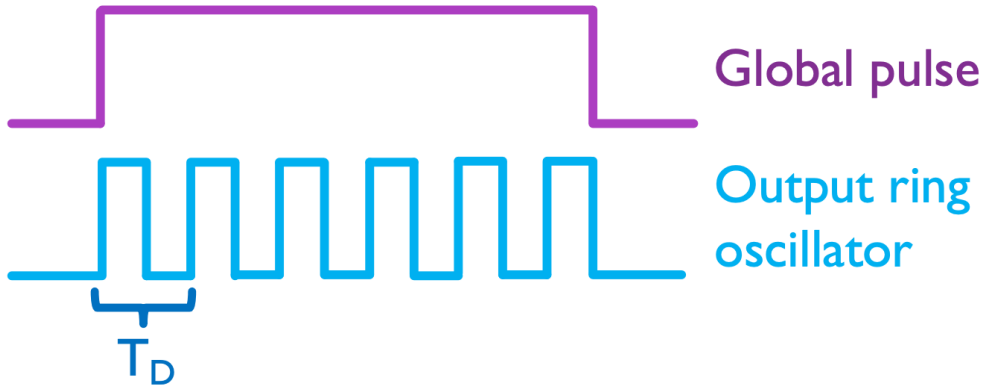
→ **Calculate frequency f or delay $T_D = 1/(N f)$**

- During irradiation ring oscillator frequency decreases

→ Characterise radiation damage to different kind of logic cells

→ **Proxy to understand gate delay**

- Speed of digital logic gates needs to be sufficient for ITk readout rates → gate delay should not increase more than 200% during ITk operation



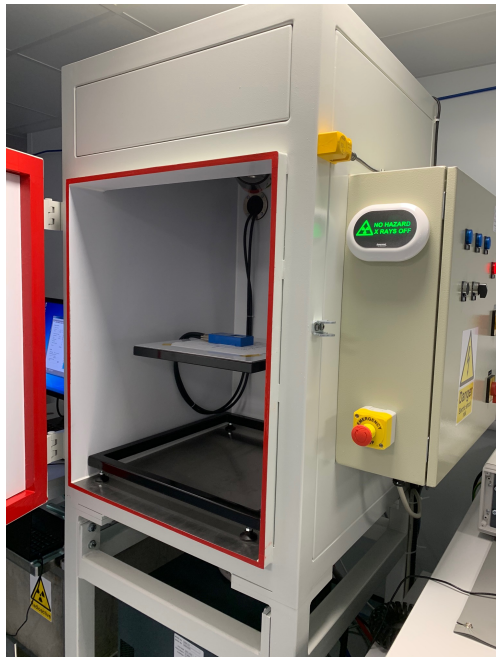
Group	Types	#
A B left B right	CLK, Inv, NAND, NOR Driving strength 0 and 4 w/ different lengths	3 x 8
B FF	Scan/standard/neg-edge D-flip-flop	6
B LVT	LVT inverter & 4-input NAND Strengths 0 and 4	4
B CAPA	Injection-capacitor loaded 4-input NAND	8

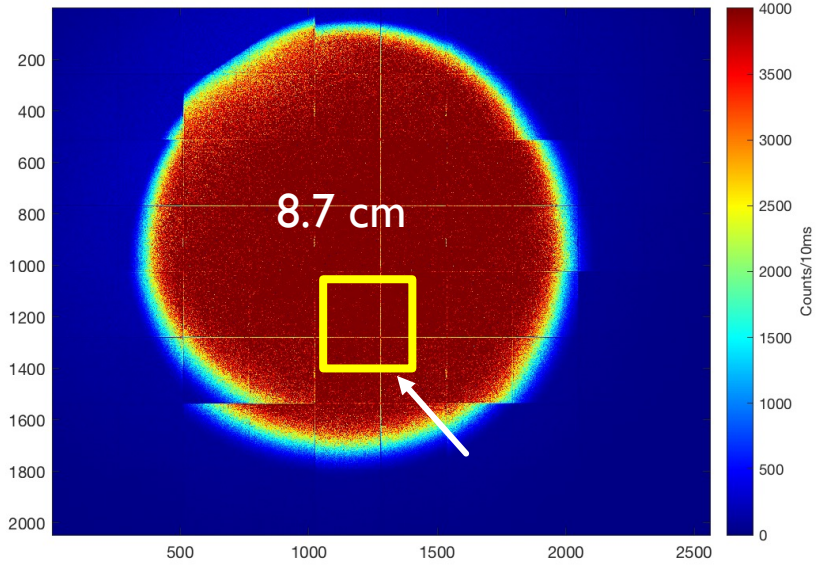
Oxford X-ray irradiation campaign

- Performing two X-ray irradiation campaigns over the last couple of months
- Set up irradiation campaign in Oxford, at **a dose rate of 5.4 Mrad/h**
- Get a quick first look at the radiation tolerance of ITkPixV2
- Focus on analog front-end, because we can go to high doses quickly
- Run a range of untuned threshold scans before and after irradiation
  - at 1000e and 2000e
  - varying chip parameters (Preamp, Vff, LCC, VDDA, TDAC etc)

  → assess the operational range of the analog front
- Run **detuning measurements** during irradiation

→ Check how quickly a threshold distribution deteriorates during irradiation





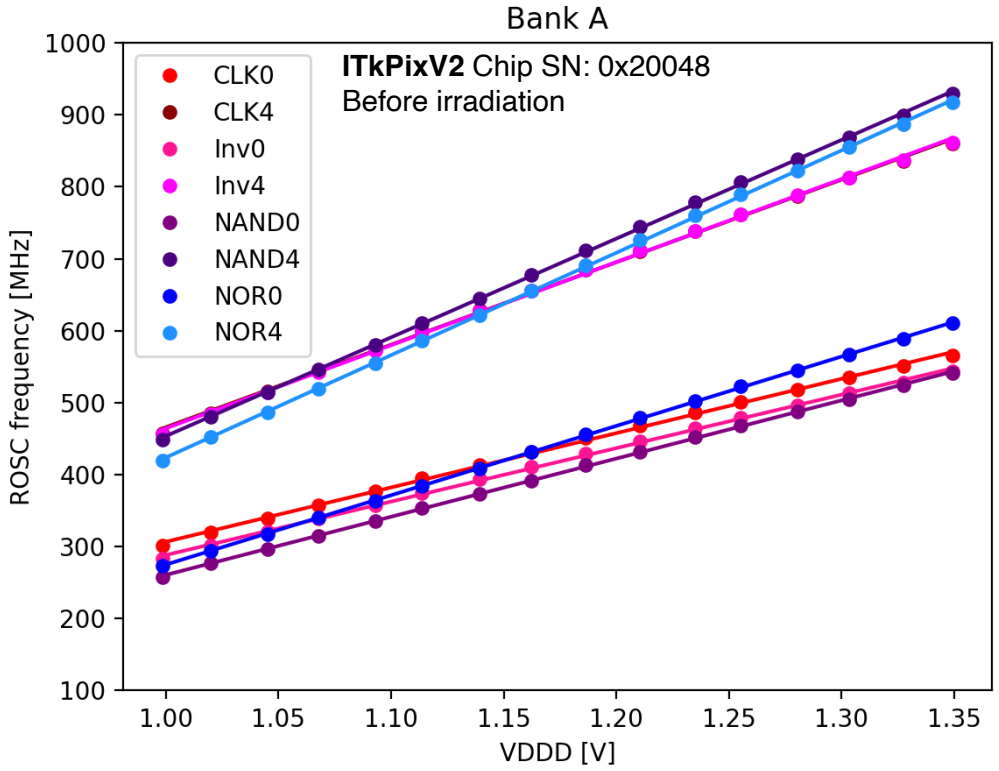
X-ray irradiation setup and beam spot @ Oxford

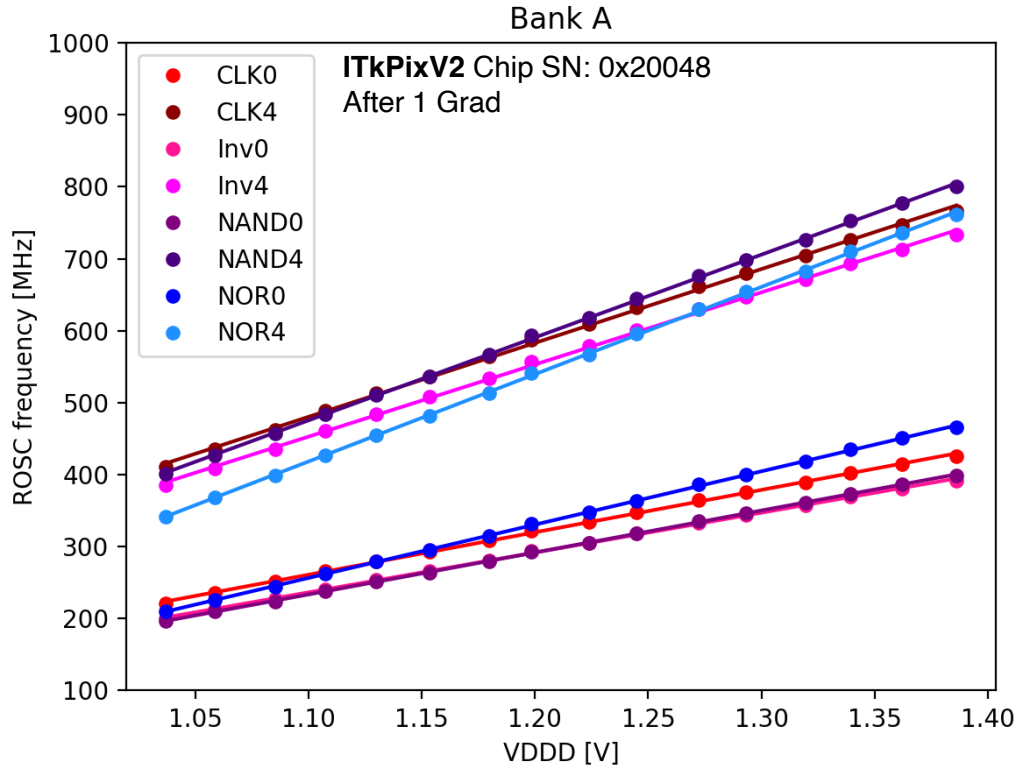
Ring oscillator vs VDDD

- Before irradiation, characterise ring oscillator frequency as a function of VDDD

→ See the expected linear behaviour with VDDD, and can use the slopes to correct ring oscillator frequencies to account for drifts in VDDD with irradiation

- Repeat the curves after irradiation, as the slopes change with irradiation and interpolate between the two points for the correction



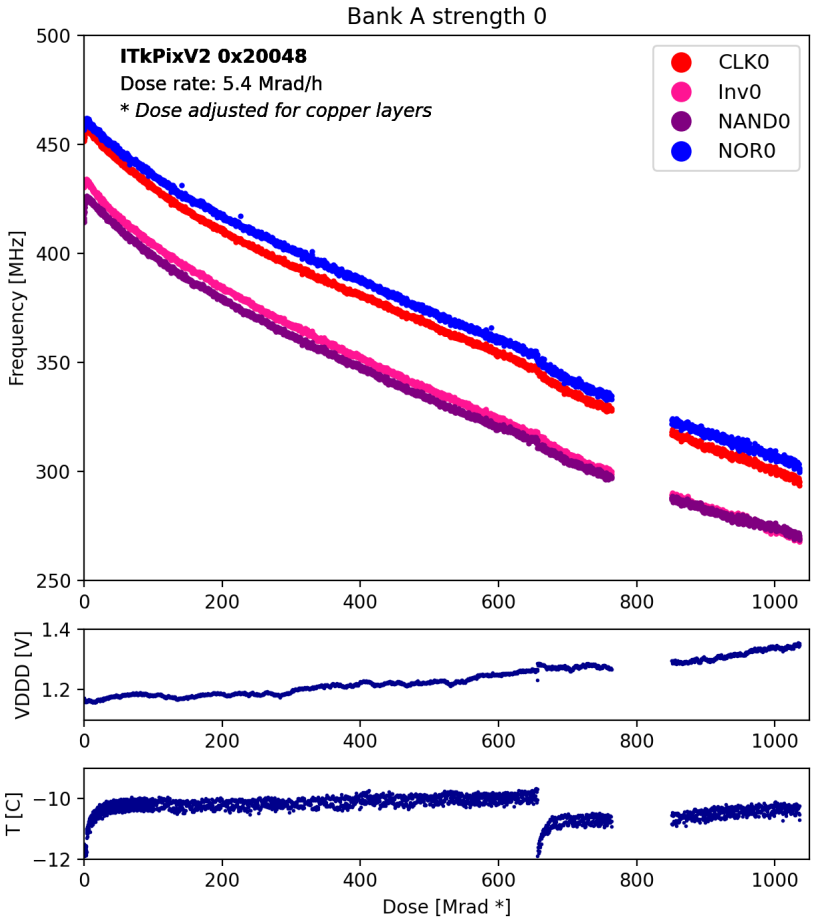


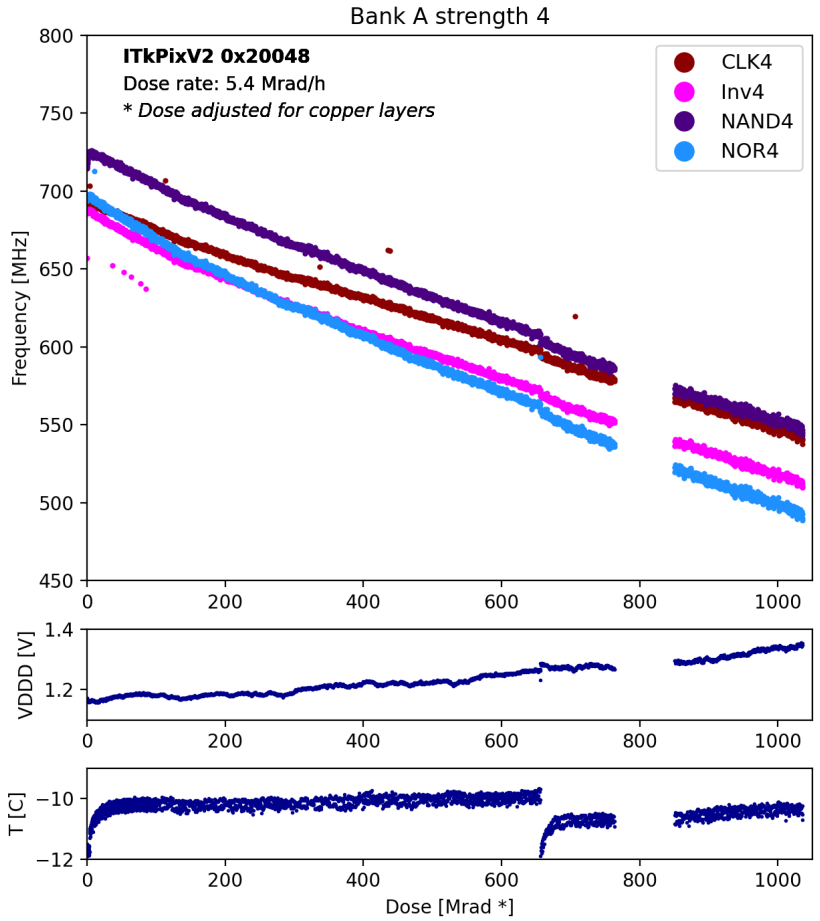
Irradiation results

- Irradiation generally went without issues
- Paused once at 600 Mrad to run threshold scans while I was still in the Oxford

→ Chip was powered and cooled

- Ran out of disk space on the machine around 800 Mrad but irradiation continued
- Temperature was very stable during irradiation
- Ring oscillator frequency shows the expected decrease with irradiation (after correcting for VDDD drift)

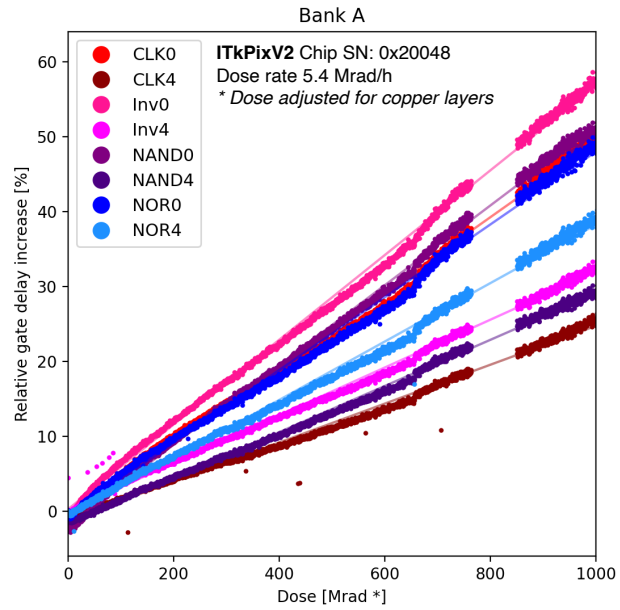


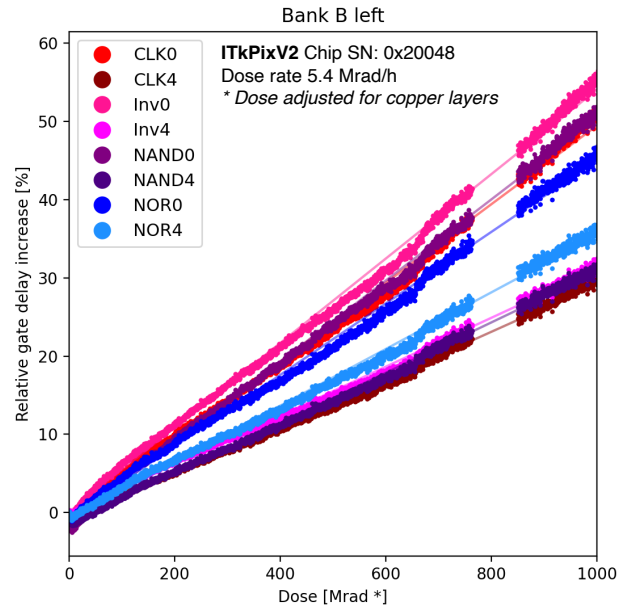


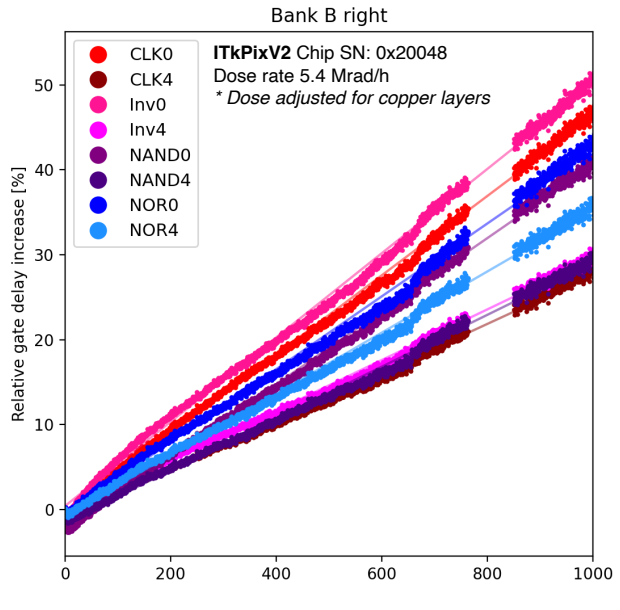
Delays

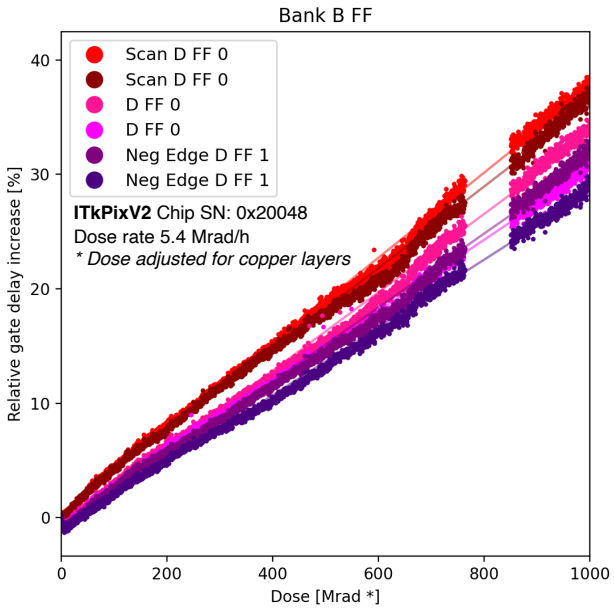
- Convert ring oscillator frequency into delay increase
- Relative delay increase as a function of dose
- ~50% increase for strength 0 gates (not used in the chip digital part)
- **~25% increase for strength 4 gates**

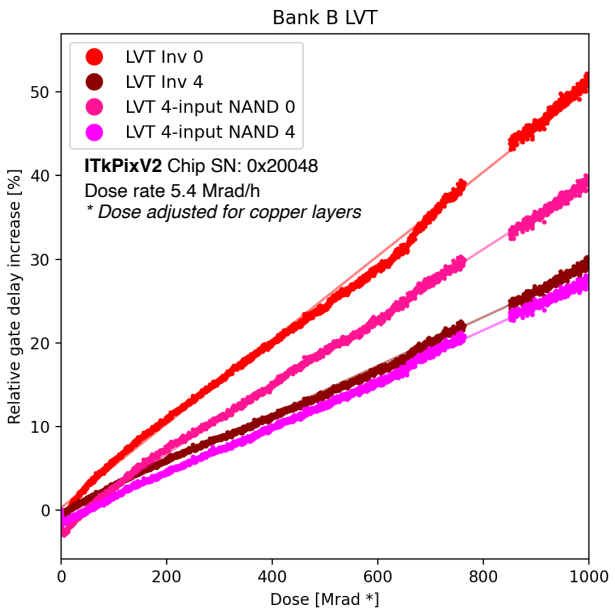
Note: this is not exactly representative of what we'll see in ITk because of dose rate effects

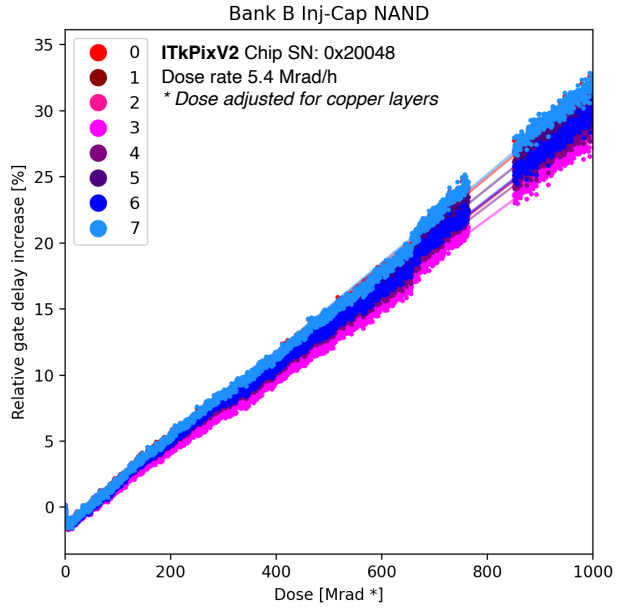




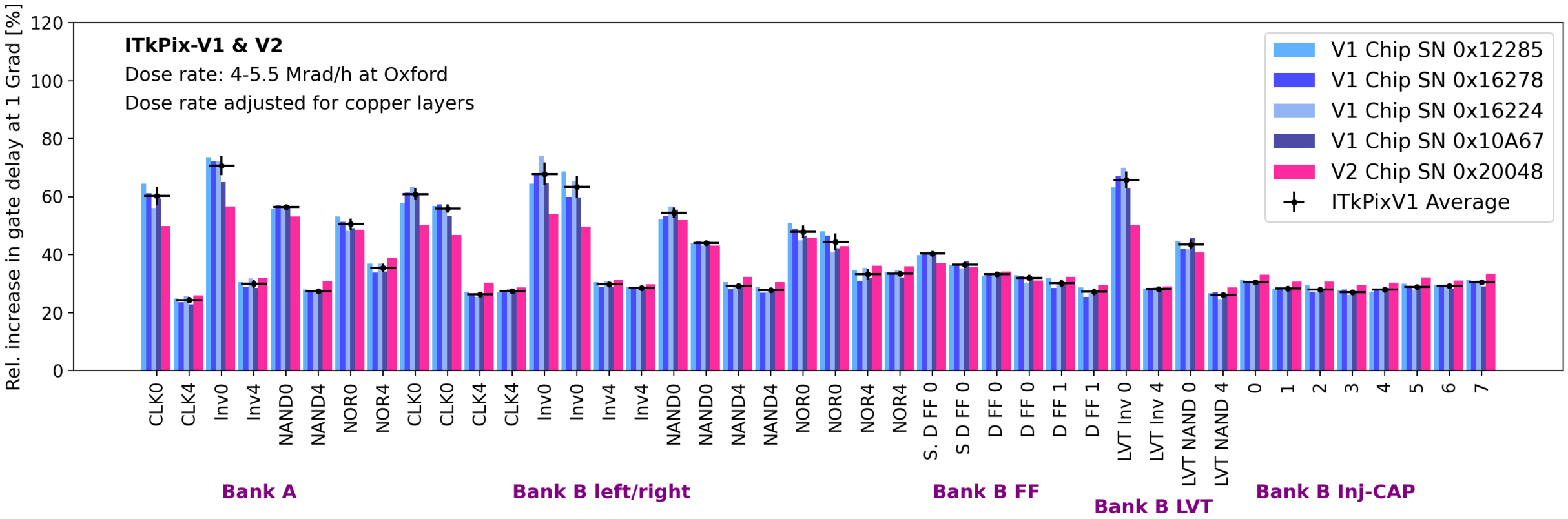








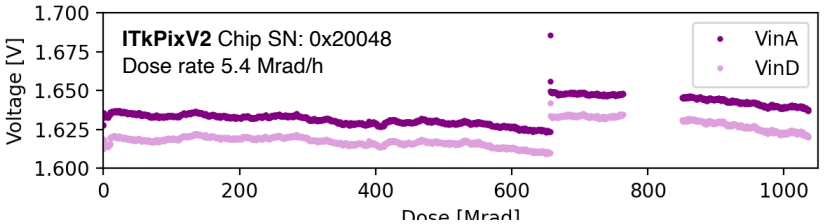
Comparison with ITkPixV1

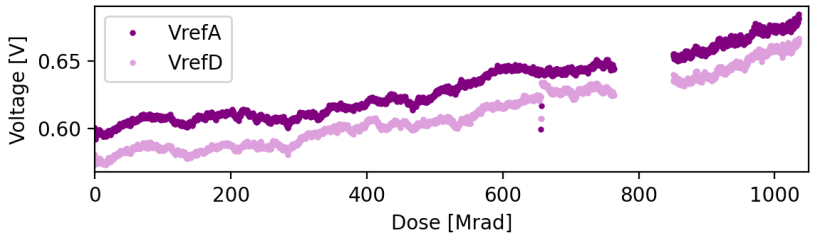


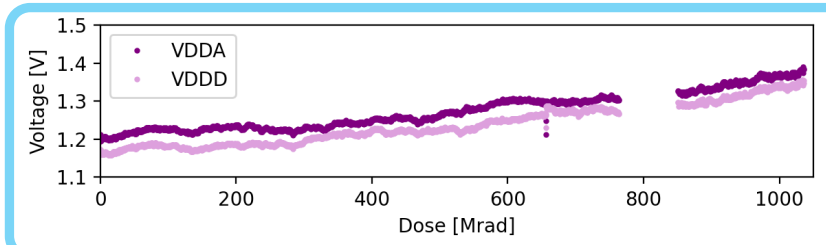
- Compare to ITkPixV1 results (obtained using the same X-ray machine)
- Compare relative increase in gate delay at 1 Grad for all gates
- **Good agreement** in general, strength 0 delay seems to increase less than for ITkPixV1 → Did we change anything about the metallisation layers covering the ring oscillators in V2?

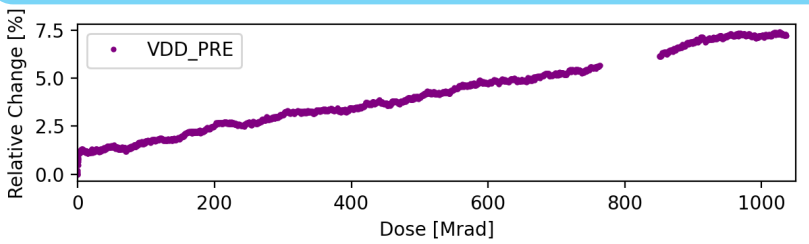
Voltages

Absolute change

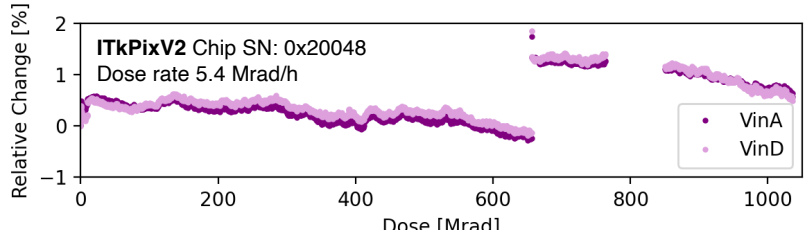


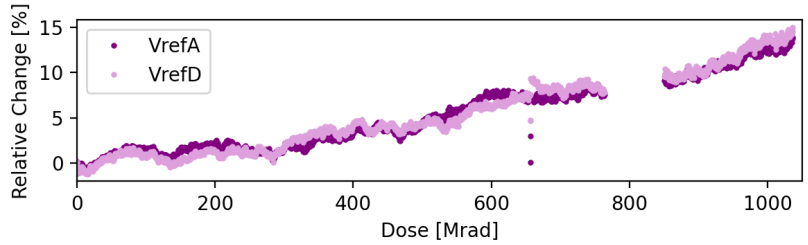


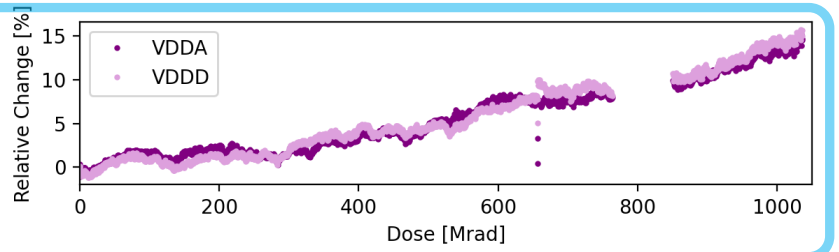


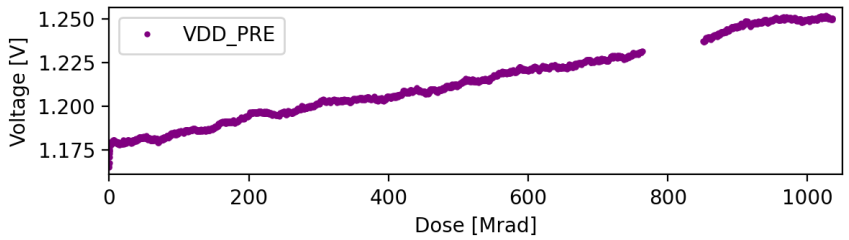


Relative change

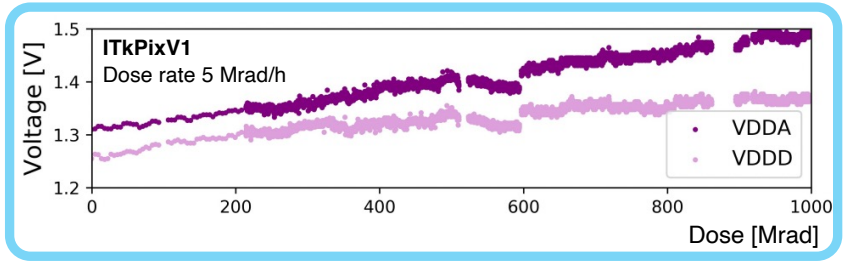








VDDA/VDDD in ITkPixV1



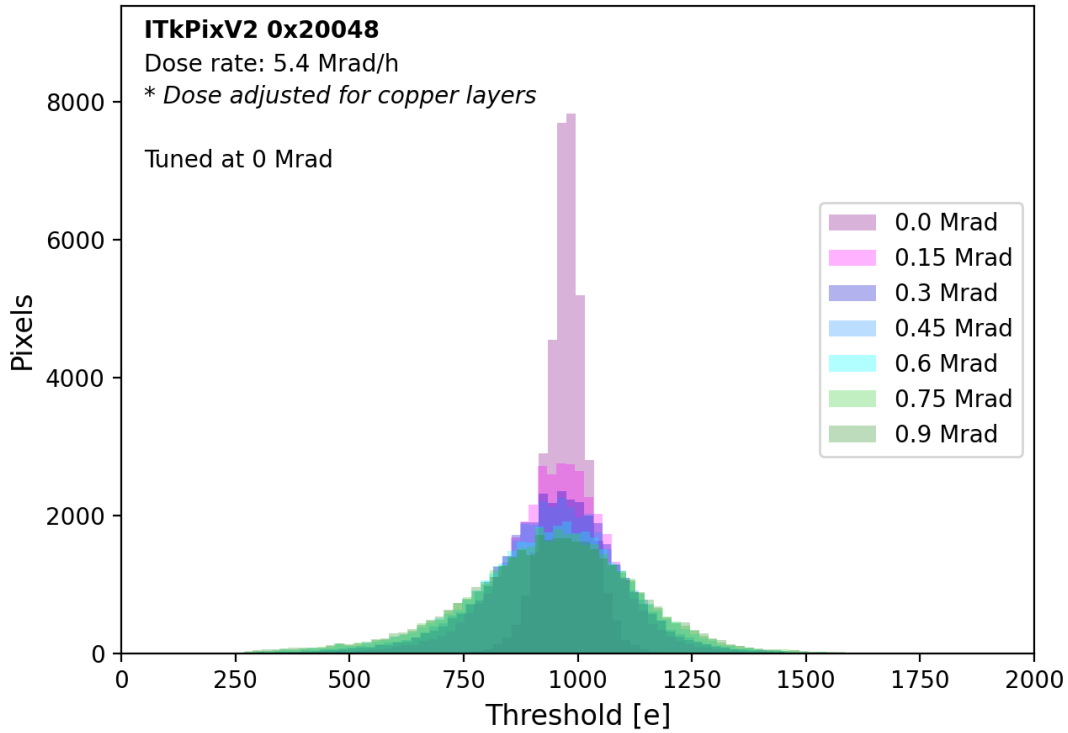
- Measures some of the chip voltages with irradiation
- Saw in irradiations of ITkPixV1 that **VDDA/VDDD voltage increases**
- VDDA increased significantly more than VDDD (+14% for VDDA, +9% for VDDD after 1 Grad)

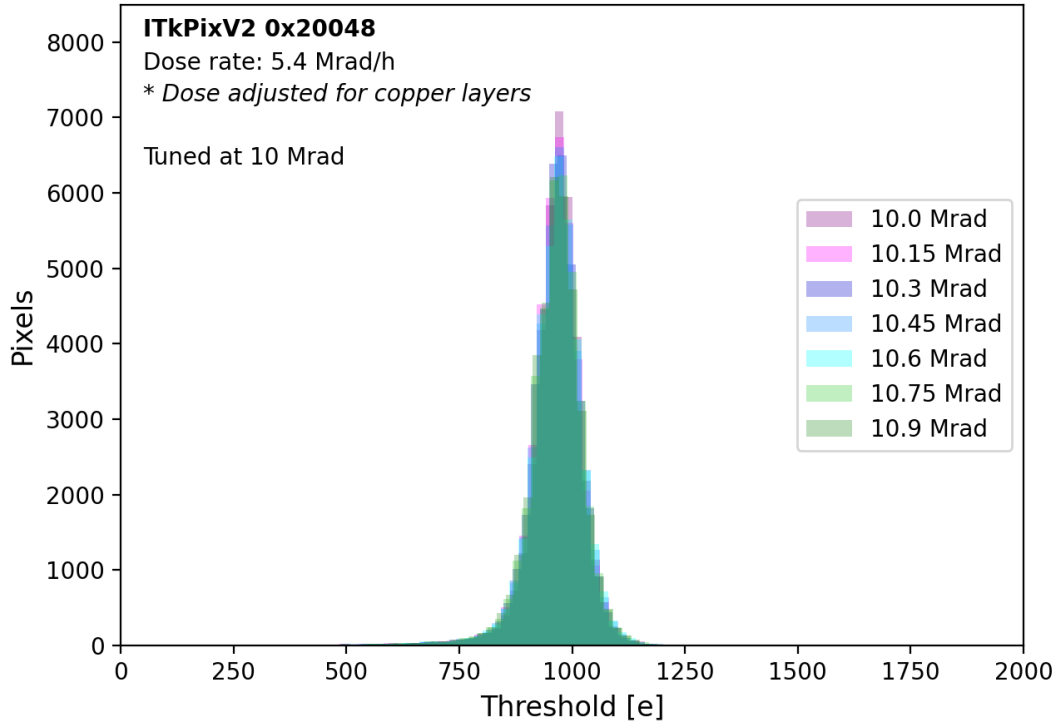
→ likely caused by increased mismatch of current mirrors caused by non-uniform chip metallisation layers

- Included two related modificiations in ITkPixV2 design:
  - More uniform metallisation layers → seem to have the desired effect
  - Larger trim bit size → Larger range of VDDA/VDDD possible

Analog front-end during irradiation

- Performed detuning measurements during irradiation → tune threshold distribution every 10 Mrad and measure threshold distribution with irradiation
- At the beginning of the irradiation threshold disperses very quickly → **most damage to the analog front-end happens in the first few Mrad of dose**
- After 10 Mrad of irradiation, threshold dispersion is much less severe



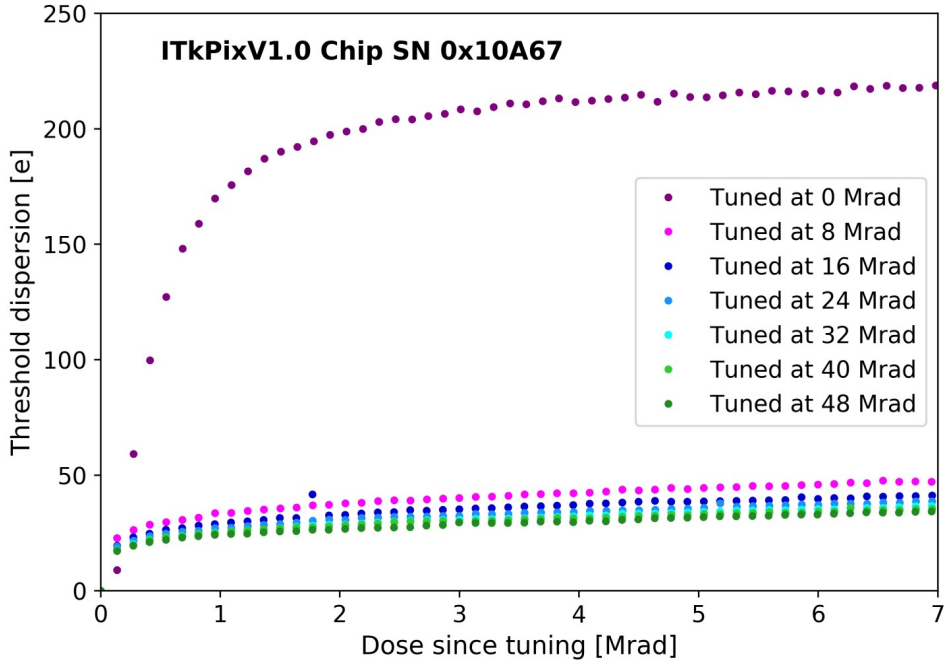


Comparison with ITkPixV1

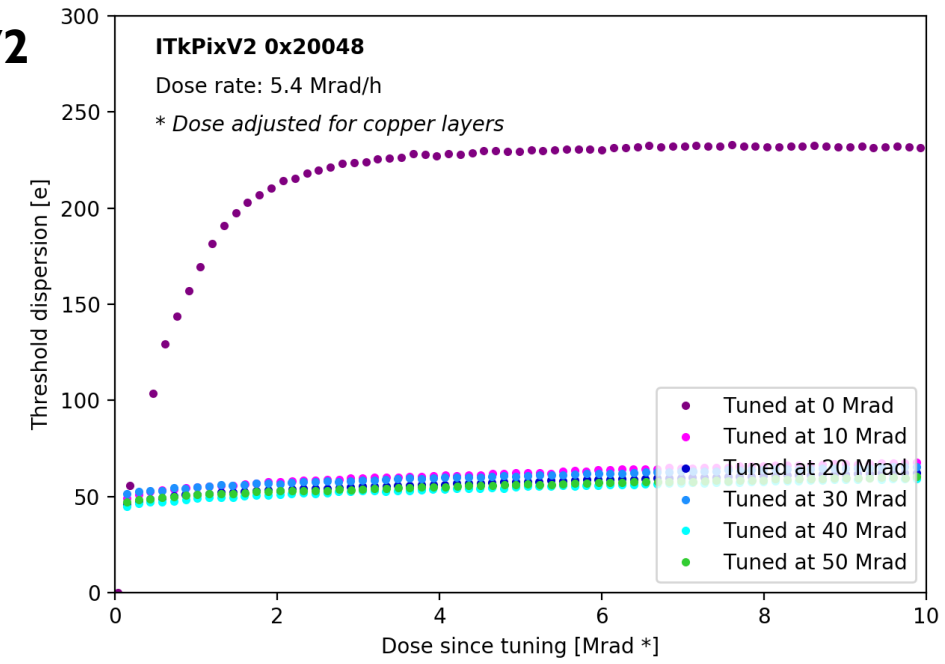
- Consider threshold pixel-to-pixel difference for each threshold scan i.e: Threshold [measurement] – Threshold [after tuning]
- **Threshold dispersion** defined as standard deviation of distribution of differences
- Observations match quite well between ITkPixV1 and ITkPixV2
- Initial jump in threshold distribution is slightly different between V1 and V2, but I think this is due to testing procedure

→ For ITkPixV1.0 threshold tuning and scans took a lot longer, so the initial threshold distribution was probably already affected by radiation (and in general, we care more about the slope anyways)

ITkPixV1



ITkPixV2



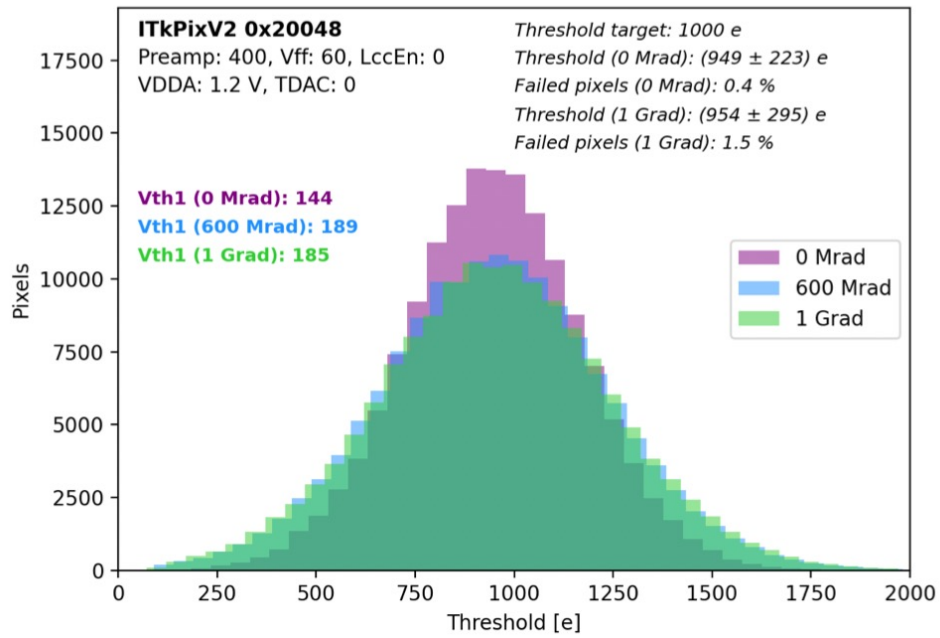
Analog front-end before and after

- Ran batch of untuned threshold scans before and after irradiation
- Generally, untuned threshold distribution gets wider with irradiation, and difference between 600 Mrad and 1 Grad is small
- For the same global threshold value, need to go to higher Vth1 values after irradiation

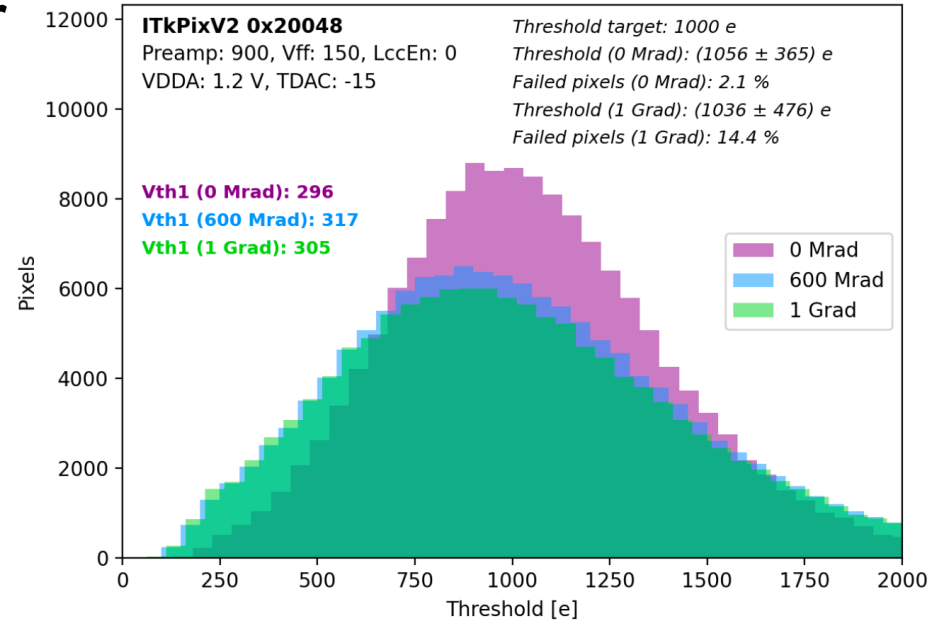
→ Automatic tuning of global thresholds didn't always coverge, need to follow up on that

→ Also need to check tuned threshold distributions after irradiation

Outer layer setting
Preamp 400
Vff 60

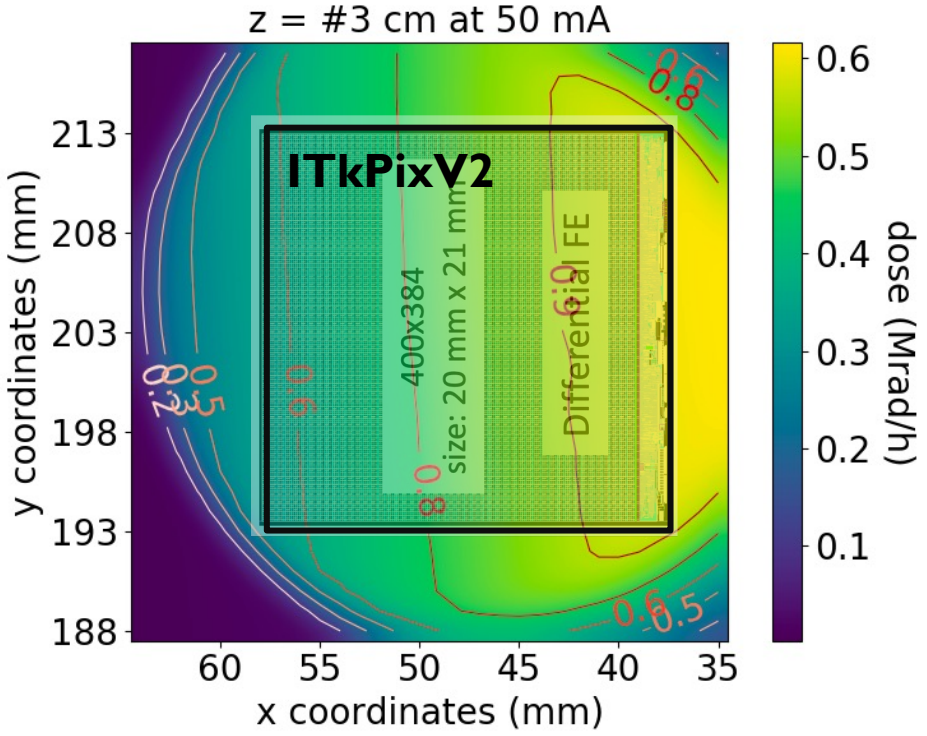


Inner layer setting
Preamp 900
Vff 150



LBL X-ray setup

- Also set up X-ray irradiation at LBL → dose rate of 0.5 Mrad/h and non-uniform beamspot
- Irradiation focused on **end of chip** (i.e. chip voltages and ring oscillators)
- Monitor everything available via the VMUX, and measure ring oscillators
- Set up proper monitoring in Grafana for X-ray machine and chip

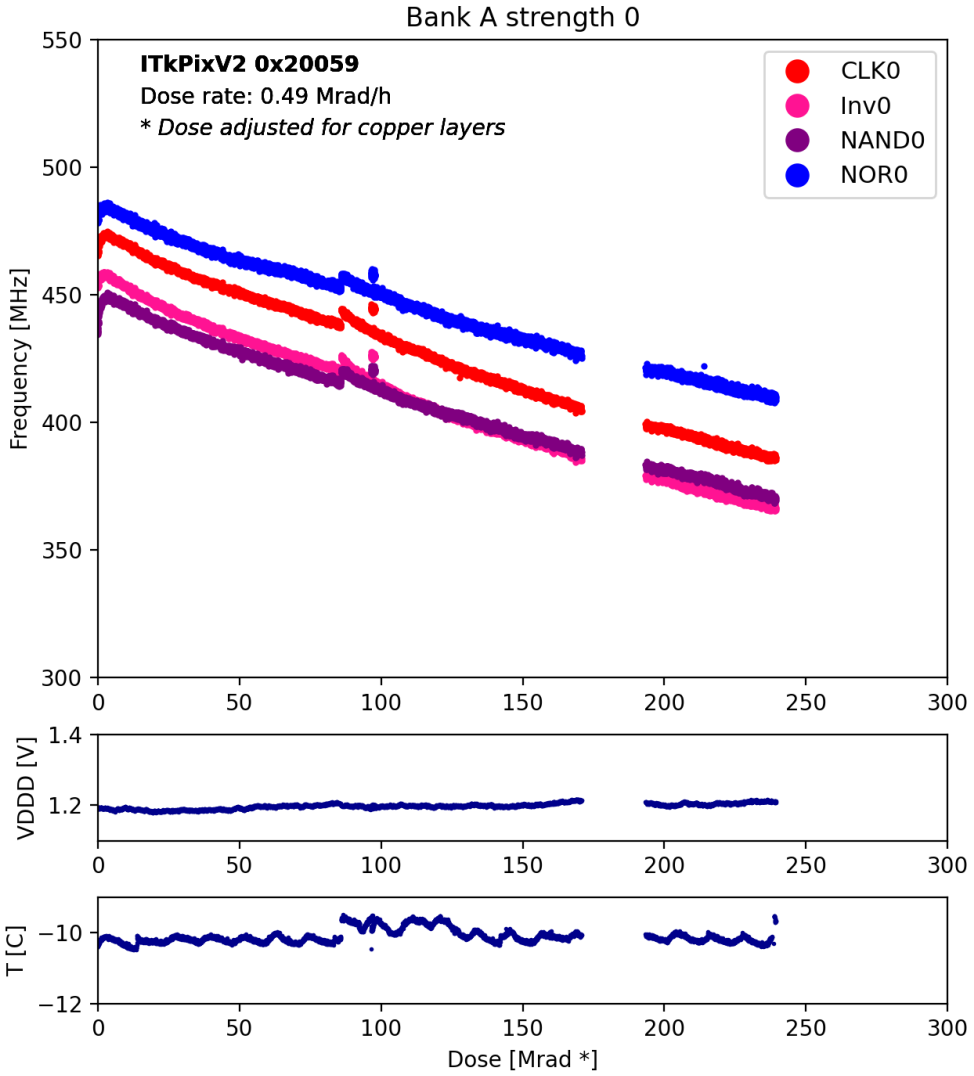


Irradiation results

- Irradiation is still running, currently at a total dose of around 250 Mrad
- Planned power outage in the lab (around 90 Mrad)

→ Chose to power down the chip and let it warm up

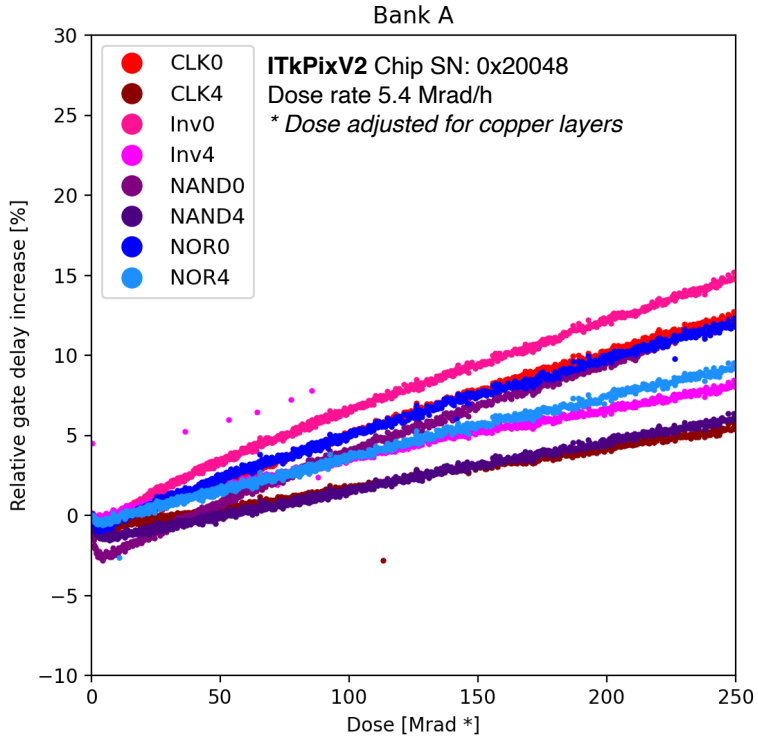
→ See some effect of annealing in the ring oscillator frequencies, but the return to the same slope quickly



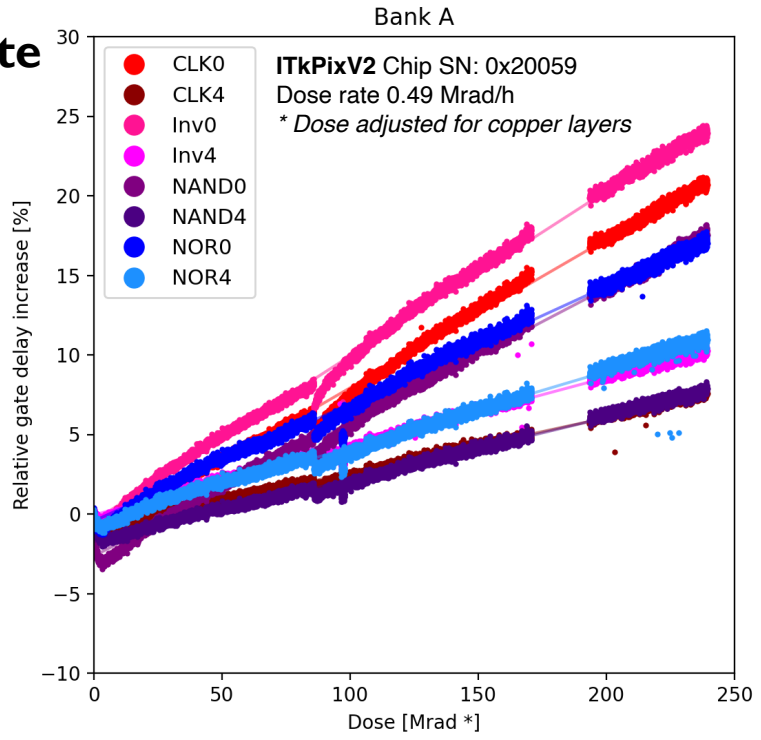
Delay increase & low dose rate effects

- Can compare the relative gate delay increase for the irradiation in Oxford and at LBL
- See more damage at LBL, caused by the factor 10 lower dose rate at LBL
- Generally, we expect (and have observed) more damage at low dose rate

High dose rate (5 Mrad/h)

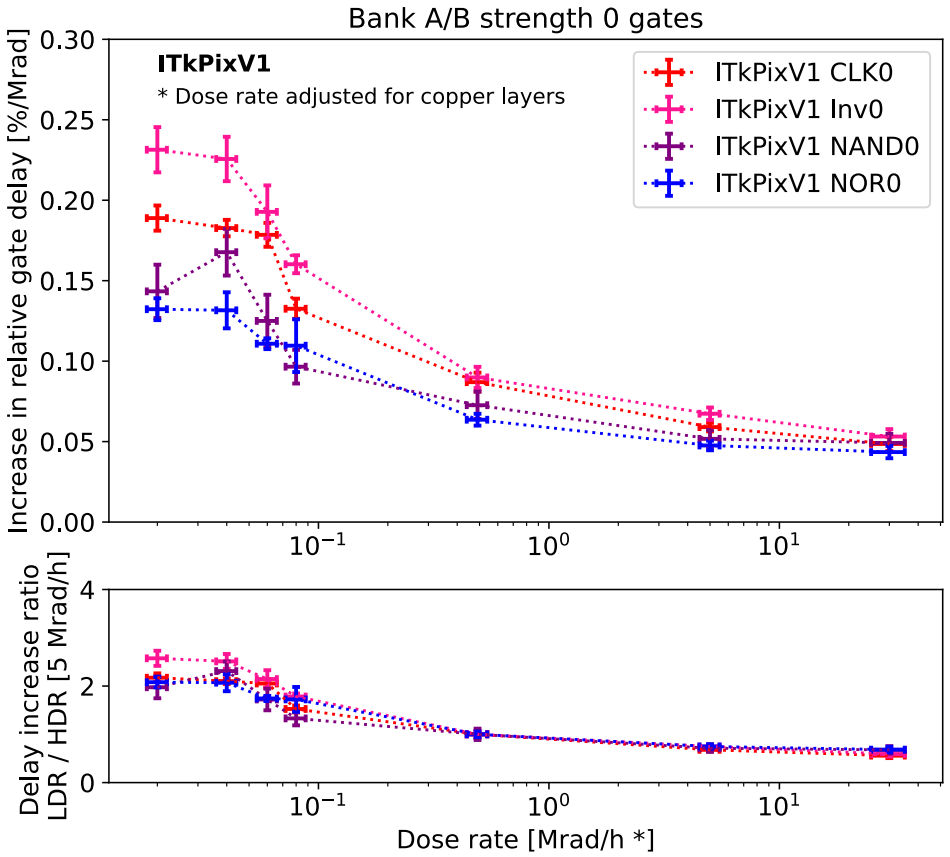


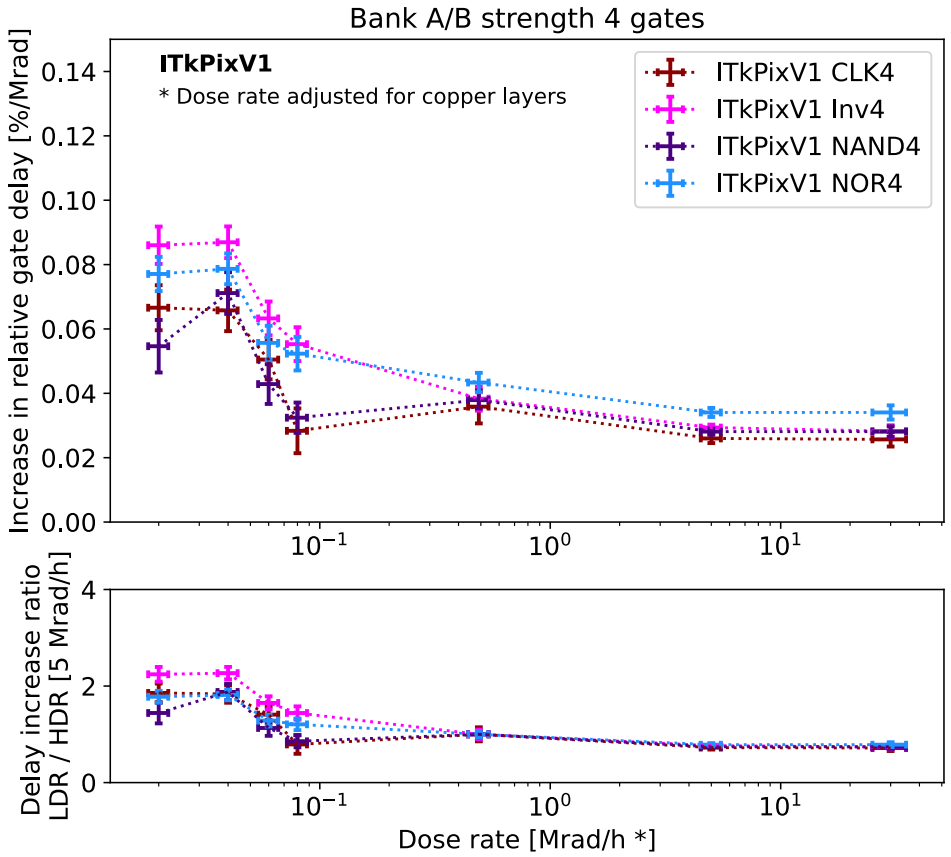
Low dose rate (0.5 Mrad/h)



Low dose rate effects

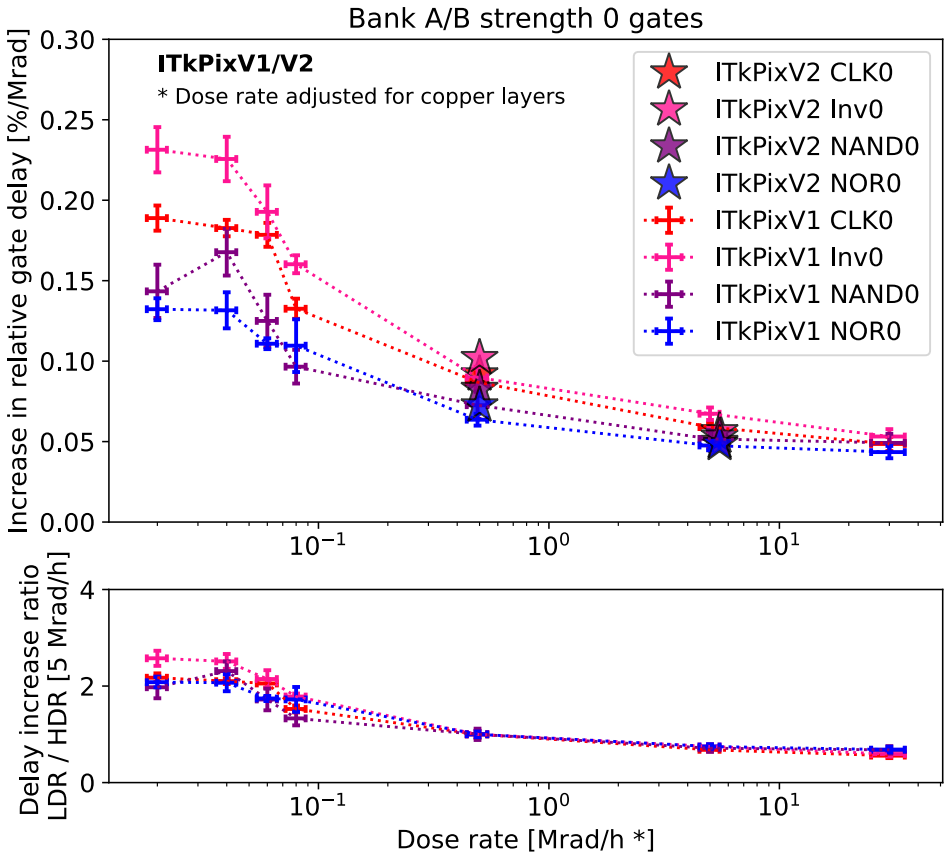
- Made some detailed investigations into dose rate effects for ITkPixV1 using X-ray irradiations at different dose rates
- Can plot delay increase as a function of dose → see around a factor 2 more damage at low dose rate

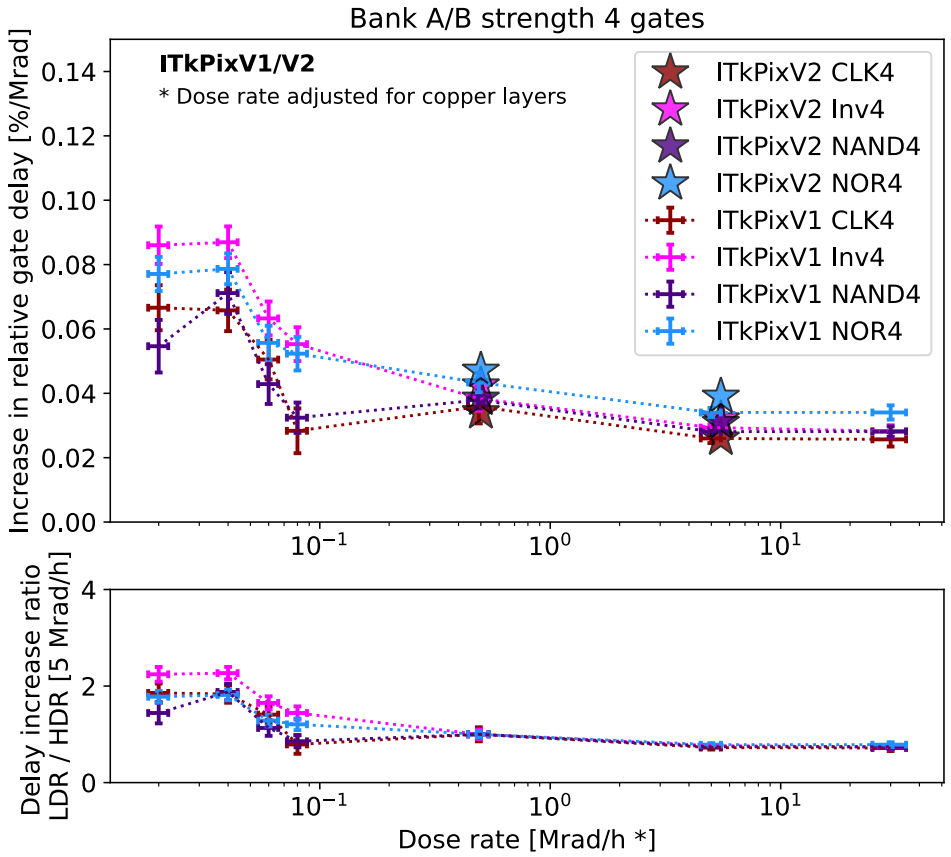




Low dose rate effects

- **Add ITkPixV2 data to this plot → Matches up really well!**





Summary

- First look at irradiation results for ITkPixV2

- X-ray irradiation campaign in Oxford focused on analog front-end → results up to 1 Grad look reasonable and match with ITkPixV1

→ Next: Finish up analog front-end measurements at 1 Grad, and then either swap out the chip to get more statistics, or continue to irradiate until failure

- X-ray irradiation in LBL focused on end-of-chip (VMUX/IMUX voltages and ring oscillators)

→ Next: Irradiate up to 1 Grad (basically until Christmas), analyse VMUX data (voltages, currents, maybe temperature/radiation sensors?)

- Will also set up long-term low dose rate irradiation with ITkPixV2 (SLIPPER v2)

Thank you!

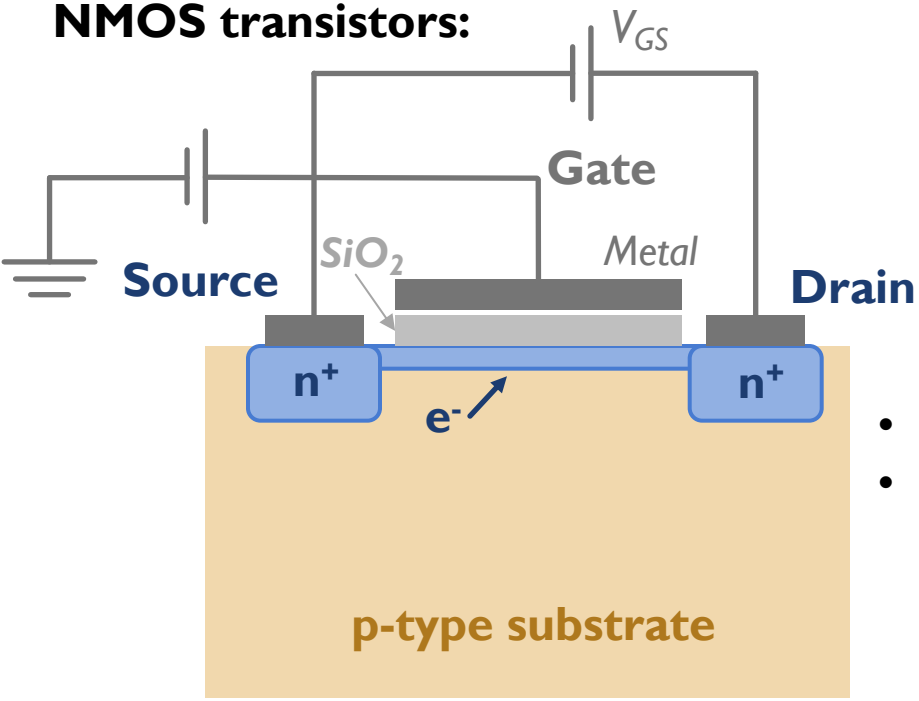
Questions?

Transistors

- MOSFET transistors are the building of current (pixel detector) electronics
- Working principle:

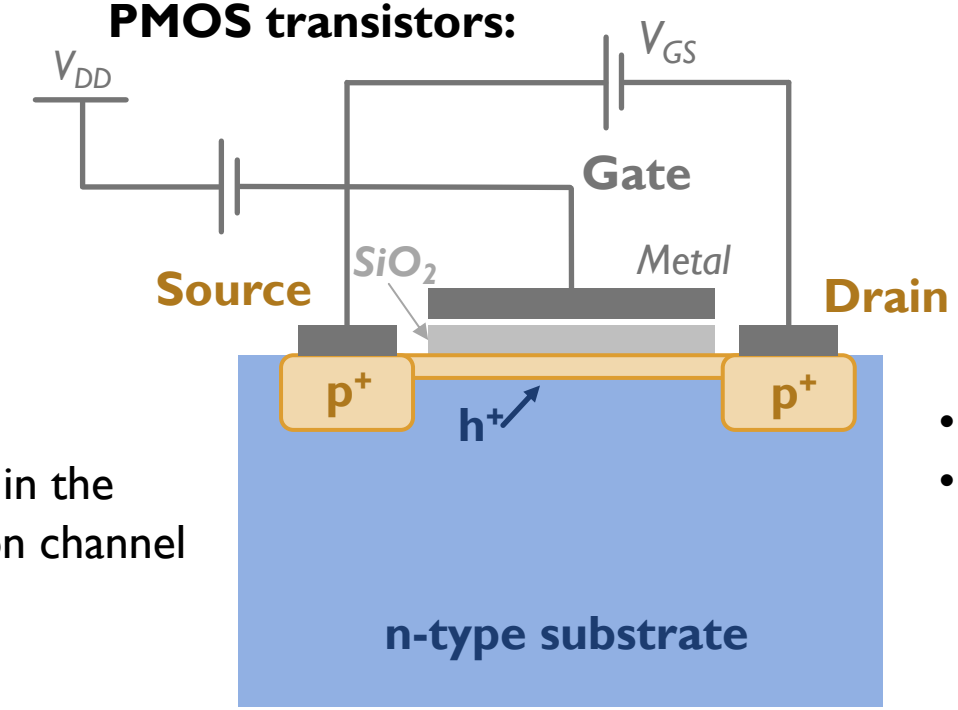
1. Voltage is applied to gate to induce a channel of free charge carriers below the Si-SiO_2 surface
2. Voltage applied between source and drain allow charge carriers to move → current

NMOS transistors:



- $V_{GS} > 0$
- Electrons in the conduction channel

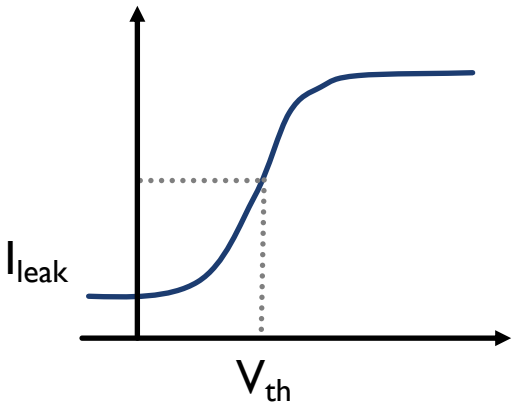
PMOS transistors:



- $V_{GS} < 0$
- Holes in the conduction channel

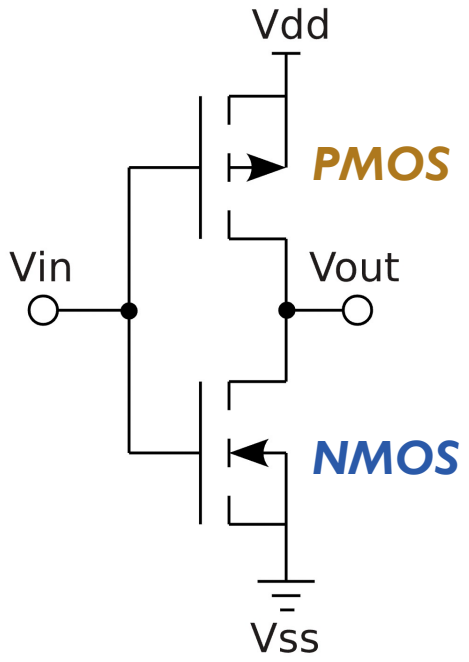
Transistors part II

Transistor turn-on curve



- Important characteristics of transistors include:
  - Transistor leakage current (I_{leak}) → current when no voltage V_{GS} is applied
  - Threshold voltage (V_{th}) → voltage at which the transistor turns on
- Various logic gates can be constructed from combinations of PMOS and NMOS gates
- E.g. Inverter gate → if you input 0, you get 1 and vice versa

CMOS Inverter

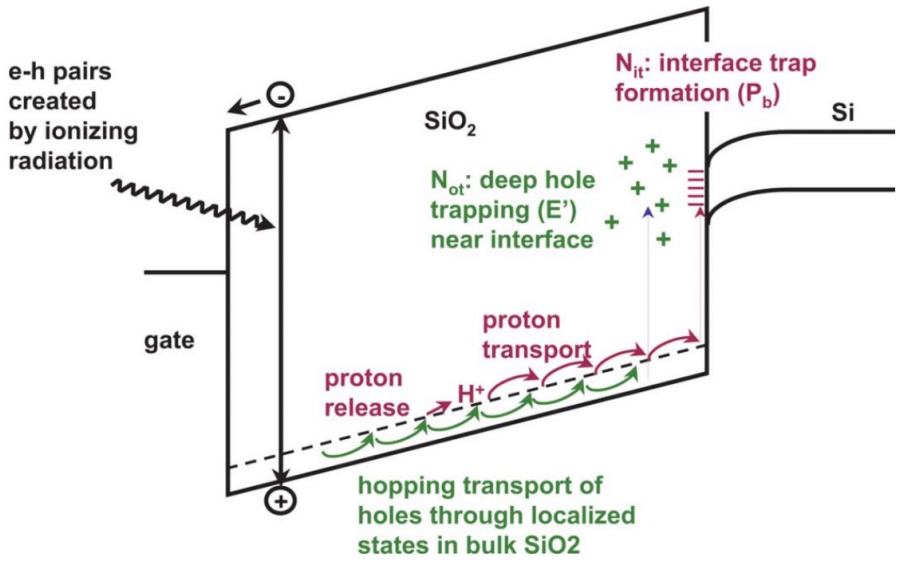


Damage to SiO_2

- In readout electronics, the damage to the SiO_2 and at the Si-SiO_2 interface are more important
- Mainly caused by ionization creating charged defect state in the oxide or at the interface → high electric fields exist in oxides, which separate the charge carriers

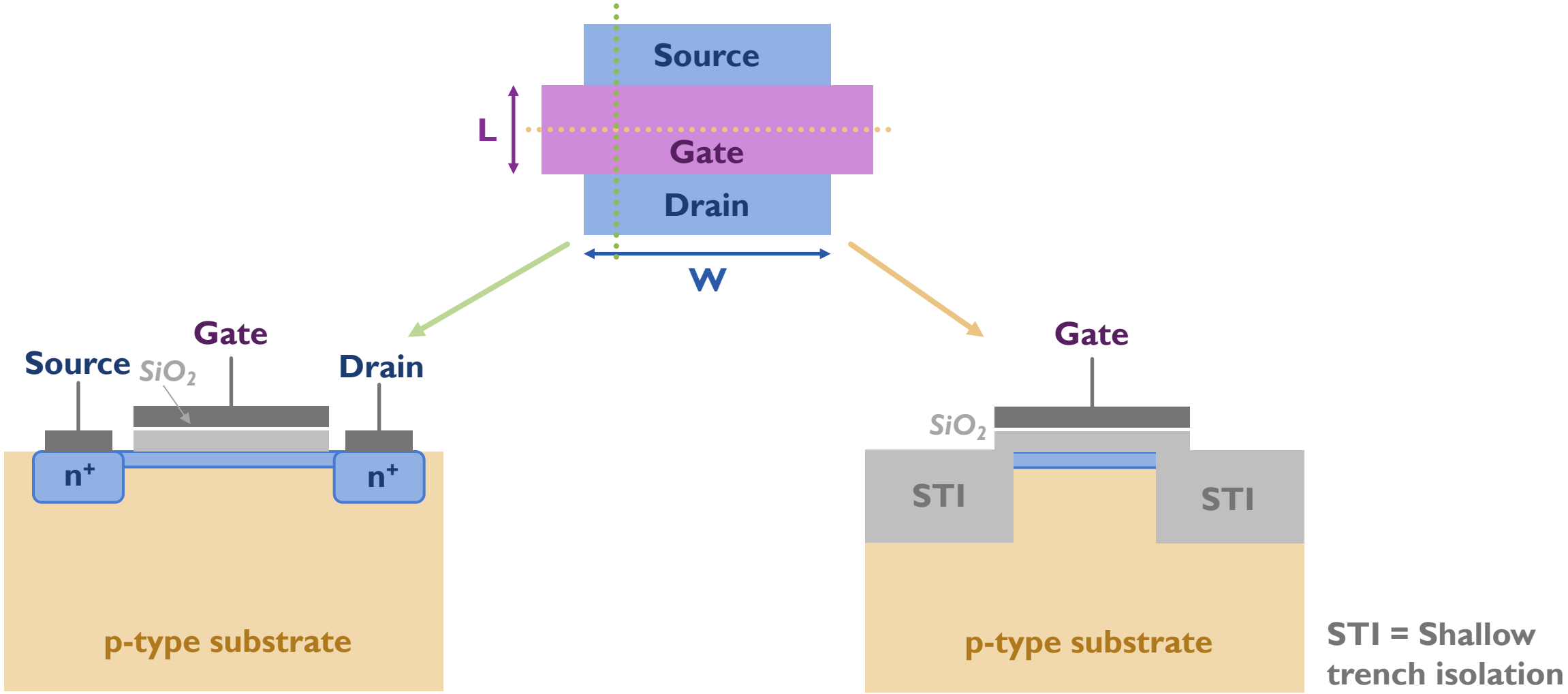
Two different effects to consider:

- Oxide charges (SiO_2) → defects in SiO_2 are always donor-like (positive), occurs relatively quickly
- Interface states (Si-SiO_2 surface)
  - → Impurity hydrogen ions released from lattice
  - → Give rise to new interface states which serve as traps
  - → Slower process due to lower mobility of hydrogen ions
  - → Can be both acceptor and donor like, depending on material
  - → Interface traps are **negatively charged in NMOS** (under positive bias) and **positively charged in PMOS** (under negative bias)



	NMOS	PMOS
Oxide charges	+	+
Interface traps	-	+

Transistors

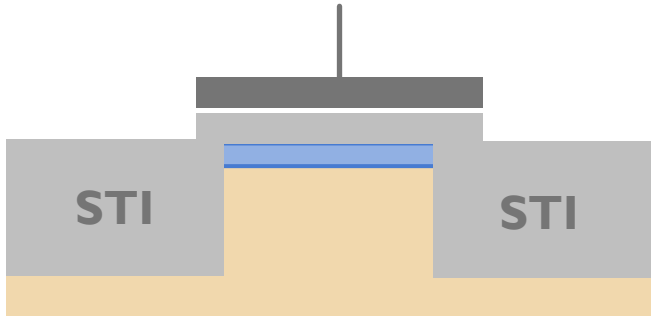


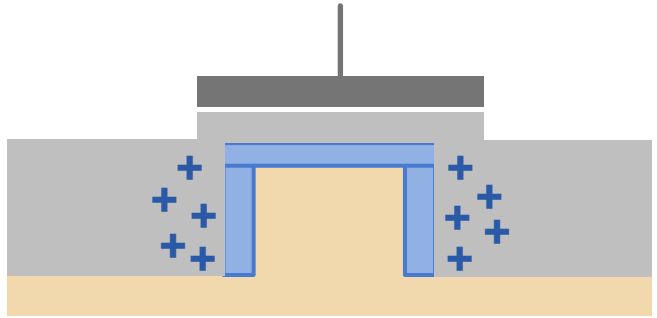
STI = Shallow trench isolation

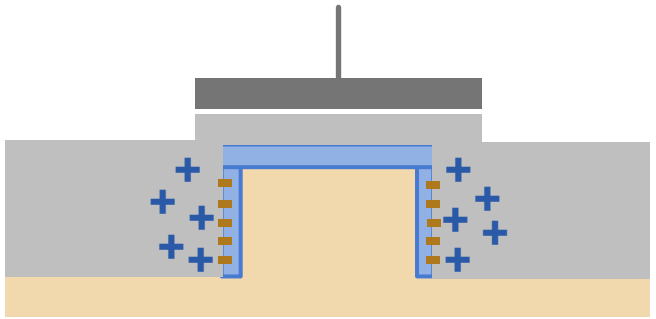
Edge effects - NMOS

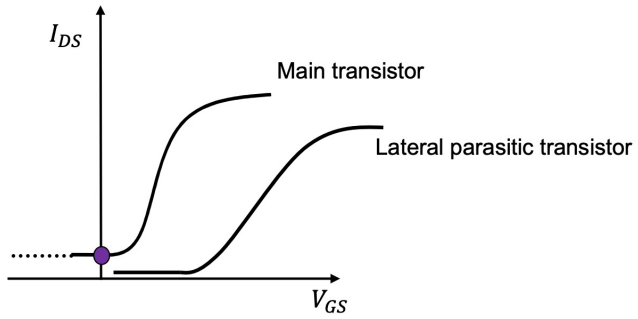
- Depending on transistor type, TID damage effects can look different
- Consider effects of radiation damage in STI
- In NMOS transistors:

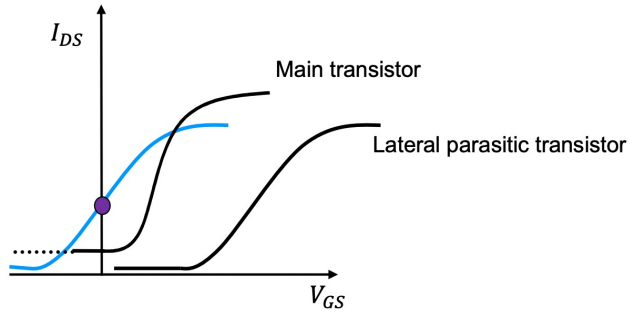
1. Fast build-up of positive oxide charges
   - → opens up another channel through which electrons can flow between source and drain
   - → Leakage current increases
   - → Threshold voltage decreases
2. Slower build-up of negative interface charges
   - → Counteracts the effect of positive oxide charges
   - → Leakage current decreases
   - → Threshold voltage increases

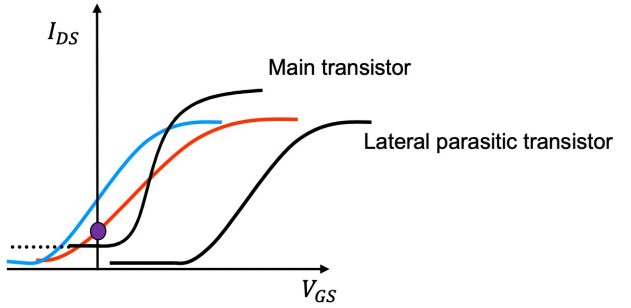










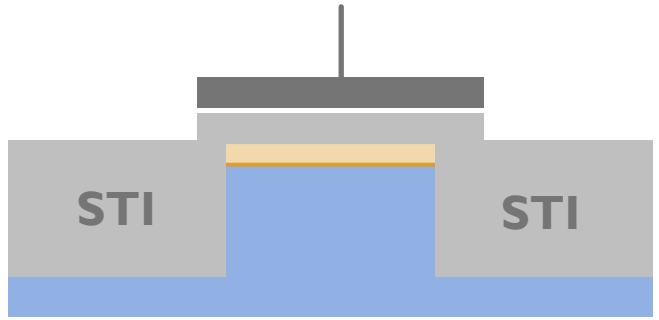


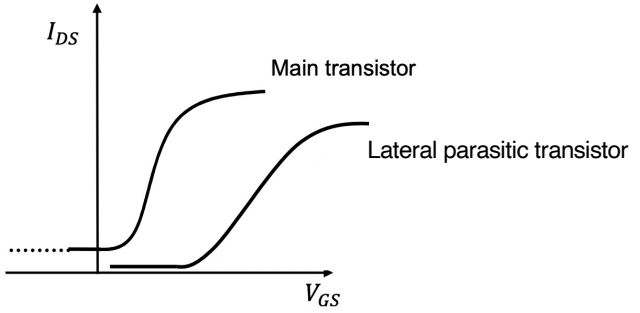
Edge effects - PMOS

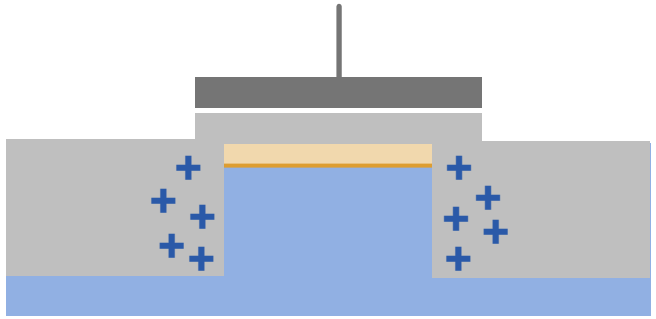
- In PMOS transistors:

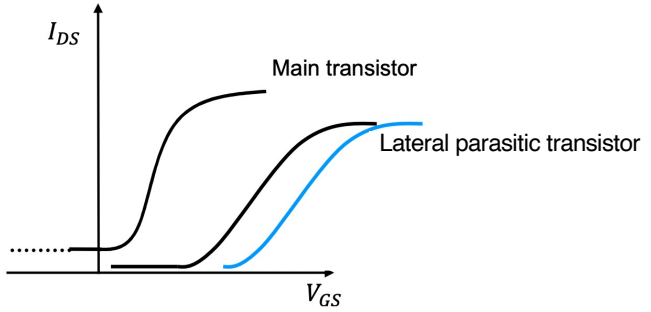
1. Fast build-up of positive oxide charges
   - → Holes in the conduction channel, so no additional channel opens up
   - → Leakage current does not increase
   - → Threshold voltage decreases
2. Slower build-up of positive interface charges
   - → Same effect as oxide charges
   - → Threshold voltage increases further

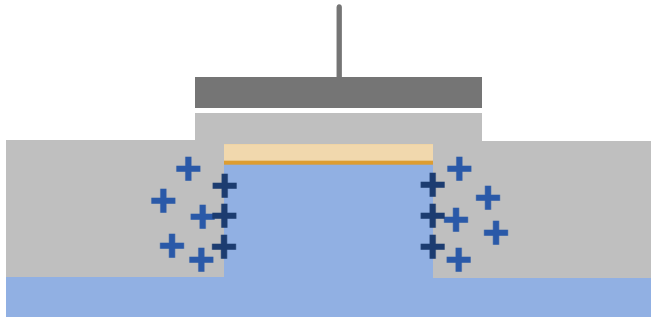
→ Mechanism known as Radiation Induced Narrow Channel Effect (RINCE)

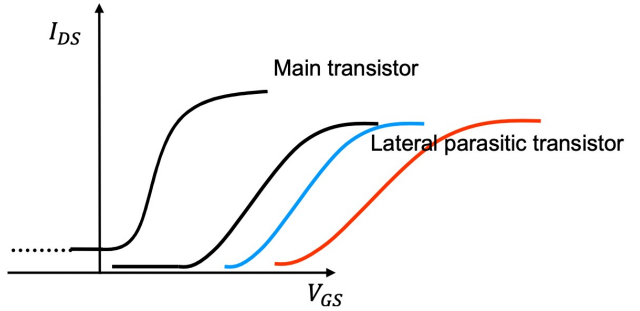








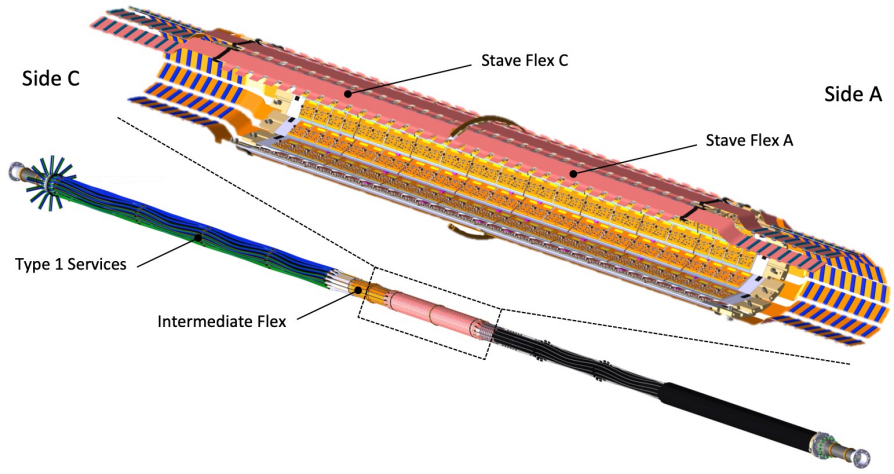


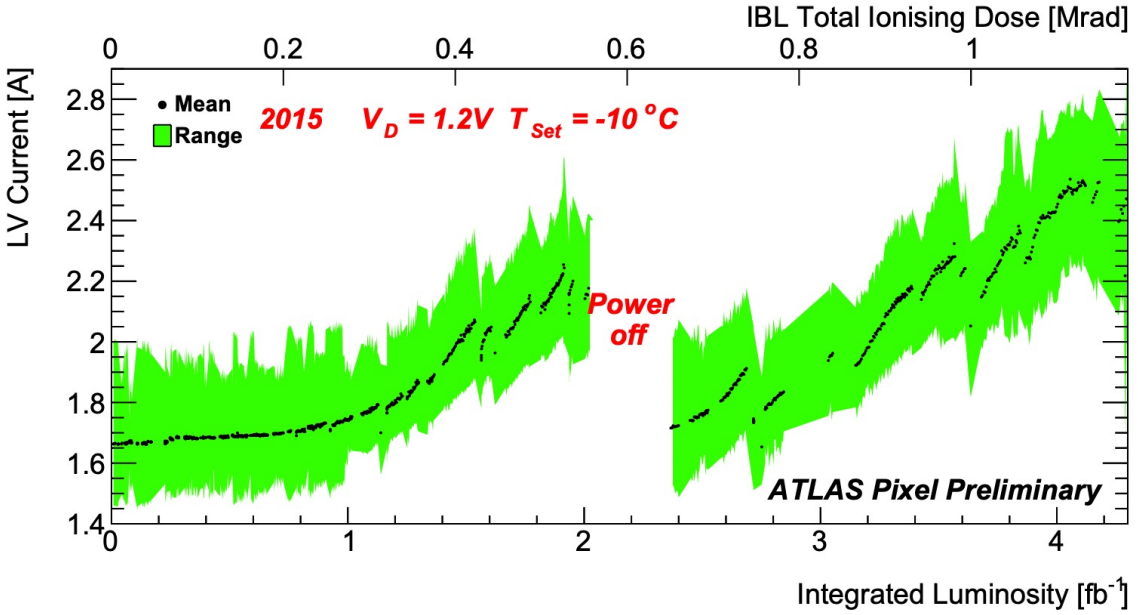


Application: TID bump in IBL

arXiv:1611.00803

- The discussed effects have been observed in detector operation, e.g. in IBL
- IBL is the innermost layer (at r=33.5 mm) of the current ATLAS pixel detector, inserted during LS1
- Readout chip designed at 130 nm CMOS technology → FE-I4
- During operation, LV current of FE-I4 chips increased significantly → Caused by increase in NMOS transistor leakage current
- Leads to various problems: increase in temperature, problems with module tuning



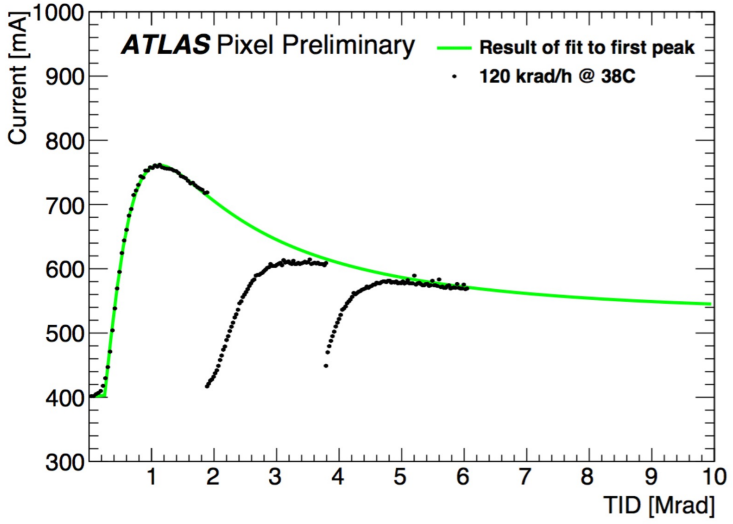


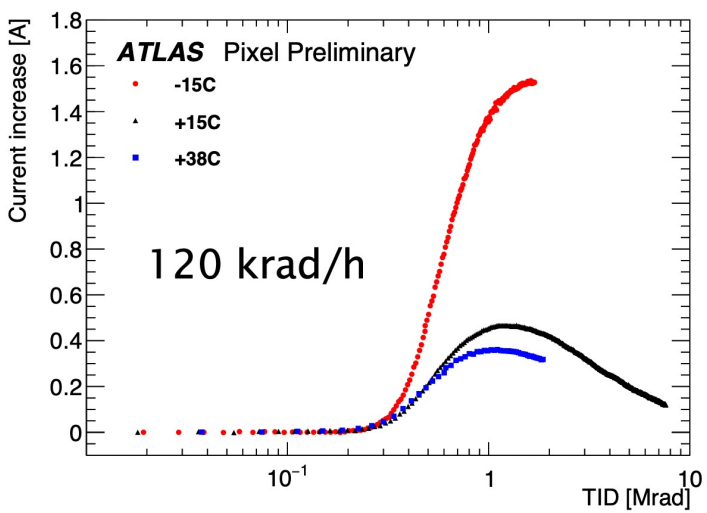
Application: TID bump in IBL

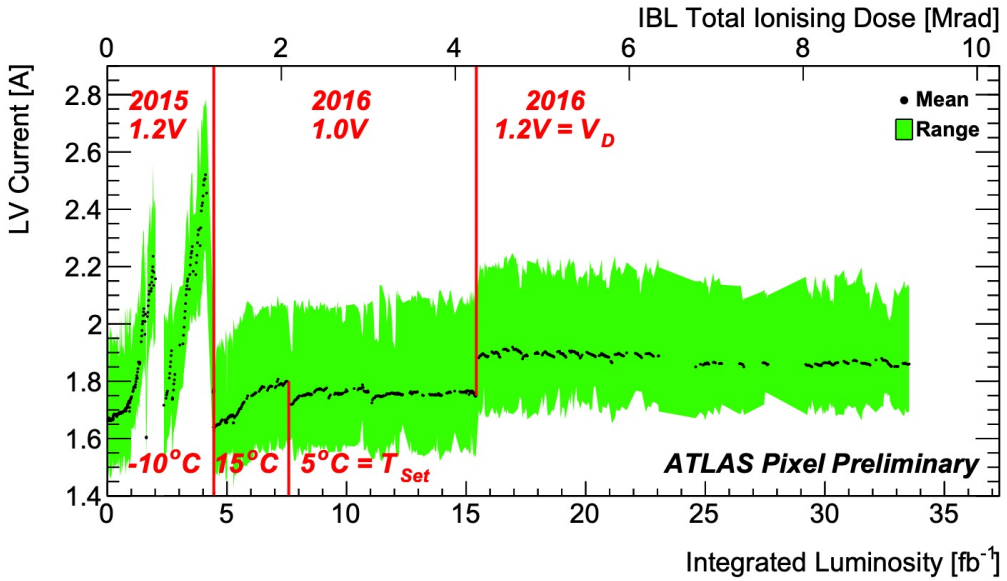
- Effect was studied in irradiation X-ray irradiation campaigns
- Findings: At a given dose rate, the current always approaches the same boundary
- The current increase is larger at higher dose rates and lower temperatures

→ As a consequence, IBL was operated at higher temperatures in 2016 (w/ reduced voltage, later increased again)

- Note: similar behaviour also observed in strips ASIC → reason for pre-irradiation of ITk strips readout chips







Low vs high dose rate

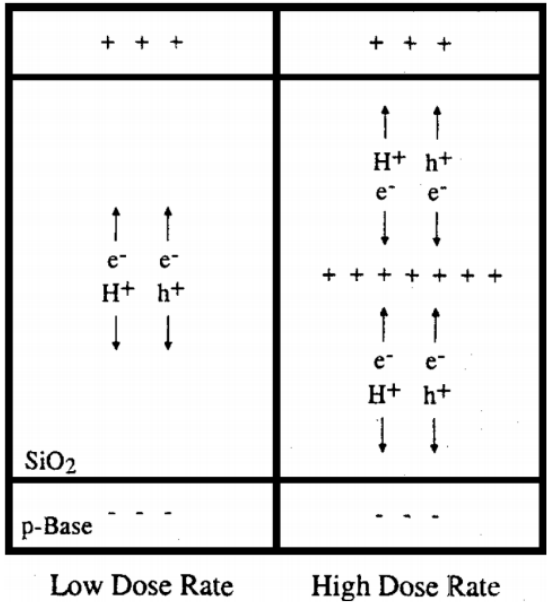


Fig. 1. Simplified representation of space-charge effects taking place during HDRs irradiation in thick oxides crossed by low electric fields (after Witczak *et al.* [6]).

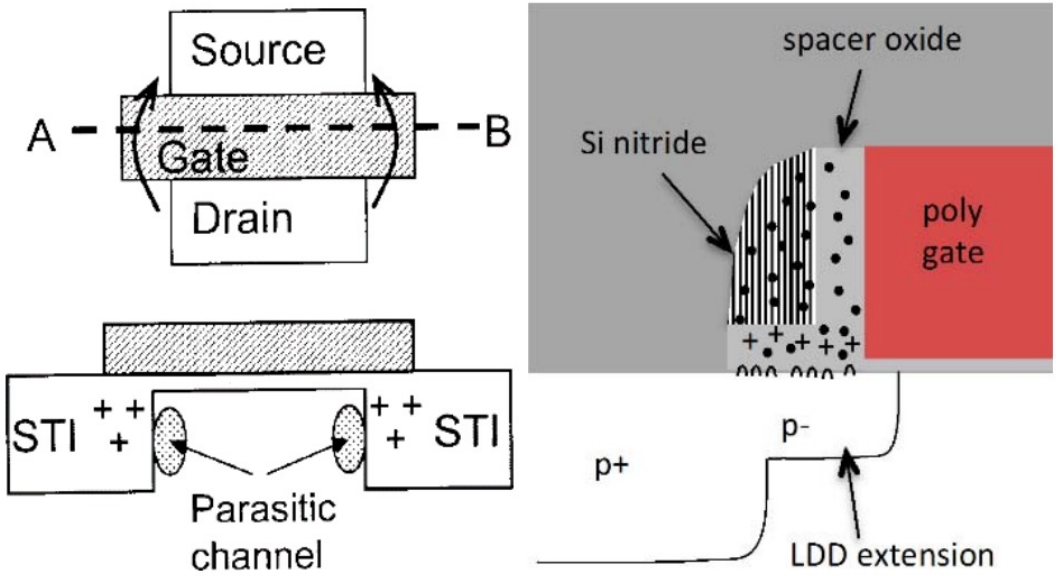


Fig. 2. Schematic illustration of charge trapping in STI field oxides (left) and LLD spacers (right) (after Faccio and Cervelli [12] and Faccio *et al.* [13]).

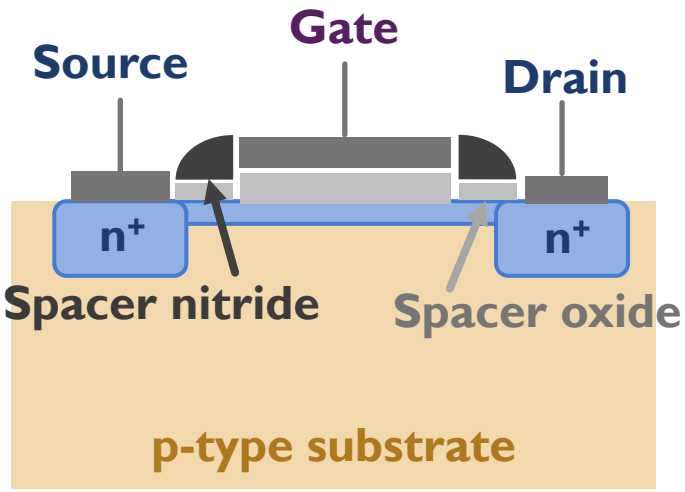
Paper

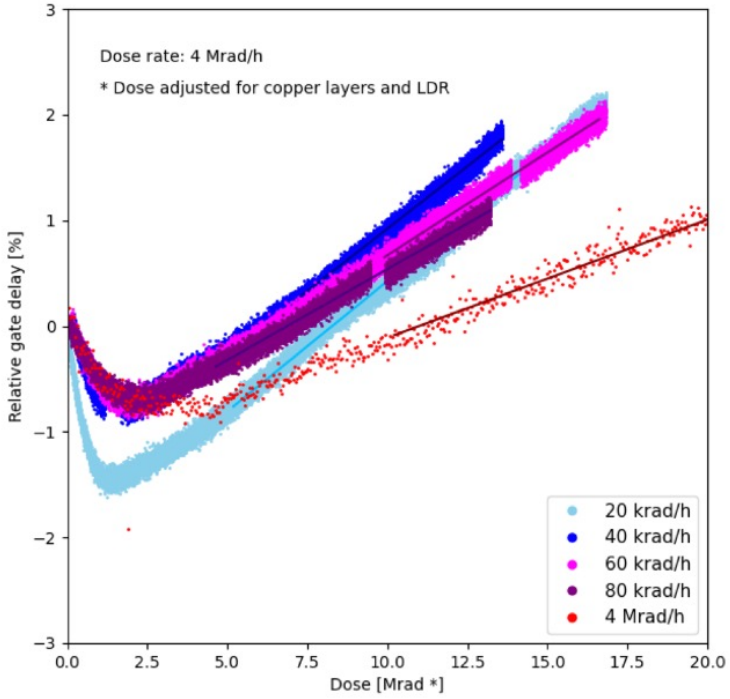
Application: ITkPixV1

- Note: ITkPixV1 chip is produced in 65 nm technology, so the conclusions discussed for FE-I4 do not hold anymore
- Can see some similar features, e.g. ring oscillator gate delay gets smaller briefly before it gets larger

→ Transistor threshold voltage first decreases , and then increases

- Additional mechanisms (radiation-induced short short channel effects - RINCE) are at work in 65 nm, e.g. due to TID damage in spacer regions
- Observations from irradiation campaigns:
  - TID damage is worse at high temperatures and at low dose rates

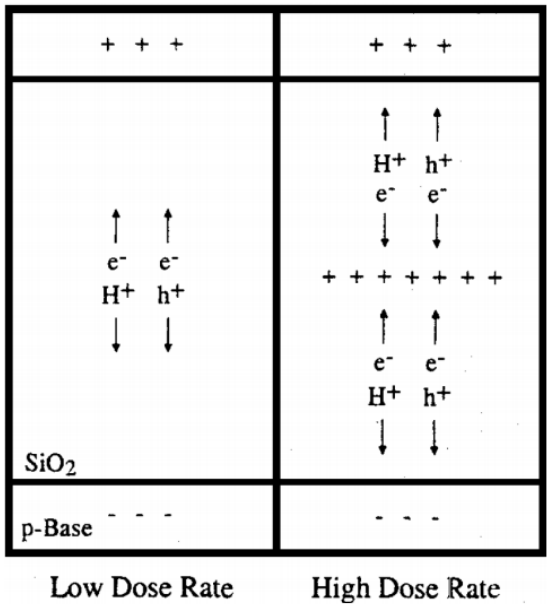


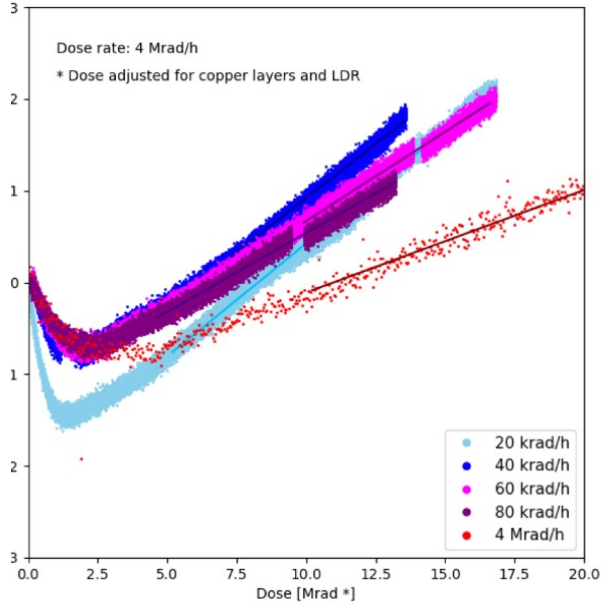


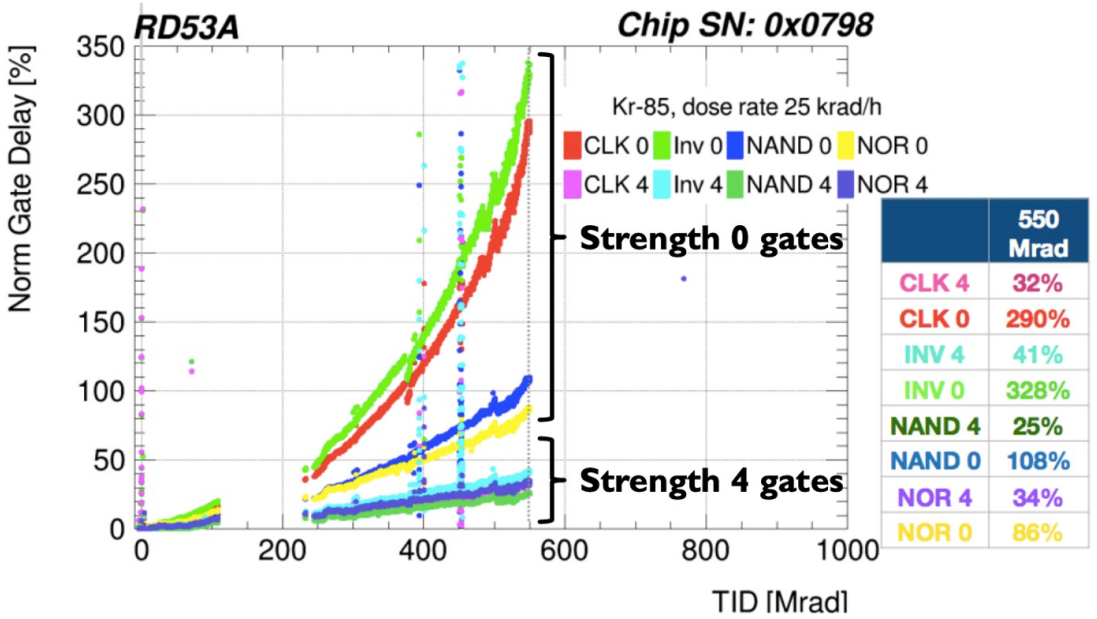
More details in: F. Faccio et al. 1, 2

Application: ITkPixV1 ring oscillators

- Dose rate effects not completely understood
- Studied for ITkPixV1 in X-ray irradiations and long-term Kr-85 irradiations
- Can derive try to conversion factors between low and high dose rates, but they depend on transistor type, size etc.
- Additionally, non-linear effect are observed at very high total doses → not fully understood







	550 Mrad
CLK 4	32%
CLK 0	290%
INV 4	41%
INV 0	328%
NAND 4	25%
NAND 0	108%
NOR 4	34%
NOR 0	86%