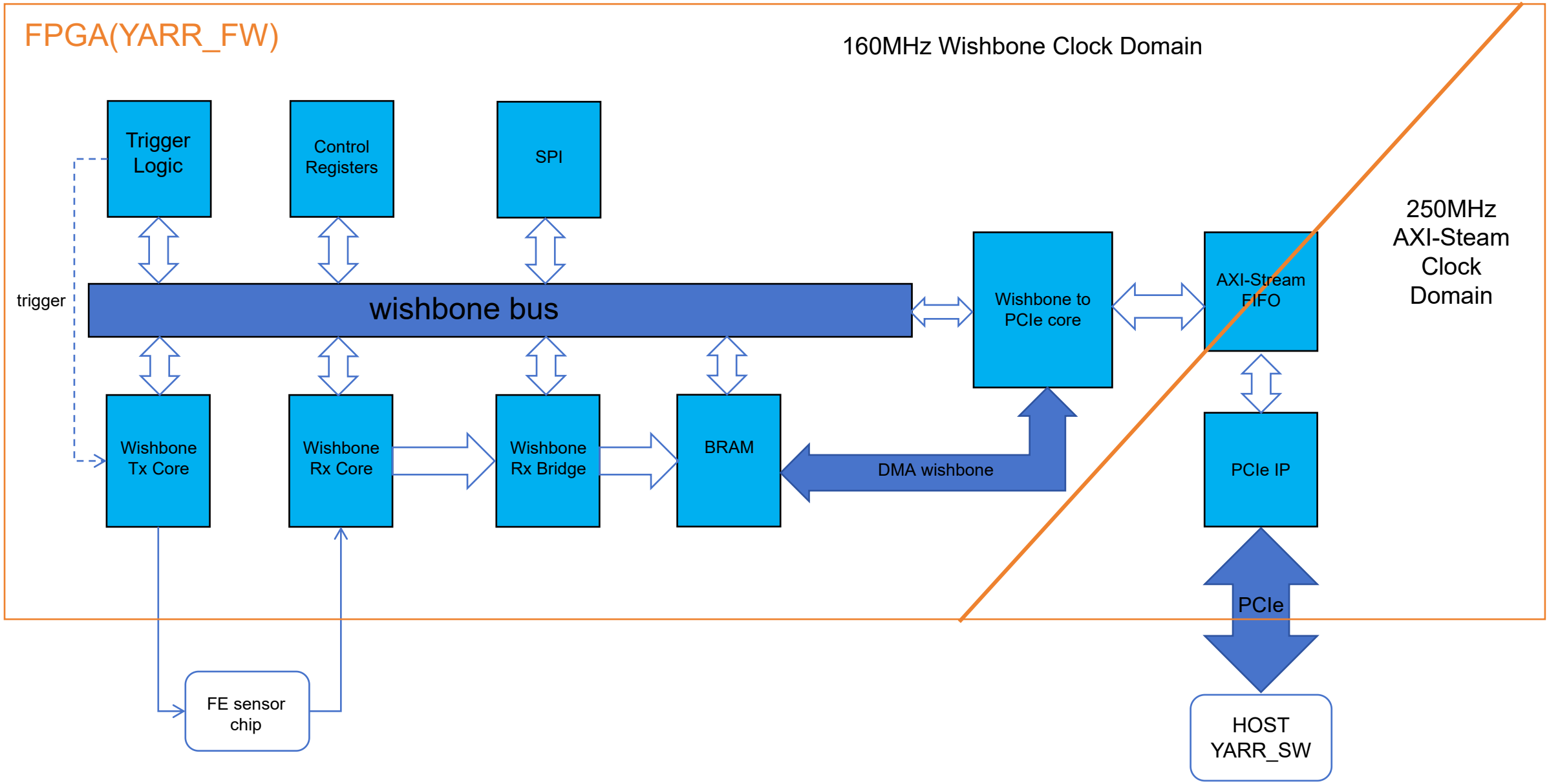
Busy Logic for BRAM

-- HongjiangCai

Wishbone Interconnect Architecture

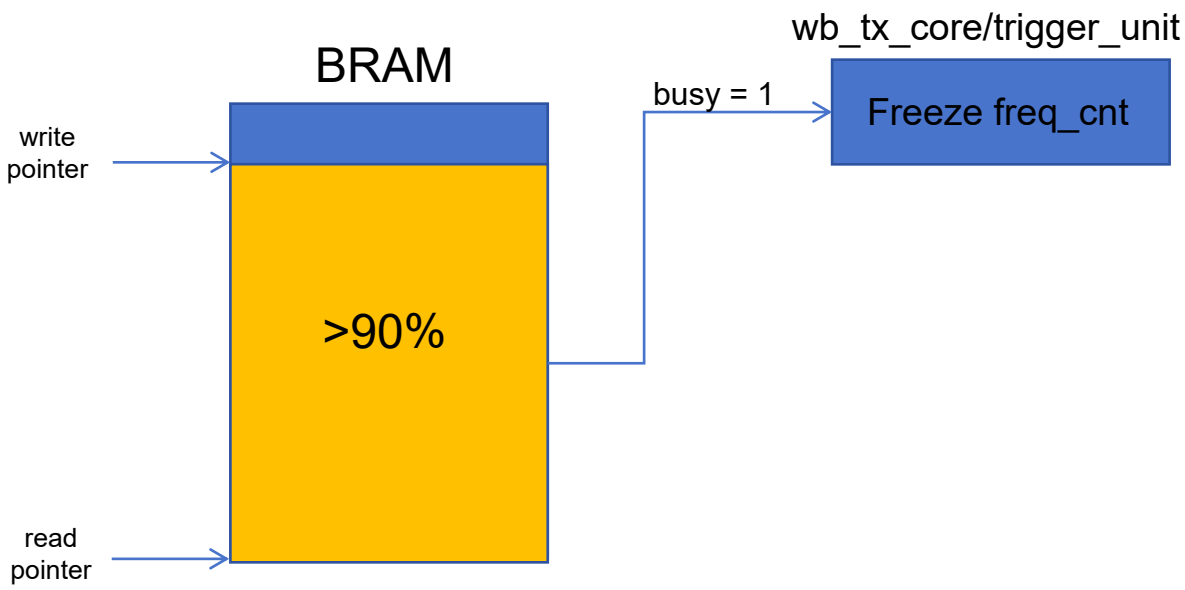


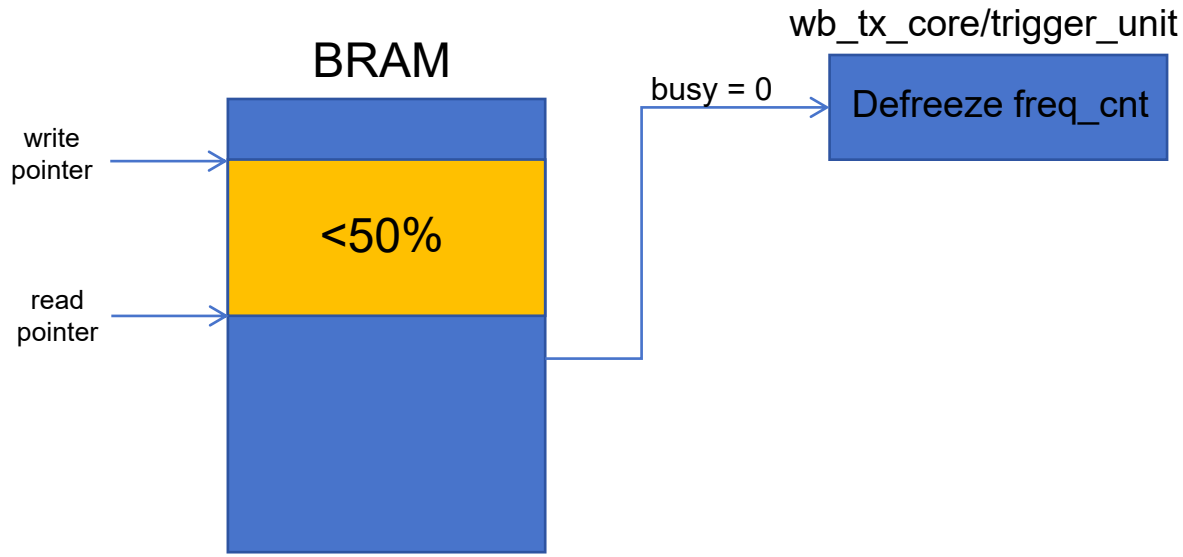
Why busy logic?

- Due to delay on allocating memory during read request, the read from host is slower than write from chips. This cause the difference between read and write pointers in BRAM on FPGA to accumulate.
- Since BRAM is a circulating memory, when difference between read and write pointers exceed its capability, an overwrite can occur and cause transmission error. (This can easily happen when more than 7 chips are connected in current system.)
- Before we fix this read/write speed issue with new read request structure, we need busy logic to prevent BRAM from overwriting.

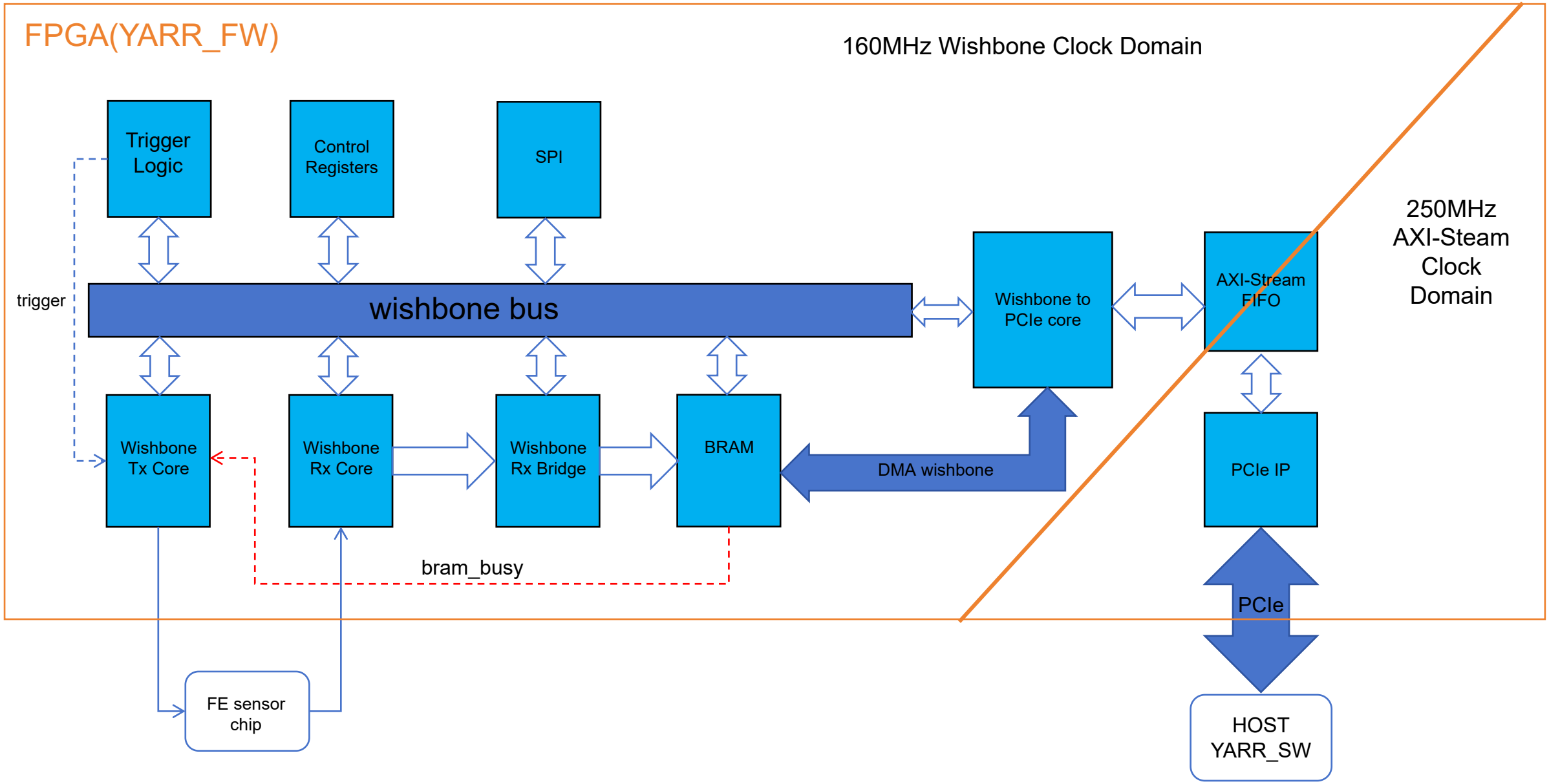
How is busy logic achieved?

- When write pointer exceed read pointer by >90% of BRAM space, busy signal is set high and send to wb_tx_core. When busy, frequency count in trigger_unit of wb_tx_core will freeze so FPGA stop sending trigger to chips.
- Then, after host read enough data out of BRAM (write pointer exceed read pointer by <50% of BRAM space), the busy signal is set low and the FPGA start to send triggers to chips again.





Wishbone with busy logic



Difficulty in implementation

- We don’t actually have registers storing the pointers. Both read and write pointers are kinda virtual in the system. => Need to retrieve these information from the system.

Solution #1

- The BRAM is dual-port. One connected to Rx Bridge mainly for write from the chips. Another connected to Wishbone_to_PCIe core mainly for read from the host.
- We can count the read/write acknowledgements and use the difference as indicator of space used in BRAM.
- Issues:
  - Some software application does read BRAM but not actually move the pointer.

    => Counters need soft reset after executing applications.
  - The read from host has some over-read mechanism to align the memory space.

    => Cause additional read acknowledgements => accumulates and difference between acknowledgement counters becomes much smaller than differences between pointers.

Solution #2

- The BRAM is dual-port. One connected to Rx Bridge mainly for write from the chips. Another connected to Wishbone_to_PCIe core mainly for read from the host.
- Record access address in different ports. Use the difference between address as indicator of space used.
  - Pros: No more acknowledgement accumulation issue from over-read mechanism because over-read mechanism reset the read address after done.
  - Cons: Need to deal with more edge cases.

Leaving LBNL...

- Leaving on Aug, 30th