28 nm TDC design

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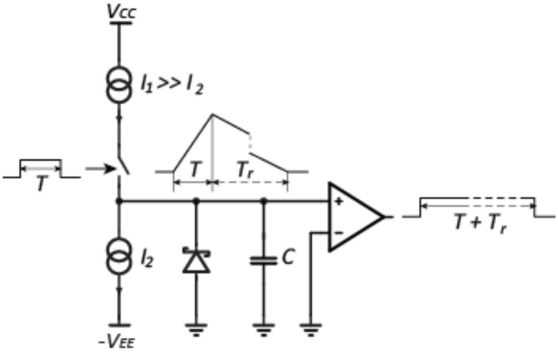
Introduction

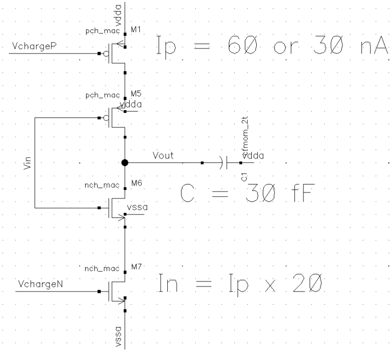
- Goal: design an in-pixel TDC with $\mathcal{O}(50\text{ ps})$ resolution, $\mathcal{O}(\mu A)$ power consumption, $\mathcal{O}(10\text{ ns})$ range (i.e. suitable for ATLAS/CMS pixels)
- Currently most developments are based on delay lines
  - Including TDCs for ATLAS/CMS Phase II timing detectors
  - Pros: can easily obtain ps-level LSB with modern technology
  - Cons: big area, high power, heavily affected by mismatches
  - In the first two submissions of the LBNL 28 nm LDRD chip ("Big Rock" and "PEBBLES"), delay line based TDCs are used as on-chip testbed to characterize the AFE (10 ps RMS, 64 ns range, 50x500μm, 35 mW)

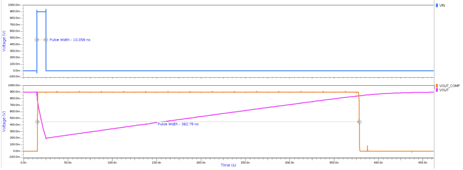
Time stretch method

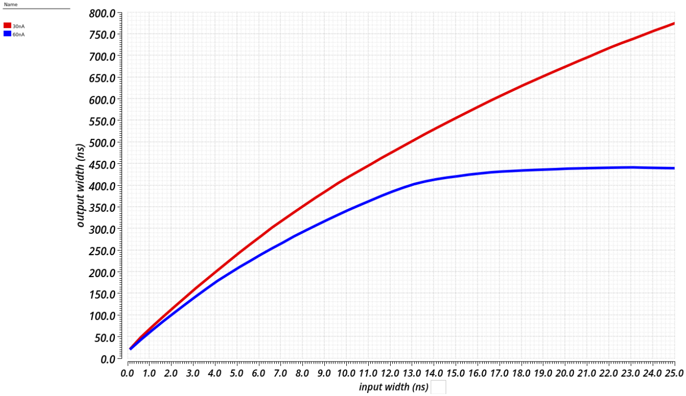
- Fast charge a capacitor in the measured time window, and discharge it slowly after that: discharge time is proportional to charge time → time gets amplified
- Pros: fewer devices/smaller area (no need for long delay line), low power (can use small capacitor)
- Cons: long conversion time (need to keep the hit rate in mind in the design)



Time stretch unit



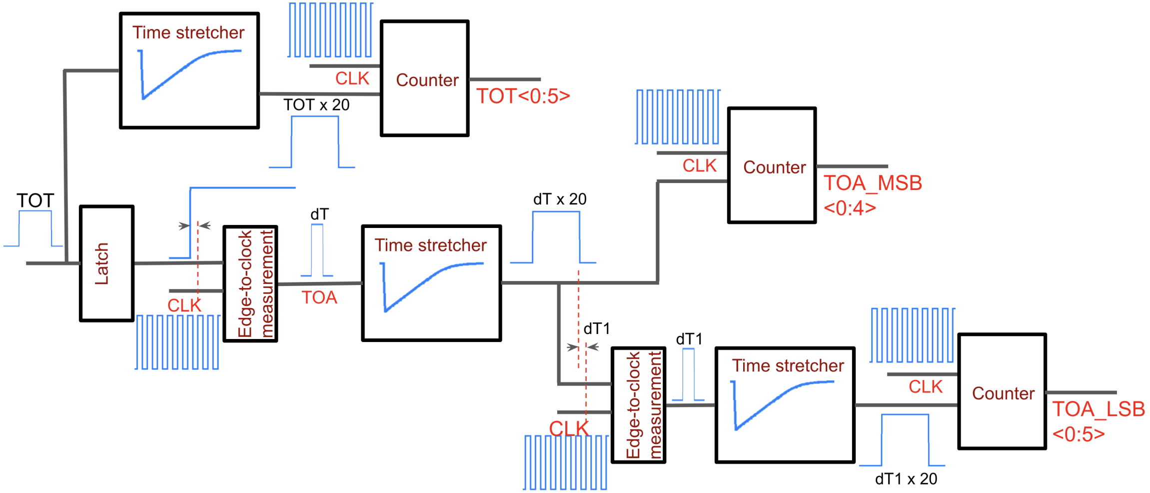




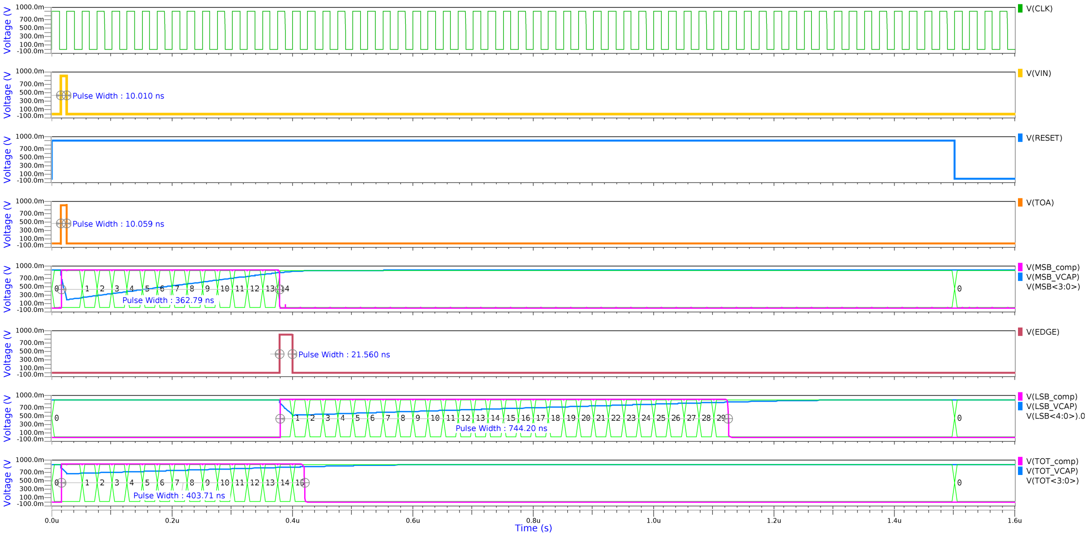
Two stage stretch

- For ATLAS pixel: 100 kHz hit rate corresponds to about 10 μs maximum conversion time
- With a 40 MHz counter to measure the amplified time:
  - For 50 ps LSB $\rightarrow$ amplify time by 500 times $\rightarrow$ 5 μs conversion time for 10 ns range (a bit too long)
  - We can do two stage amplifications: first amplify original pulse by 20 times, then use 40 MHz counter to get MSB, then stretch the remaining pulse by another 20 times to get LSB $\rightarrow$ conversion time can be reduced to $\sim 1\mu$s

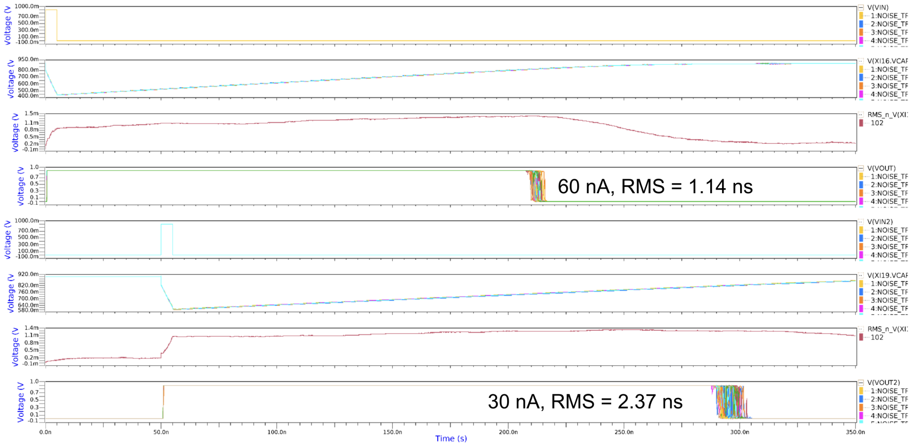
Two stage stretch schematics



Full chain simulation



Time stretcher noise



- Higher charge current $\rightarrow$ less noise, but also smaller range
- For the first stage (60 nA, 13 ns range), effective noise is $1.14/40 \sim 0.03$ ns
- For the second stage (30 nA, 25 ns range), effective noise is $2.37/1600 \sim 0.001$ ns

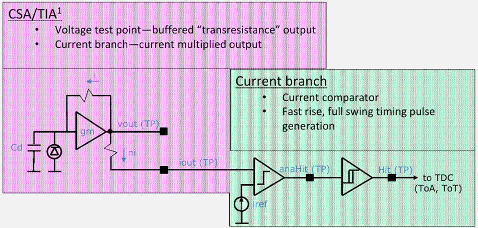
Summary of TDC spec and simulation performance

Variable	requirement	result (simulation)
Time resolution	< 50ps	LSB: $\sim$ 25 ps noise: $\sim$ 30 ps total: $\sim$ 40 ps
Area	$< 30 \times 50\mu$m	$15 \times 13\mu$m analog $23 \times 13\mu$m digital (counters) $38 \times 13\mu$m total
Power	$< 10\mu$W average	$< 5\mu$W during conversion
Range	10 ns	13 ns
Hit rate	$\sim$100 kHz	max conversion time $\sim$ 2 us (500 kHz)

Stay tuned for in silicon test result (coming soon this Fall) !

Backup slides

Analog Frond End



1. Pierre Jarron, et. al, *A transimpedance amplifier using a novel current mode feedback loop*, 1996

Metric	Requirement	Simulated
Idc	~ 4 uA	6 uA
ToA S.D. (0.5 fC inj @ 0.15 fC)	~ 50 ps	50-60 ps
ENC	< 100 e RMS	80-90 e RMS
Threshold S.D.	*	...
Timewalk (1.2 ke – 30 ke)	*	~ 3.5 ns
ToT	*	2-20 ns
Area	< 30 x 30 um	10 x 30 um

ToA Edge Distribution—"jitter"