Module Electrical QC & LocalDB

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on behalf of module electrical QC and LocalDB team

Upgrade week, May 2023

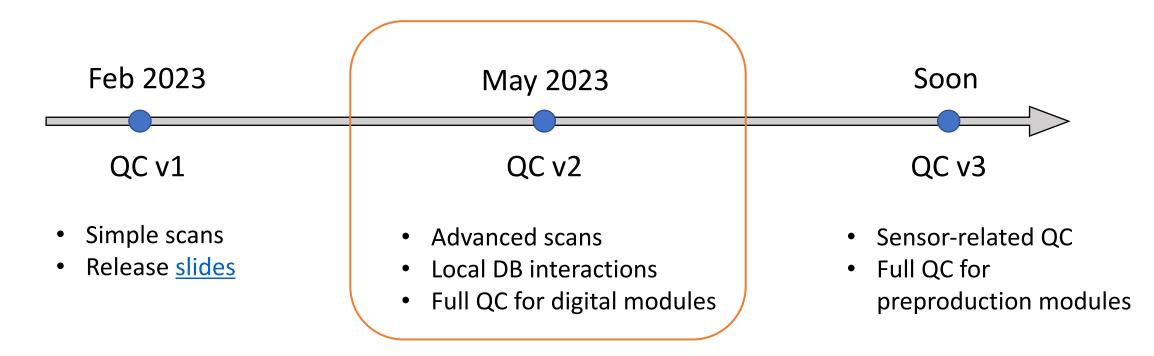
https://indico.cern.ch/event/1223748/





Module electrical quality control (QC): Define testing procedures and specifications to ensure that modules perform electrically well, providing tools for testing

LocalDB: intermediate aggregation place at testing sites of the of the QC data during production



Specifications and procedures are documented: <u>AT2-IP-QA-0025 v.1</u> (latest version on <u>Gitlab</u>)



Electrical specification and QC procedures for ITkPixV1.1 modules

| Project Document No.: Institute Document No.: | Created: 24th | n March 2022 | Page: I of 29 |
|---|----------------|--------------|---------------|
| AT2-IP-XX-XXXX | Modified: 26th | January 2023 | Rev. No.: 0.1 |

For pre-production and production, specifications will change but electrical testing procedure will stay the same

We have currently defined specifications using the pre-production BoM. But all digital modules are using the LBL BoM \rightarrow digital modules slightly out of some spec Full suite of tests:

| Simple | First power-up ADC calibration + update chip configs Analog readback + update chip configs SLDO qualification Vcal calibration + update chip configs Injection capacitance + update chip configs Low power mode Over voltage protection |
|----------|--|
| scans | Over-voltage protection Undershunt protection (QC v3: not ready) |
| | 10. Data transmission (QC v3: not ready) |
| | 11. Link sharing (QC v3: not ready) |
| Advanced | 12. Minimum health test |
| \prec | 13. Tuning + update chip configs |
| scans | 14. Pixel failure analysis |

Section 3 of <u>electrical QC document</u>

The goal of these tools is to:

- Make electrical testing procedure easier and faster
- Standardize testing across different sites

| Measurement | Analysis | Database interactions |
|------------------------|-------------------------------------|--|
| <u>module-qc-tools</u> | <u>module-qc-</u> analysis-tools | <u>module-qc-</u> <u>database-tools</u> |

Python-based packages with minimal requirements for use:

- Computer with <u>YARR</u> and >=Python3.7
- Command-line control of lab equipment (i.e. labRemote)

Thank you to QC-v2 developers:

Kehang Bai, Timon Heim, Kosuke Itabashi, Marija Marjanovic, Lingxin Meng, Maria Mironova, Hideyuki Oide, Elisabetta Pianori, Giordon Stark, Emily Thompson, Connor Waits

Documentation in README's

| README.md |
|--|
| module-qc-tools v1.3.2rc0 |
| A general python tool for running ITkPixV1.1 module QC tes |
| Table of contents |
| 1. Requirements |
| 2. Installation |
| 3. Usage |
| 4. Configuration and external commands |
| 5. Measurements |
| 1. ADC calibration |
| 2. Analog readback |
| 3. SLDOVI |
| 4. VCal calibration |
| 5. Injection capacitance |
| 6. Low Power Mode |
| 7. Overvoltage protection |
| 6. Output data |
| 7. Schema check |
| 8. Time Estimates |
| 9. Upload results to localDB |
| 10. For developer |

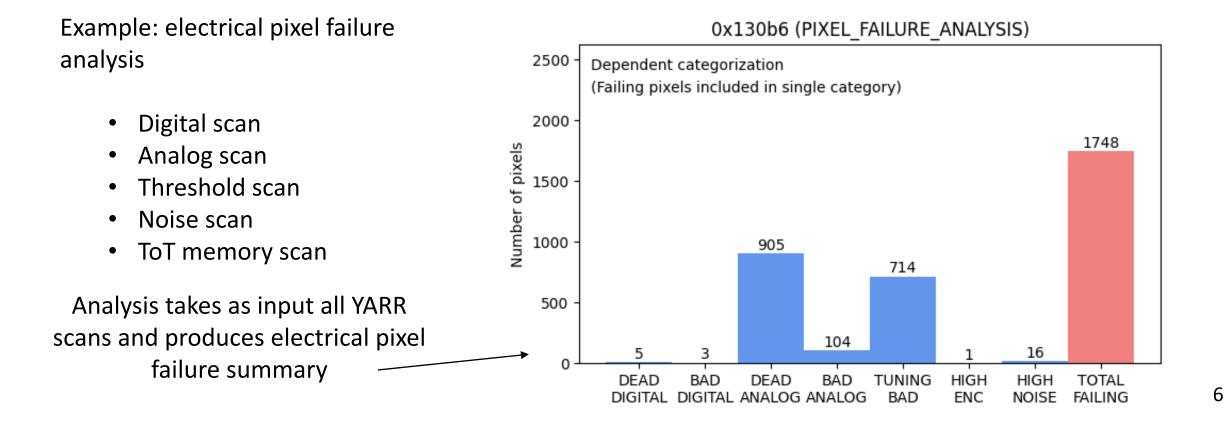
New in QC-v2

Analysis of advanced scans has been integrated into QC-tools framework



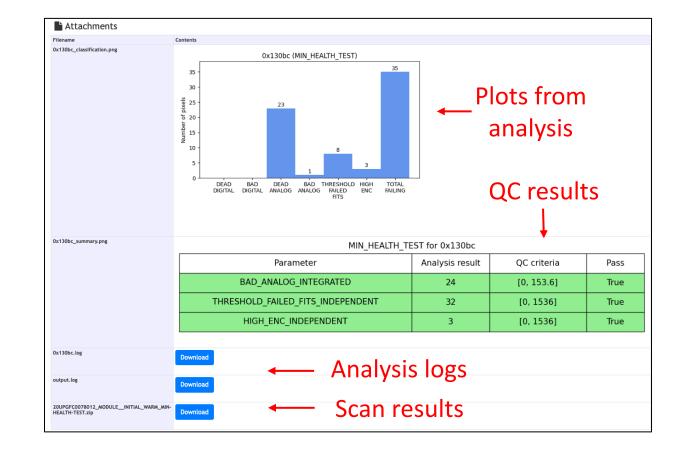
Advanced scans: minimum health test, tuning, and electrical pixel failure analysis

Each advanced scan requires user to run YARR scans – see <u>Appendix B.9</u> for details



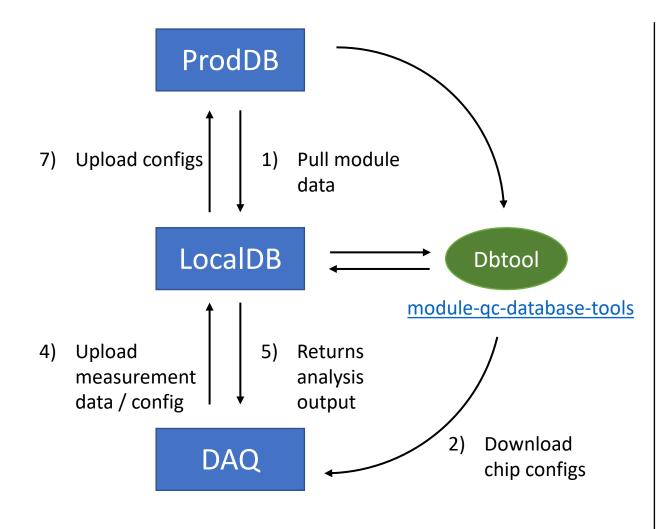
Implemented full QC flow with QC-tools and LocalDB / prodDB communication

(screenshot of simple scan analysis output)



New in QC-v2: Communication with LocalDB

QC-v2 workflow:



3) Run measurement 6) Update chip configs <u>module-qc-tools</u> <u>module-qc-analysis-tools</u>

Major change since QC-v1: analysis of QC data performed in LocalDB

We have tested this workflow at LBNL – it works!

All steps except first and last are bash-scriptable (example from LBNL)

Notes:

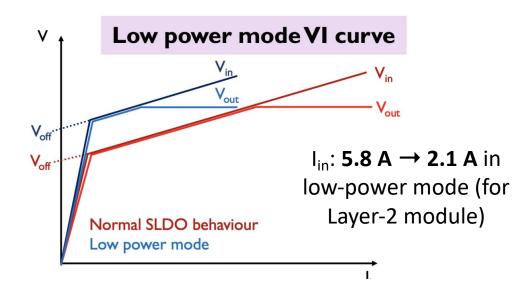
Step 2: The Dbtool will obtain chip configs from previous stage or if not present, will generate from wafer probing

Steps 4-5 performed together: on upload LocalDB performs analysis and returns results when finished

Steps 3-6 repeated for each simple scan. Advanced scan workflow differs slightly (see backup)

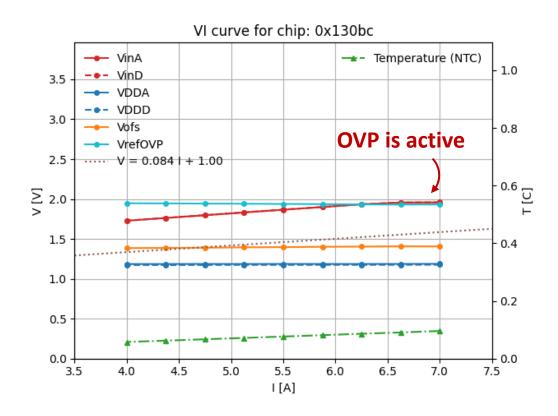
More simple scans have been integrated into QC-tools framework

Low-power mode increases V_{offset}, allowing for chip to become operational for testing at lower I_{in}



- Low-power mode switch implemented in <u>firmware</u>
- Requires special low-power chip configs

Over-voltage protection (OVP) prevents V_{in} from exceeding 2V. OVP is tested in low-power mode.



How long does it take to perform electrical QC on a quad module?

| Measurement | Analysis |
|-------------|----------------------------------|
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| TBD | TBD |
| TBD | TBD |
| | |
| | |
| | |
| TBD | TBD |
| | |
| | Measurement TBD TBD TBD |

We have some ideas for speeding up simple scans

- re-write scans to reduce number of times needed to upload configs
- reduce granularity
- remove duplicate measurements of GND

Next steps for module electrical QC (QC-v3)

We have made significant progress in previous 3 months, and we have a clear path forward on missing items:

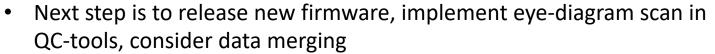
| | | Stage 1 (dig | gital module) warm | | Stage 2(full QC) | | | | | | |
|------------|----------------|--------------------------------|-----------------------------|-----------------------------|-------------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Step | 1 | 2 | 3 | 4 | | spec | procedure | measurement | analysis | local db | database |
| | first power-up | | | | | \checkmark | \checkmark | NA | NA | NA | NA |
| | | config from DB (Wafer probing) | | | | NA | NA | | NA | NA | |
| | | C | ADC calibration | | | \sim | \checkmark | | \checkmark | \checkmark | \checkmark |
| | | | Analog readback | | | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark |
| | | | SLDO VI | | | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark | \checkmark |
| _ | | | Vcal calibration | | | \sim | \checkmark | | \checkmark | \checkmark | \checkmark |
| _ow | | | Injection Capacitance | | | \sim | \checkmark | | \sim | | \checkmark |
| Low level | S | imple 丿 | | config from DB (elec QC) | | NA | NA | | NA | NA | |
| | S | cans | | LP mode | | \sim | \checkmark | | \checkmark | | |
| | | | | Undershunt protection | | | | | | | |
| | | | | Data Transmission | | | | | | | |
| | | | | Overvoltage protection | | | | | | | |
| Adv | vanced | Min. health test | | | | \sim | \checkmark | | \checkmark | | |
| Hig | cans \prec | | Tuning | | | | | | | | |
| High level | | | (Elec) Pixel Failure 1.0 | ſ | Pixel Failure 2.0 | | | | | | |
| - | | | Sensor-relate | d OC | source scan | | | | | | |
| | | | | | disc bump | | | | | | |
| | | | | | 0-bias | | \checkmark | | | | \checkmark |

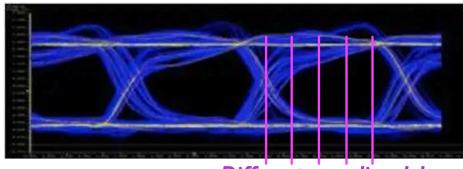
Only two remaining simple scans needs to be integrated:

- 1. Under-shunt protection Lowers V_{ref} to reduce I_{load} if I_{load} approaches I_{in}
 - Testing procedure has been proposed specifications and integration into tools still needed
 - See recent <u>update</u> from Konstantin Mauer

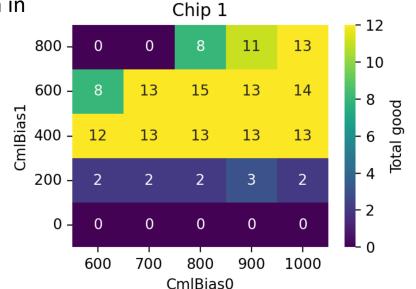
2. Data transmission

 Operation at 1.28 Gbps is more stable after adding new deserialiser in YARR firmware, allowing for manual varying of sampling delay (see recent <u>update</u> from Maria Mironova).





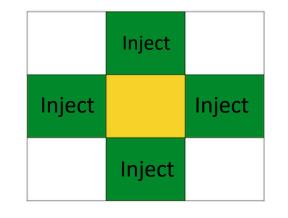
Different sampling delays

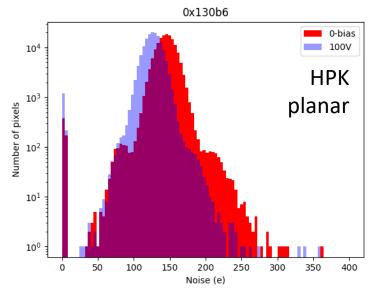


Full pixel failure test – following scans have been partially **implemented into QC-tools framework**, but **missing procedure / specifications** – we need all module / sensor types to converge quickly

- Merged bump scan
 - Inject moderate charge into neighboring pixels, do not expect cross-talk unless merged
- Disconnected bump scan
 - Inject very high charge into neighboring pixels, expect crosstalk if connected
- Zero-bias scan
 - Compare noise from threshold scan with and without sensor biased
- Source scan
 - Run source scan, expect hits if connected

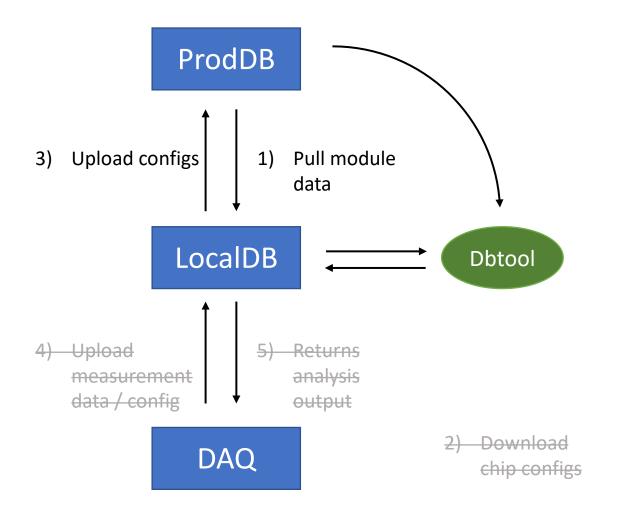
We will develop procedure and specifications based on what we have available at LBNL (currently two modules, one HPK planar and one Advacam micron)





Coming soon in QC-v3

QC-v3 workflow:



2) Run measurement 6) Update chip configs module-qc-tools For QC-v3 (full QC flow), we envision:

Simplified workflow, further automation

- No handling of chip configs in local file system
- YARR communicates directly with localDB, obtaining chip configs when running measurements
- Update of chip configs happens in localDB with analysis
- Wrap in GUI: no need to open terminal

Site qualification update

Qualification for blocks 11.1-11.3 is progressing

We will release qualification for block 11.4 (advanced scans) soon, and am working towards what is needed for sensor-related QC with pre-production modules

Mention how many sites have qualified?

Review team:

Electrical QC coordinators + Abhishek Sharma, Jon Taylor, Yannick Dieter, Anastasia Kotsokechagia, Emily Thompson

Email us:

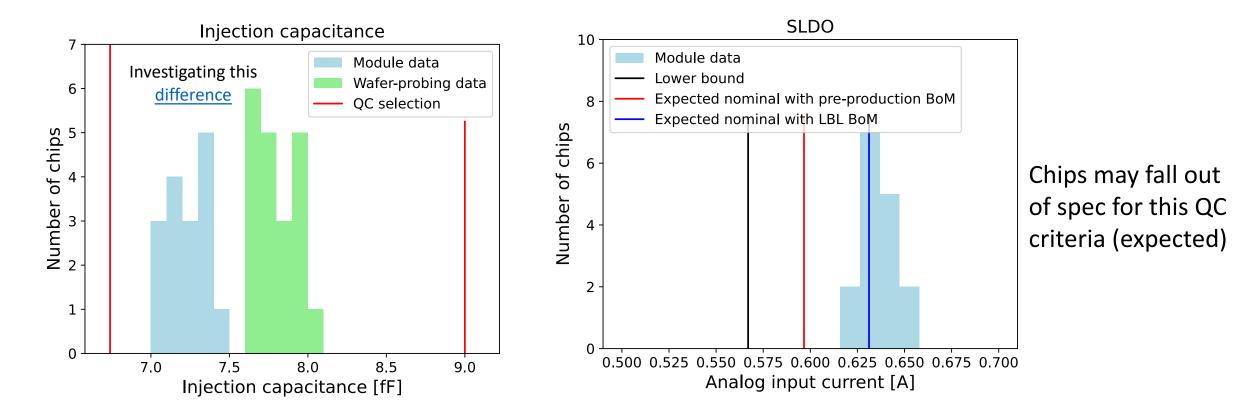
itk-pixel-module-electricalQCreview@cern.ch

| 11 | Digital module tests | | |
|----|----------------------|--------------------------------------|-------|
| | 11. | 1 First power-up | TRUE |
| | 11. | 2 Minimal tests | TRUE |
| | 11. | 3 Simple scans | TRUE |
| | 11. | 4 Advanced scans | FALSE |
| | 11. | 5 Swapping module | FALSE |
| | 11. | 6 Quad & Triplet Complementary stage | FALSE |

From Module Site Qualification

Update this

Analysis of 5 digital modules tested at LBNL:



Next steps: More in-depth analysis, perform analysis from data in prodDB, allow comparison of module QC results at different stages.

- We have framework for full workflow in place including simple scans, advanced scans, and communication with LocalDB
- Adding / changing electrical tests will be significantly easier now that we have framework in place
- Our focus in the next few weeks:
 - Finishing up simple scans
 - Sensor-related QC
 - Releasing remaining site qualification blocks
 - Improving / speeding up workflow

Backup

Resources

Electrical QC Documentation:

- Module electrical QC document (<u>EDMS</u>, <u>Gitlab</u>)
- Module QC Stages and Tests
- Module Site Qualification
- Template for module QC qualification (11.1-11.3): <u>template</u>

Support:

- <u>Electrical testing meeting</u>: **Tuesdays, 5 pm CET**
- Follow regular updates from electrical QC in Module WG meeting: Thursdays, 4 pm CET
- The <u>Mattermost</u> Electrical Testing channel
- Make an <u>issue</u> on gitlab : report problems encountered during testing, helps keep discussions in the same thread if mattermost gets too hectic
- Above support is sufficient so far, however module QC group will setup "office hours" if needed

LoclaIDB useful links:

Local Database User Support mattermost

LocalDB documentation

LocalDB issue tracker

LocalDB demo videos

Development of tools

https://gitlab.cern.ch/atlas-itk/pixel/module

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| | Maintainer | ★ 3 | 16 hours ago |
| | Maintainer This project contains the code used to analyze the data from electrical testing of | ★ 2 | 16 hours ago |
| | M module QC database tools 合 | ★ 0 | 23 hours ago |
| | 🗇 I itkpix-electrical-qc 🕂 | ★ 2 | 1 day ago |
| | 3 days ago | | |

So far we have received **positive and constructive feedback** – we encourage users to document their difficulties / questions in issues so we can develop in a transparent way

People can contribute! Get in touch with us if you want to help develop.

Follow technical discussion of tools at the <u>Electrical testing</u> <u>meeting</u> (Tuesdays, 5 pm CET) Eventually we will use QC data from pre-production to optimize QC procedure in production

We are not there yet. At the moment we want to collect data to:

- Adjust QC specifications
- Understand what is the module yield driver
- How frequently do we need to re-perform tests? Do chip parameters change? If so, why?

To facilitate analysis of QC results prior to prodDB-readiness, we have setup submission to google sheets via module-qc-analysis-tools

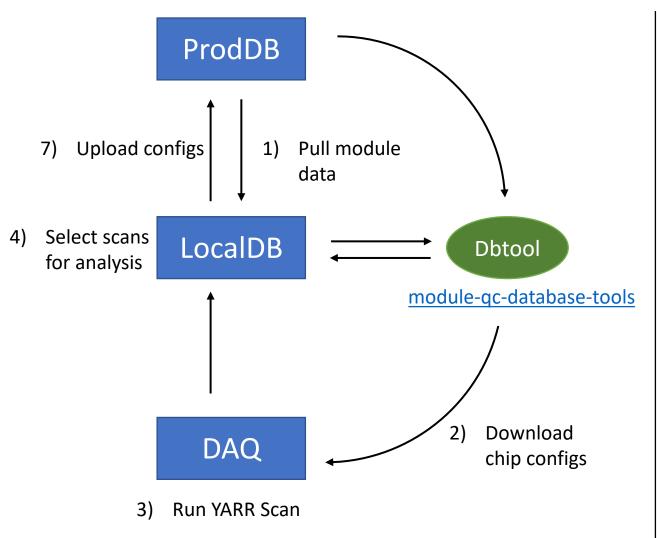
- Module-qc-analysis-tools will produce URL's (1 / chip / test), and user needs to copy/paste URL into browser to submit results (details in <u>SQ template</u>)
- View submitted results <u>here</u>

| Failure | Scan type | Criteria |
|--------------------|-----------------|---|
| Digital Dead | Digital Scan | Occupancy<1% of injections |
| Digital Bad | Digital Scan | Occupancy $< 98\%$ or $> 102\%$ of injections |
| Analog Dead | Analog Scan | Occupancy<1% of injections |
| Analog Bad | Analog Scan | Occupancy<98% or>102% of injections |
| Tuning Bad | Threshold Scan | Pixel threshold - Mean threshold distribution $> 5 \times 40e^*$ |
| High ENC | Threshold Scan | Mean pixel noise $< 200e$ (L0) or $< 300e$ (L1/L2) |
| Noisy | Noise Scan | Occupancy> 10^{-6} hits per BC |
| ToT Memory Failure | ToT Memory test | Occupancy $<100\%$ of injections |

Table 10: Electrical pixel failure categories

From electrical QC document

QC-v2 workflow (advanced scans):



Notes:

Step 2: The Dbtool will obtain chip configs from previous stage or if not present, will generate from wafer probing

Steps 3: YARR runs scan, updates chip configs locally, and uploads scan results and updated chip configs to LocalDB

Step 4: User selects YARR scans on LocalDB viewer to perform complex analysis

Steps 3, 4 is repeated for each advanced scan.

Qualification for blocks 11.1 – 11.3 released, coming soon: 11.4 - 11.5 and 12.2

How does qualification work?

- 1. Sites follow directions in <u>electrical QC document</u>
- 2. Sites are required to use some tools (database, analysis) and strongly encouraged to use measurement tool
- 3. Sites get help via <u>mattermost</u>, creating an issue in <u>gitlab</u>, or by attending <u>electrical QC meeting</u>
- 4. When ready, they prepare slides following <u>template</u>
- 5. Upload slides + material to cernbox, use SQ webapp to upload link, send an email to electrical QC coordinators