QT Status

Luc Le Pottier

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Overview

- Charge Injection for Magnetic Triggering
  - Still is not working
  - Error is always related to external triggers not being seen
  - This error **doesn't** happen unless we try to inject charge
  - I've done a number of debugging tasks on this (detailed in next few slides)
  - In general, we are going to try a few more things, and then wrap up
- QT Future
  - Starting the transition into the second part of my QT
  - This involves developing a suite of tests for the powerboards on modules
  - Starting discussions & work now.

Things I tried this week

Through discussions in `ITSDAQ-talk`, I've ruled out various things that I was considering as causes for our problems:

- Low trigger rate doesn't matter (limited regular 3PG data taking rate and found that everything still worked)
- Despite slow network connection, it should be fast enough for what we need (thanks Peter)

Bruce recommended checking various HSIO registers that indicate whether the external triggers are being recognized, finding the following:

- Wrote a utility which checks whether certain HSIO registers are increasing or not
- Used this to log when triggers are running at various points in both a normal and an external 3PG scan
- This can be used to monitor the value of any hardware registers throughout a scan

Things to Try:

I had a long meeting with Bruce, where we came up with a few ideas:

- **Change the trigger type** after burst setup calibration and run External3PG → should see 3PG with no charge injected at all (sanity check for the errors)
  - **Did this**, found that the scan ran normally. This implies that the burst setup is the problem.
- Try running **manual bursts** for debug, rather than an entire scan. That way we can iterate more quickly once we know that the problem comes from the burst setup calibration.
- Try **increasing/decreasing the trigger rate** - apparently our trigger rate could be either too high or too low
  - 20KHz rate might be too high for the charge injection pulse cycle time?
  - Or, 20KHz might be too low - you could see more HPR packets than triggers (this doesn't seem right to me)
- Bruce tried to write a testing script for me after our meeting, which I have been experimenting with.
- Lastly, we discussed Ian's suggestion of switching the Nexys FPGA, but Bruce did not think this would do anything given our errors (though I still want to try it)

Scan Loop Example

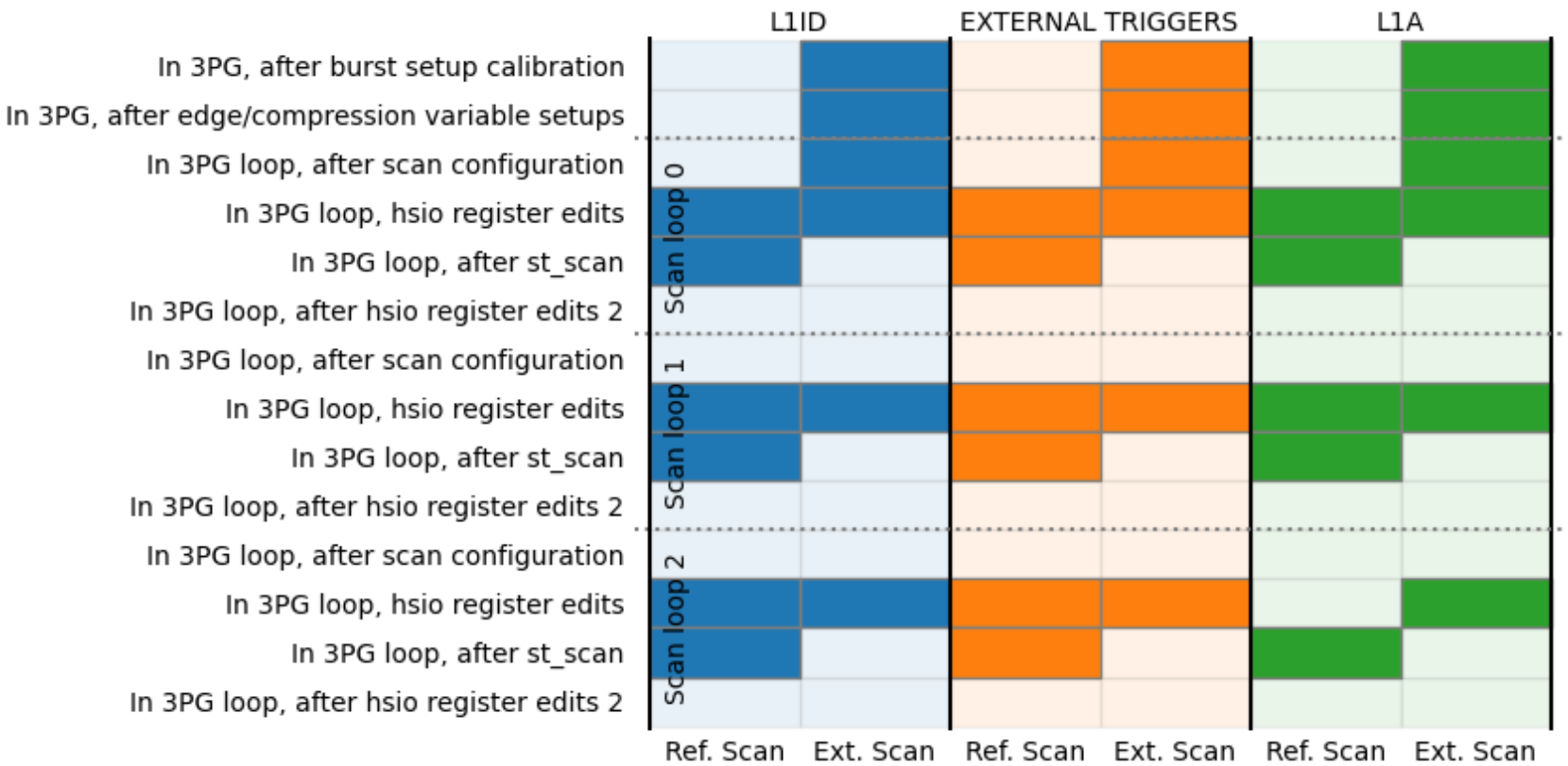


Figure 1: Example plot of a few FPGA register flags their comparison in the reference and external 3PG scans. This gives us an idea of approximately when external triggers stop working.

Bruce's Testing Script

- This script has only a single burst, and saves the data to a text file using a debug burst
- So far we have been able to check exactly what data is coming through when we use external triggers/manually stop HPRs, and it looks like HCC HPRs are the only ones that don't come through
- This means we are getting some data, but missing the HCC data
- Iterating with Bruce on this daily

	L1ID	EXTERNAL TRIGGERS	L1A	Capture Starts Count (diff)	Ext Trig 0 Count (diff)	L1ID (31:0) (diff)
Start of Script	False	False	False	0	0	0
After BurstSetupCalibration	False	False	False	0	0	0
After SingleBurst sequence load	False	False	False	4	0	2
After SingleBurst call	True	True	False	36	84780	82682
End of Script	False	False	False	0	16	16

Figure 2: HSIO dump information for single external burst testing script

Magnetic Triggering Summary

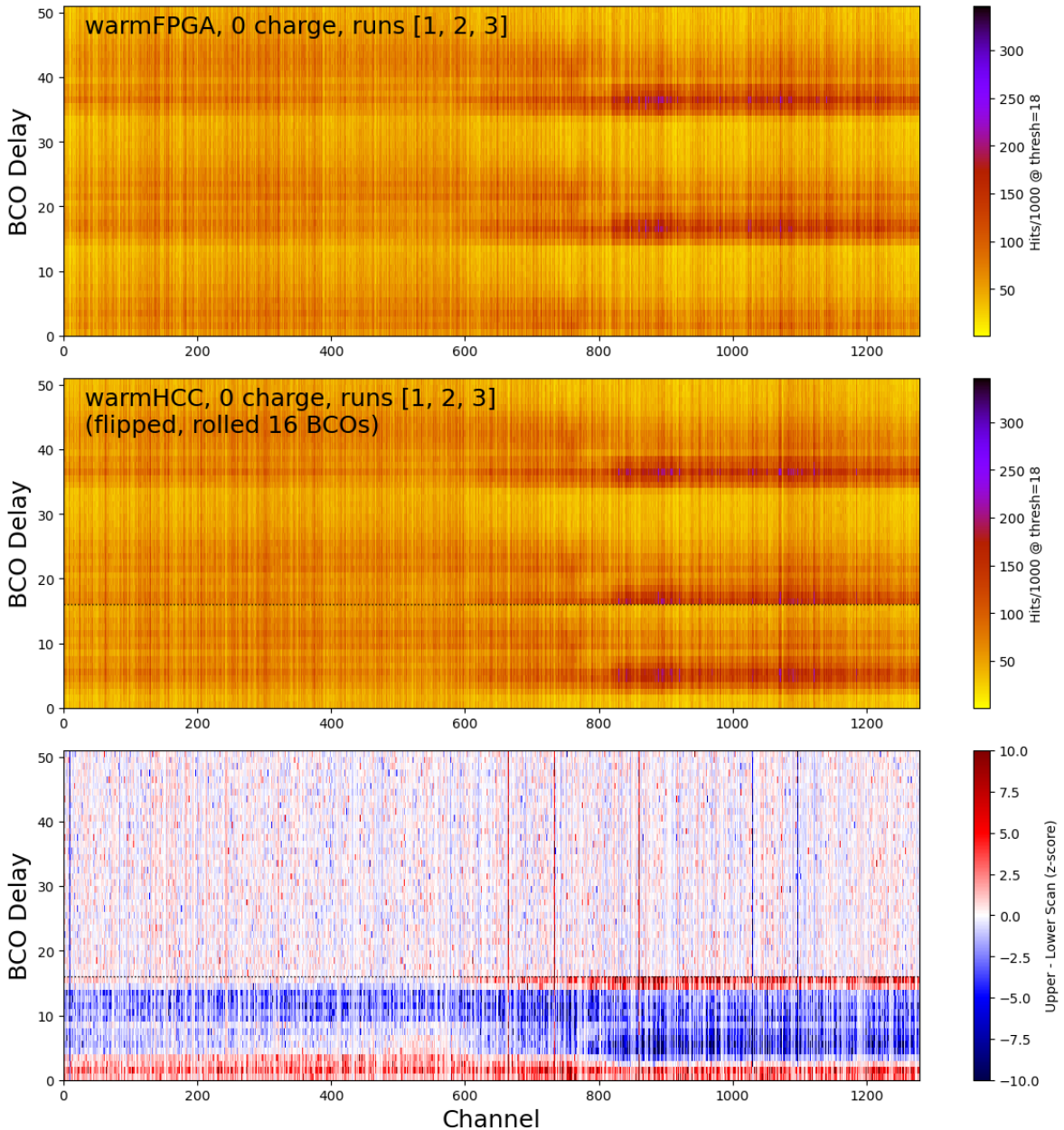
- While there *are* more things to try, I am also starting to transition over to the module testing of powerboards.
- Though I didn't achieve the goal of injecting charge properly with the external trigger, we did succeed in setting up a test stand for external triggering, and learned a lot about what things don't work for charge injection
- As such, part of the wrapping up for this project will be to condense the notes I've taken throughout the project into a TWiki page, describing the setup, operation, and development for external trigger scans at LBL.
- I'll start this project now, as part of the finishing up of the external trigger scans.

Motivation

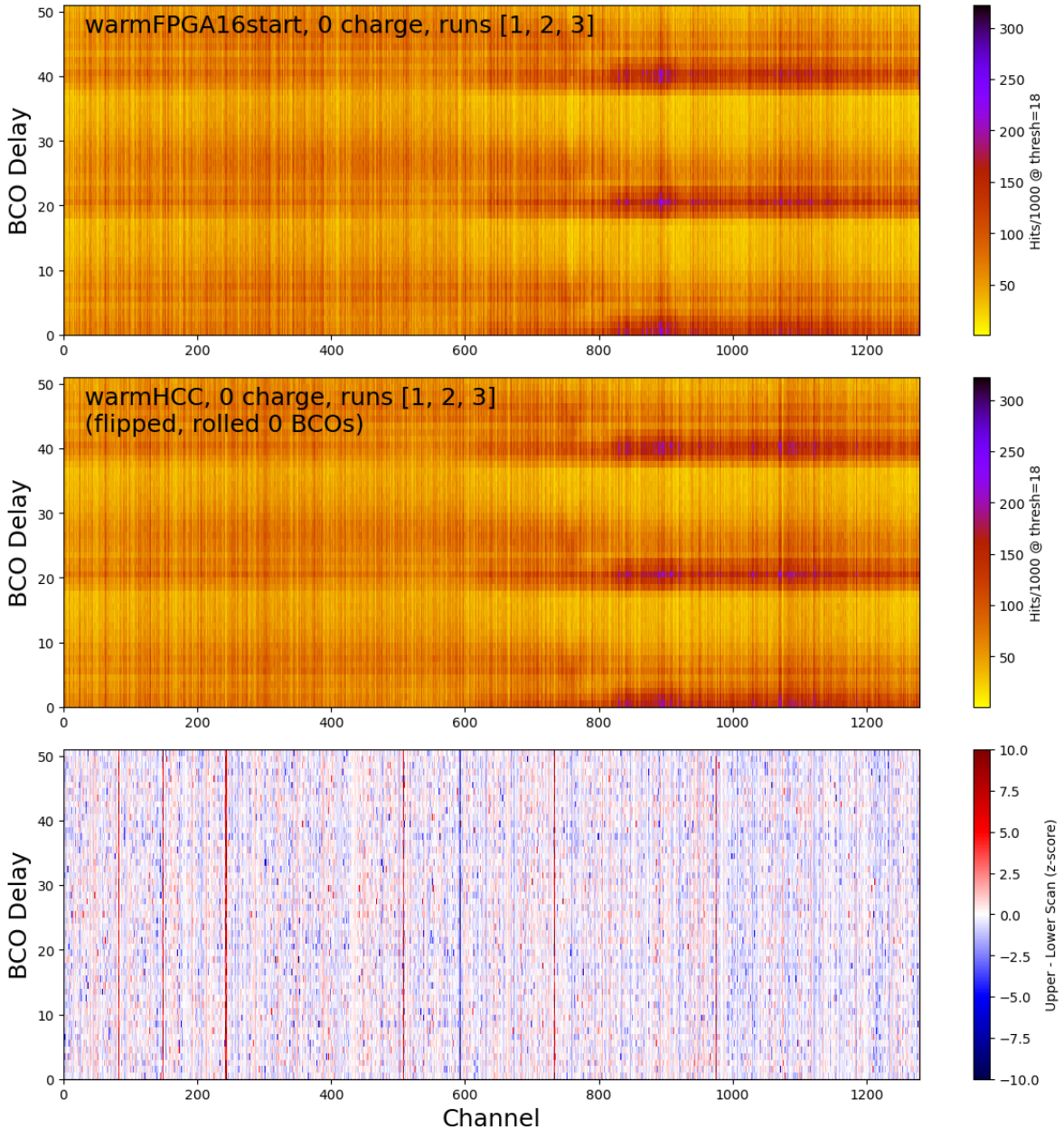
While waiting for other things to run, I also looked at ensembling many external trigger scan runs and checking that they look like what we expect

- In particular I wanted to verify that changing the FPGA delay register had the same effect as changing the HCC latency.
- Found that the FPGA delay needed to be set to start at 16 BCOs in order to match up with the HCC latency scans starting at 0, and the HCC scans needed to be flipped entirely.
- This makes sense given that they are targeting latency vs. delay.

Scan Comparison: N=3, HCC latency flipped & rolled



Scan Comparison: N=3, FPGA delay offset by 16 BCOs



Scan Comparisons

- The scans match up very well when the FPGA delay is given some fixed offset, which makes sense
- This method gives us a good idea of what identical scans should look like,
- Also provides a framework for ensembling scans and reducing the relative uncertainties between them.

Module tests of Powerboards: ideas

I am just starting this work, beginning with looking through the document Timon sent me. For now, I am

- Figuring out which tests are implementable on modules (many will not be possible)
- Seeing if I can implement a few tests that Bruce asked about specifically:
  - Want to know if the PTAT temperature measurements are valid
  - Measure output current of AMACs

I'll start with the first test and determine the feasibility of the others as I get more involved.

Outlook

Brief summary of status:

- External triggering is coming to an end, with a few loose threads to follow regarding charge injection. This will culminate in a TWiki manual describing the LBL external triggering setup.
- Module level powerboard testing is now becoming a focus, and starts with some research into how tests are currently being done.