High Granularity Timing Detector
Module production at IFAE

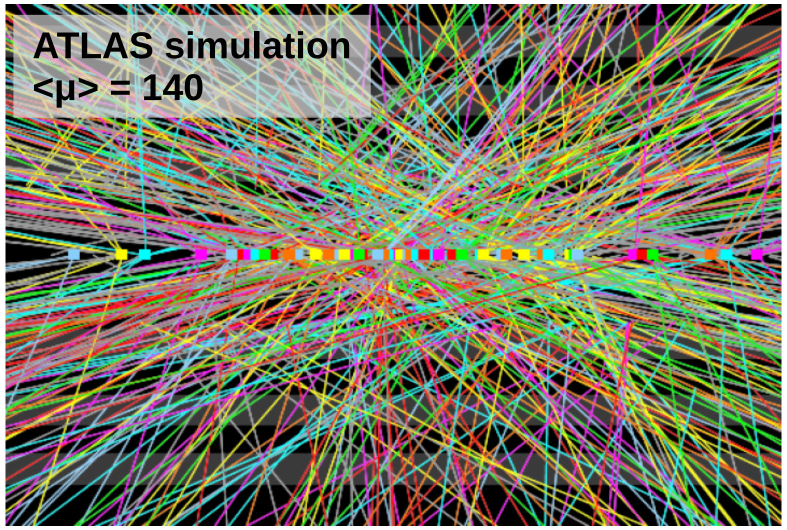
P. Fernández-Martínez, on behalf of IFAE's *ATLAS pixels group*

LBNL ATLAS group instrumentation meeting – *14 Apr 2023*

Institut de Física d'Altes Energies

BERKELEY LAB

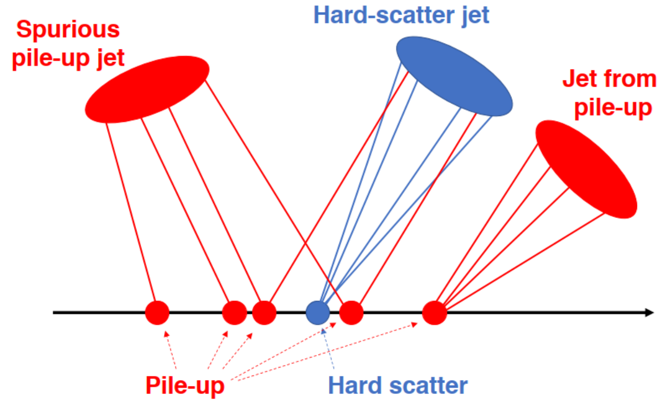
Pile-up challenge in HL-LHC



J. Wang (2017)– arXiv:1710.05245

- Increase in luminosity lead to more interactions per BC → Pile-up

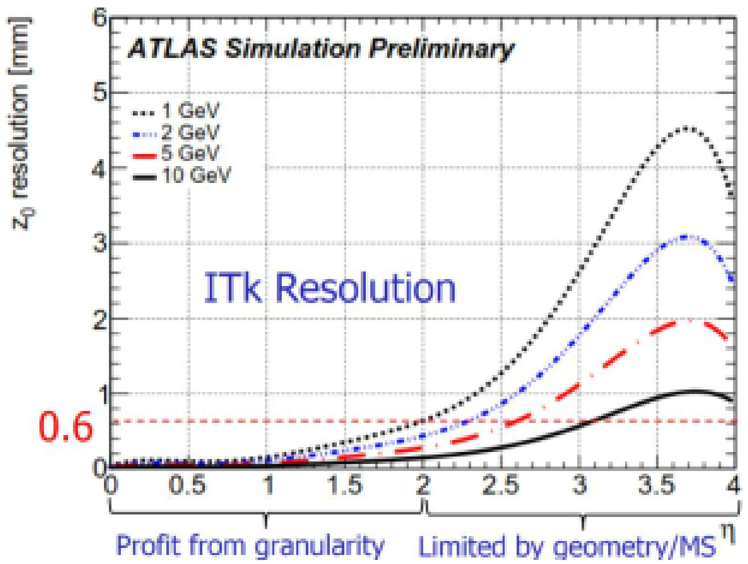
	Energy	Instantaneous $\mathcal{L}$	Integrated $\mathcal{L}$	Pileup
Run 2 LHC	13 TeV	2×10^{34} cm^{-2}s^{-1}	300 fb^{-1}	37
HL-LHC (Nominal)	14 TeV	5×10^{34} cm^{-2}s^{-1}	3000 fb^{-1}	140
HL-LHC (Ultimate)	14 TeV	7.5×10^{34} cm^{-2}s^{-1}	4000 fb^{-1}	200



Vertices spread out with σ_Z=45 mm over ~175 ps

with 1.6 vertex/mm → < 0.6 mm ITk resolution

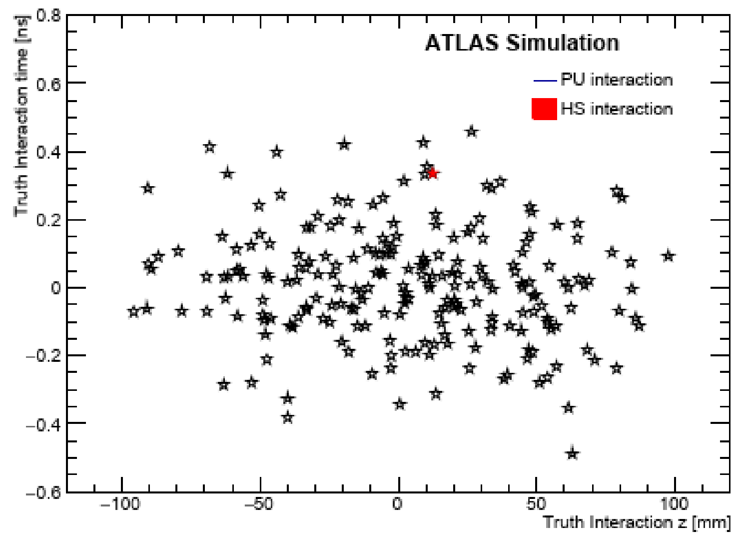
Pile-up can add jets, create spurious jets, alter the properties of hard scattered jets → degrading physics performance



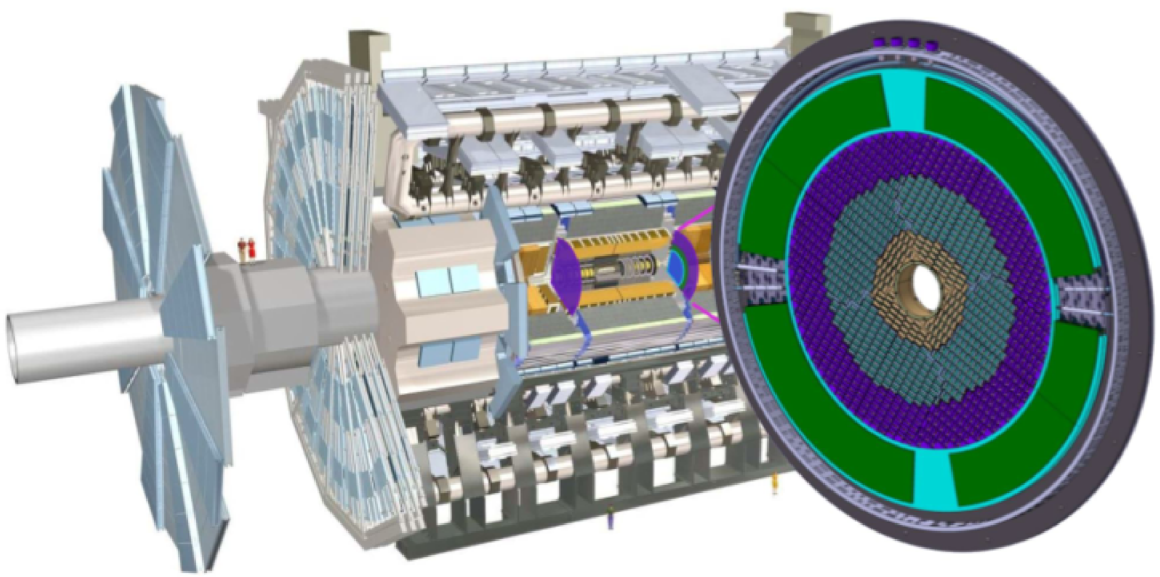
ITk performs well up to |η| ~ 2-2.7

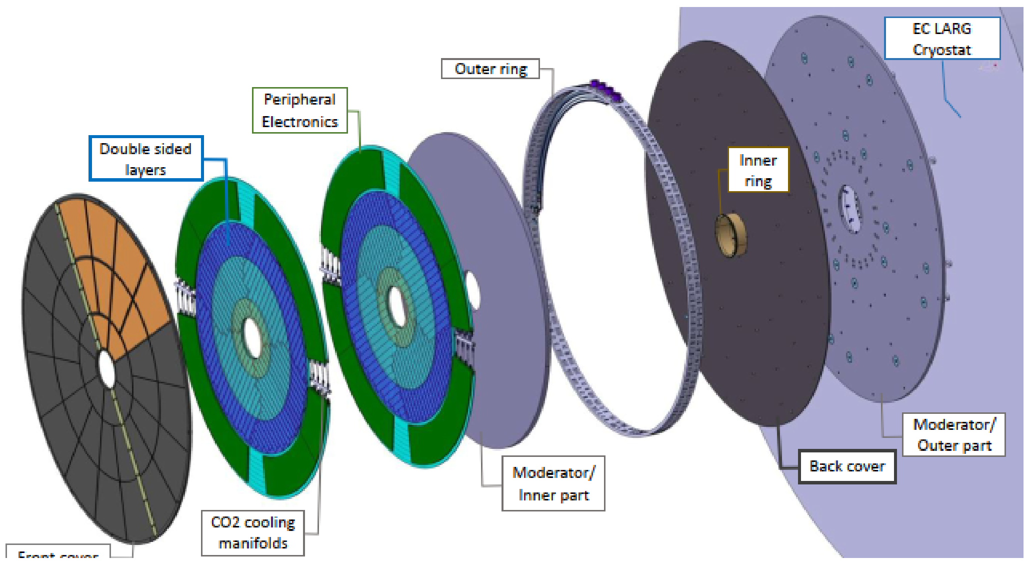
Assigning time to each track in 2.7< |η| < 4.0

30-50 ps time resolution per track ~ x6 pile-up rejection



High Granularity Timing Detector





HGTD Features

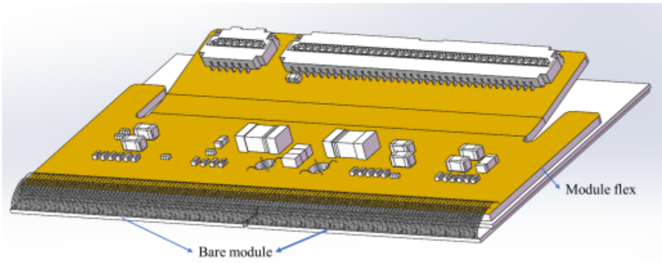
- Two disks located in the gap region between the barrel and the end-cap calorimeters
- Distance in z of ±3.5 m from the nominal interaction point
- Envelope of the vessel has a radial extent of 110 to 1000mm and 125 mm in Z
- Covering 2.4 <|η|<4, 120 mm < r < 640 mm
- Each layer is doubled-sided: modules mounted on the front and back sides of a common cooling disk, and rotated to overlap
- Structure divided in concentric rings with different active sensor overlap: 70%, 50%, 20%
- 8032 modules of 30x15 pads (4 cm x 2 cm). Pad size 1.3 mm x 1.3 mm
- Instrumented with Low Gain Avalanche Detectors (50 µm thick)

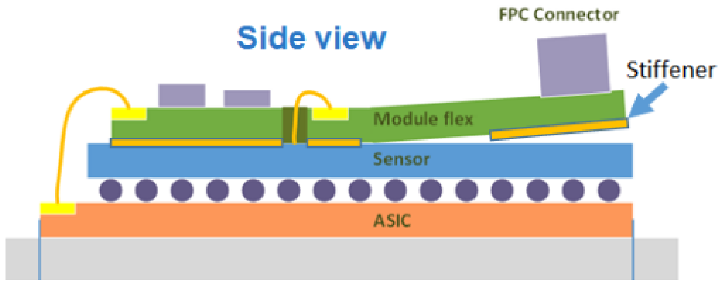
HGTD Requirements

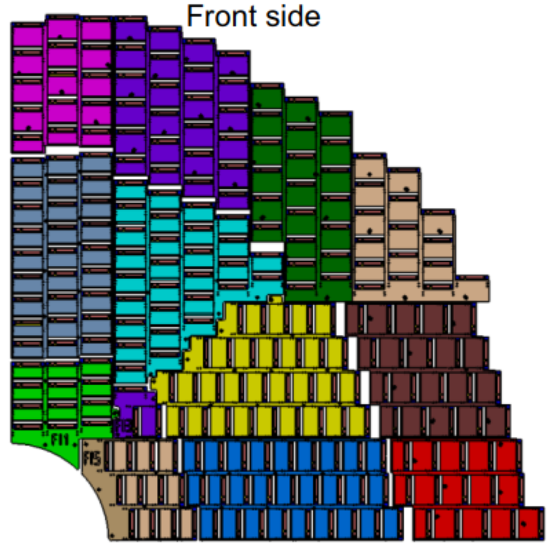
- Minimum charge of 4 fC
- Hit time resolution of 30 ps (start) and 50 ps (after 4000 fb^{-1})
- Radiation hardness: 2.5×10^{15} n_{eq}/cm^2, TID = 2 Mgy
- Operation Temp = -30° C

HGTD Modules and support units

- HGTD Module: 2 bare modules (hybrids) attached and wire-bonded to a single flex PCB (module flex)



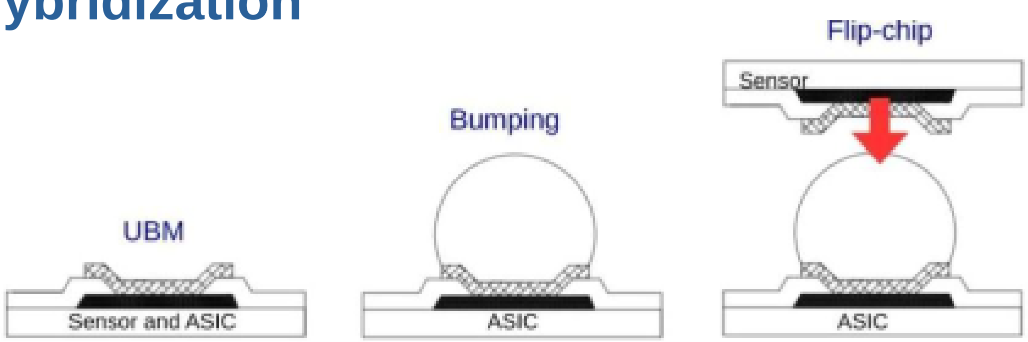


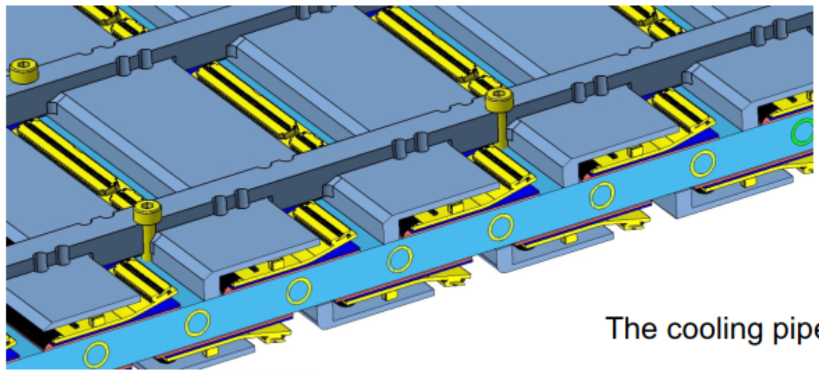


2x13 detector units per quarter (front and back side)

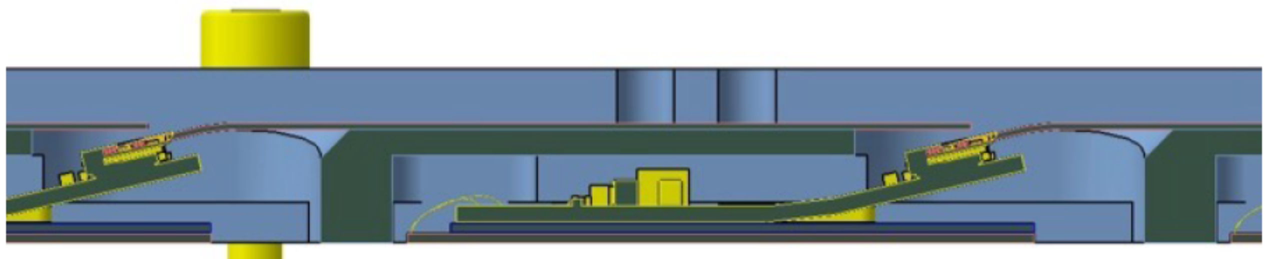
- Each hybrid consists of a LGAD sensor (15 × 15 pads) interconnected to a ALTIROC readout chip through bump-bonding
- Signals and power are routed to the module flex through a flexible cable of different lengths (flex tails)

Hybridization





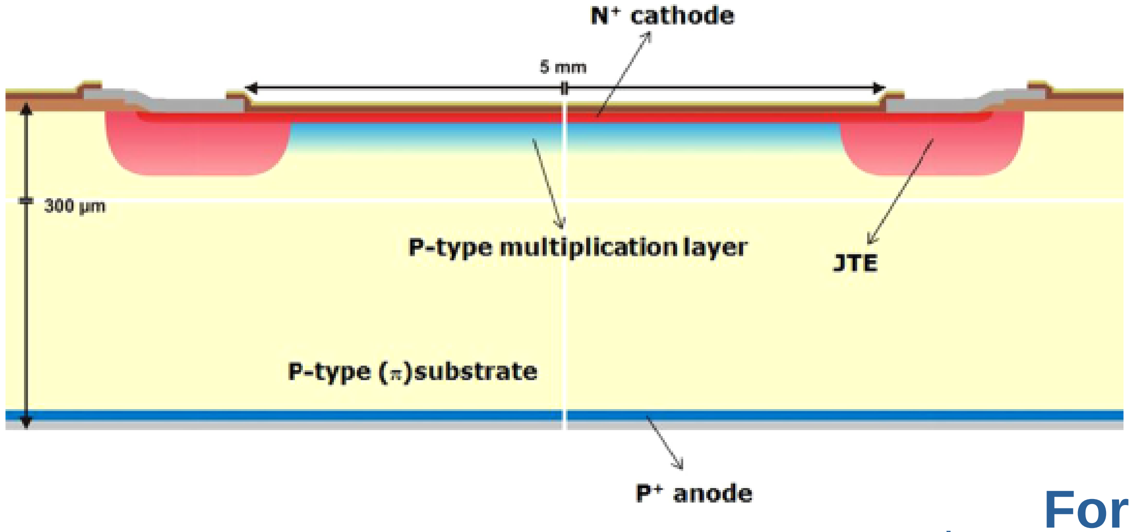
Direct contact with cooling plate
The cooling pipes and the two layers are shown

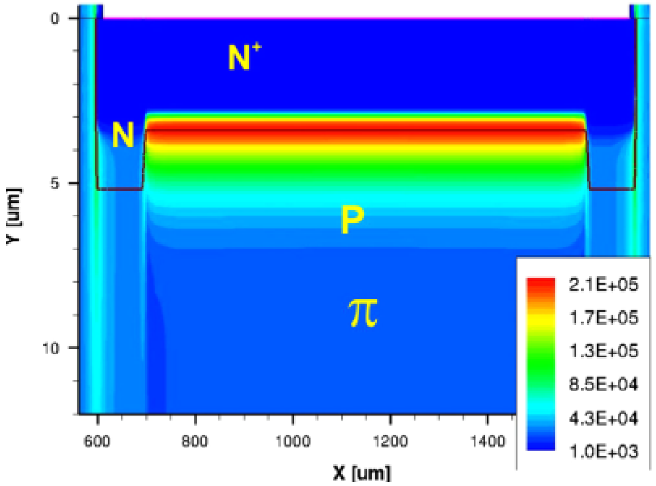


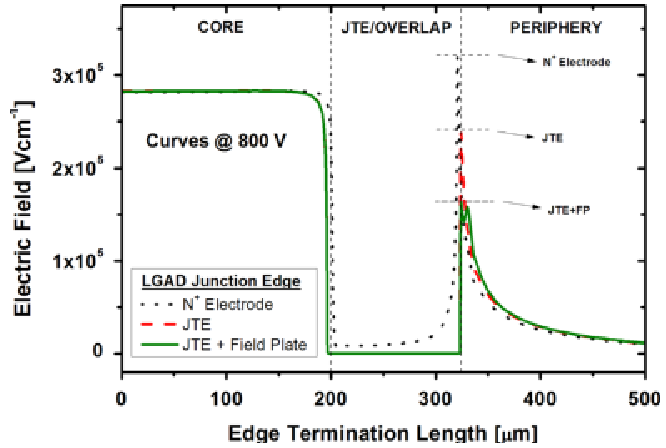
Wire bonding protection - module flex and flex tail connected

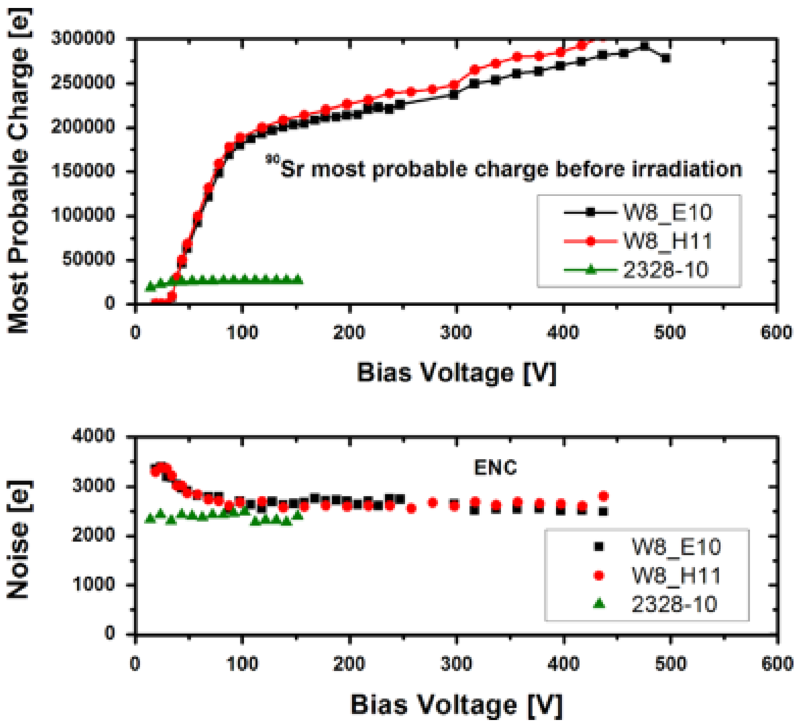
LGAD Sensors

- Originally developed by CNM and RD50





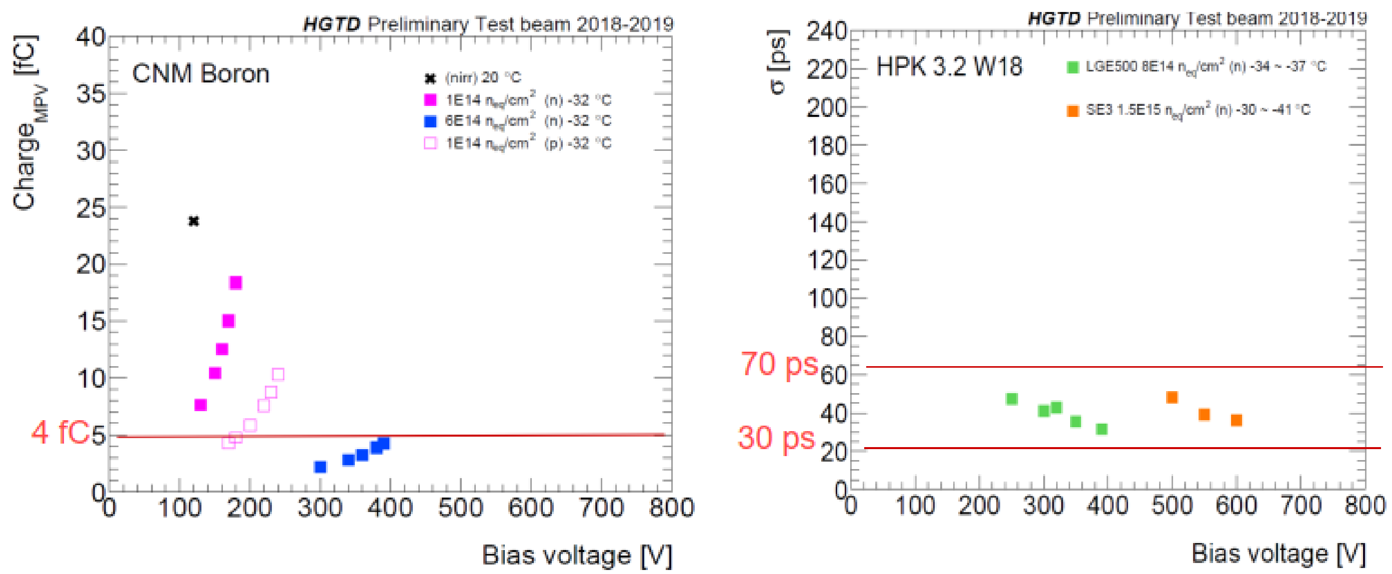




G. Pellegrini et al. DOI: 10.1016/j.nima.2014.06.008

For HGTD

- **50 µm** active thickness
- Internal gain: > **20** before irradiation, and **> 8** at the end of lifetime
- Small rise time: ~ 0.5 ns, fast charge collection ~1 ns



R. Mazini: ATL-HGTD-SLIDE-2021-352

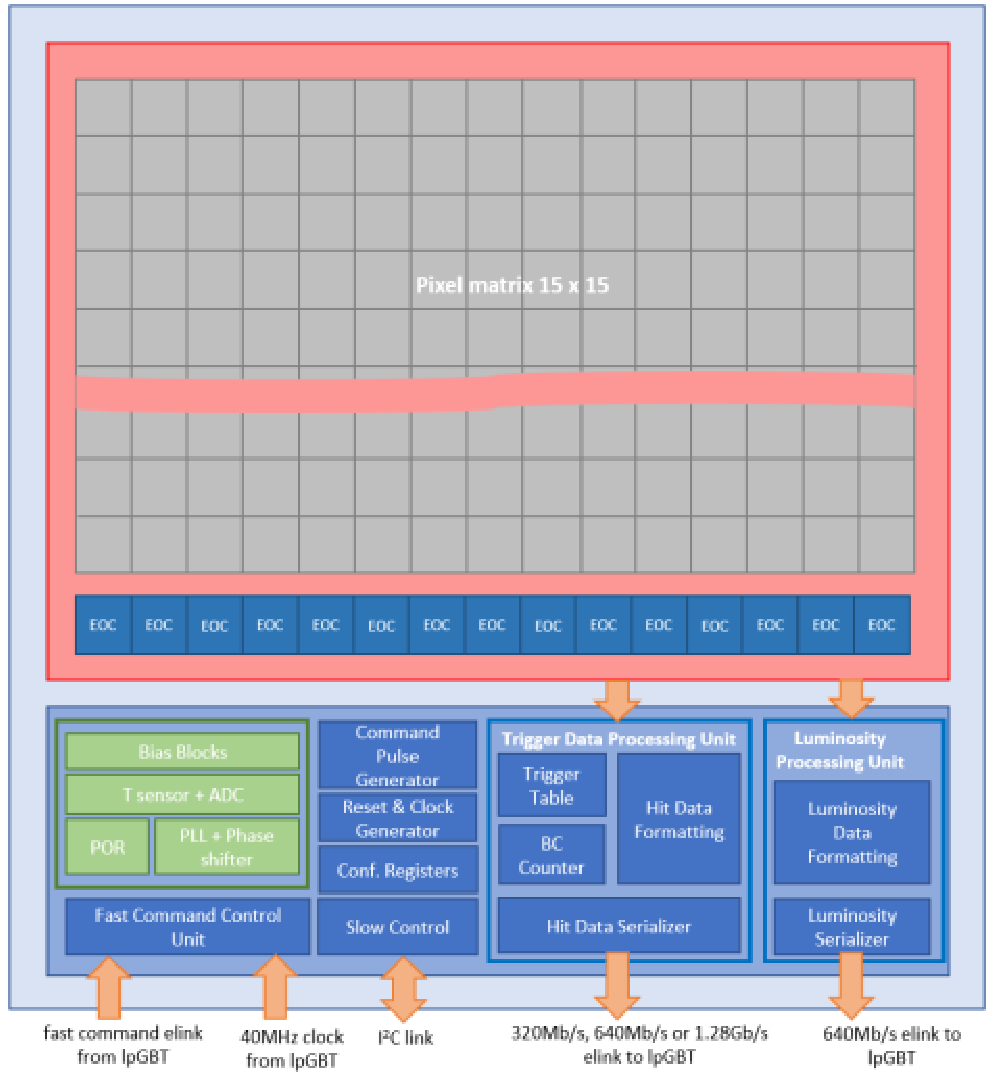
Readout ASIC: ALTIROC

ATLAS **L**GAD **T**iming **I**ntegrated **R**eadOut **C**hip

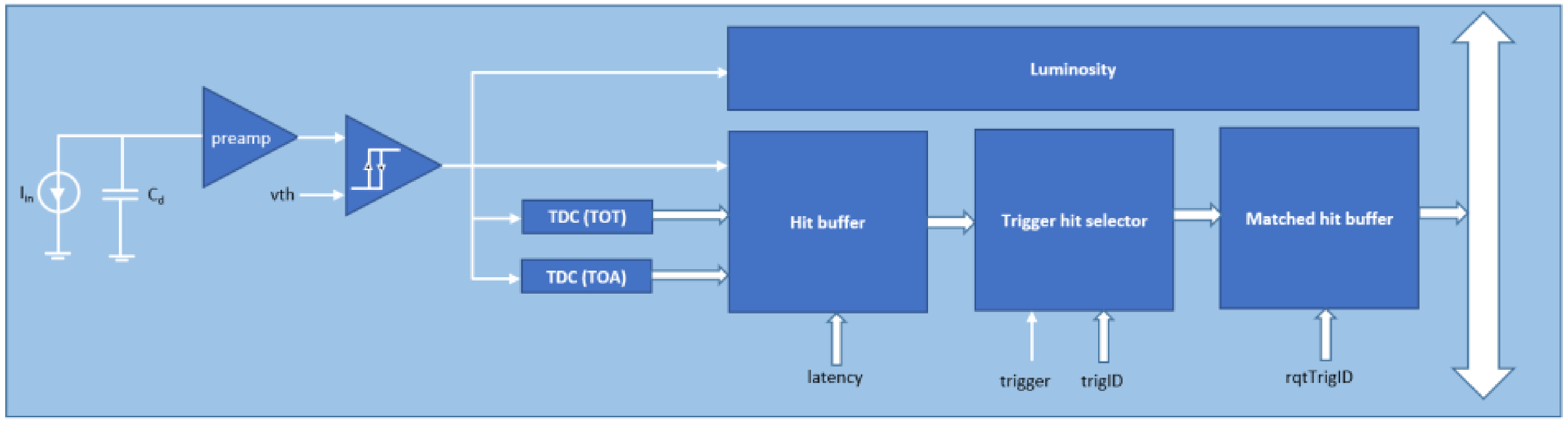
- Technology:130 nm CMOS from TSMC. Total of 225 readout channels (15x15)
- Several improved versions. Latest in use: **ALTIROC2**... ALTIROC3 (rad-hard version) coming soon!

Two measurements:

- **TOA** and **TOT** per hit/pixel. Transmitted only upon reception of L0/L1 trigger with latency up to 35 µs
- **Luminosity**: Number of hits per ASIC/BC



Pixel Electronics

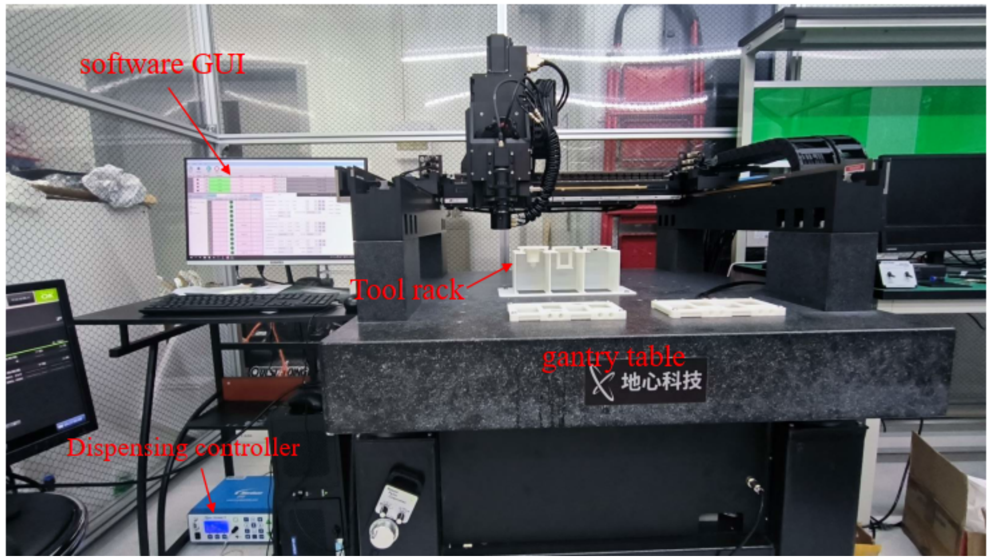


- 2 Flavours of preamplifier: Voltage (VPA) or transimpedance (TZ)
  - Time walk correction made with Time over Threshold (TOT) architecture
- 2 Time to Digital Converters (TDC): TOA and TOT (different time window)
- Hit processor: buffer until L0/L1 triger (~ 1 MHz)
- Trigger hit selector and Match hit buffer (to select and store only trigger-associated events)

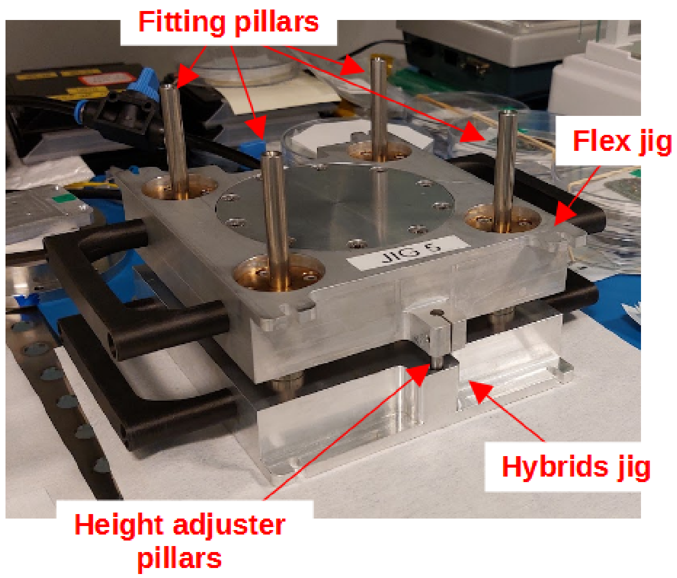
Module Production: Assembly sites

Chinese Institutes (IHEP, USTC)
- Same procedure, instruments and tools

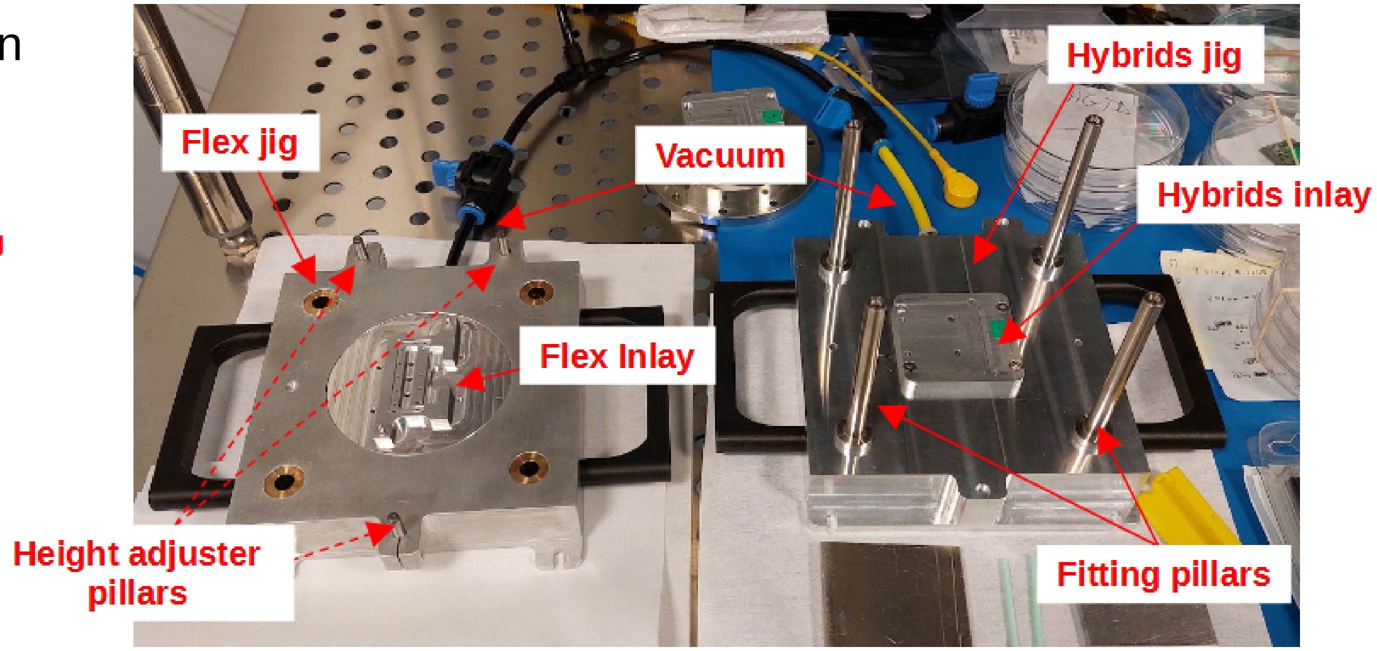
Gantry system: Robotic pick & place for systematic assembly



European and Moroccan Institutes (UJG-Mainz, JIClab, IFAE and MAScIR)
- Similar tools, so far with variations.
  Will eventually converge to the optimal version



Adjustable jigs: Manual but repeatable



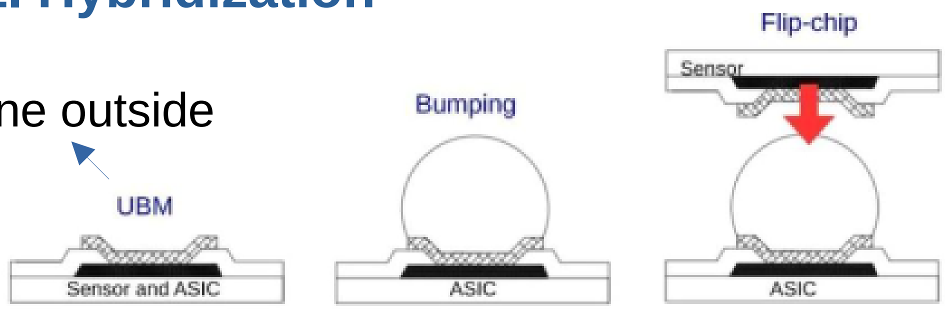
IFAE

HGTD Module Production at IFAE

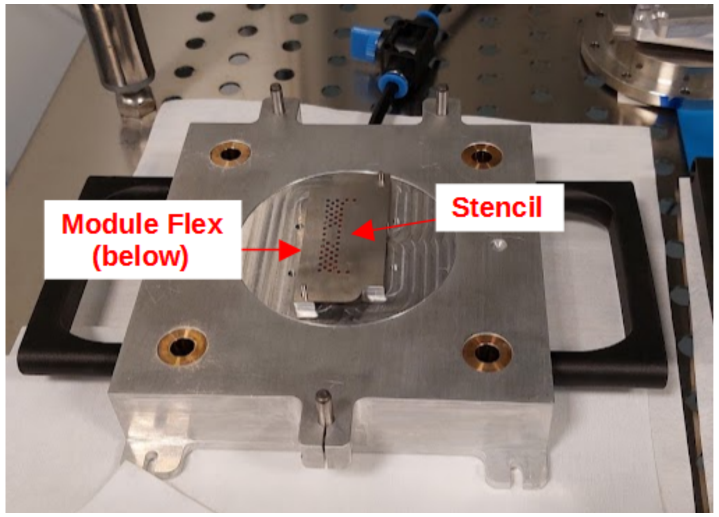
- IFAE takes part in all the steps of the module production
- Our share: 10% ~ 800 modules!

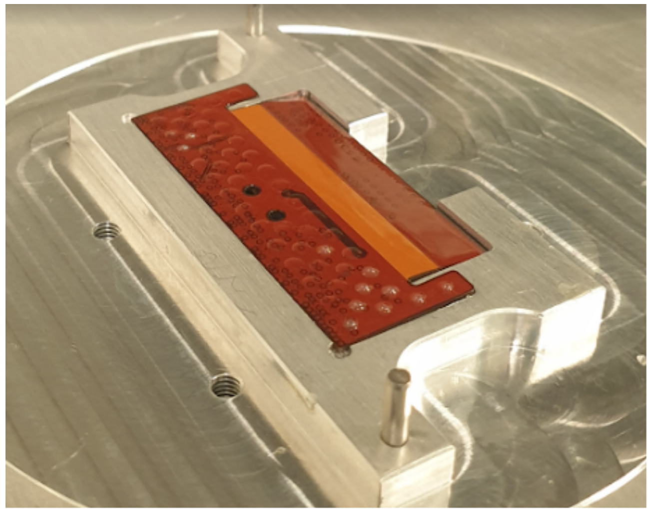
1. Hybridization

Done outside

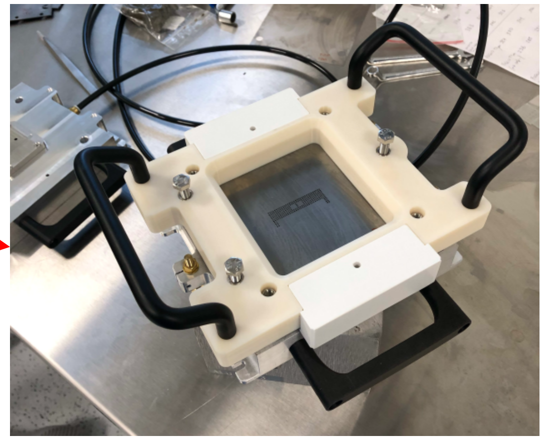


2. Glue delivery

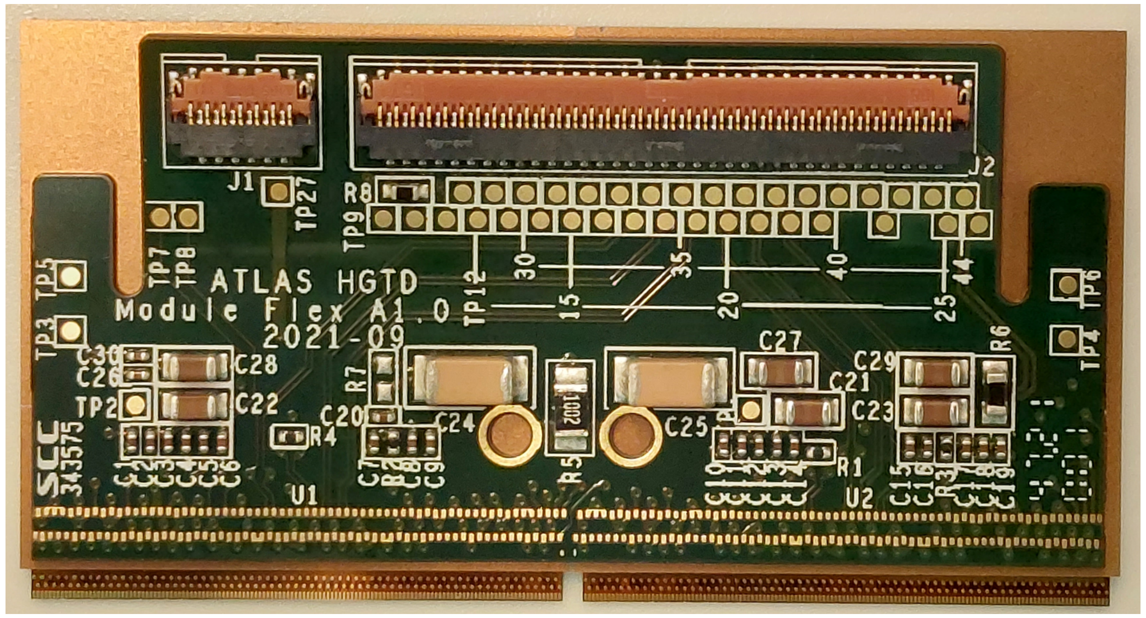




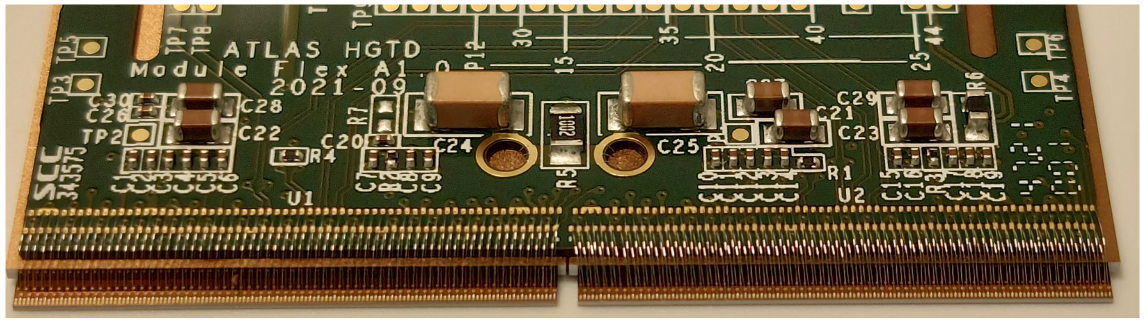
Will eventually move to this kind of stencil



3. Module Attachment and Metrology



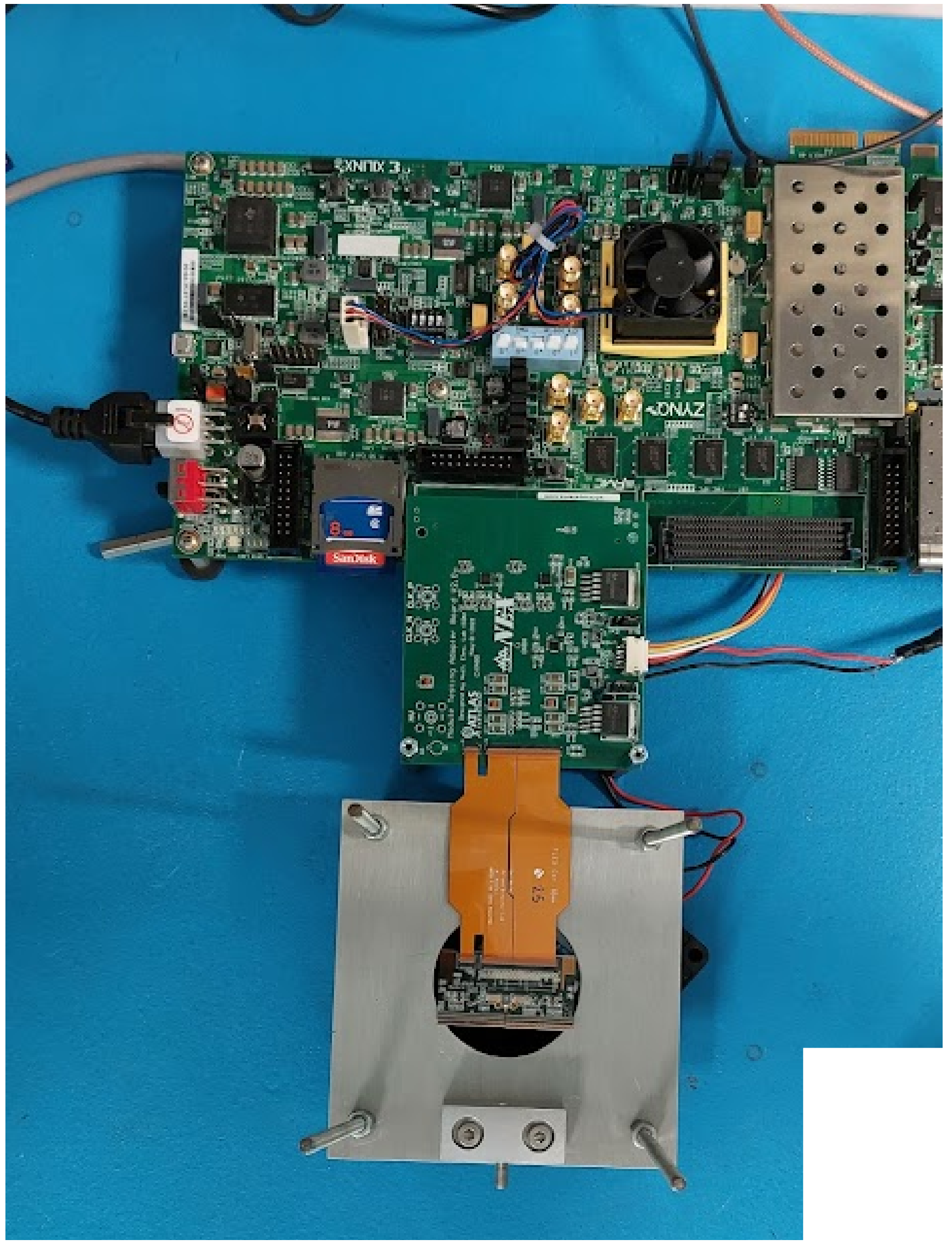
4. Wire bonding and pull tests



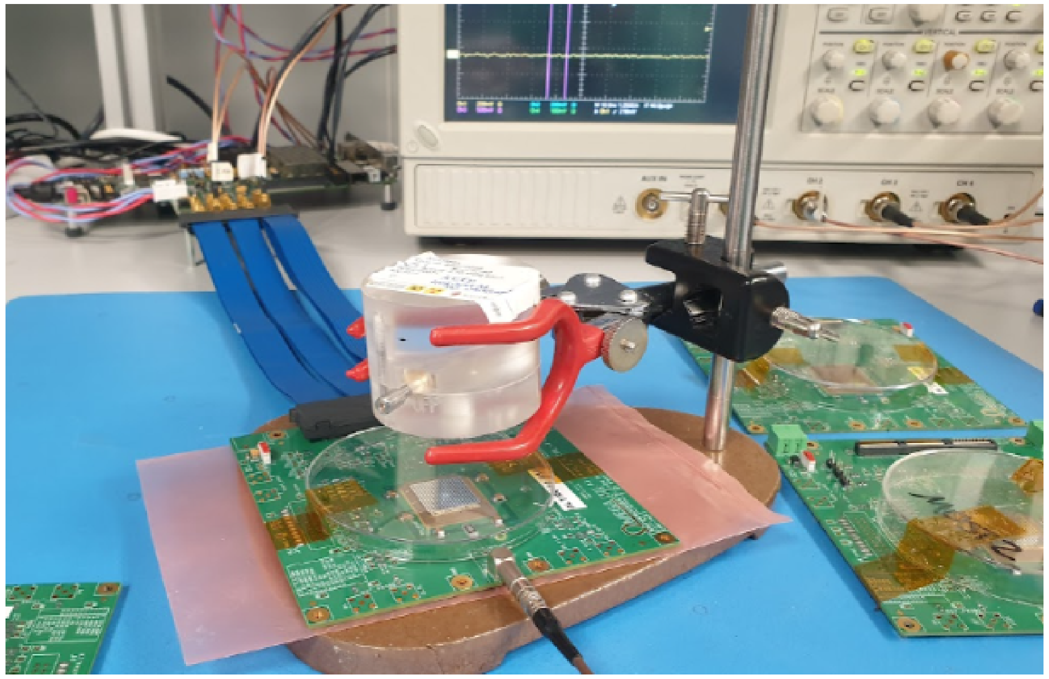
HGTD Module Testing at IFAE

Measurement Steps

- Chip **communication** and register **configuration**
- **Set** discrimination **threshold** (first Global, then for individual pixels)
- **Threshold scan** (efficiency vs charge)
- Noise scan with Sr-90 source (**bump connectivity**)
- We don’t do timing measurements yet
- Additionally, thermal stress tests

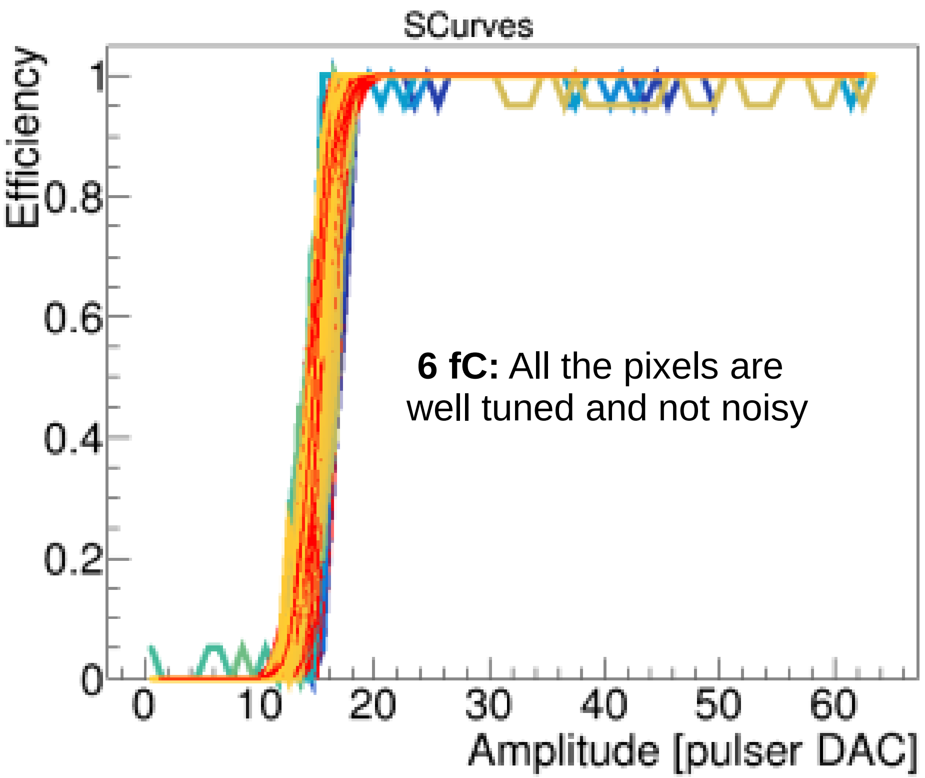


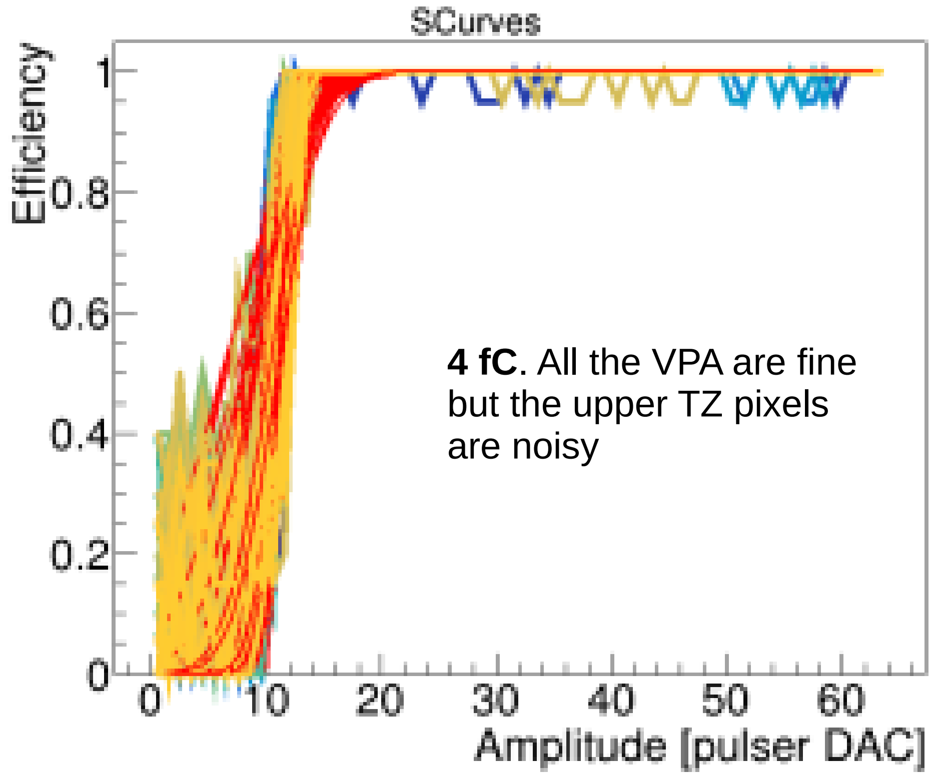
Readout system (Alvin) developed at IFAE

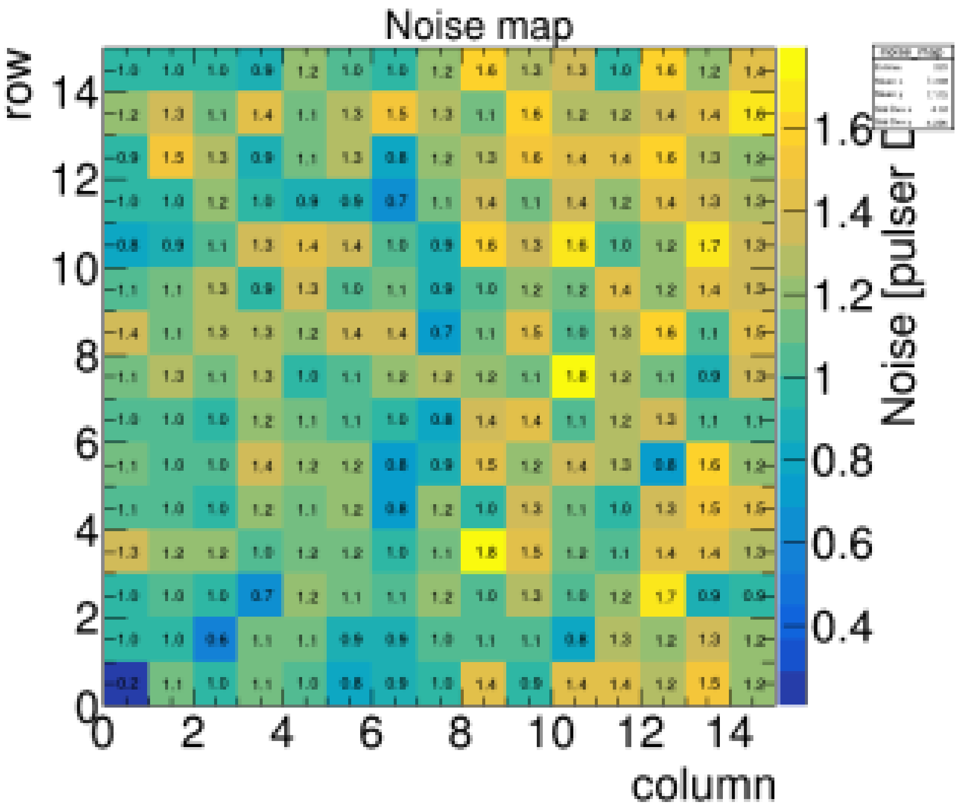


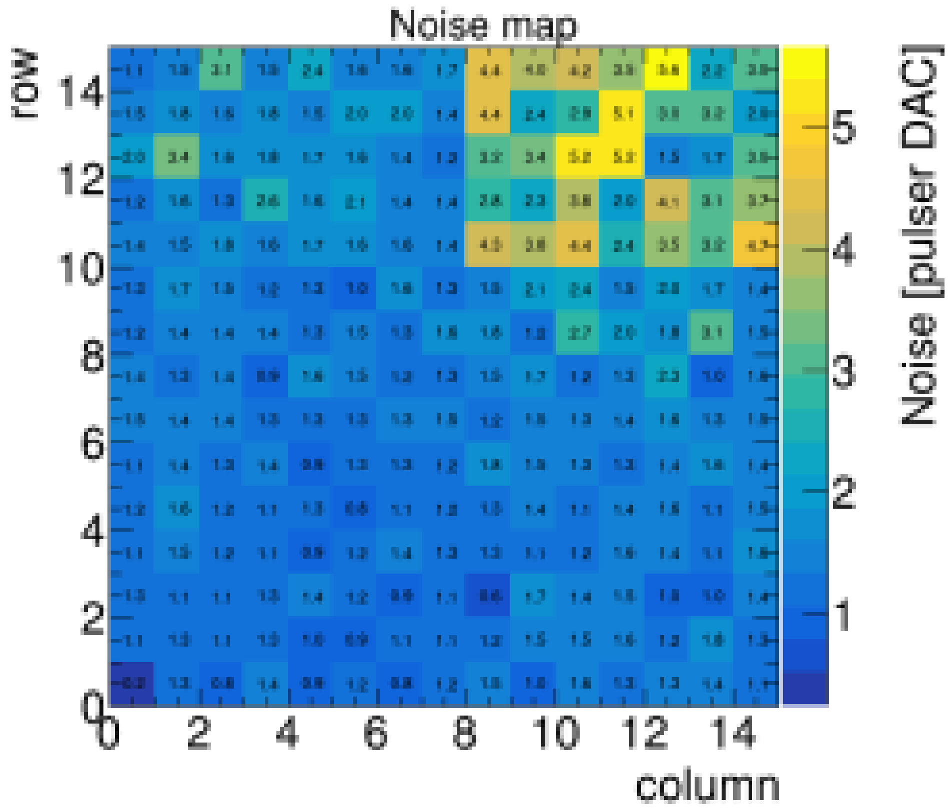
HGTD Module Testing at IFAE

V. Gautam
L. Castillo
S. Terzo



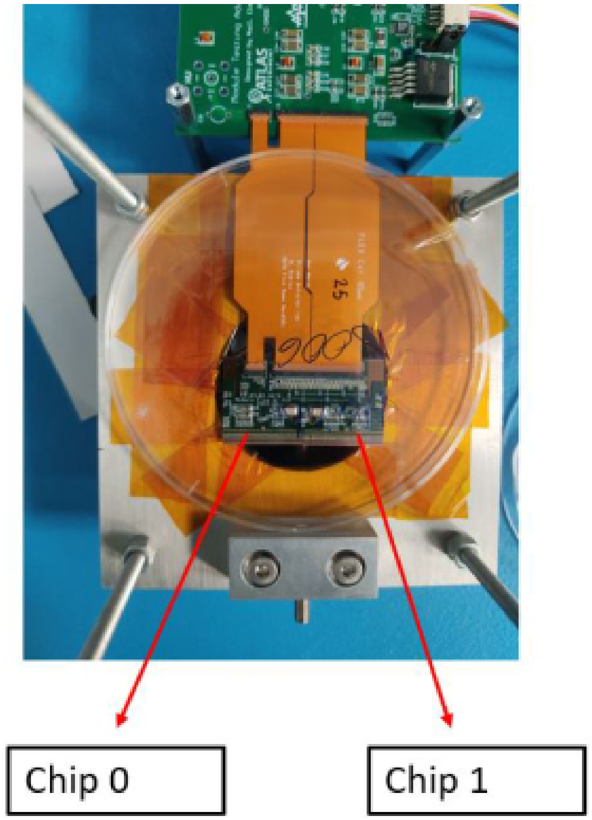


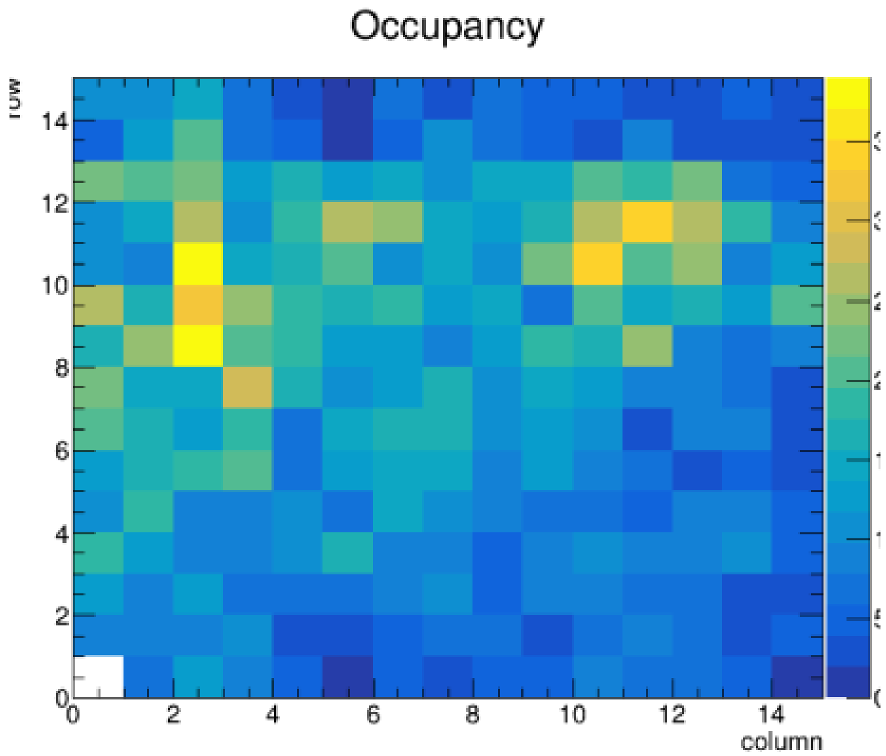




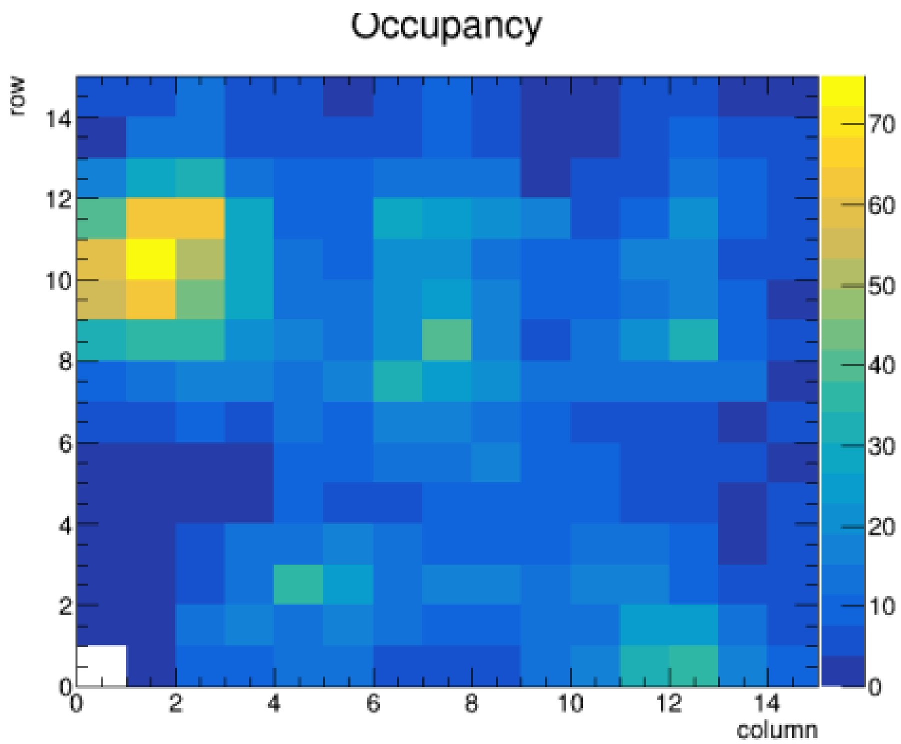
HGTD Modules: Bump connectivity

V. Gautam
L. Castillo
S. Terzo





Chip 0



Chip 1

HV = 180 V.

Threshold = 10fC.

- Full HGTD modules with the flex assembled for demonstrator tests.
- Sr-90 Source scan with M002 shows 100% bump connectivity.

Outlook

- **High Granularity Timing Detector** (HGTD) included in the upgraded ATLAS to mitigate the pile up issue in the 2.4 < |η| < 4.0 region (will also provide a luminosity measurement)
- Two discs located between the barrel and the end-cap calorimeters. Double-side instrumented with LGAD modules of 30x15 pads (1.3 mm x 1.3 mm pad size). Rotated to ensure overlap.
- LGAD sensors (50 µm thick) exhibit moderate signal gain, small rise time, and fast charge collection, to give charge collection > 4fC (after irradiation) and time resolution down to 30 ps (before irradiation)
- ALTIROC readout ASIC to measure TOA and TOT per hit/pixel, only transmitted upon arrival of L0/L1 event trigger, and number of hits per BC (luminosity) → Extensive tests on vs.2, ALTIROC3 (rad-hard) coming soon.
- Over 8000 HGTD Modules (2 bump-bonded LGAD-ALTIROC hybrids attached to a single PCB flex) to be produced in 6 assembly sites in 3 continents. Assembly methods under development, evaluation and setting up.
- IFAE is fully implicated in all the steps of the module production: Hybridization, module assembly, and module testing → Readout system (Alvin) developed at IFAE
- **Present status**: First prototypes, with non-final version of the parts (neither sensor, nor ASIC, nor flex) already produced in most of the assembly sites and progressing in the characterization

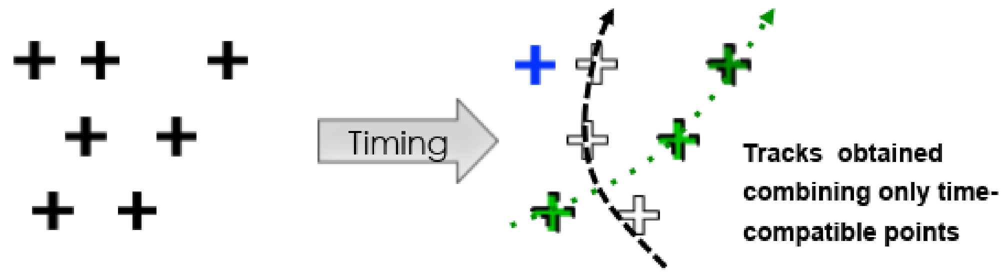
  → Targeting at the implementation of the demonstrator unit (full operative 54-module prototype unit). To be ready in the next few months.

Back up

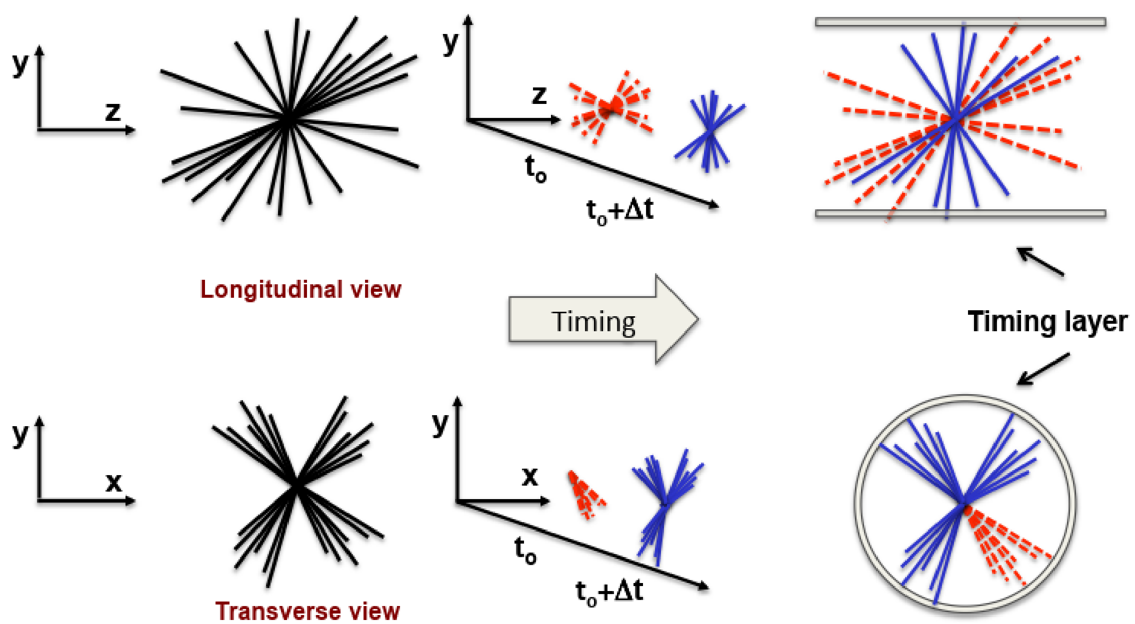
Timing detectors

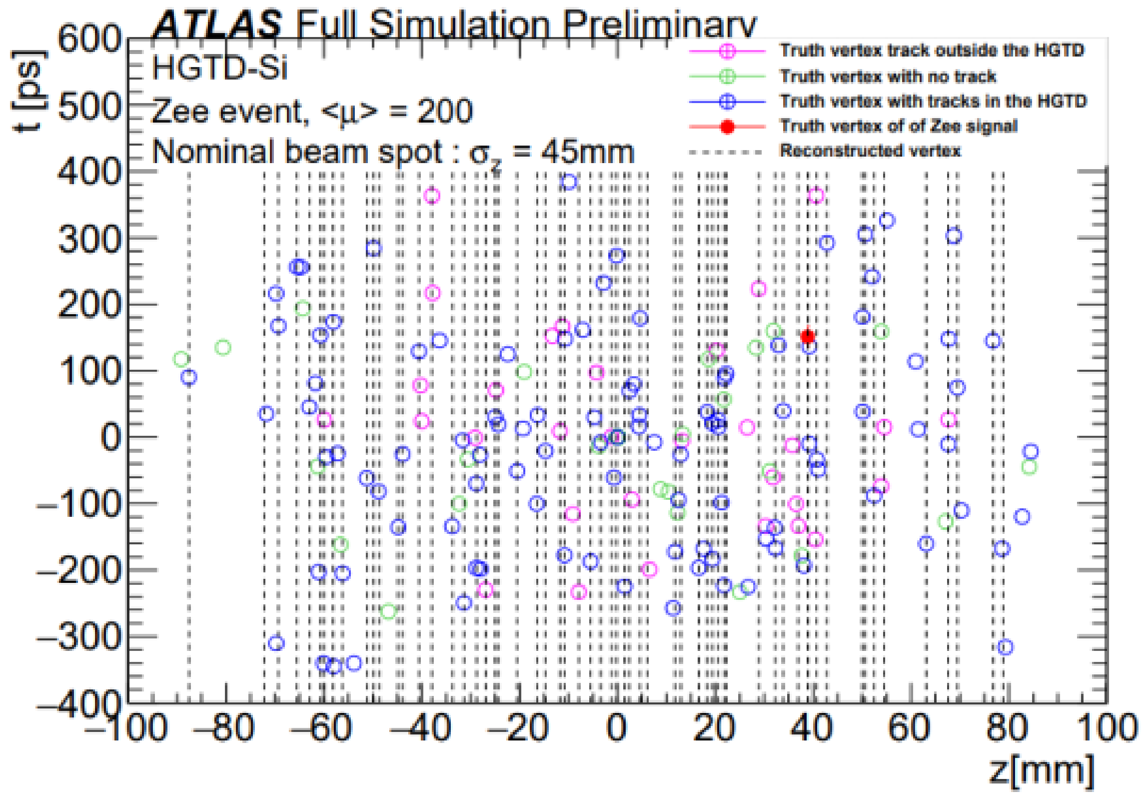
- The option of having a full tracker with **time measurement associated to each point** of the track is not fully available yet

...and would require a lot to the readout circuit!!



- Instead: **Timing Layer**





Specifications

R. Casanova - IFAE

- Charge dynamics : up to 100 fC
- Noise : < 0.5 fC
- Cross talk : < 2 % to guarantee single hit with 2 fC threshold

- TOA :
  - Measurement window > 2.5 ns
  - Jitter : 25 ps for Q > 10 fC
    70 ps for Q > 4 fC
  - Conversion time < 25 ns (TDC lsb of 20 ps)

- TOT :
  - For 100 fC, TOT < 20 ns

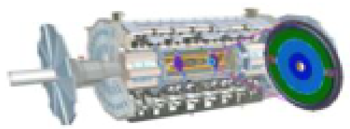
Landau MPV	4 fC	> 10 fC
Time Walk contribution rms (ps)	25	10
TOT resolution for VPA (ps)	120	120
TOT resolution for TZ (ps)	120	70

  - Conversion time < 25 ns
  - TDC lsb of 120 ps enough but TZ better use with 40 ps

- 40 MHz Clock of the TDC :
  - Jitter < 10 ps
  - ASIC global clock aligned with better than 100 ps
  - Clock skew between channels in ASIC : +/- 150 ps

- Luminosity
  - Provide ASIC number of hits per bunch crossing on two time windows
  - Similar alignment as for the clock but skew relaxed to +/- 200 ps

- ASIC power dissipation < 1.2 W



ATLAS HGTD

Omega

Requirements for the ASIC

HGTD key requirement: Time resolution per track, combining multiple hits, is 30 ps at the start of lifetime to 50 ps after 4000 fb-1 => Time resolution /hit must be < 40 ps at start and 85 ps (70 ps) at the end of lifetime for the inner radius (outer radius)

Main contributors:

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

with $$\sigma_{elec}^2 = \sigma_{Time\ walk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2$$

Maximum jitter (σ_{elec})	**25 ps at 10 fC at the start of the HL-LHC and 70 to 85 ps after 4000 fb-1 for 2.5 fC**
TDC contribution	**< 10 ps**
Time walk contribution	**< 10 ps**
TDC conversion time	**< 25 ns**

PAD size	1.3 x 1.3 mm^2 x 50 µm => **Cdet = 4 pF**
ASIC size and channels /ASIC	2x2 cm2 225 channels/ASIC
Single PAD noise (ENC)	**< 1500 e- or 0.25 fC**
Minimum threshold	**1 fC**
Dynamic range	**2.5 fC** to 100 fC

TID Tolerance	Inner region (R<320 mm): **4.7 MGy** (Modules replaced after 2000 fb^{-1}) Worst case at R=320mm: **5.1 MGy**

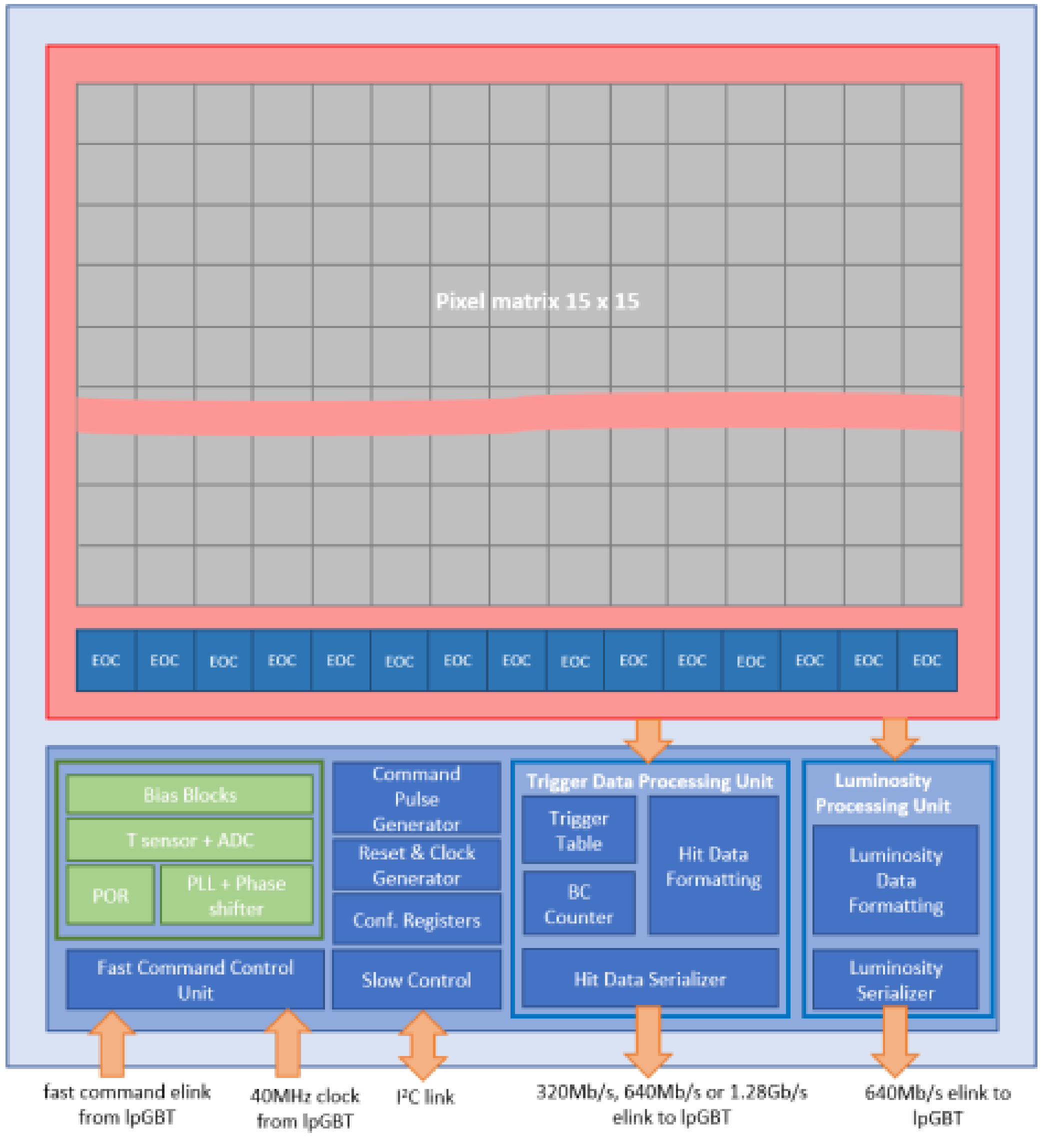
⇒ ASIC designed in CMOS 130 nm

Voltage and Power dissipation per ASIC	1.2V and 300 mW cm^{-2} => 1.2 W/ASIC (225 ch) or **4.4 mW/channel** and 200 mW for the common part

Overall architecture

R. Casanova - IFAE

- Technology: 130 nm CMOS from TSMC
- 15 x 15 pixel matrix with a pixel size of 1.3 x 1.3 mm^2
- In-pixel electronics:
  - **Analog:** preamp + discriminator + 2 TDCs.
  - **Digital:** data acquisition, 2 buffers and zero suppression.
  - **Data:** TOA, TOT, AddrRow, TriggerID, Luminosity.
- End Of Column cell (EOC) to handle the column readout.
- Luminosity processing unit:
  - Sums column luminosity
  - Time window generation
  - Transmission speed: 640 Mb/s
- Trigger data processing unit:
  - Processing of incoming triggers
  - Readout of pixel matrix (TOT and TOA)
  - Transmission speed: 320, 640, and 1280 Mbps
- Fast command control unit:
  - Processing of 8 bits fast commands: trigger L0A/L1A, BC reset, Global reset, …
  - Serial transmission at 320 Mbps (1 command per bunch crossing)
- Slow control:
  - I2C link
  - to configure the periphery and the pixels

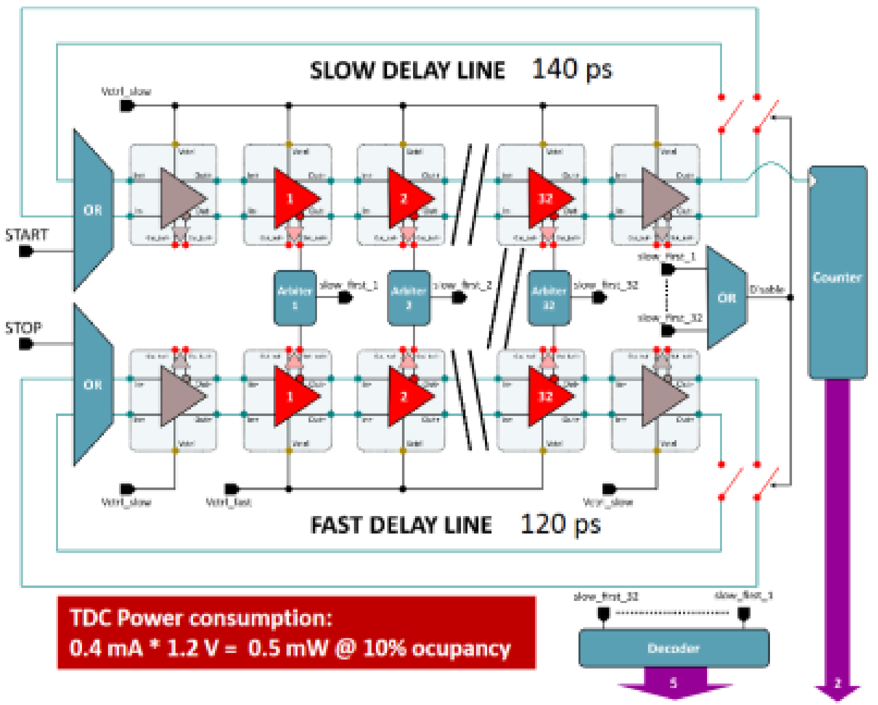


ATLAS HGTD

Pixel electronics (TDCs)

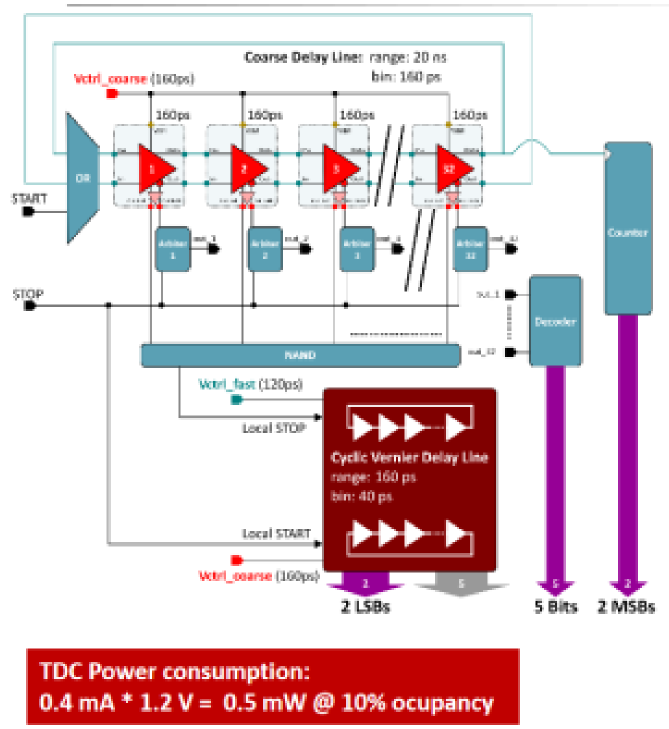
R. Casanova - IFAE

TOA

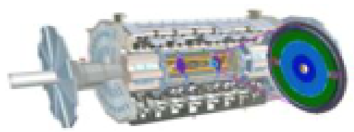


- Cycling Vernier delay line
- Resolution: 20 ps
- Range: 0 - 2.5 ns (7-bits)
- Cycling configuration used in order to reduce the total number of Delay Cells

TOT



- Coarse delay line
- Resolution: LSB = 120 ps
- Range: 0 - 30 ns (8-bits)



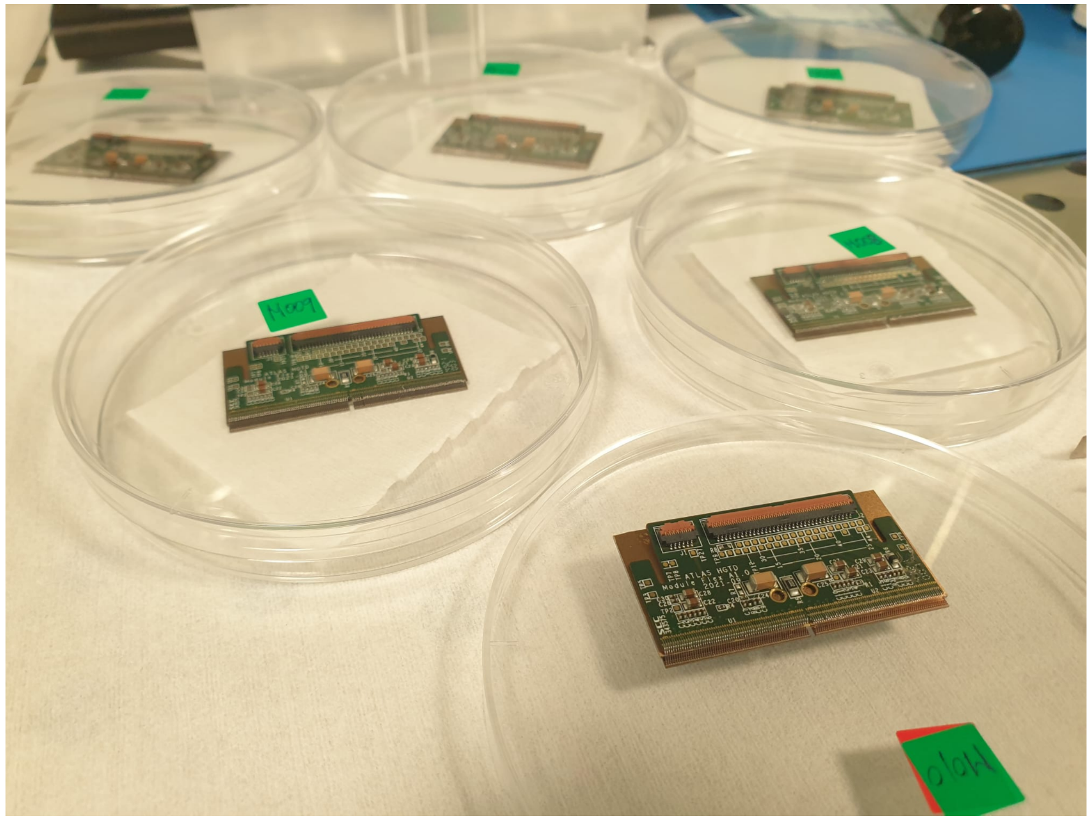
Demonstrator modules at IFAE:

	SN	Sensors	ASICs	UBM	Hybrids	WB	Issues	Status
M005	20WMO111000005	FBK	ALTIROC2	AEMTec	IFAE	IFAE	No	TB tested
M006	20WMO111000006	FBK	ALTIROC2	AEMTec	IFAE	IFAE	No	TB tested
M007	20WMO111000007	FBK	ALTIROC2	AEMTec	IFAE	IFAE	No	TB tested
M008	20WMO111000008	FBK	ALTIROC2	AEMTec	IFAE	IFAE	No	TB tested
M009	20WMO111000009	FBK	ALTIROC2	CNM	IFAE	IFAE	No	TB tested
M010	20WMO111000010	FBK	ALTIROC2	CNM	IFAE	IFAE	No	TB tested

1: Assembly site (IFAE)
1: Demonstrator
1: Batch
0000XX: Serialization

[DB Info]

- No major issues during the assembly
  - Small glue spillage in M007 at the right wing (no pads affected)
  - M009 and M010 sensors show many scratches and damage at the corners (during UBM)
- Wire bonding carried out without problems



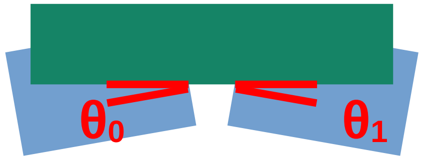
Metrology (I): Size and positioning

	Glue [mg]	Weight [g]	Length [mm]	Gap [µm]	Δ F-C 0 (av.) [mm]	Δ F-C 1 (av.) [mm]	θ_0 [deg]	θ_1 [deg]
Targ.	13.0	~3.000?	41.150	> 50	1.719	1.719	< ±0.1	< ±0.1
M005	12.0	3.051	41.168	109.9	1.643	1.647	-0.030	-0.083
M006	13.5	3.071	41.121	81.8	1.633	1.603	-0.049	+0.188
M007	14.9	3.047	41.102	107.1	1.650	1.647	-0.034	-0.059
M008	10.5	3.066	41.133	92.6	1.585	1.638	+0.051	-0.053
M009	13.3	3.072	41.115	77.8	1.603	1.619	-0.011	-0.168
M010	11.7	3.031	41.125	90.1	1.559	1.539	+0.127	+0.138

Flex – chip distance

- All the modules show shorter values than nominal (jigs alignment)

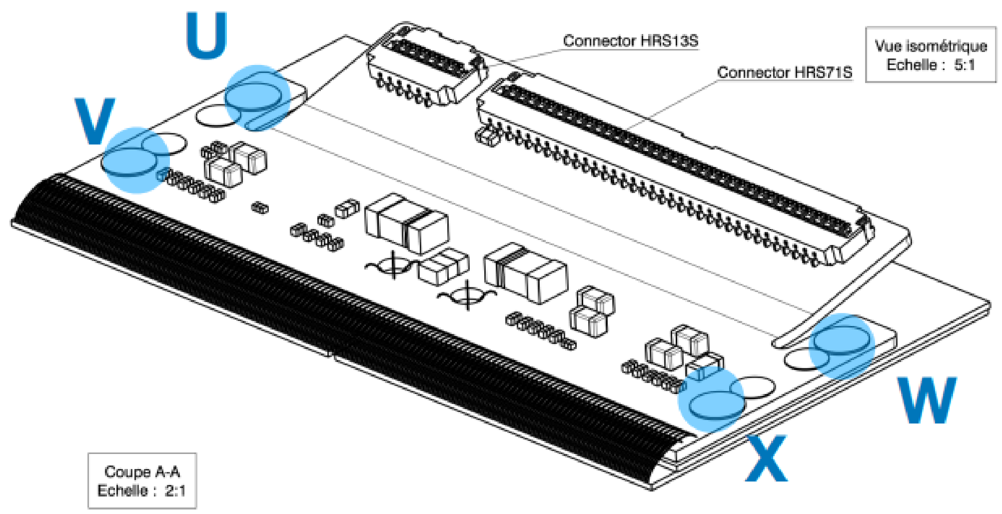
Rotation



- Some hybrids show rotation out of specs (but not by far)
- No problems with WB
- M010 seems that the flex was slightly misplaced

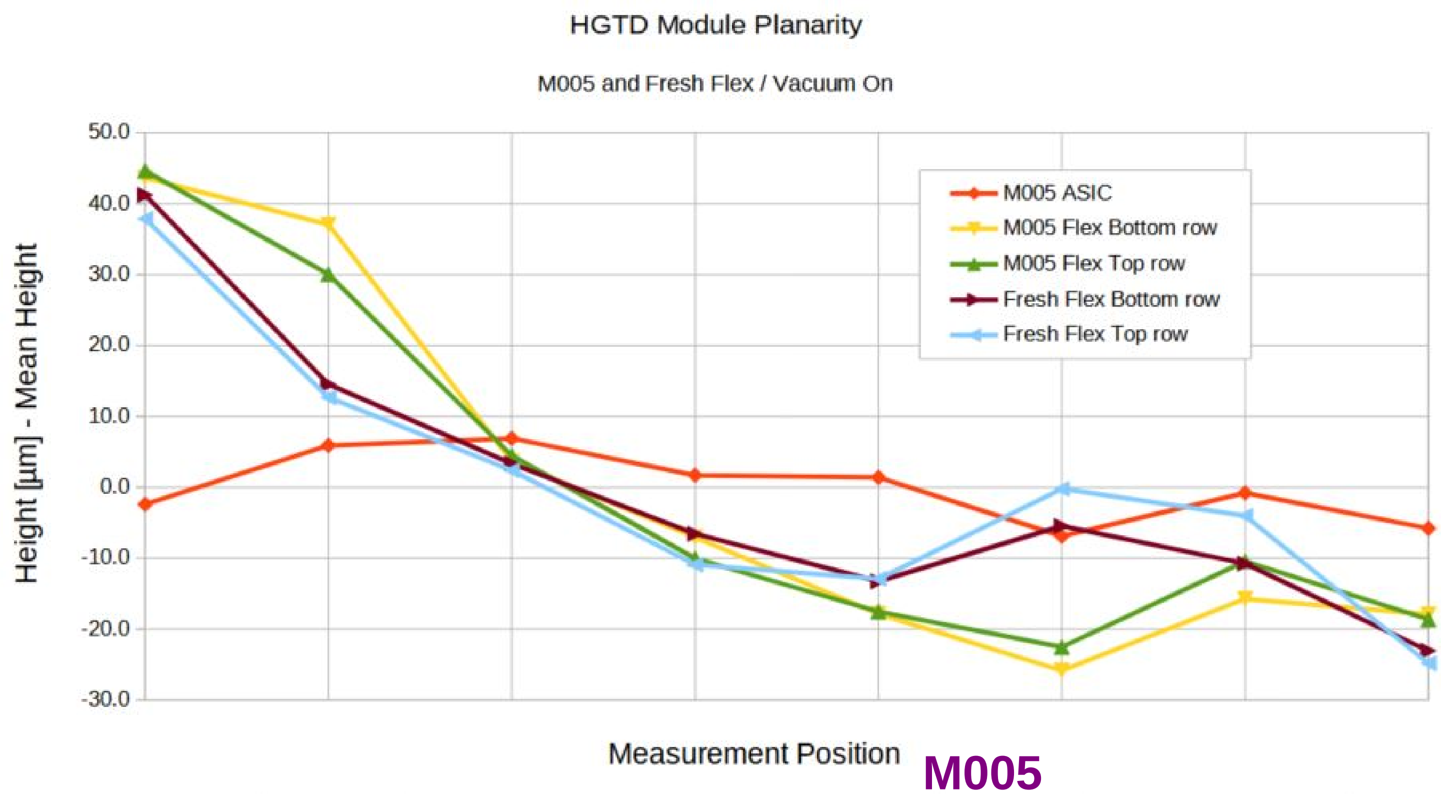
Metrology (II): Thickness

[mm]	U	V	W	X	Δ [µm]
M005	1.454	1.503	1.490	1.477	49
M006	1.456	1.480	1.478	1.497	41
M007	1.441	1.480	1.509	1.510	69
M008	1.459	1.487	1.486	1.480	28
M009	1.452	1.516	1.464	1.489	65
M010	1.463	1.454	1.496	1.463	42
Mean	1.454	1.487	1.487	1.486	33



- All modules are thinner at point U (assembly or flex?)
- Average thickness ~1.490 mm (except point U)
- Difference between max and minimum thickness within the module is always below 70 µm

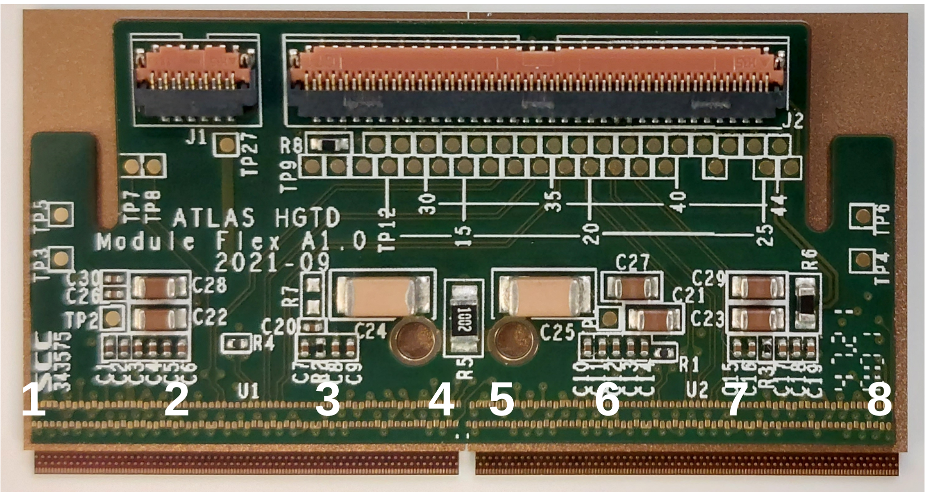
Metrology (III): Planarity



- Height values = Z of the pad – Z of the base
- Measured on M005 and a fresh flex
- Same points for the top and bottom rows of pads on the flex and the ASIC pads
- Plot: For each row, distance of height in each point wrt mean height for this row

Δ between highest and lowest < 70 µm

Same tendency in assembled module and fresh flex



M005

[mm]	1	2	3	4	5	6	7	8
ASIC	0.294	0.302	0.303	0.298	0.298	0.290	0.296	0.291
Top Row	1.523	1.517	1.483	1.473	1.462	1.454	1.464	1.462
Bot. Row	1.524	1.510	1.484	1.470	1.462	1.457	1.469	1.461

Flex

[mm]	1	2	3	4	5	6	7	8
Top Row	0.550	0.523	0.512	0.502	0.495	0.503	0.498	0.486
Bot. Row	0.546	0.521	0.511	0.498	0.496	0.508	0.505	0.484