Low Power Mode

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Weekly student instrumentation meeting

31/03/2023

BERKELEY LAB

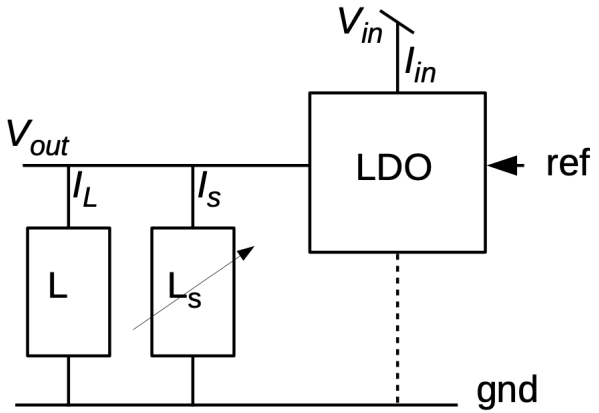
ATLAS EXPERIMENT

Introduction

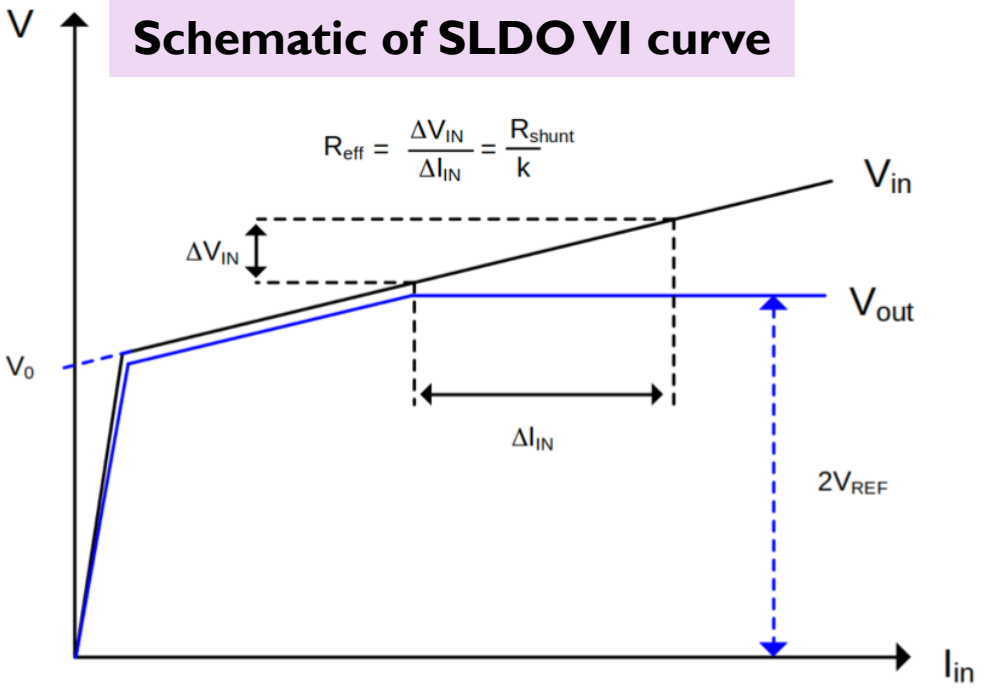
- ITkPixV1 modules will be operated in a serial power chain, suppying a constant current
- To allow this, the chip has a SLDO circuit, which powers the main load (the chip) and the internal load (shunt element)
- The shunt element is designed such that it achieves the required input current, regardless of what the chip does
- Put in V_{in} which regulates voltage to V_{out}
- Linear behaviour driven by R_{eff}
- Offset voltage V_0 (or V_{ofs}) is set by a separate circuit
- Overall behaviour can be described as:

$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}} \qquad [V_{in} > V_0]$$

Schematic of LDO circuit



Schematic of SLDO VI curve



Low power mode circuit

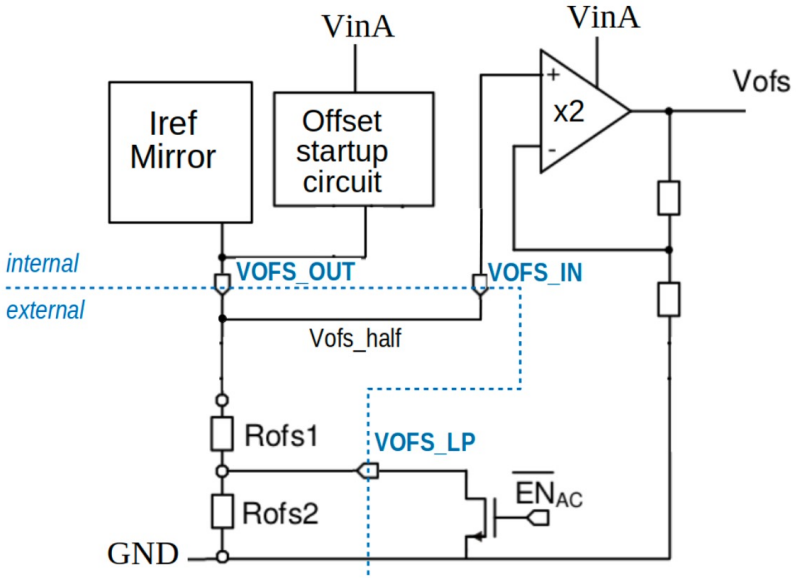
- In nominal operation we need a current of ~6 A, to achieve the required operating voltage of ~1.8 V (for an SLDO output voltage of 1.2 V with some overhead)

→ Chips require active cooling during operation like this

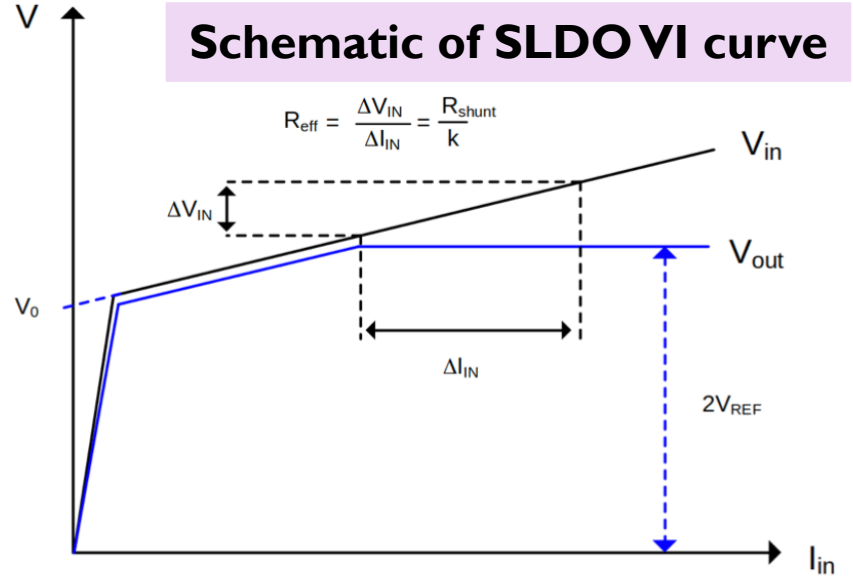
- This complicates running quick tests to establish chip healthiness, e.g. during detector commissioning
- Chip has the capability to run in low power mode, where not all chip functionality is available, but e.g. reading/writing registers can be checked
- Enabling low power mode is implemented in the chip through a switch (internal to the chip), and two external resistors R_{ofs1} and R_{ofs2}

→ By default the switch is conductive, meaning only resistor R_{ofs1} is used (leading to a nominal V_{ofs} of around 1 V)

V_{offset} generation circuit



Schematic of SLDO VI curve



Low power mode circuit

- If the switch is turned off, both R_{ofs1}+R_{ofs2} are used, leading to a larger offset voltage
- In turn, this means that the required SLDO output voltage of 1.2 V is reached at lower currents

- The switch is turned on and off by providing an AC signal

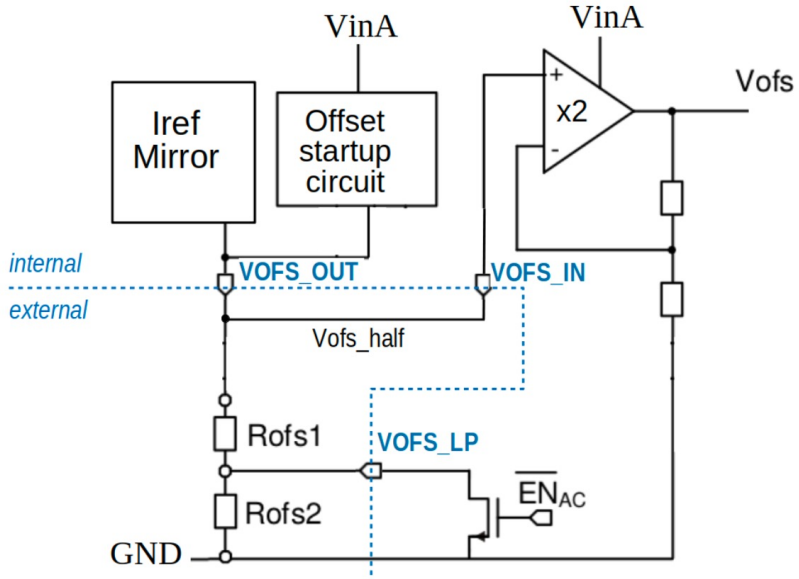
→ Use AC signal, because ground is not well-defined in a serial power chain

→ Only planned to be used during commissioning, when it is possible to provide this signal externally using a function generator

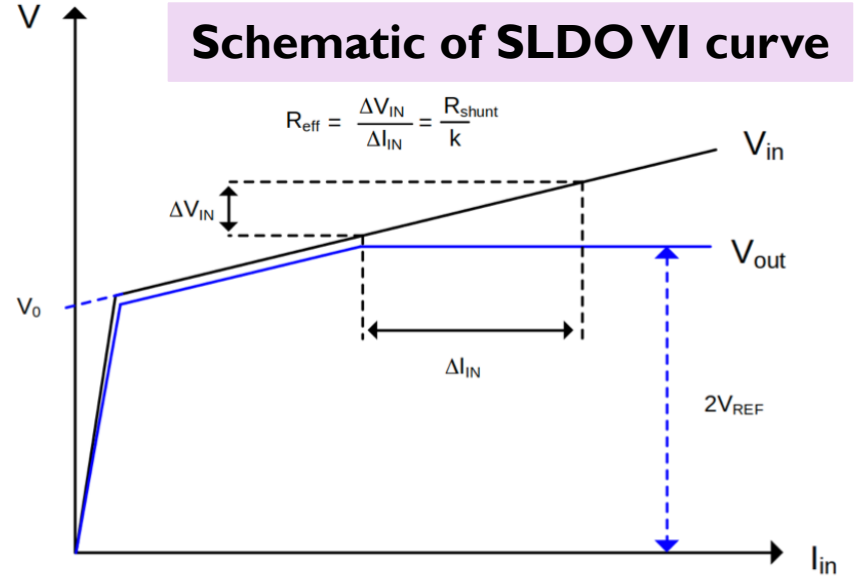
- But, in the meantime we need to be able to test this functionality during module QC

→ Provide the AC signal via the DisplayPort cable directly from the YARR FPGA

V_{offset} generation circuit



Schematic of SLDO VI curve



YARR implementation

- Implemented executable in YARR, which writes several registers that steer parameters for enabling low power mode:

```
./bin/switchLPM on/off
-e <int>: enabled TX channels (from binary number, e.g. for 1111 provide 15)
-s <int> spec number
-f <int> AC signal frequency in kHz
```

- Can send one signal per DP port on Ohio card → by default all of them are switched on or off, but there is the option to select which ones you want
- Spec number is configurable (default is 0)
- Can select which AC signal frequency to use → requirements is > 80 kHz for a square wave signal

FW implementation

- Implemented AC signal by scaling one of the standard clocks (160 MHz) in the firmware:
  - Define low power mode enable signal
  - Take 160 MHz clock to drive a counter
  - If counter is about a certain number (set by frequency parameter), switch the low power mode signal

  → Get AC signal with a particular frequency
  - Depending on the enable register, output the AC signal to one of the FPGA pins which is then connected to one of the pins on the display port

Output AC signal

Enable register

```
    -- End of low power mode pulse and control register
    lpm_pulse_o <= lpm_pulse_s and ctrl_reg_0_s(c_TX_CHANNELS-1 downto 0);

    -- Prescaler for low power mode AC signal
    lpm_pulse_gen: process(clk_160_s, rst_n_s)
    begin
        if (rst_n_s = '0') then
                lpm_pulse_s <= (others => '0');
                lpm_cnt <= (others => '0');
        elsif (rising_edge(clk_160_s)) then
                lpm_cnt <= lpm_cnt + 1;
                ctrl_reg_1_t <= ctrl_reg_1_s;
                if (lpm_cnt >= unsigned(ctrl_reg_1_t)) then
                        lpm_cnt <= (others => '0');
                        lpm_pulse_s <= not lpm_pulse_s;
                end if;
        end if;
    end process lpm_pulse_gen;
```

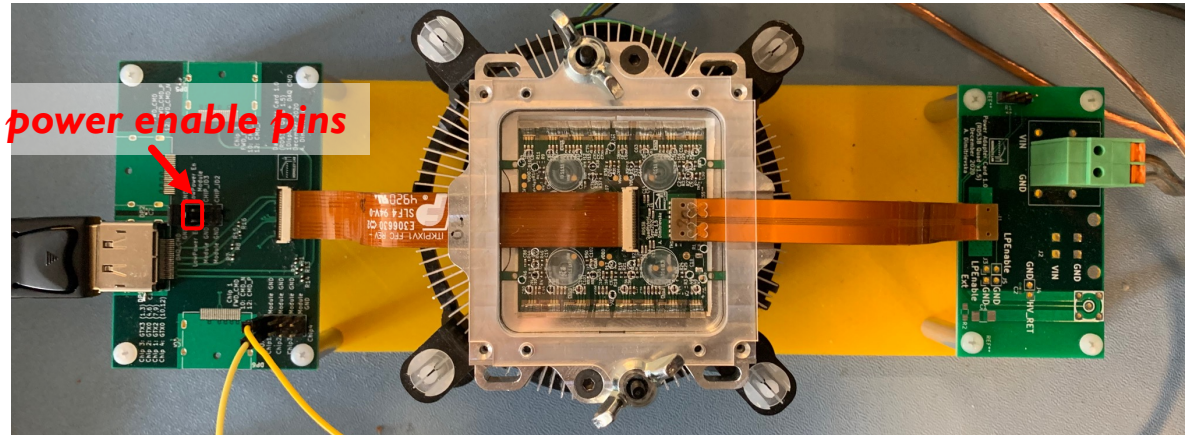
Standard 160 MHz clock

Counter condition based on set frequency

AC pulse testing

- Tested low power enable on ITkPix Quad
- Data adapter card has low power enable pins (which should have a jumper if using low power mode)
- Can also probe the low power enable signal on these pins

→ Firmware seems to generate the signal with the desired frequency



100 kHz signal

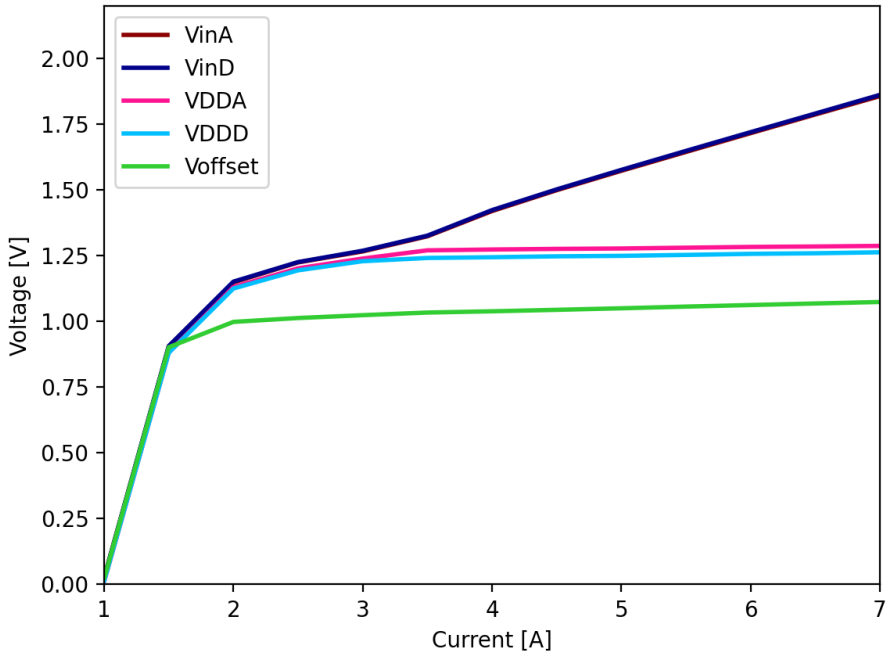
66 kHz signal

Results

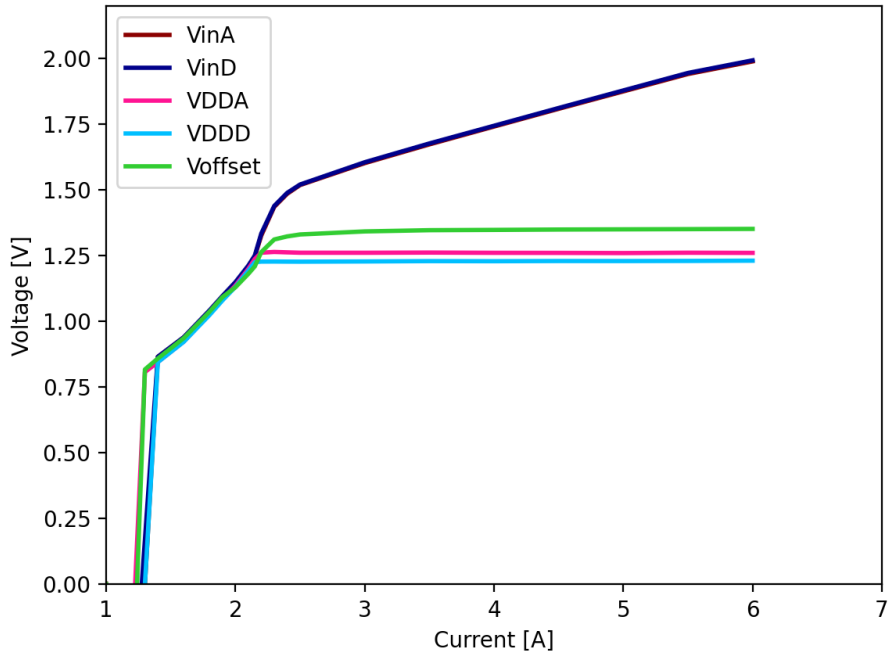
- Tested low power mode by taking SLDO VI curves
- Note: To make full use of low power mode also need to low power config (switching off all core columns and preamplifier)
- With low power mode enable it is possible the reach an output voltage of 1.2 V already at a current of ~2 A

→ Enabling the low power mode from the YARR DAQ works as expected and is ready to be used in QC

Nominal



Low Power Mode



Thank you!

Questions?

Powering circuit