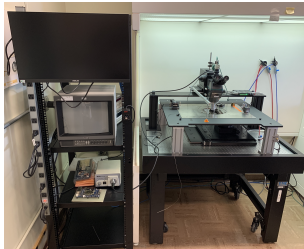


# Wafer Probing Update

Maurice Garcia-Sciveres, Timon Heim, **Elliot Reynolds**

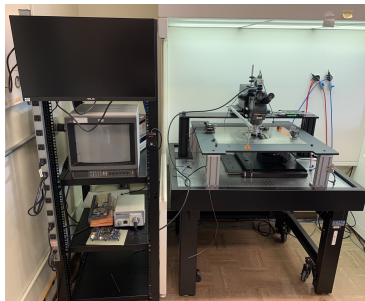
LBLN Instrumentation Meeting, 17<sup>th</sup> March 2023



**BERKELEY LAB**



- Preparing to qualify as a backup site for ITk pixel wafer probing
- “Custom” probe station assembled: vibration isolation table, laminar flow hood, vacuum chuck, microscope, Zaber X-Y and Z stages
- We have an RD53a wafer, an ITkPixV1 wafer, and single chip, and the necessary relevant probe cards, and well as the KX1 and KX2 BDAQ boards



11	-	-	-	B	C	C	B	-	-	-
10	-	B	B	<b>A</b>	C	B	<b>A</b>	C	-	-
9	-	C	C	B	B	A	A	A	A	-
8	B	C	B	B	A	A	B	C	A	-
7	C	A	C	B	B	B	C	A	C	A
6	B	A	B	B	A	A	B	A	B	C
5	<b>A</b>	A	A	<b>A</b>	A	A	<b>A</b>	A	A	<b>A</b>
4	A	B	A	A	B	C	B	X	X	B
3	B	A	A	A	B	B	B	C	C	-
2	B	B	A	A	B	B	B	B	A	-
1	-	C	A	A	A	B	B	A	-	-
0	-	-	B	<b>A</b>	A	B	<b>A</b>	-	-	-
	0	1	2	3	4	5	6	7	8	9

11	-	-	-	B	C	C	B	-	-	-
10	-	B	B	<b>A</b>	C	B	<b>A</b>	C	-	-
9	-	C	C	B	B	A	A	A	A	-
8	B	C	B	B	A	A	B	C	A	-
7	C	A	C	B	B	B	C	A	C	A
6	B	A	B	B	A	A	B	A	B	C
5	<b>A</b>	A	A	<b>A</b>	A	A	<b>A</b>	A	A	<b>A</b>
4	A	B	A	A	B	C	B	A	A	B
3	B	A	A	A	B	B	B	C	C	-
2	B	B	A	A	B	B	B	B	A	-
1	-	C	A	A	A	B	B	A	-	-
0	-	-	B	<b>A</b>	A	B	<b>A</b>	-	-	-
	0	1	2	3	4	5	6	7	8	9

With chip-by-chip corrections. Only re-measured manually changed chips and previously **X** chips

- Updated to KX2 board and latest BDAQ software/firmware version 1.7
- Working on single chip to get scans running
- Attempted various scans, with mostly default parameters (and a little hacking), and resulting in differing success so far...

Scan/test	Running (even with errors)
Register scan	✓
Digital scan	✓
Analog scan	✓
Threshold scan	✓
Noise occupancy scan	✓
External trigger scan	✗
Source scan (random trigger)	✓
Tune TLU	✗
Injection delay scan	✗
In time threshold scan	✗
Crosstalk scan	✓
Hitor calibration	✓

- 1 Implement remaining scans/tests, and check parameters on these scans/tests
  - Should this be left for later?
- 2 Implement contact sensing and height map to control vertical movement
- 3 **Test movement+electrical tests working on ITkPix v1.1 wafer**
- 4 Deep-clean of probe station, and procure nano structures for probe card cleaning and heat sink for BDAQ board
  - Currently uncertain due to my ankle

# Preliminary Scan Results



# Register Scan

- Writes random data into the specified registers, then reads back the data and compares read and written data



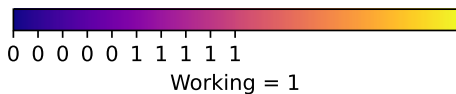
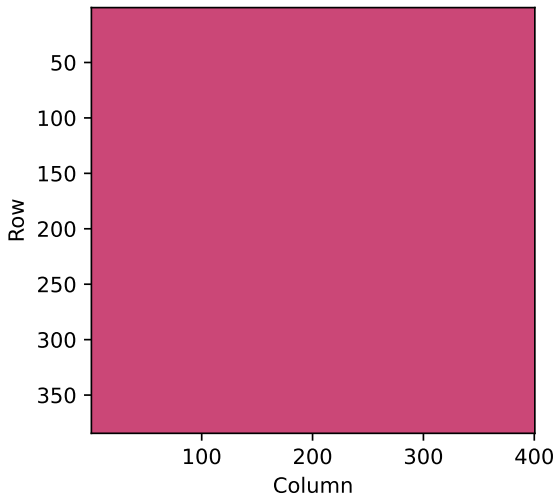
This is a bdaq53 pixel\_register\_scan for chip 0x162BC.  
Run 20230317\_022047\_pixel\_register\_scan was started 2023-03-17 02:20:47.

Scan config	Value	ITkPixV1 config	Value
test_pattern	170	DAC_PREAMP_I_DIFF	895
trigger_pattern	0xffffffff	DAC_PREAMP_R_DIFF	895
		DAC_PREAMP_TL_DIFF	895
		DAC_PREAMP_TR_DIFF	895
		DAC_PREAMP_T_DIFF	895
		DAC_PREAMP_M_DIFF	895
		DAC_PRECOMP_DIFF	300
		DAC_COMP_DIFF	523
		DAC_VFF_DIFF	160
		DAC_TH1_L_DIFF	220
		DAC_TH1_R_DIFF	220
		DAC_TH1_M_DIFF	220
		DAC_TH2_DIFF	0
		DAC_LCC_DIFF	200
		LEACKAGE_FEEDBACK	0

ITKPixV1 preliminary

Chip S/N: 0x162BC

Map of Working Pixel Registers ( $\Sigma = 153600.0$ )



# Digital Scan

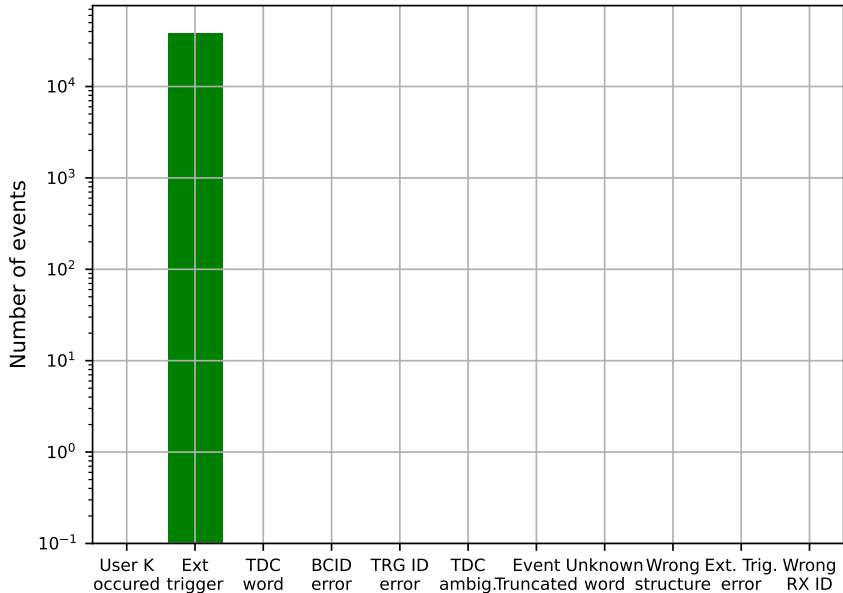
- Digital signal injected into every enabled pixel
- Only a few pixels are injected at once and the injection mask is shifted until all enabled pixels have been injected

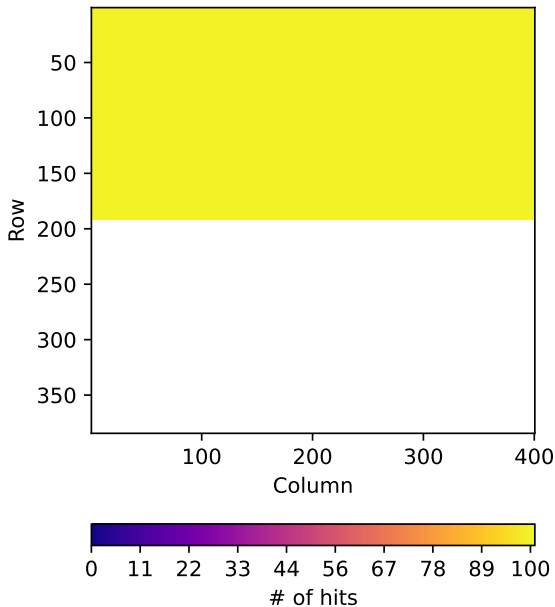


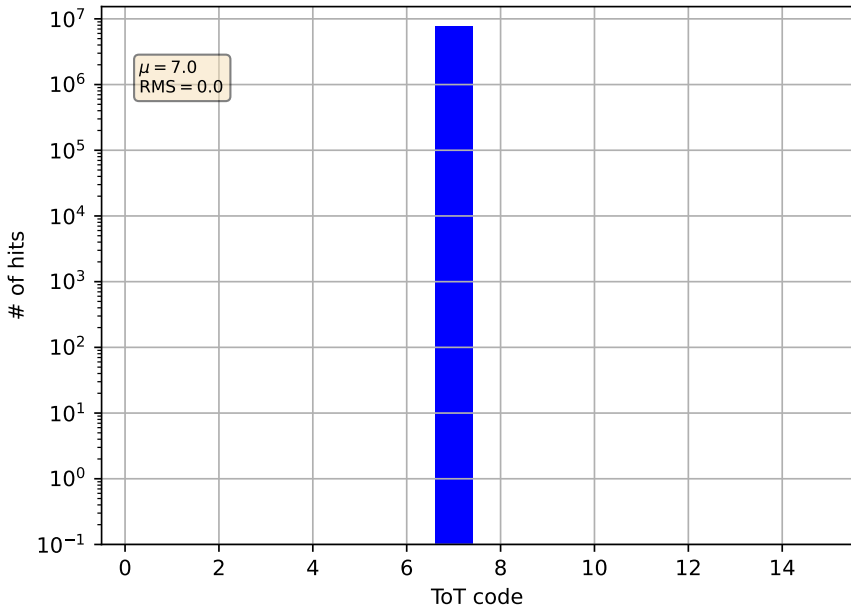
This is a bdaq53 digital\_scan for chip 0x162BC.  
Run 20230208\_145656\_digital\_scan was started 2023-02-08 14:56:56.

Scan config		ITkPixV1 config	
Scan config	Value	ITkPixV1 config	Value
n_injections	100	DAC_PREAMP_L_DIFF	895
start_column	0	DAC_PREAMP_R_DIFF	895
start_row	0	DAC_PREAMP_TL_DIFF	895
stop_column	400	DAC_PREAMP_TR_DIFF	895
stop_row	192	DAC_PREAMP_T_DIFF	895
trigger_pattern	0xfffffff	DAC_PREAMP_M_DIFF	895
		DAC_PRECOMP_DIFF	300
		DAC_COMP_DIFF	523
		DAC_VFF_DIFF	160
		DAC_TH1_L_DIFF	220
		DAC_TH1_R_DIFF	220
		DAC_TH1_M_DIFF	220
		DAC_TH2_DIFF	0
		DAC_LCC_DIFF	200
		LEACKAGE_FEEDBACK	0

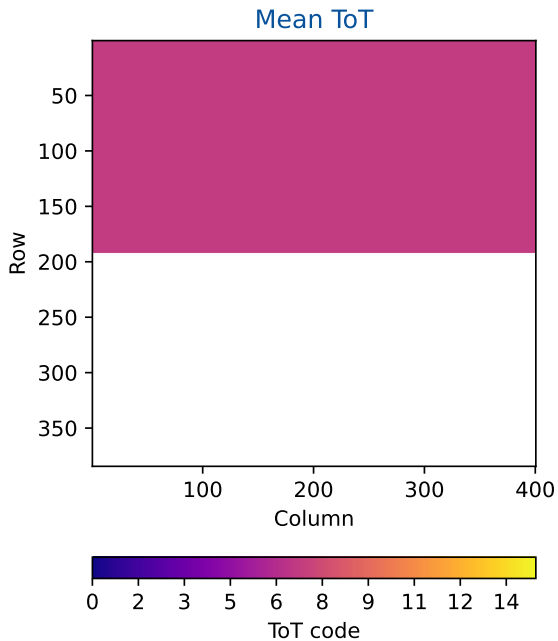
Event status ( $\Sigma = 38400$ )

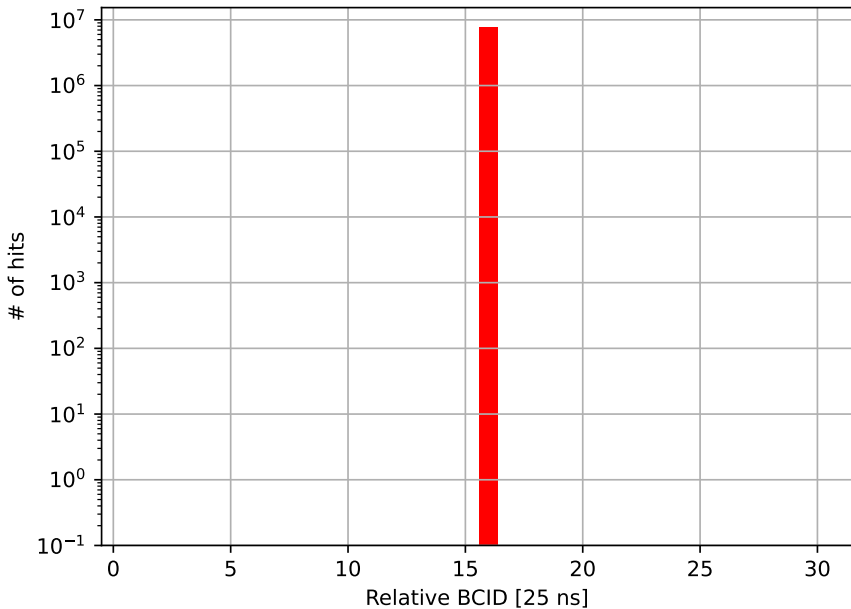


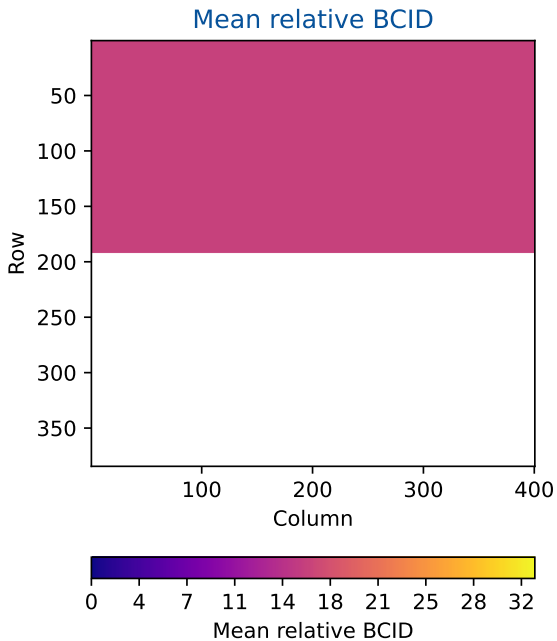
Occupancy ( $\Sigma = 7680000$ )

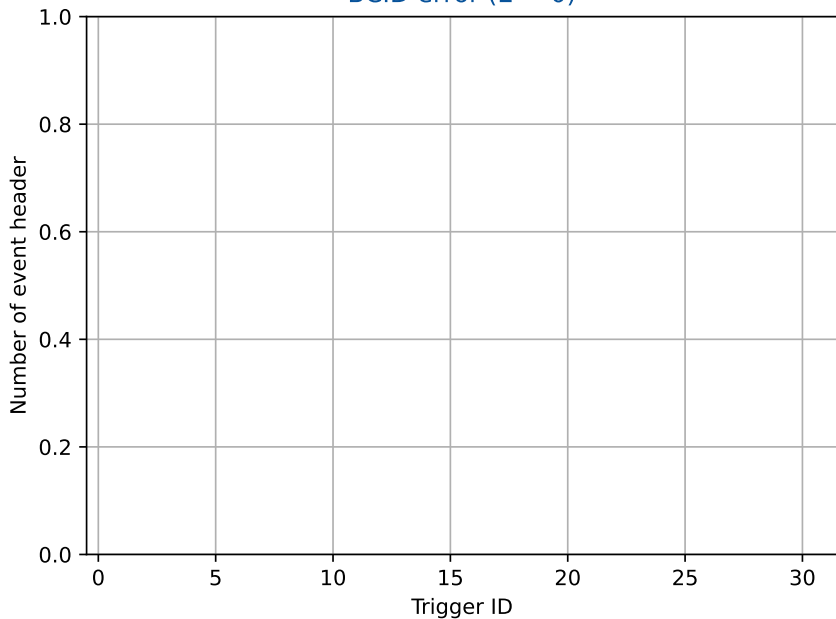
Time-over-Threshold distribution ( $\Sigma = 7680000$ )



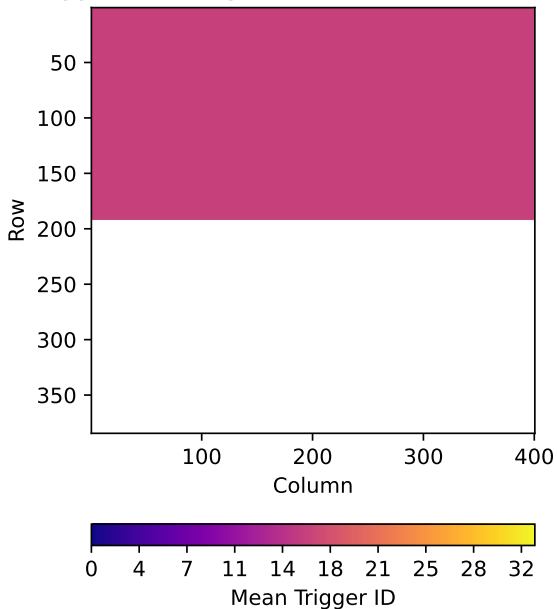


Relative BCID ( $\Sigma = 7680000$ )



BCID error ( $\Sigma = 0$ )

## Trigger ID Histogram without Error correction



# Analog Scan

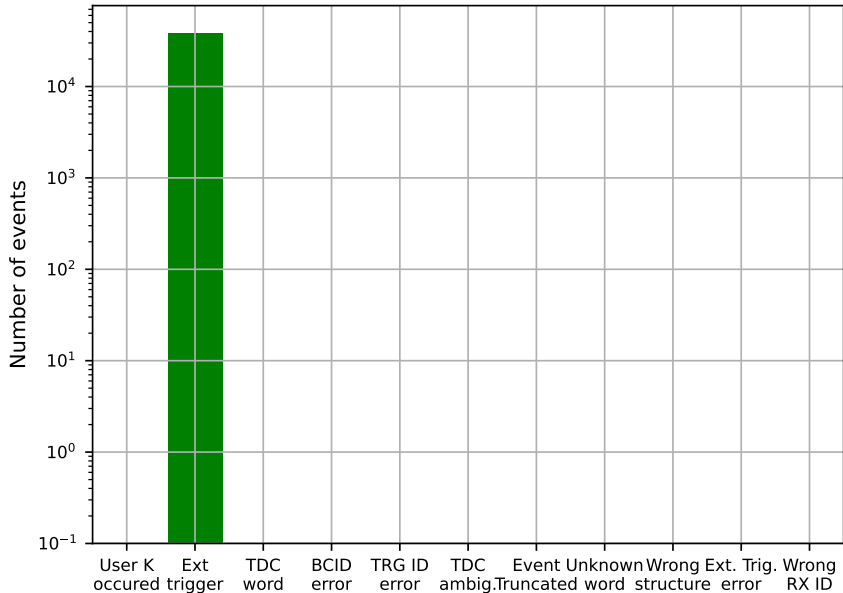
- Analog pulse injected into every enabled pixel
- Only a few pixels are injected at once and the injection mask is shifted until all enabled pixels have been injected



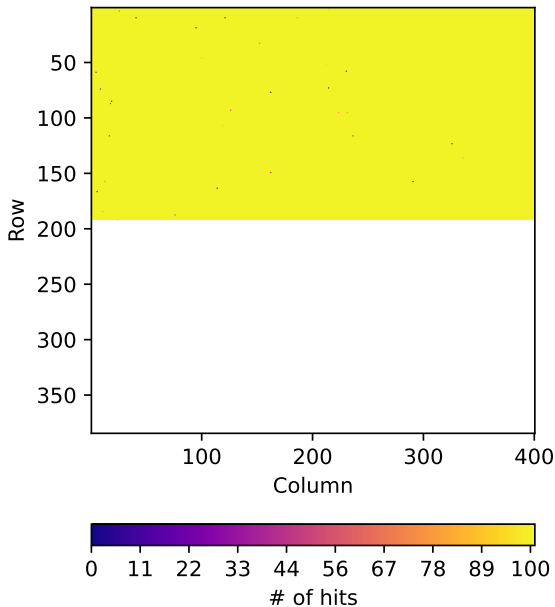
This is a bdaq53 analog\_scan for chip 0x162BC.  
Run 20230317\_013841\_analog\_scan was started 2023-03-17 01:38:41.

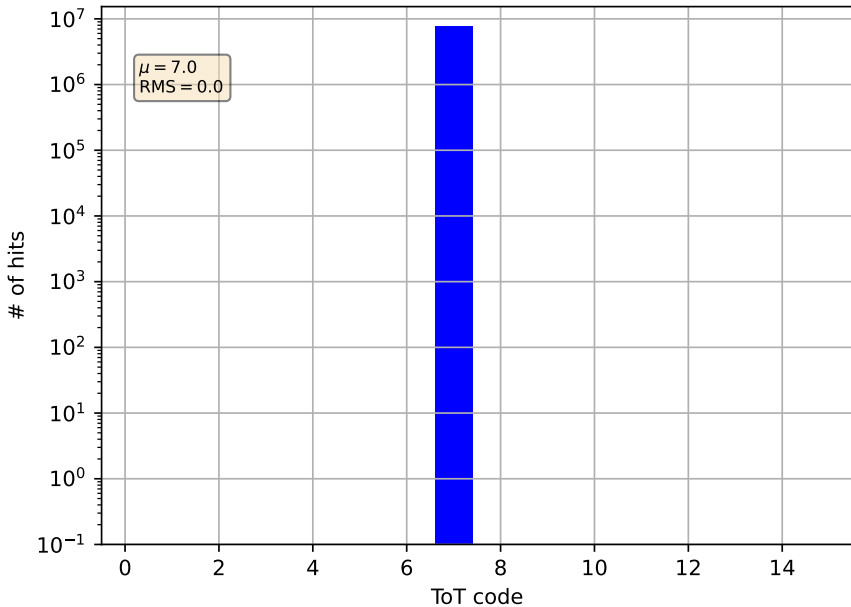
Scan config	Value	ITkPixV1 config	Value
VCAL_HIGH	1300	DAC_PREAMP_I_DIFF	895
VCAL_MED	500	DAC_PREAMP_R_DIFF	895
n_injections	100	DAC_PREAMP_TL_DIFF	895
start_column	0	DAC_PREAMP_TR_DIFF	895
start_row	0	DAC_PREAMP_T_DIFF	895
stop_column	400	DAC_PREAMP_M_DIFF	895
stop_row	192	DAC_PRECOMP_DIFF	300
trigger_pattern	0xf0ffff	DAC_COMP_DIFF	523
		DAC_VFF_DIFF	160
		DAC_TH1_L_DIFF	220
		DAC_TH1_R_DIFF	220
		DAC_TH1_M_DIFF	220
		DAC_TH2_DIFF	0
		DAC_LCC_DIFF	200
		LEACKAGE_FEEDBACK	0

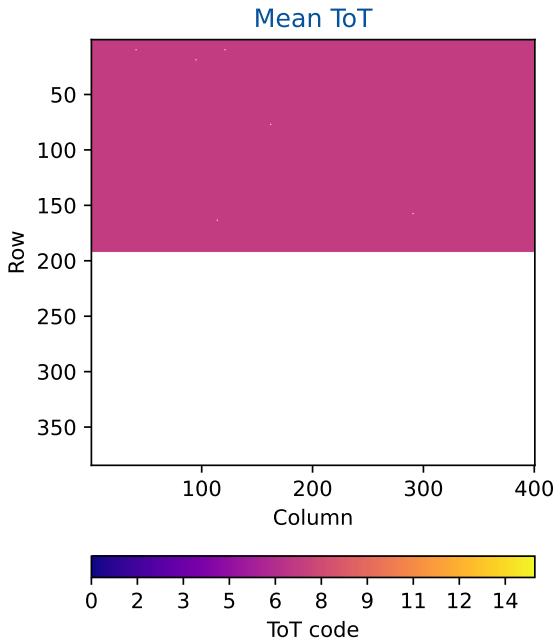
Event status ( $\Sigma = 38400$ )

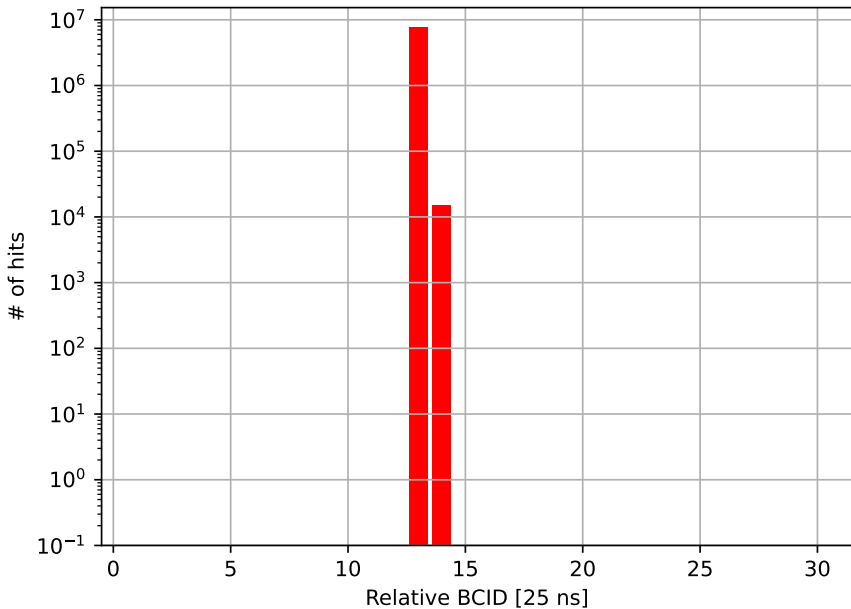


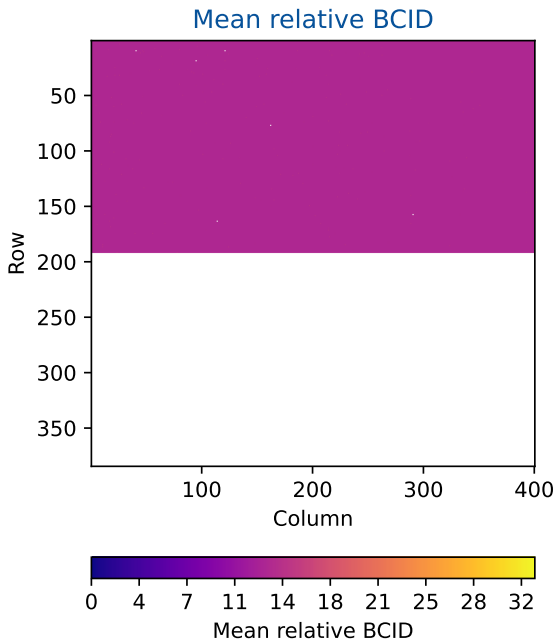


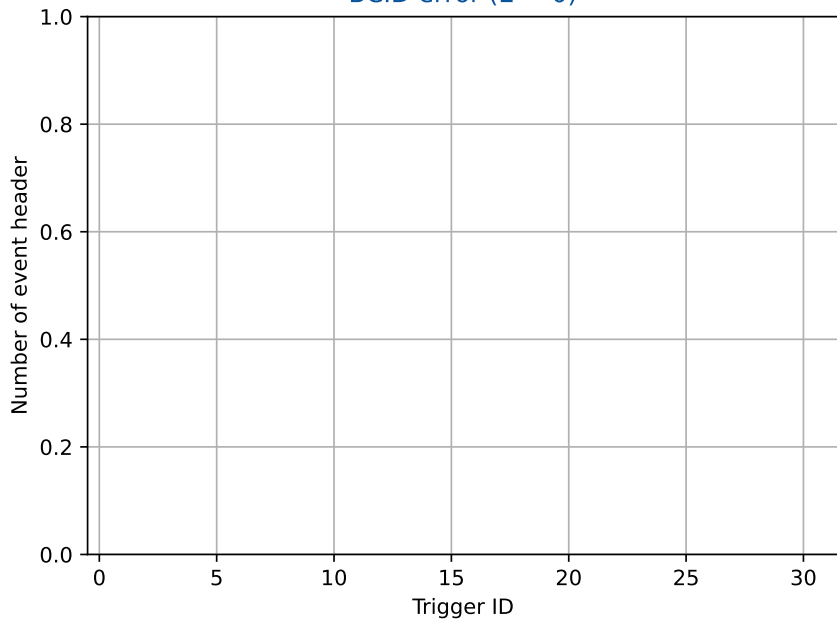
Occupancy ( $\Sigma = 7678085$ )

Time-over-Threshold distribution ( $\Sigma = 7678085$ )

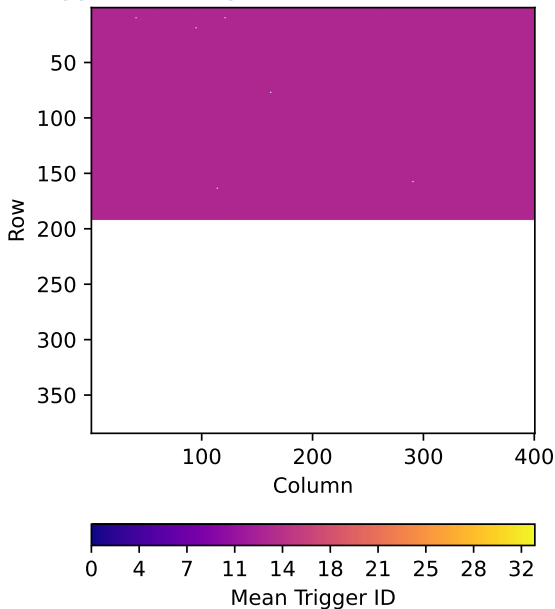


Relative BCID ( $\Sigma = 7678085$ )

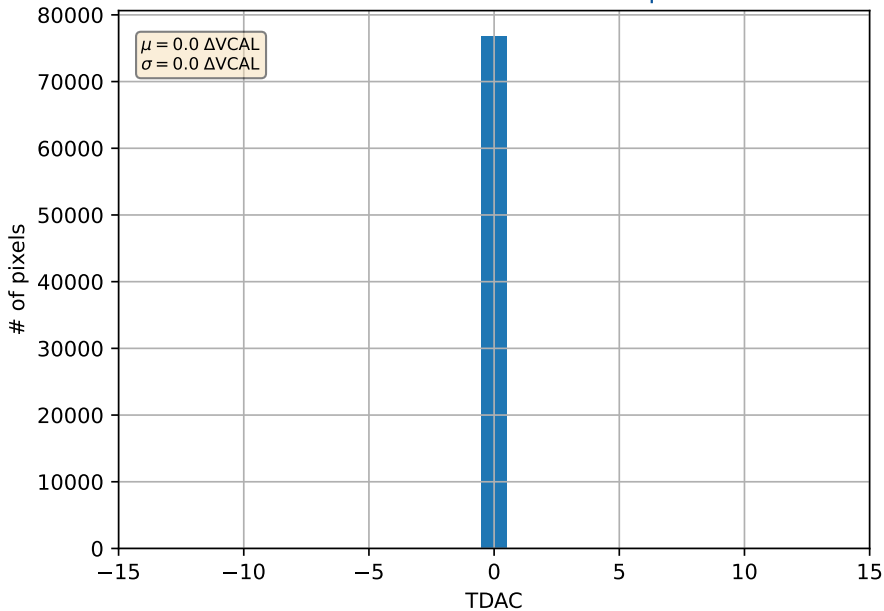


BCID error ( $\Sigma = 0$ )

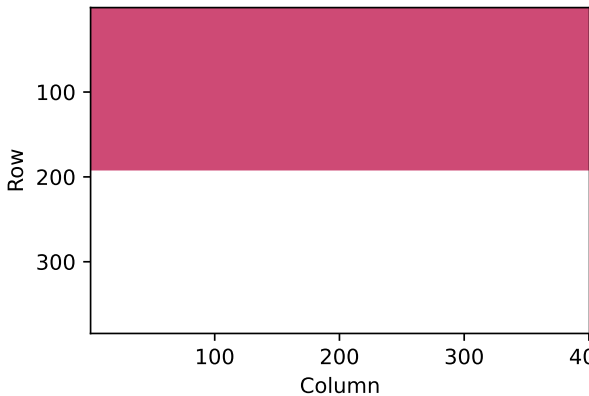
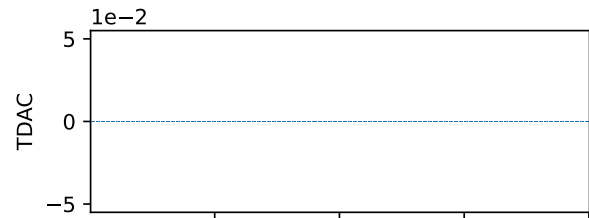
### Trigger ID Histogram without Error correction



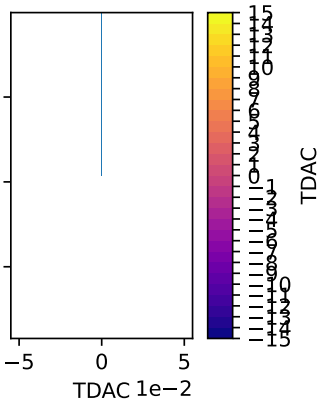
## TDAC distribution for enabled pixels



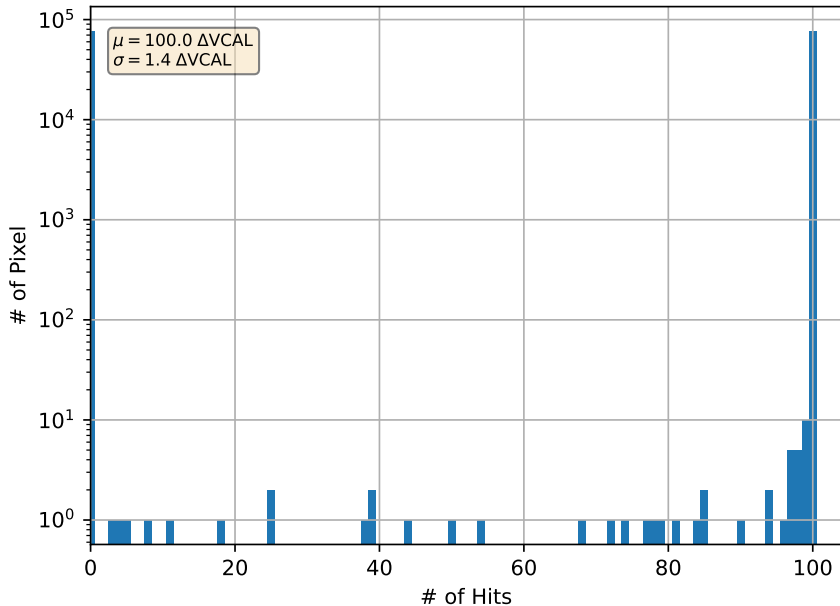




TDAC map  
with projections  
( $\Sigma = 0$ )



Hits per Pixel (logscale)



# Threshold Scan

- Lower value of differential injection DAC is set to a fixed value, while the higher value is scanned over a defined range
- This yields the S-curves for every enabled pixel, which show the the amount of hits in a pixel at a given injection value
- From a fit to this curve, the threshold and noise of every pixel is determined

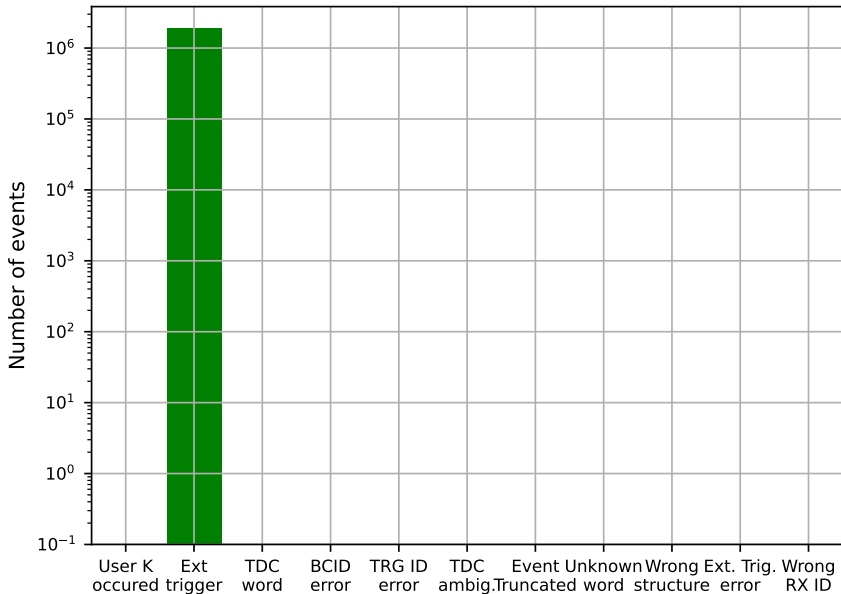


This is a bdaq53 threshold\_scan for chip 0x162BC.  
Run 20230317\_024402\_threshold\_scan was started 2023-03-17 02:44:02.

Scan config	Value	ITkPixV1 config	Value
VCAL_HIGH_start	700	DAC_PREAMP_L_DIFF	895
VCAL_HIGH_step	10	DAC_PREAMP_R_DIFF	895
VCAL_HIGH_stop	1200	DAC_PREAMP_TL_DIFF	895
VCAL_MED	500	DAC_PREAMP_TR_DIFF	895
n_injections	100	DAC_PREAMP_T_DIFF	895
start_column	128	DAC_PREAMP_M_DIFF	895
start_row	0	DAC_PRECOMP_DIFF	300
stop_column	264	DAC_COMP_DIFF	523
stop_row	192	DAC_VFF_DIFF	160
trigger_pattern	0xffffffff	DAC_TH1_L_DIFF	220
		DAC_TH1_R_DIFF	220
		DAC_TH1_M_DIFF	220
		DAC_TH2_DIFF	0
		DAC_LCC_DIFF	200
		LEAKAGE_FEEDBACK	0

$$\text{Charge calibration: } y [e^-] = x [\Delta\text{VCAL}] \cdot (4.65 \pm 0.40) \left[ \frac{e^-}{\Delta\text{VCAL}} \right] + (0 \pm 60.00) [e^-]$$

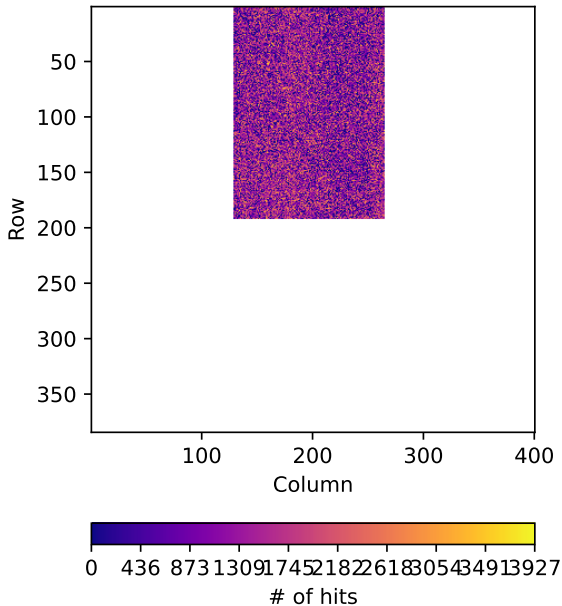
Event status ( $\Sigma = 1920000$ )

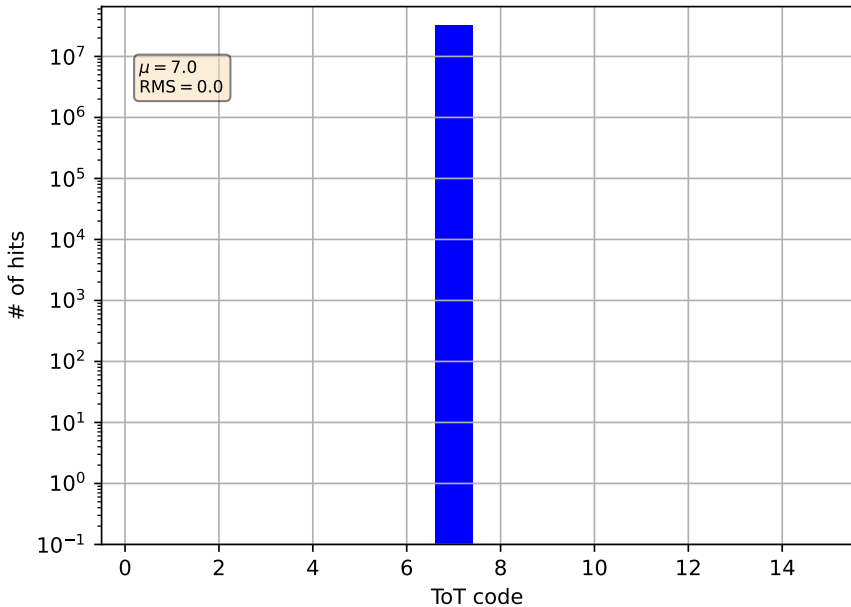


ITKPixV1 preliminary

Chip S/N: 0x162BC

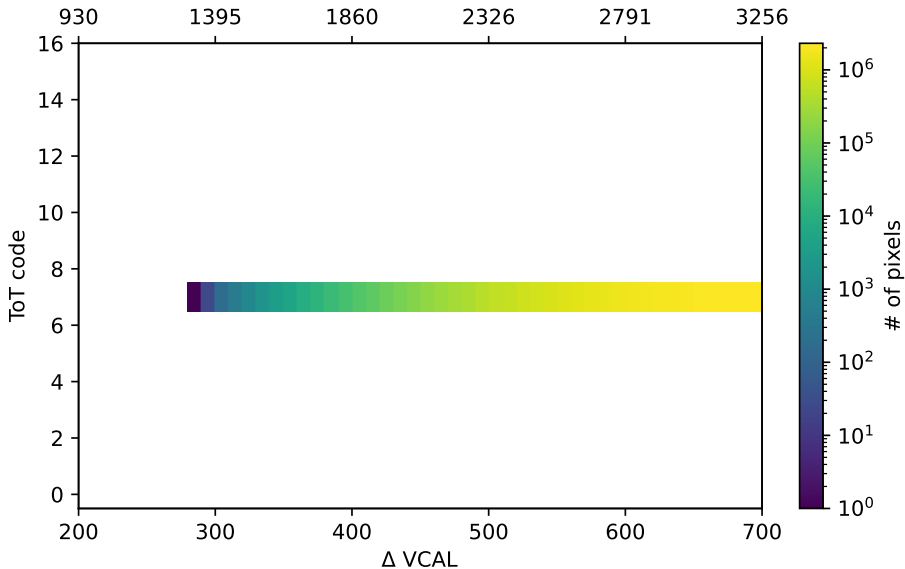
Integrated occupancy ( $\Sigma = 32782464$ )



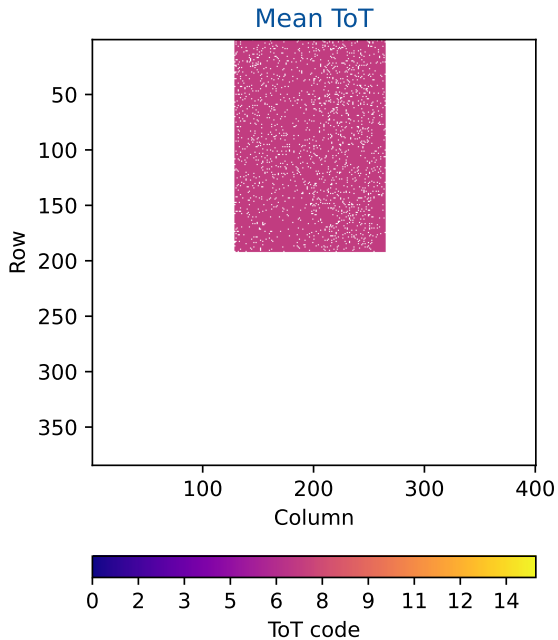
Time-over-Threshold distribution ( $\Sigma = 32782464$ )

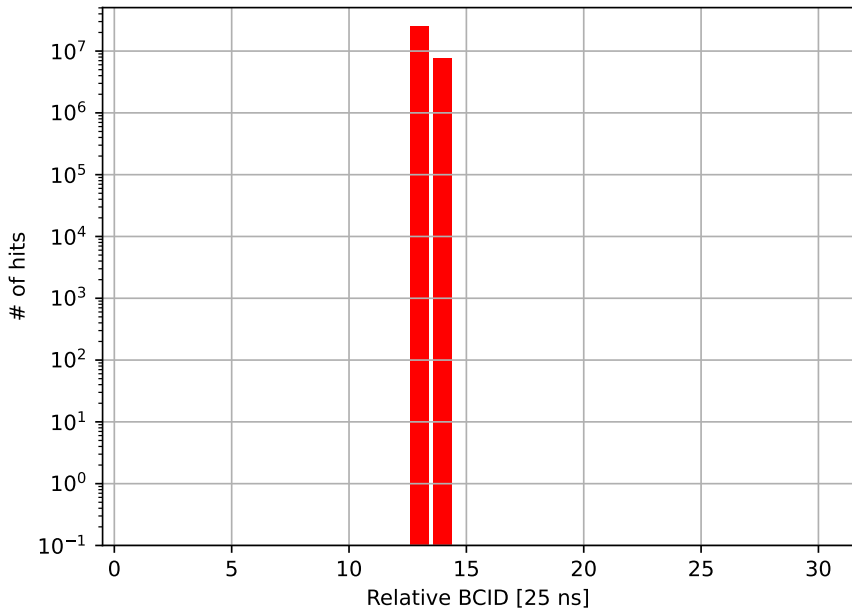
## ToT Scan Parameter Histogram for 26112 pixel(s)

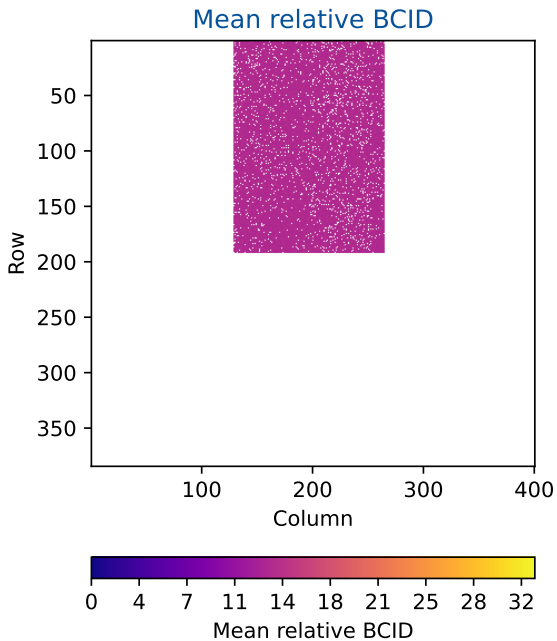
Electrons

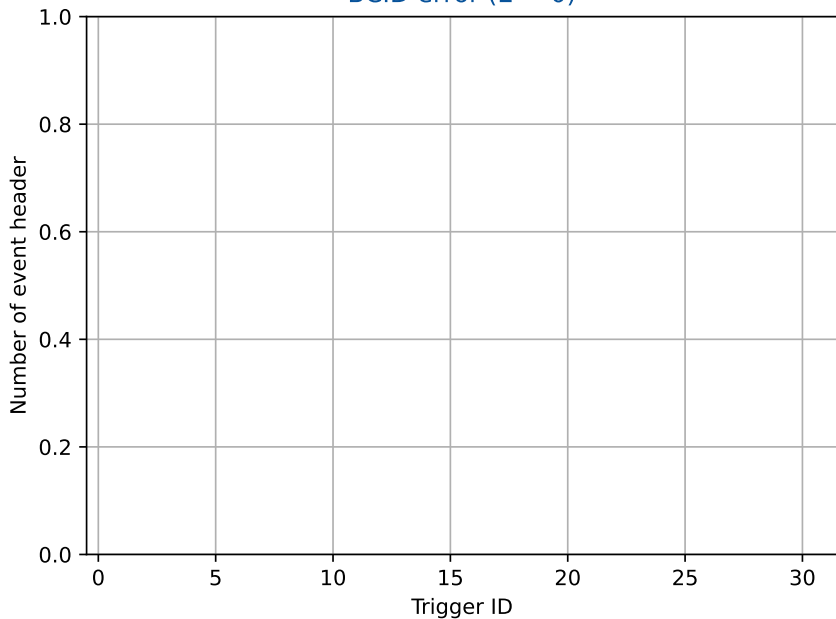




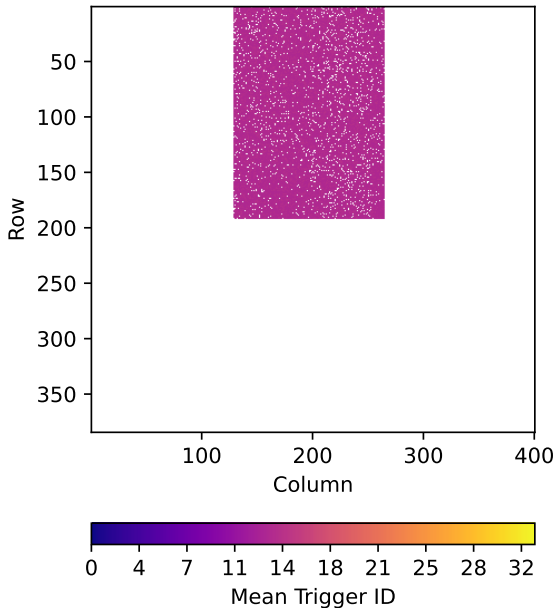


Relative BCID ( $\Sigma = 32782464$ )

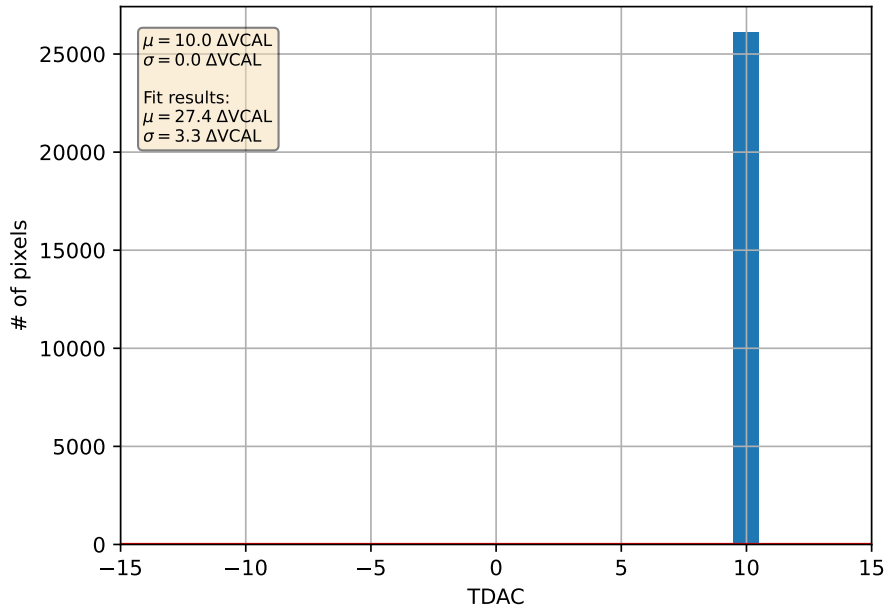


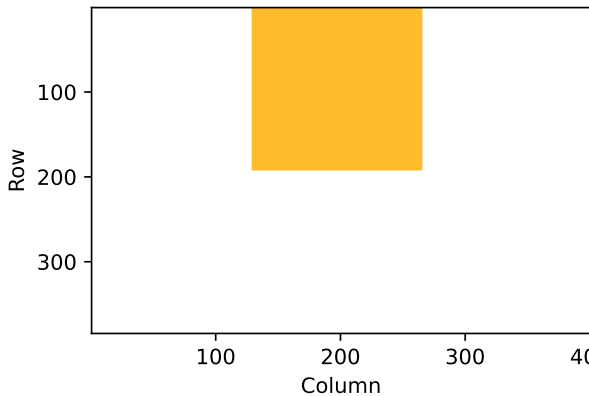
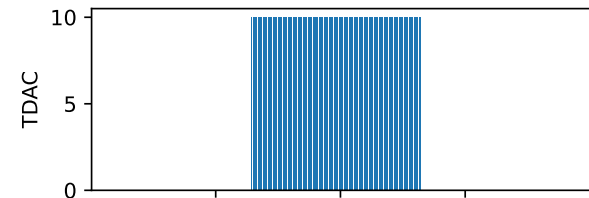
BCID error ( $\Sigma = 0$ )

## Trigger ID Histogram without Error correction

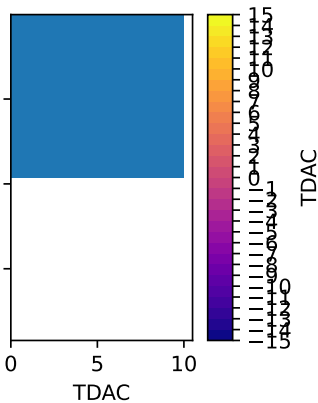


## TDAC distribution for enabled pixels

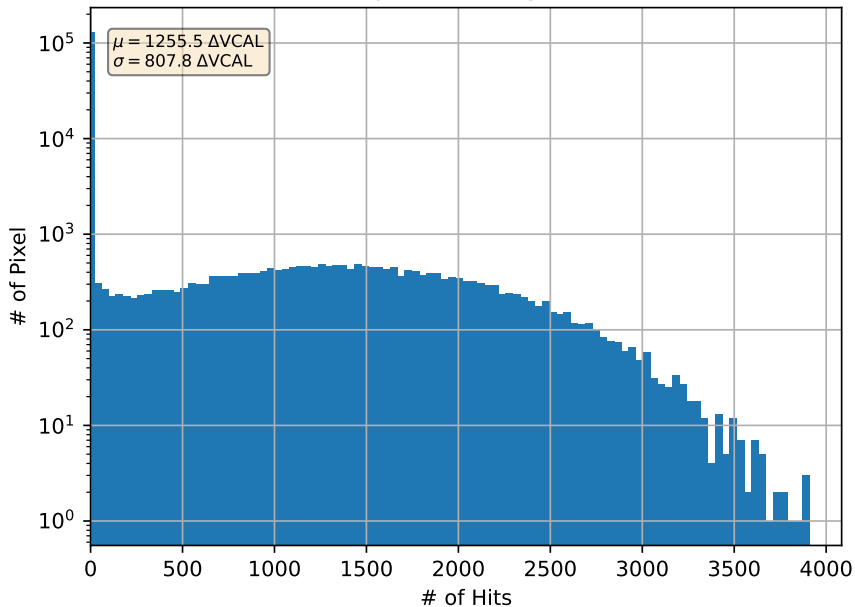




TDAC map  
with projections  
( $\Sigma = 261120$ )

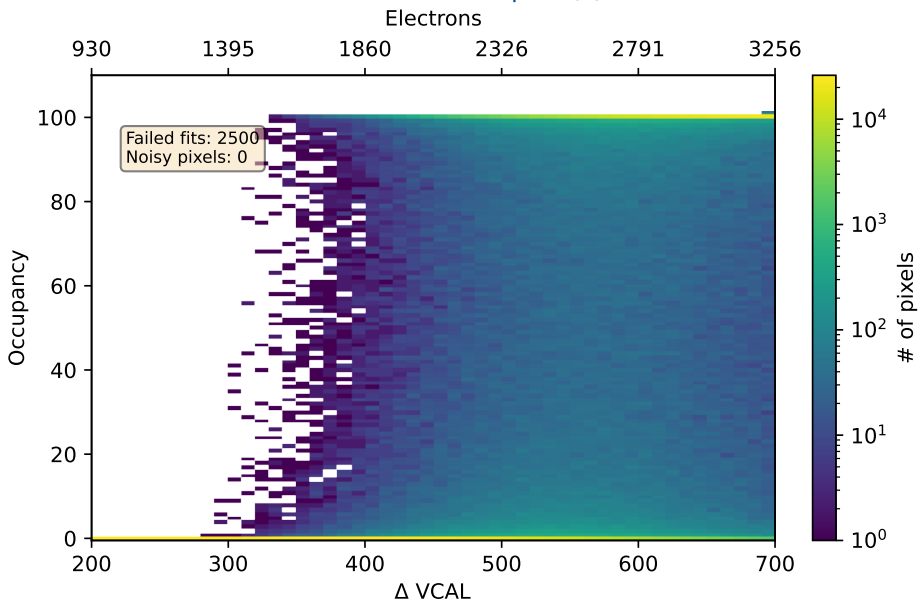


## Hits per Pixel (logscale)

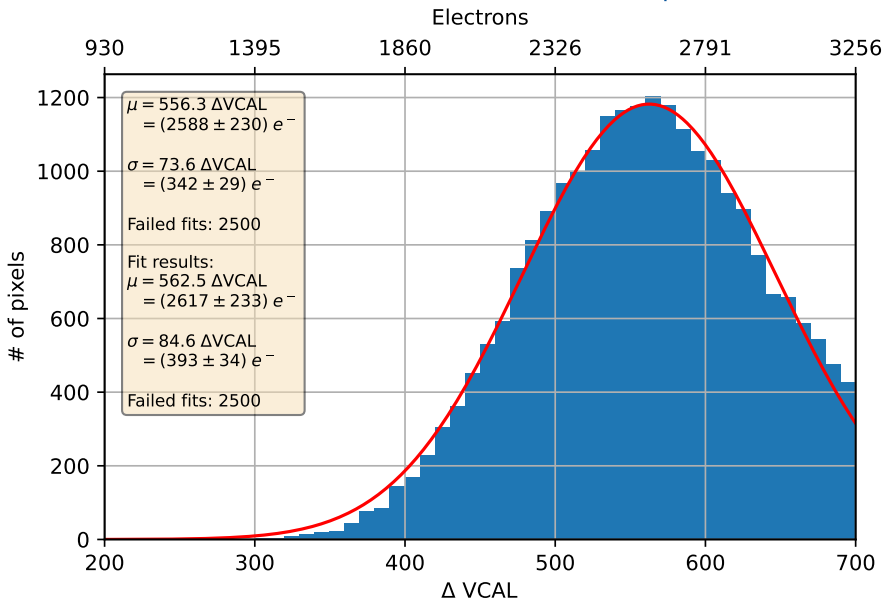




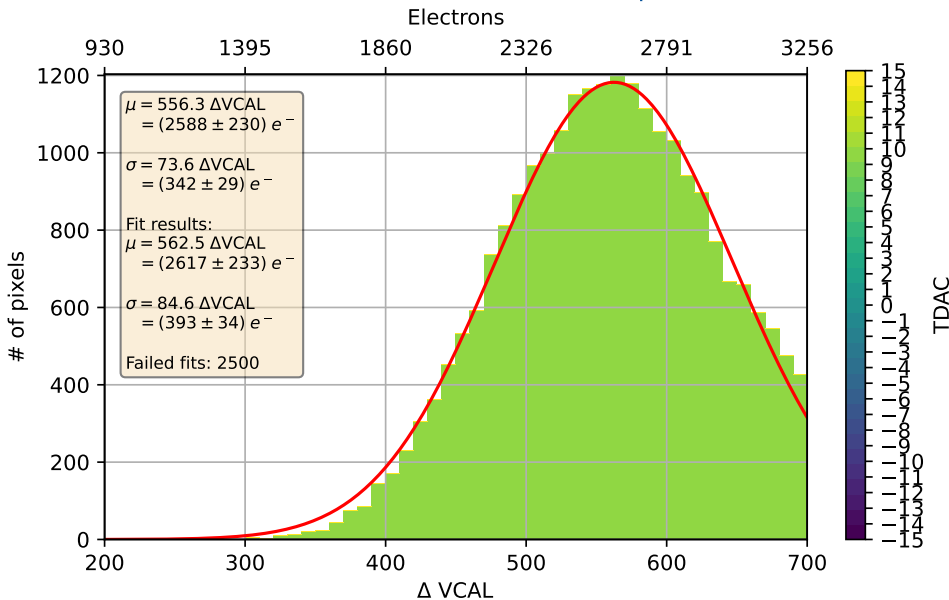
## S-curves for 26112 pixel(s)

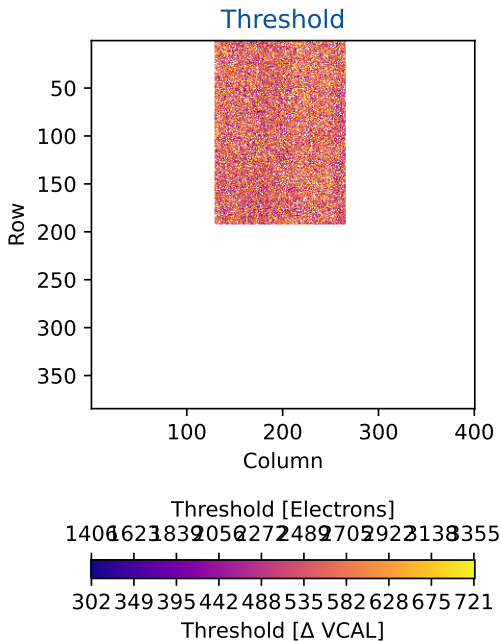


## Threshold distribution for enabled pixels

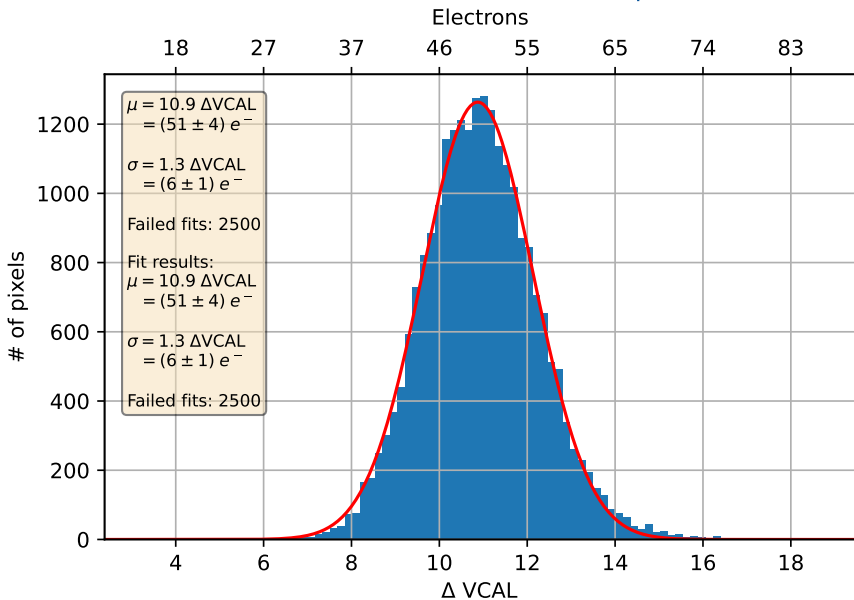


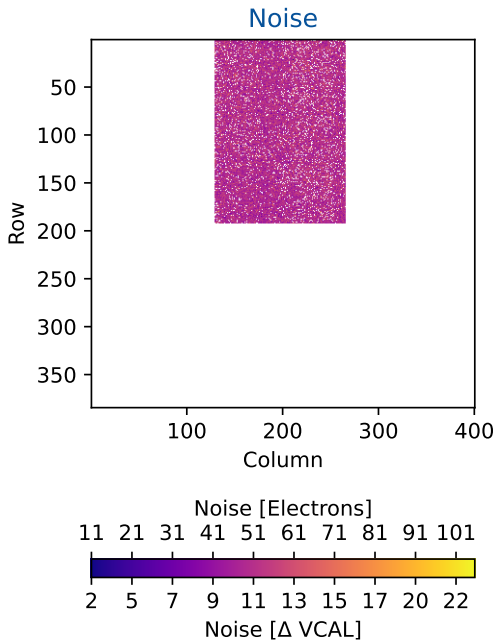
## Threshold distribution for enabled pixels





## Noise distribution for enabled pixels





# Noise Occupancy Scan

- Sends triggers without injection into enabled pixels to identify noisy pixels



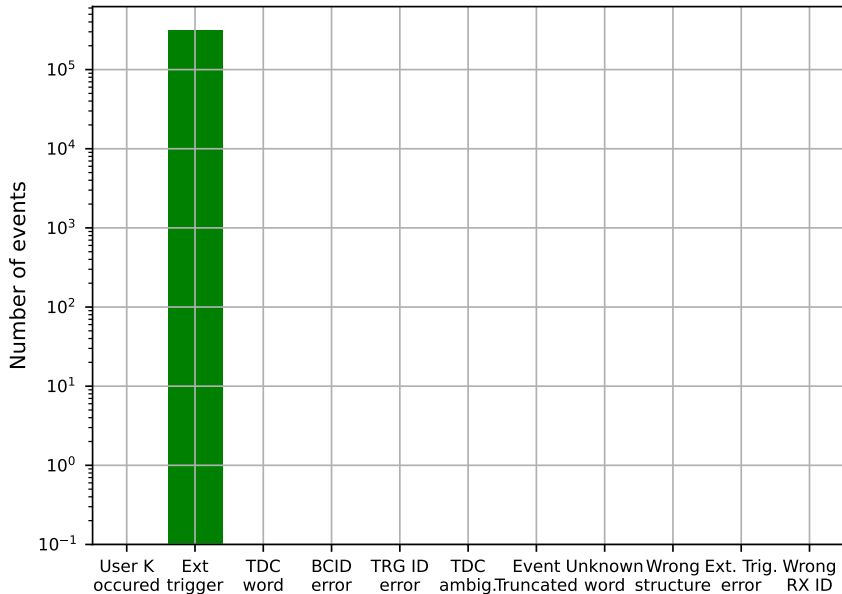
This is a bdaq53 noise\_occupancy\_scan for chip 0x162BC.

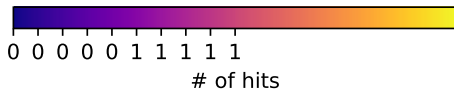
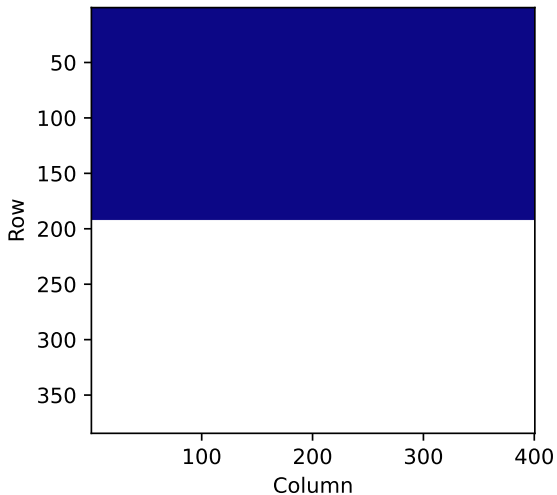
Run 20230317\_021905\_noise\_occupancy\_scan was started 2023-03-17 02:19:0

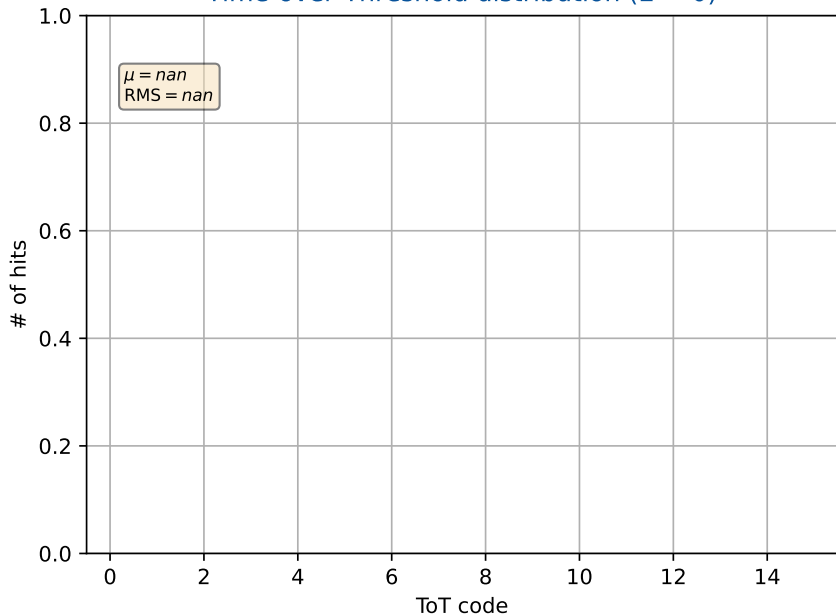
Scan config		Value	
min_occupancy	10	DAC_PREAMP_I_DIFF	895
n_triggers	10000000.0	DAC_PREAMP_R_DIFF	895
start_column	0	DAC_PREAMP_TL_DIFF	895
start_row	0	DAC_PREAMP_TR_DIFF	895
stop_column	400	DAC_PREAMP_T_DIFF	895
stop_row	192	DAC_PREAMP_M_DIFF	895
trigger_pattern	0xffffffff	DAC_PRECOMP_DIFF	300
wait_cycles	400	DAC_COMP_DIFF	523
		DAC_VFF_DIFF	160
		DAC_TH1_L_DIFF	220
		DAC_TH1_R_DIFF	220
		DAC_TH1_M_DIFF	220
		DAC_TH2_DIFF	0
		DAC_LCC_DIFF	200
		LEACKAGE_FEEDBACK	0



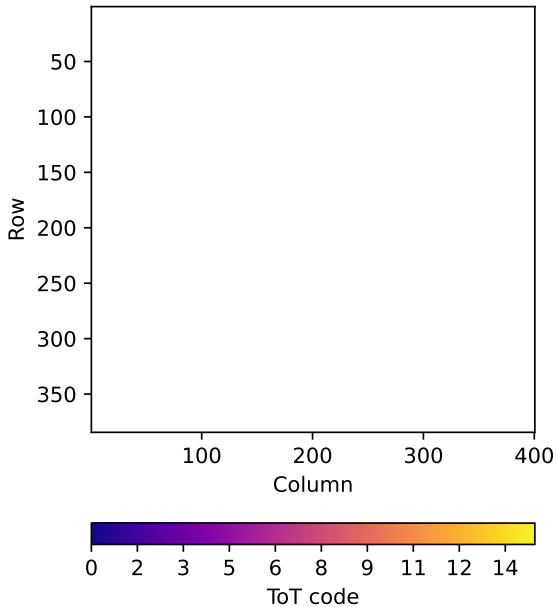
Event status ( $\Sigma = 312500$ )

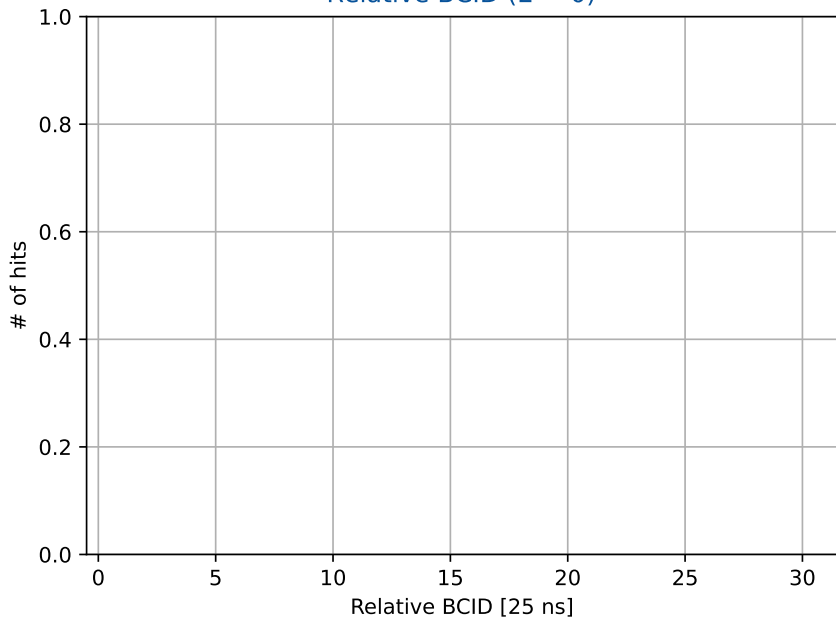


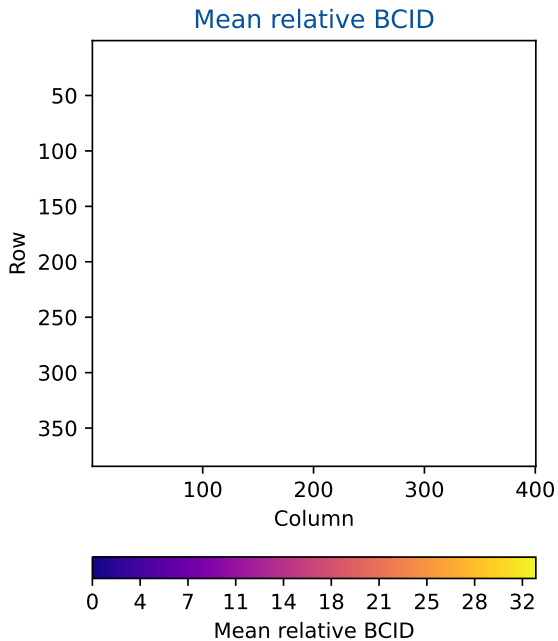
Occupancy ( $\Sigma = 0$ )

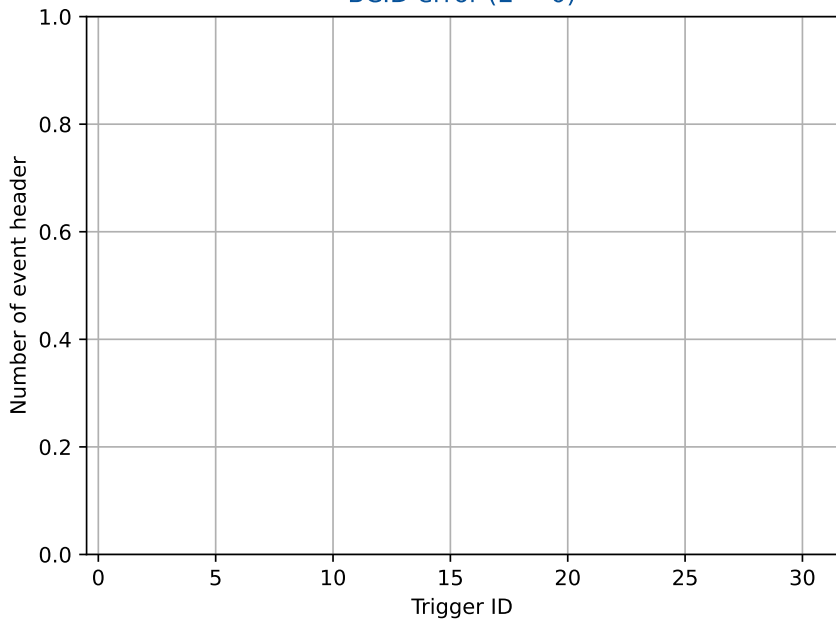
Time-over-Threshold distribution ( $\Sigma = 0$ )

## Mean ToT

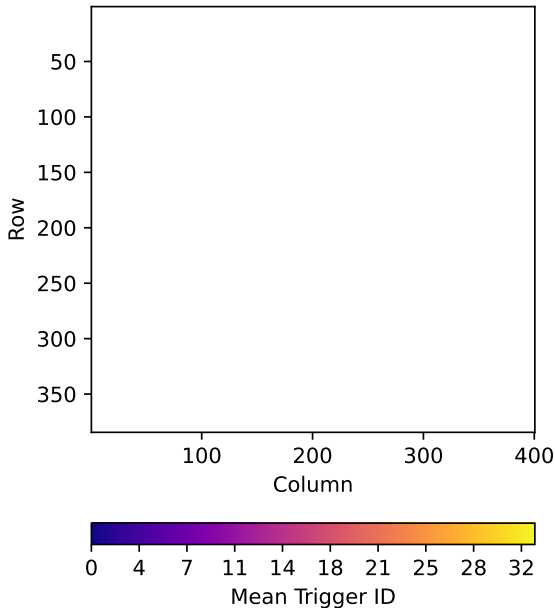


Relative BCID ( $\Sigma = 0$ )



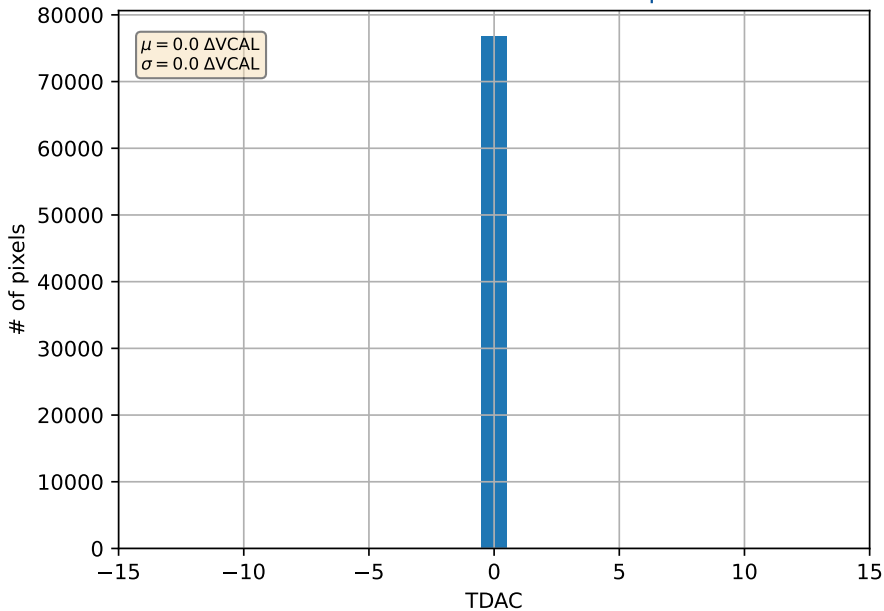
BCID error ( $\Sigma = 0$ )

Trigger ID Histogram without Error correction



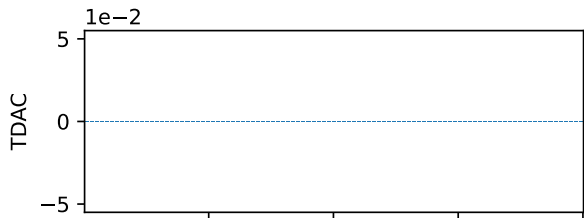


## TDAC distribution for enabled pixels

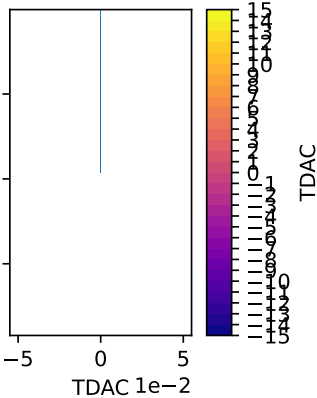
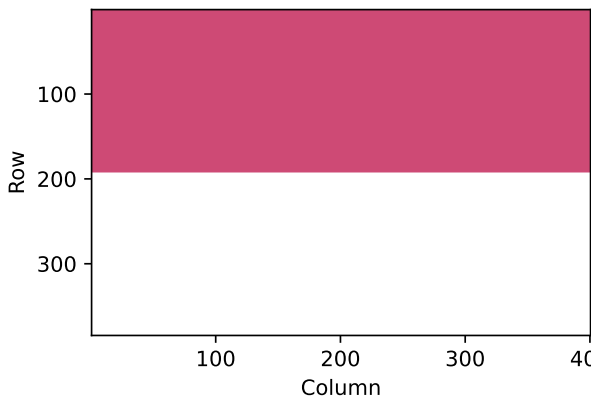


ITKPixV1 preliminary

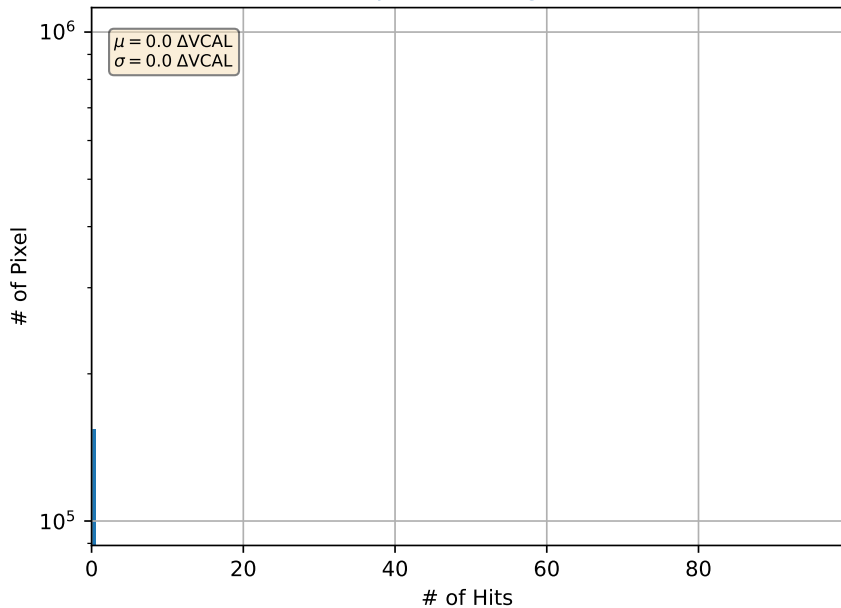
Chip S/N: 0x162BC



TDAC map  
with projections  
( $\Sigma = 0$ )



## Hits per Pixel (logscale)



# Source Scan (Random Trigger)

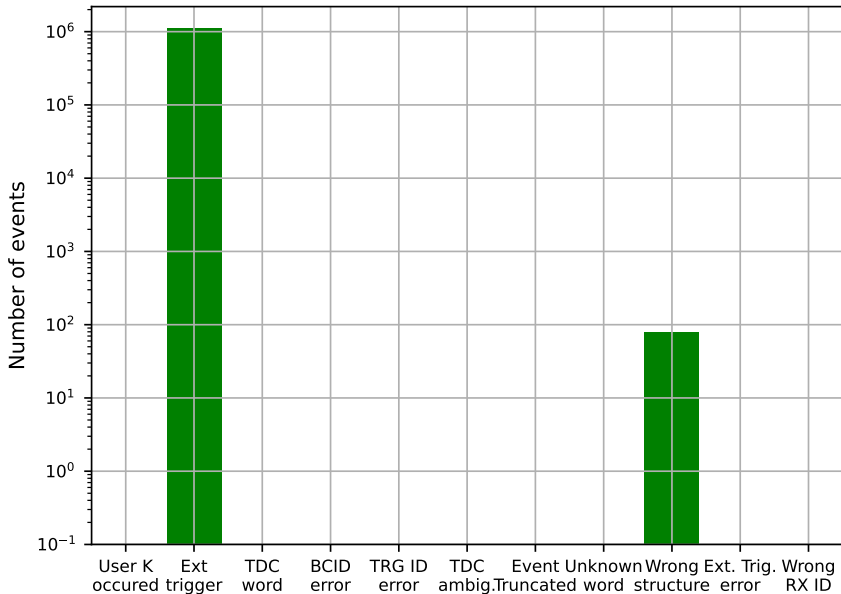
- A BDAQ self-trigger (external trigger) scan, using the HitOr as the trigger input

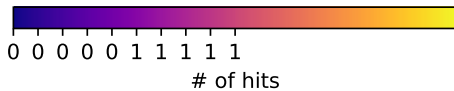
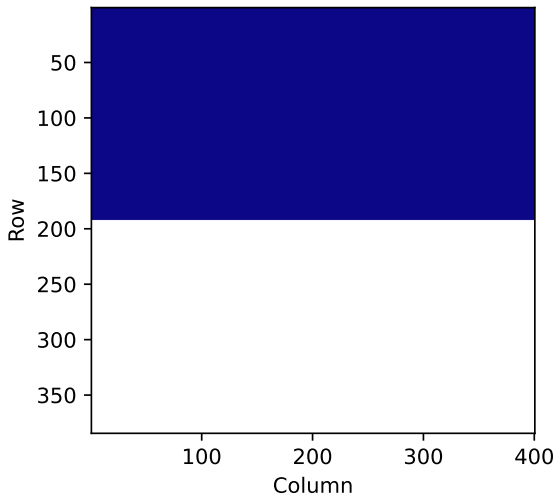


This is a bdaq53 source\_scan\_random\_trigger for chip 0x162BC.  
Run 20230317\_024142\_source\_scan\_random\_trigger was started 2023-03-17 01:

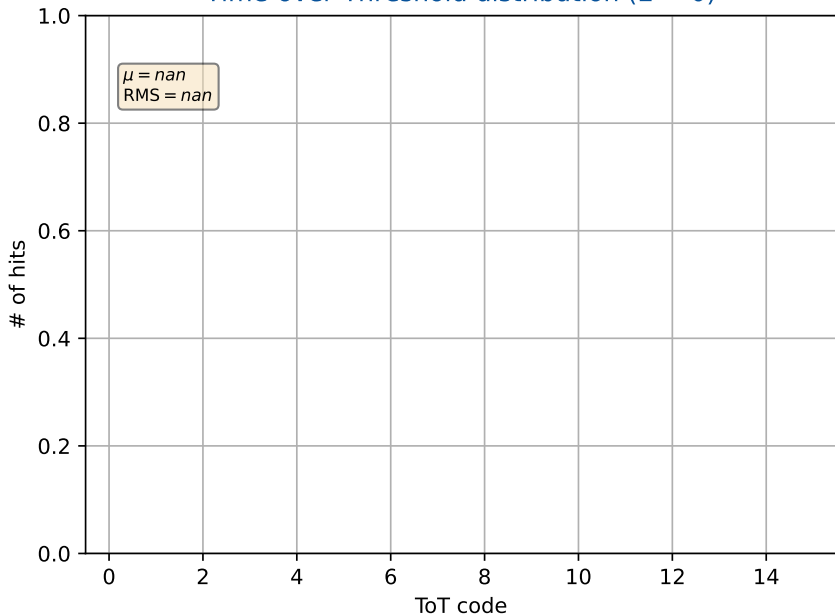
Scan config	Value	ITkPixV1 config	Value
bench	{'TLU': {'TRIGI	DAC_PREAMP_I_DIFF	895
n_triggers		DAC_PREAMP_R_DIFF	895
scan_timeout	30	DAC_PREAMP_TL_DIFF	895
start_column	0	DAC_PREAMP_TR_DIFF	895
start_row	0	DAC_PREAMP_T_DIFF	895
stop_column	400	DAC_PREAMP_M_DIFF	895
stop_row	192	DAC_PRECOMP_DIFF	300
trigger_delay	65	DAC_COMP_DIFF	523
trigger_latency	100	DAC_VFF_DIFF	160
trigger_length	32	DAC_TH1_L_DIFF	220
trigger_pattern	0xffffffff	DAC_TH1_R_DIFF	220
use_tdc	False	DAC_TH1_M_DIFF	220
veto_length	500	DAC_TH2_DIFF	0
wait_cycles	40	DAC_LCC_DIFF	200
		LEAKAGE_FEEDBACK	0

Event status ( $\Sigma = 1098833$ )



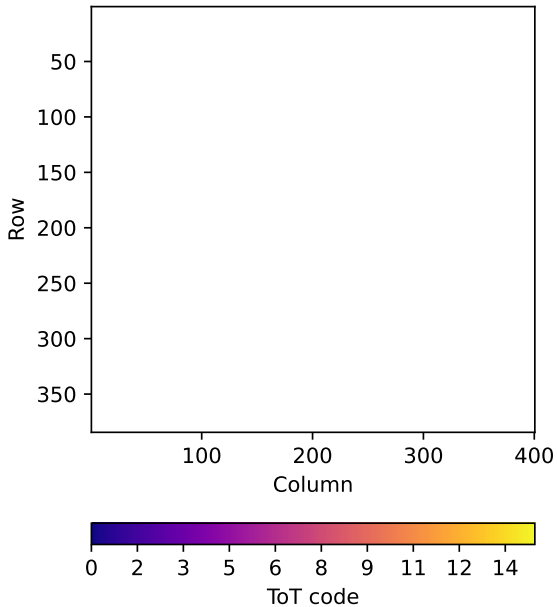
Occupancy ( $\Sigma = 0$ )

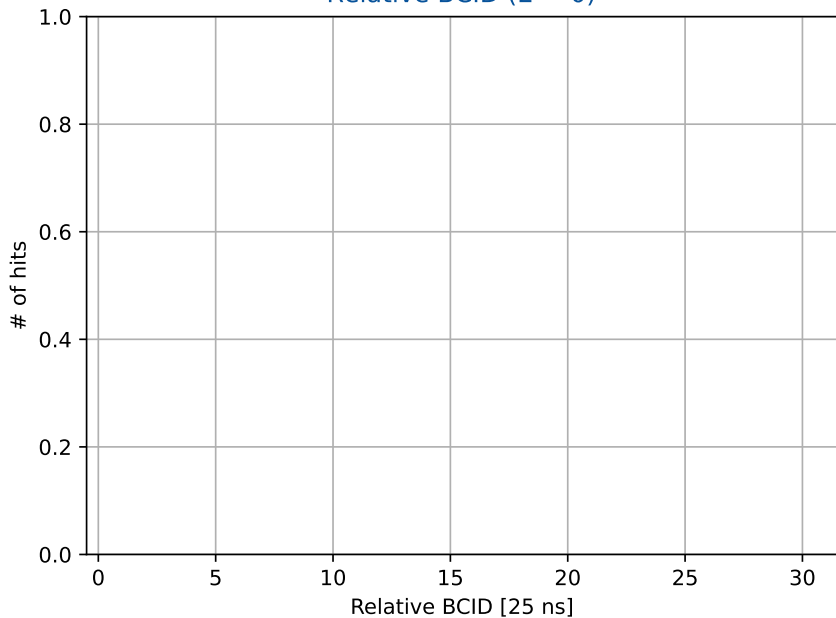
Time-over-Threshold distribution ( $\Sigma = 0$ )

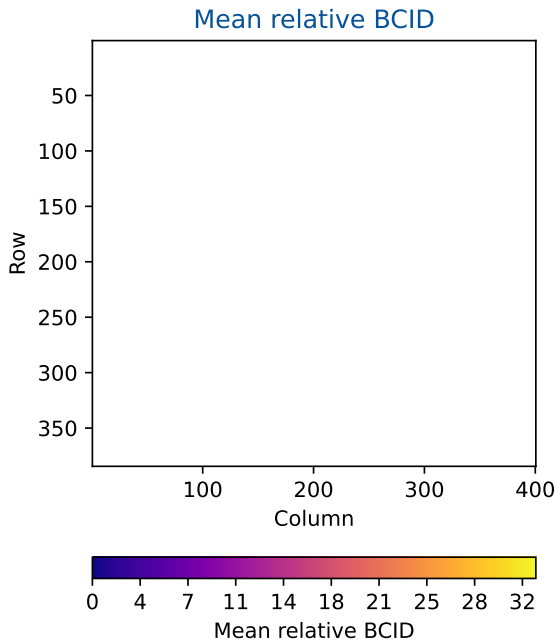


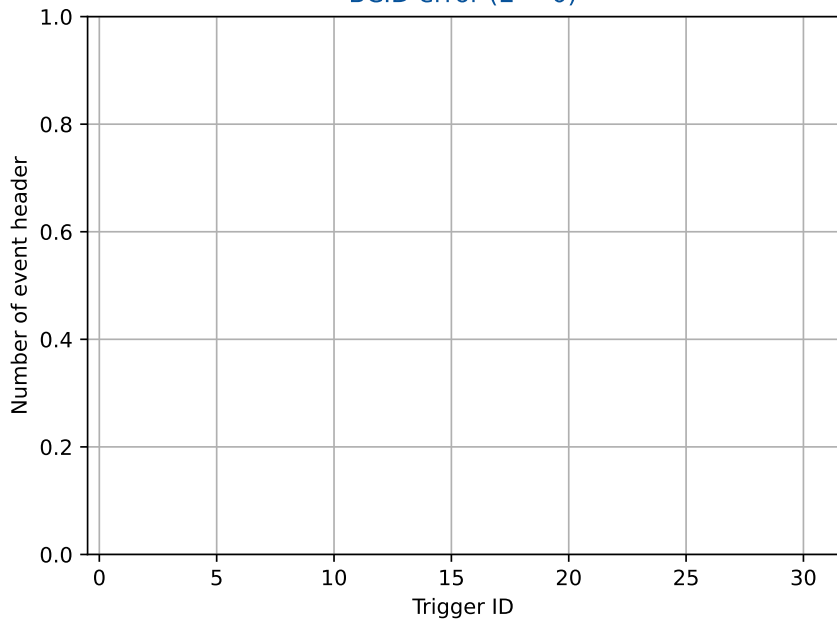


## Mean ToT

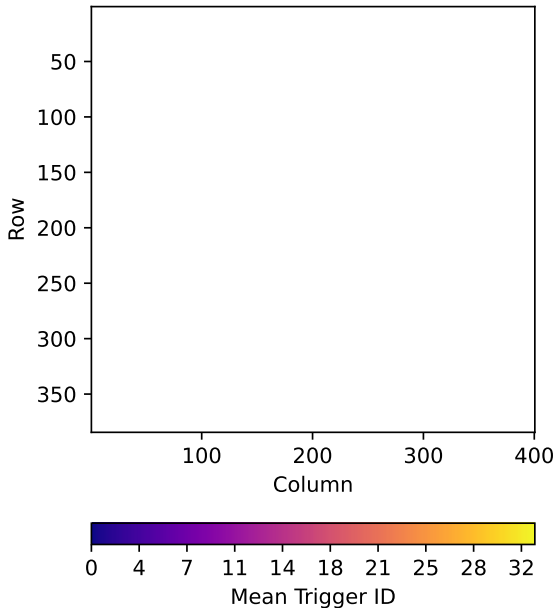


Relative BCID ( $\Sigma = 0$ )

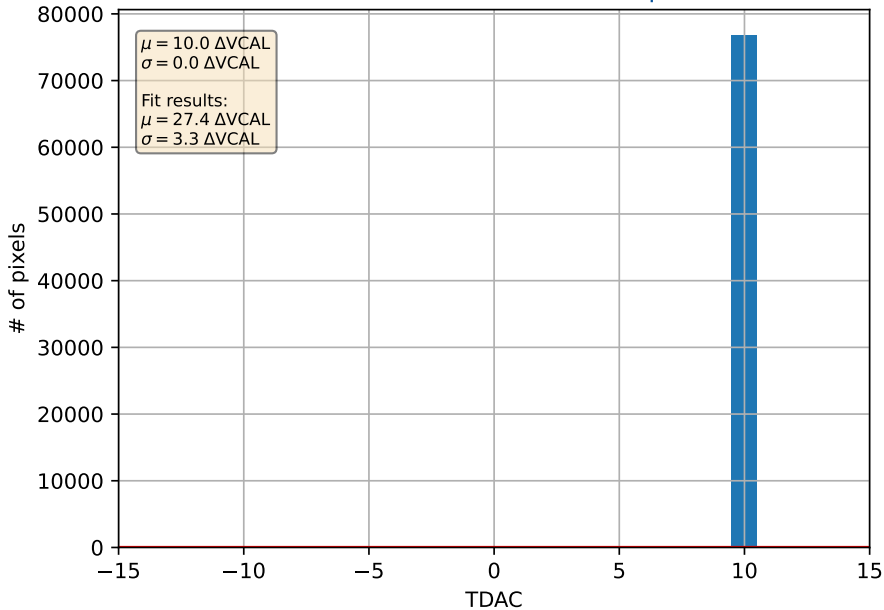


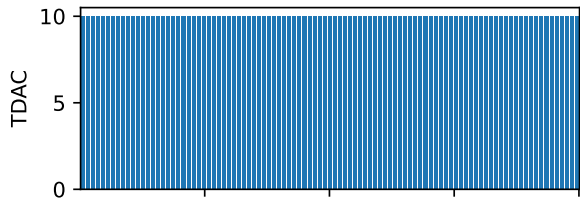
BCID error ( $\Sigma = 0$ )

Trigger ID Histogram without Error correction

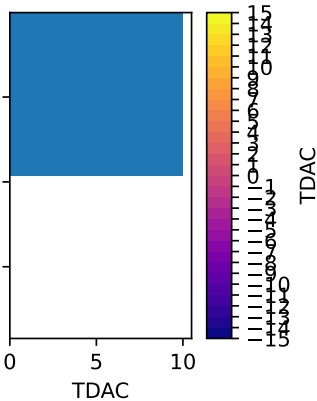
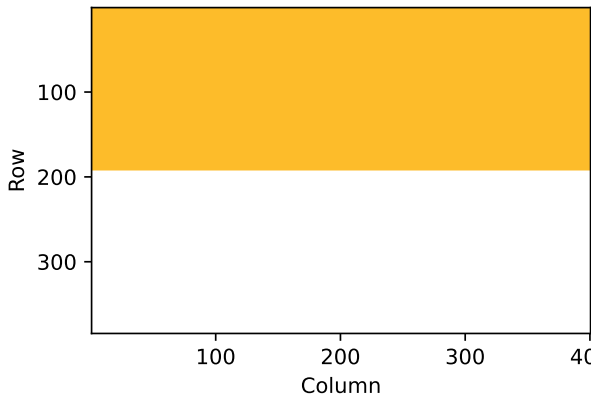


## TDAC distribution for enabled pixels

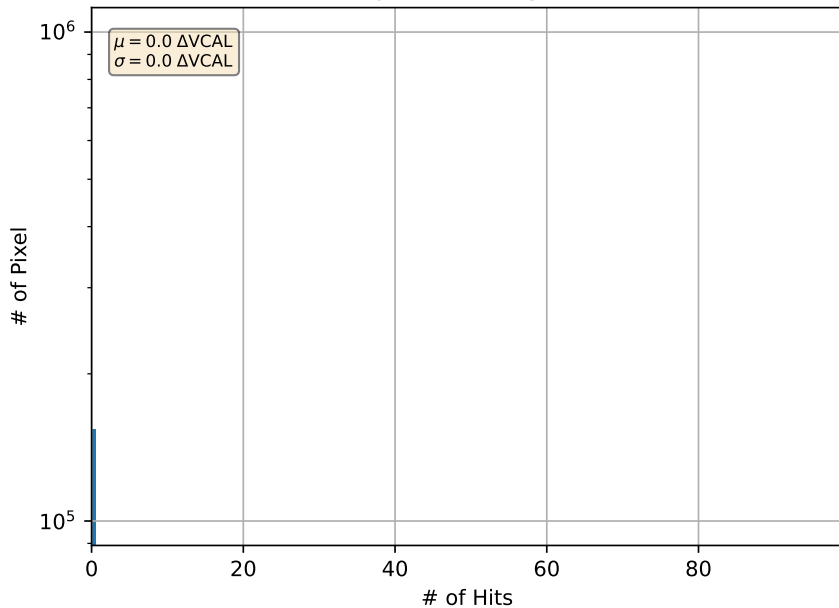




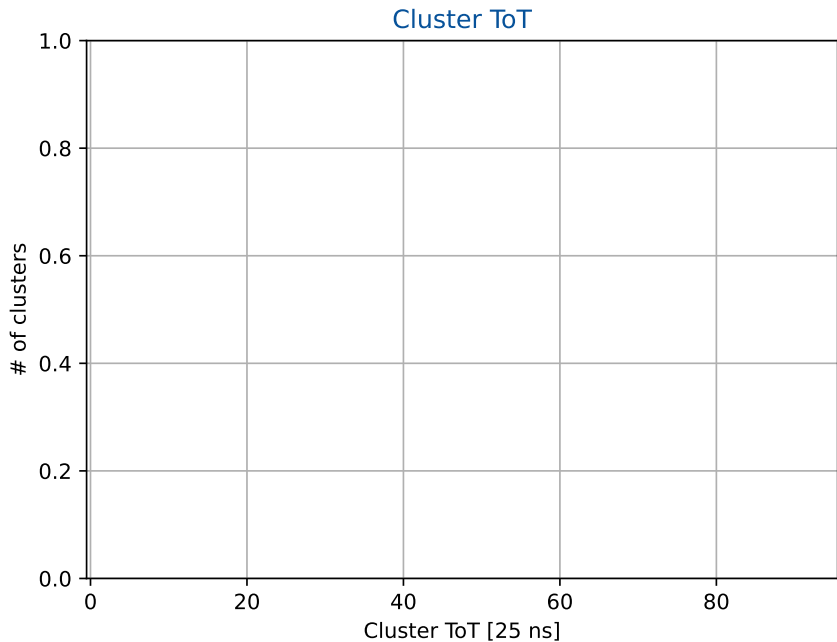
TDAC map  
with projections  
( $\Sigma = 768000$ )



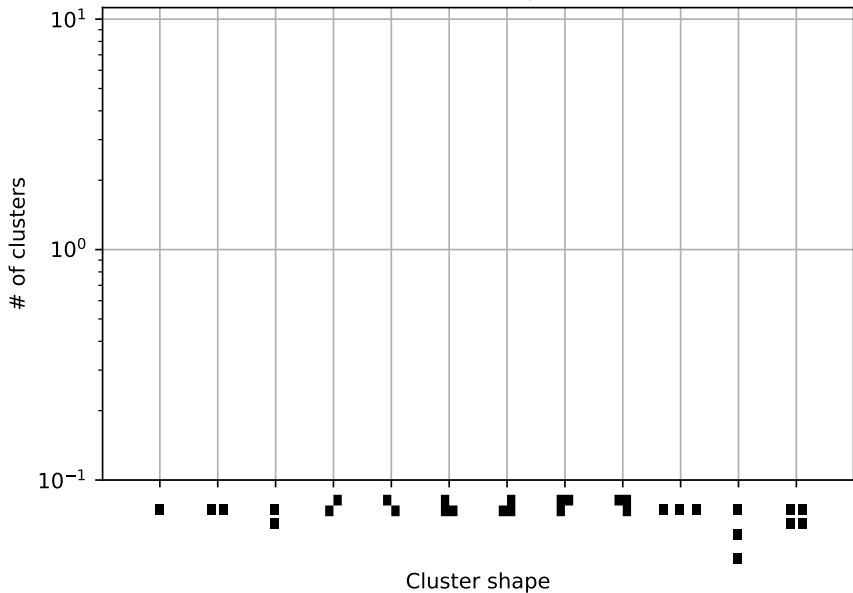
## Hits per Pixel (logscale)



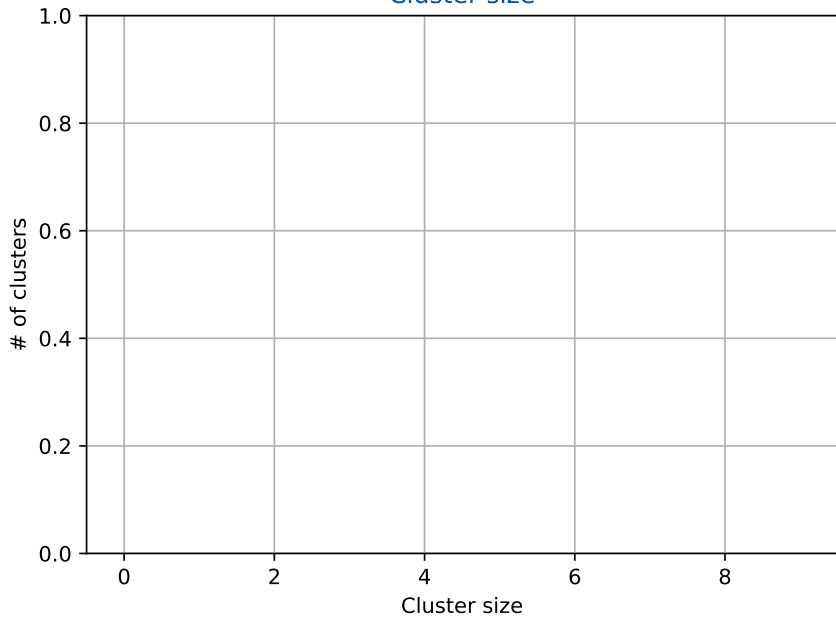




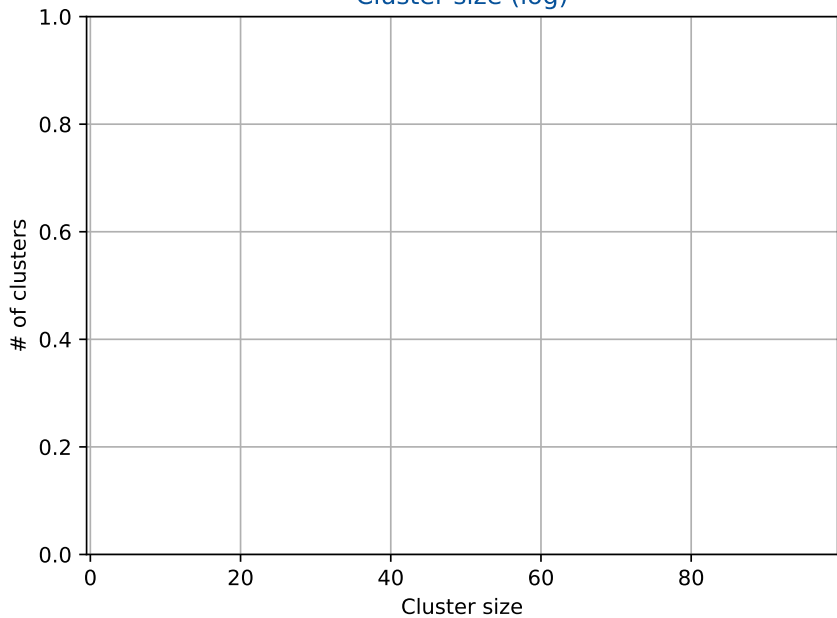
## Cluster shapes



Cluster size



Cluster size (log)



# Crosstalk Scan

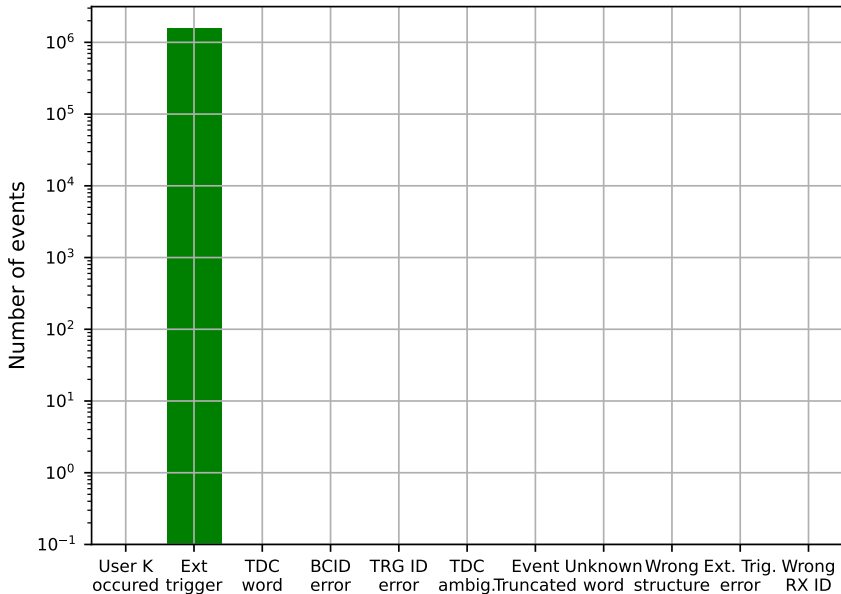
- This reads out one pixel while injecting neighbouring pixels using different injection mask patterns to check for crosstalk
- The principle is the same as in a threshold scan

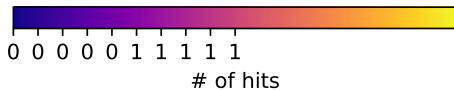
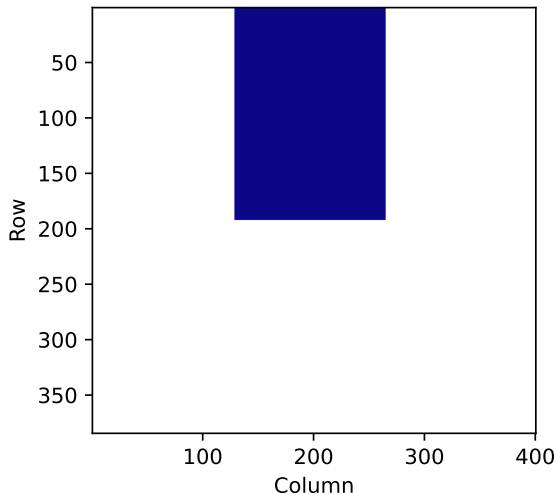
This is a bdaq53 crosstalk\_scan for chip 0x162BC.  
 Run 20230317\_014028\_crosstalk\_scan was started 2023-03-17 01:40:28.

Scan config	Value	ITkPixV1 config	Value
VCAL_HIGH_start	0	DAC_PREAMP_L_DIFF	895
VCAL_HIGH_step	102	DAC_PREAMP_R_DIFF	895
VCAL_HIGH_stop	4096	DAC_PREAMP_TL_DIFF	895
VCAL_MED	0	DAC_PREAMP_TR_DIFF	895
injection_type	cross_injector	DAC_PREAMP_T_DIFF	895
n_injections	100	DAC_PREAMP_M_DIFF	895
start_column	128	DAC_PRECOMP_DIFF	300
start_row	0	DAC_COMP_DIFF	523
stop_column	264	DAC_VFF_DIFF	160
stop_row	192	DAC_TH1_L_DIFF	220
trigger_pattern	0xfffffff	DAC_TH1_R_DIFF	220
		DAC_TH1_M_DIFF	220
		DAC_TH2_DIFF	0
		DAC_LCC_DIFF	200
		LEAKAGE_FEEDBACK	0

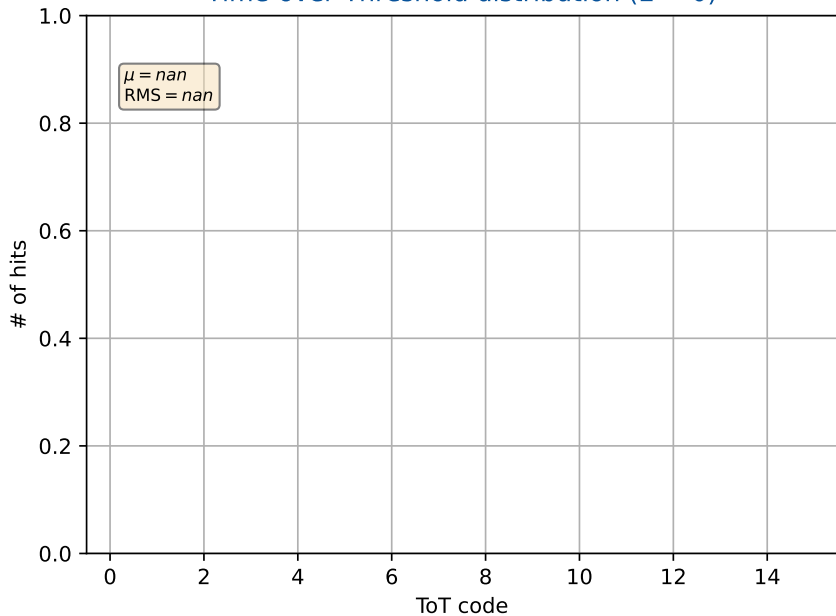
$$\text{Charge calibration: } y [e^-] = x [\Delta\text{VCAL}] \cdot (4.65 \pm 0.40) \left[ \frac{e^-}{\Delta\text{VCAL}} \right] + (0 \pm 60.00) [e^-]$$

Event status ( $\Sigma = 1574400$ )

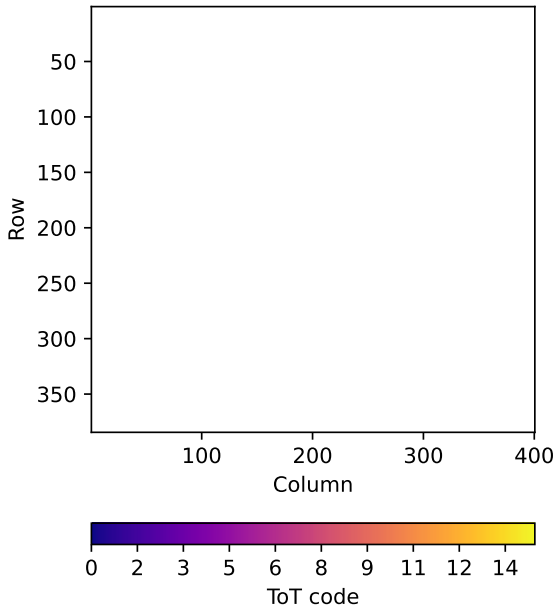


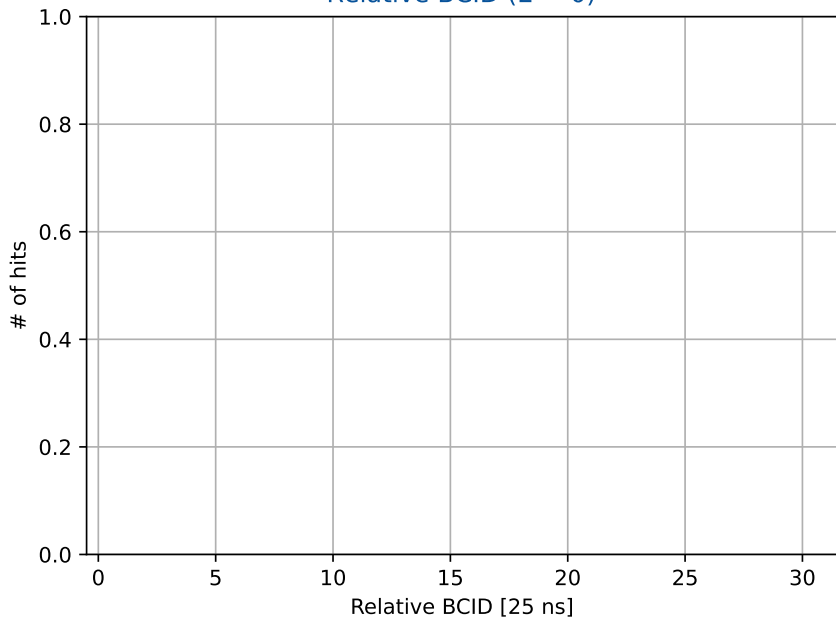
Integrated occupancy ( $\Sigma = 0$ )

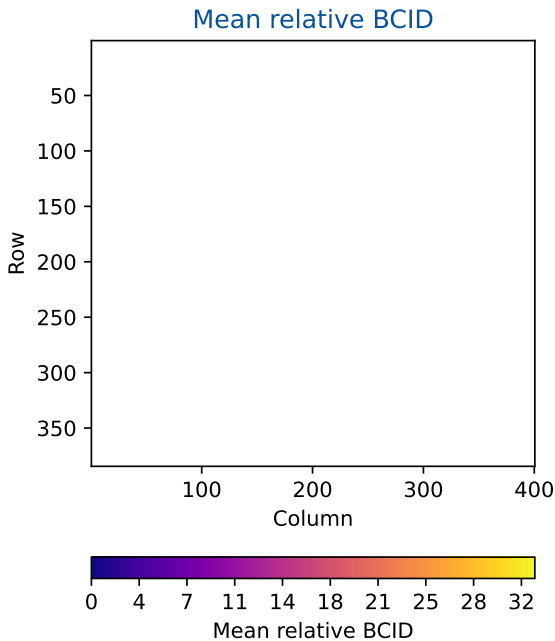


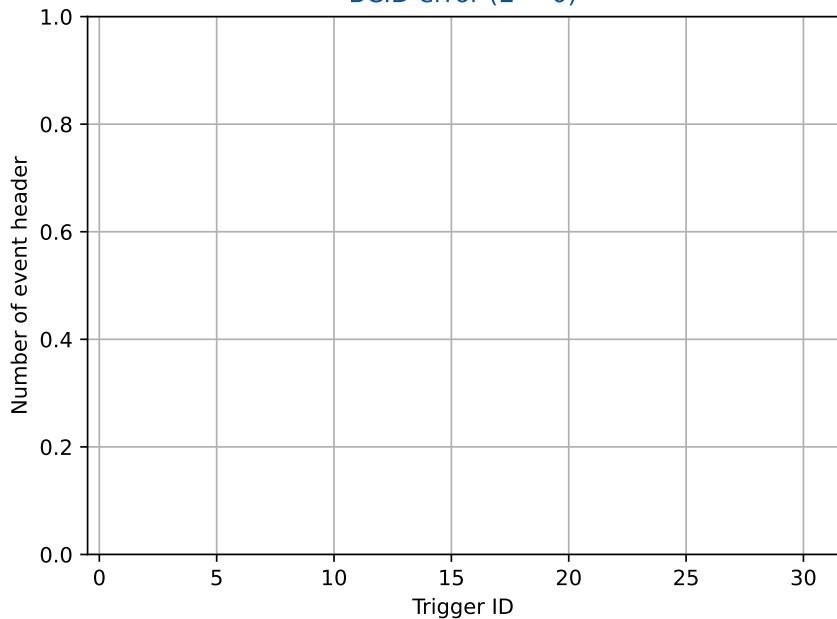
Time-over-Threshold distribution ( $\Sigma = 0$ )

## Mean ToT

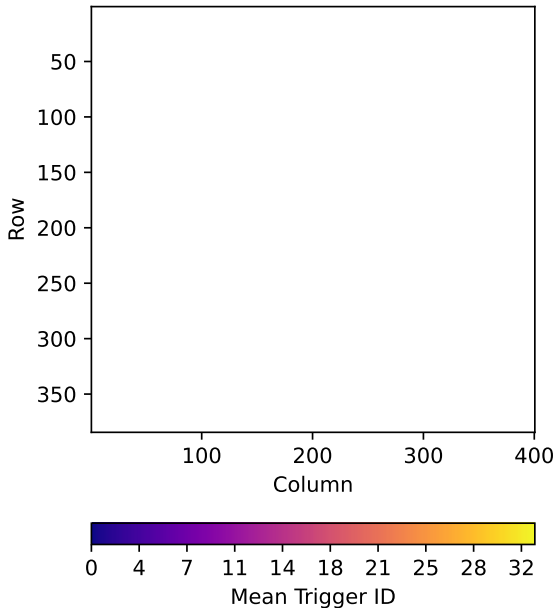


Relative BCID ( $\Sigma = 0$ )

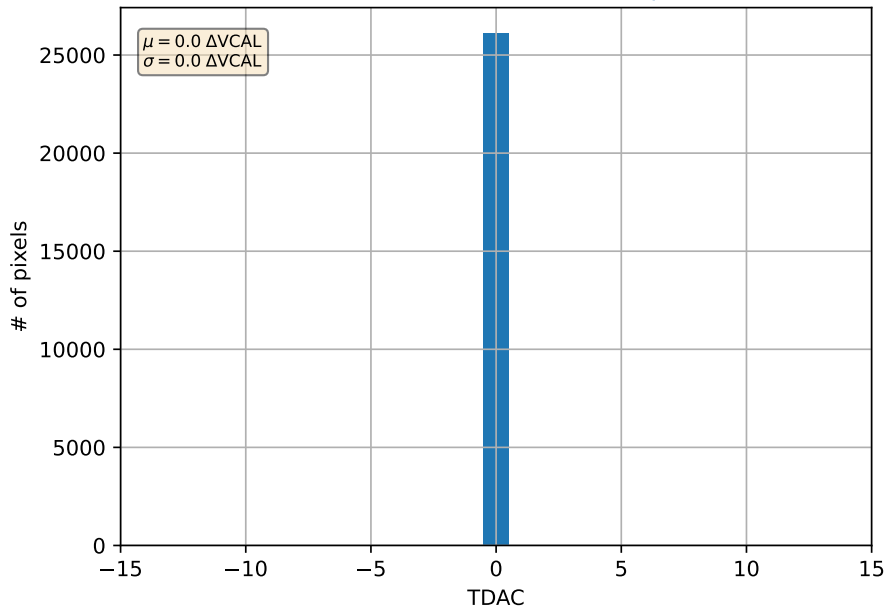


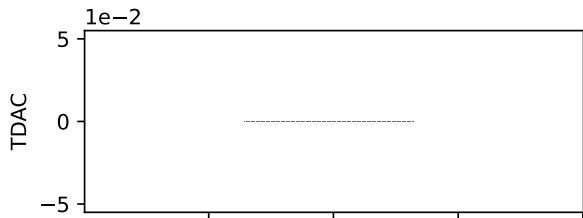
BCID error ( $\Sigma = 0$ )

Trigger ID Histogram without Error correction

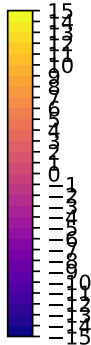
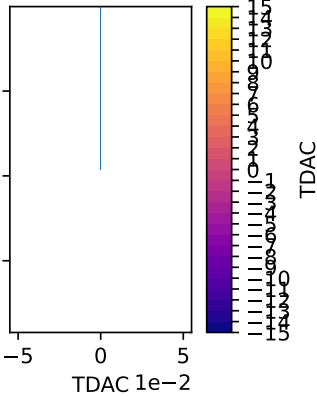
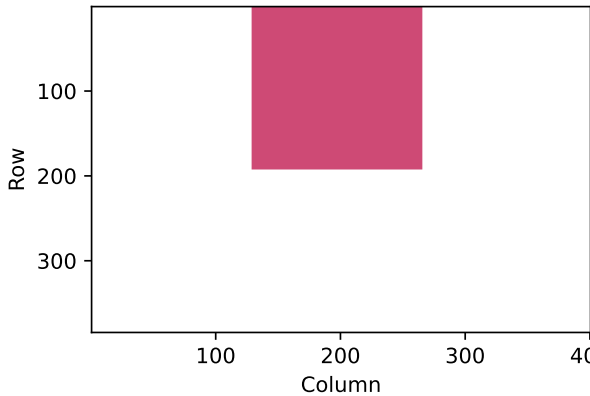


## TDAC distribution for enabled pixels



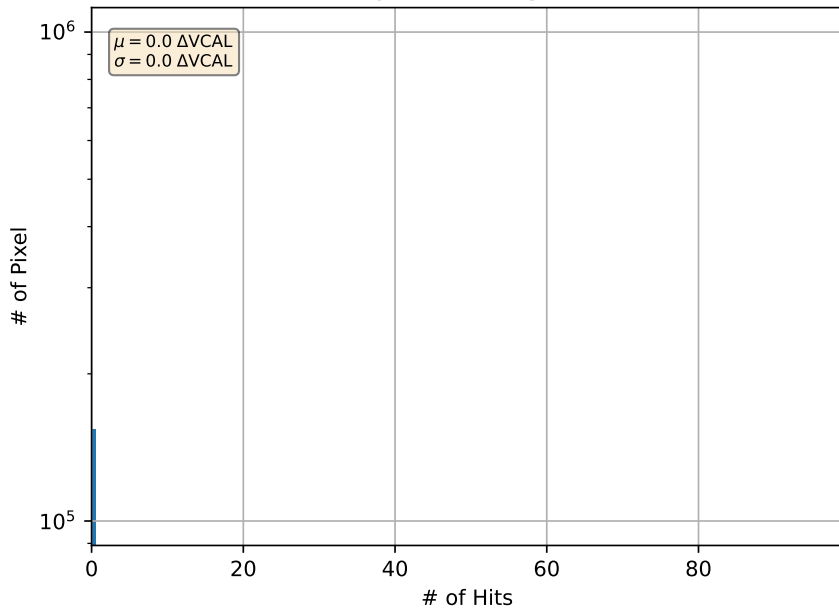


TDAC map  
with projections  
( $\Sigma = 0$ )





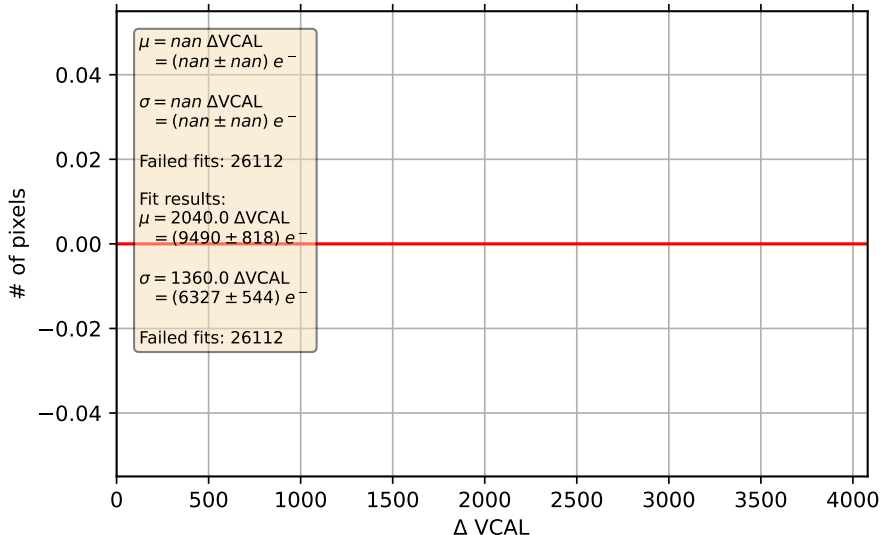
## Hits per Pixel (logscale)



## Threshold distribution for enabled pixels

Electrons

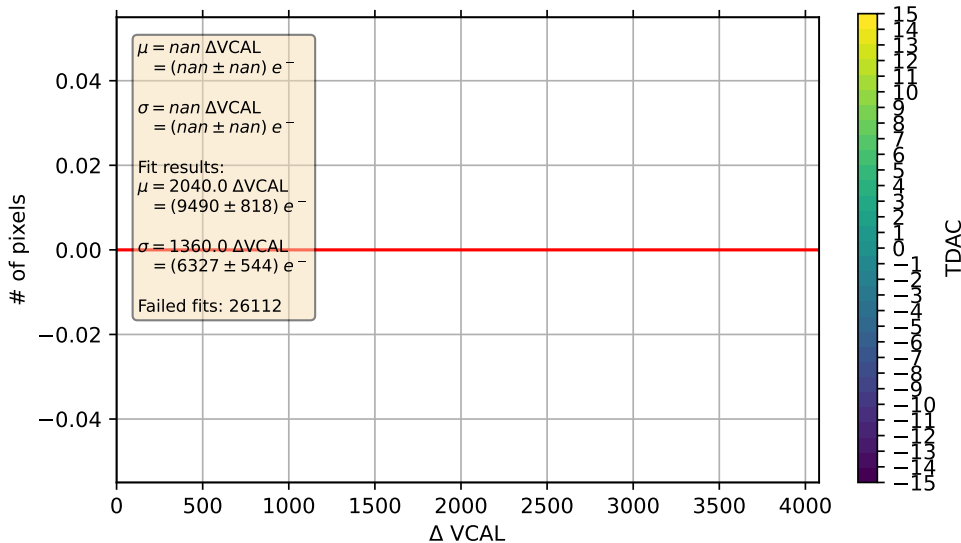
0 2326 4652 6978 9304 11630 13956 16282 18608

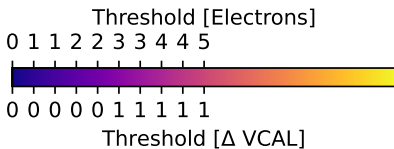
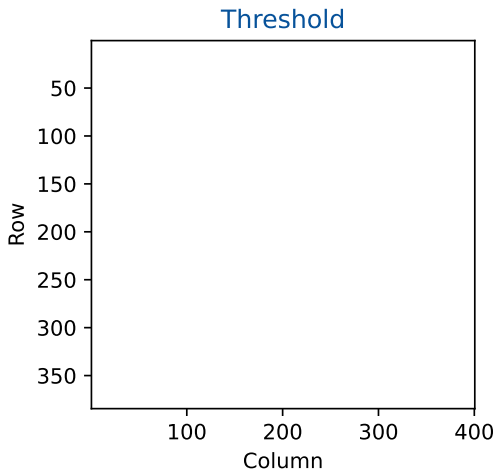


## Threshold distribution for enabled pixels

Electrons

0 2326 4652 6978 9304 11630 13956 16282 18608





# Hitor Calibration

- Calibrates the Hitor for every pixel using the charge injection circuit
- Different charges are injected and the response of the Hitor is measured using the TDC module
- Relationship between Delta VCAL and TDC values is obtained, which is needed for a precise charge measurement

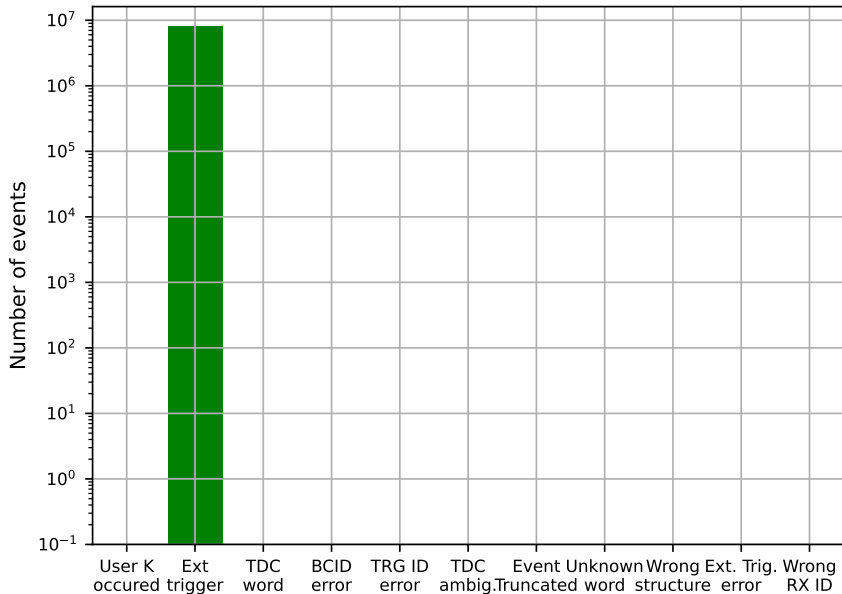


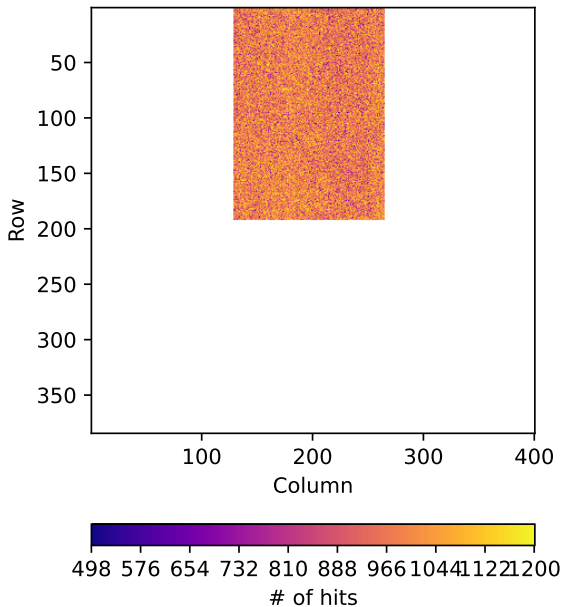
This is a bdaq53 hitor\_calibration for chip 0x162BC.  
Run 20230317\_040923\_hitor\_calibration was started 2023-03-17 04:09:23.

Scan config	Value
VCAL_HIGH_values	range(900, 20)
VCAL_MED	500
n_injections	100
start_column	128
start_row	0
stop_column	264
stop_row	192
trigger_pattern	0xffffffff

ITkPixV1 config	Value
DAC_PREAMP_I_DIFF	895
DAC_PREAMP_R_DIFF	895
DAC_PREAMP_TL_DIFF	895
DAC_PREAMP_TR_DIFF	895
DAC_PREAMP_TL_DIFF	895
DAC_PREAMP_M_DIFF	895
DAC_PRECOMP_DIFF	300
DAC_COMP_DIFF	523
DAC_VFF_DIFF	160
DAC_TH1_L_DIFF	220
DAC_TH1_R_DIFF	220
DAC_TH1_M_DIFF	220
DAC_TH2_DIFF	0
DAC_LCC_DIFF	200
LEACKAGE_FEEDBACK	0

Event status ( $\Sigma = 8078400$ )



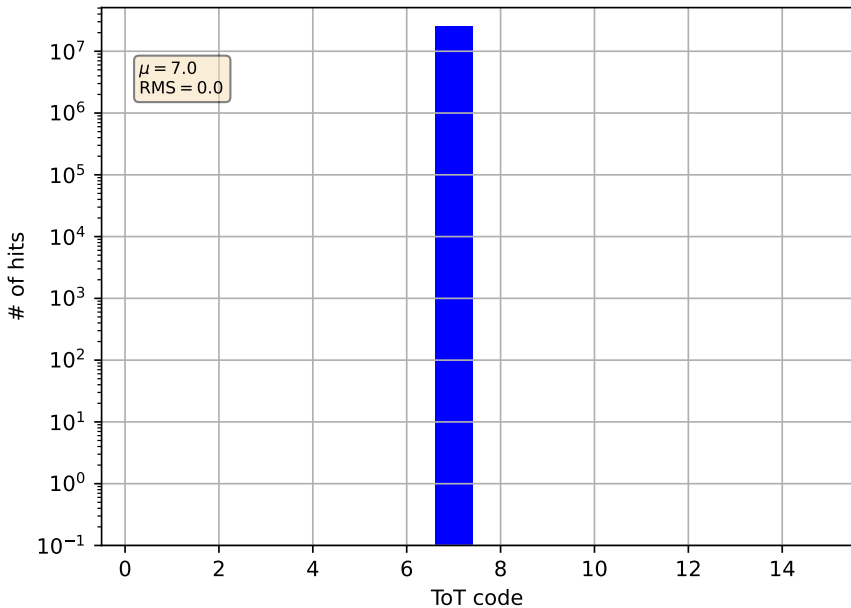
Occupancy ( $\Sigma = 25437700$ )



ITKPixV1 preliminary

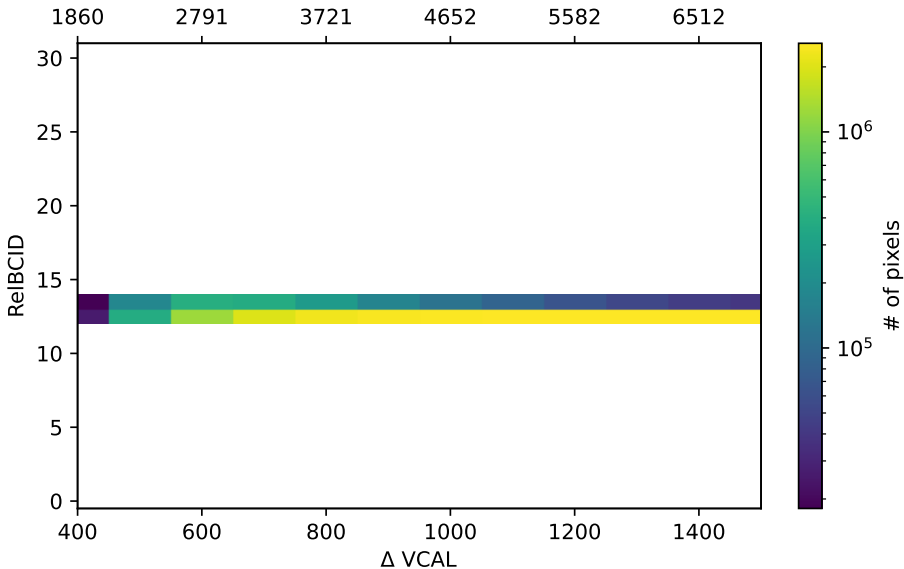
Chip S/N: 0x162BC

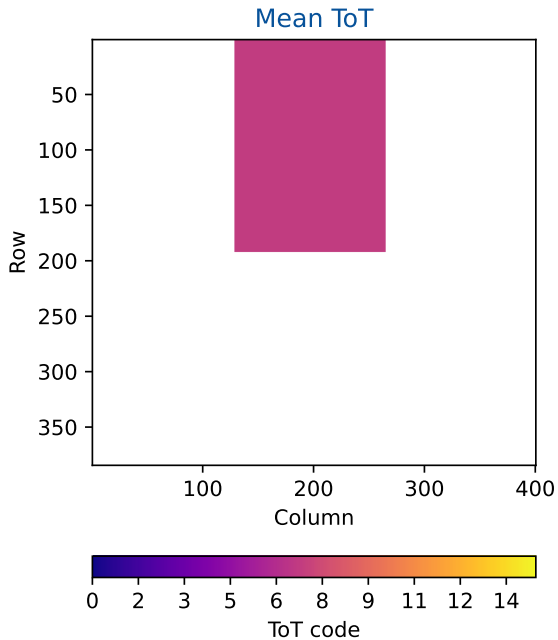
Time-over-Threshold distribution ( $\Sigma = 25437700$ )

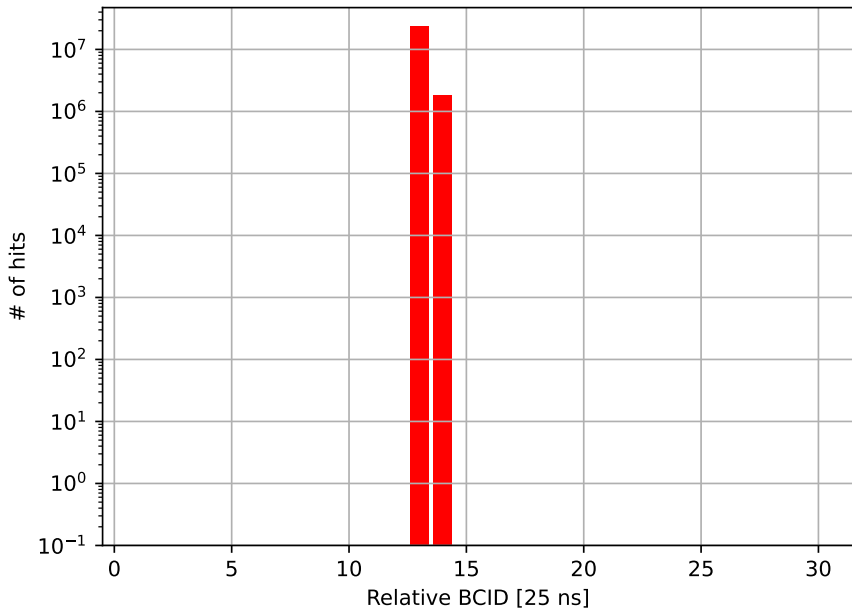


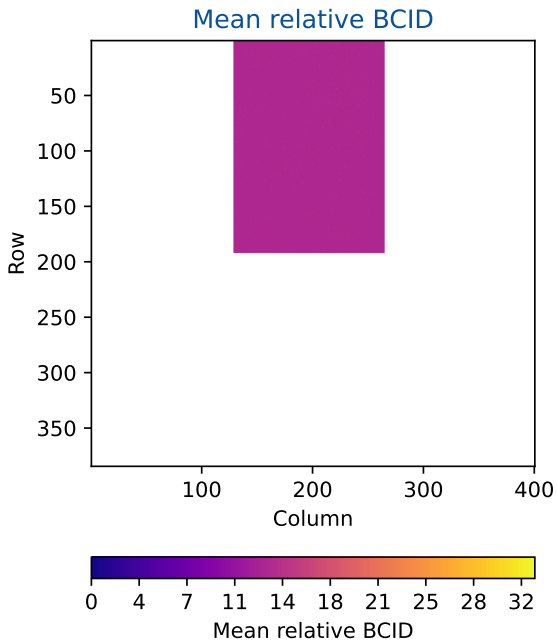
### RelBCID Scan Parameter Histogram for 26112 pixel(s)

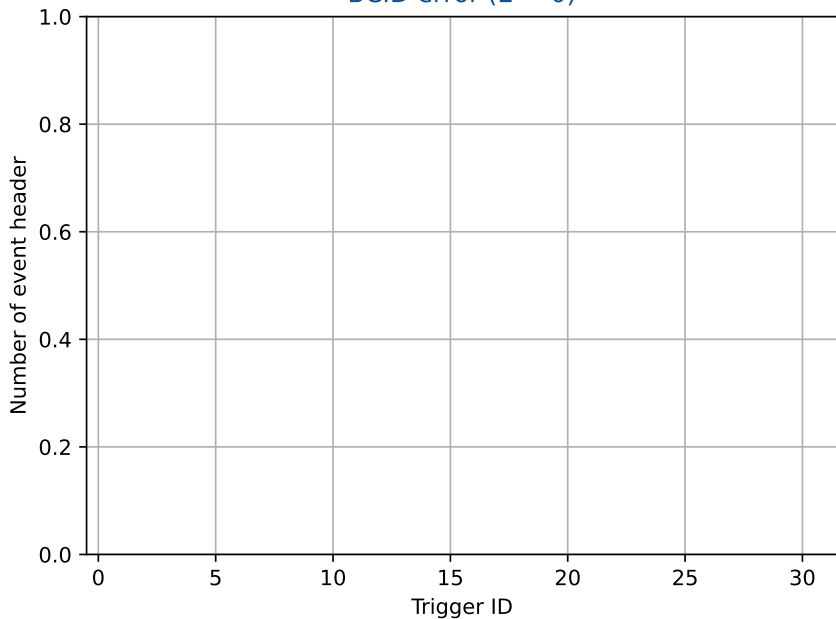
Electrons



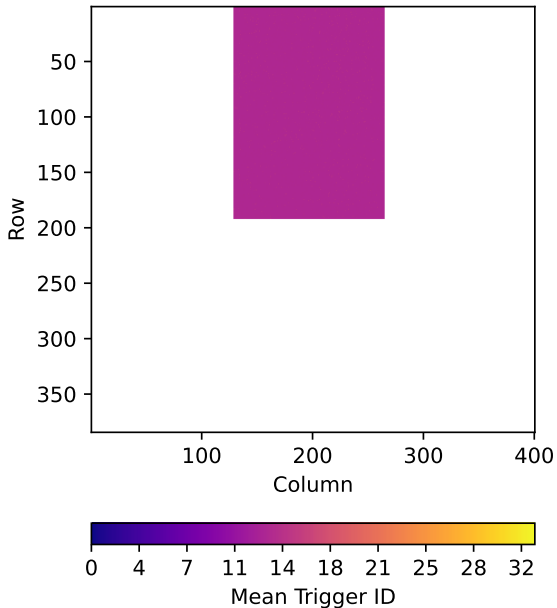


Relative BCID ( $\Sigma = 25437700$ )



BCID error ( $\Sigma = 0$ )

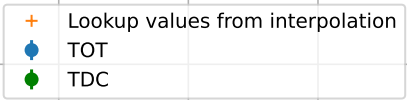
## Trigger ID Histogram without Error correction



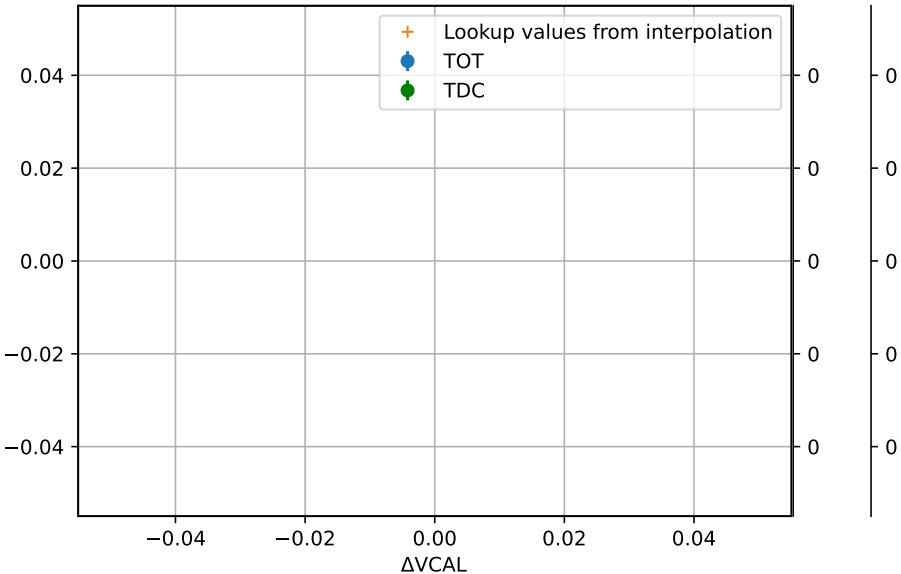
Mean ToT/TDC for pixel (222, 108)

TDC

TOT



TOT/TDC [ns]

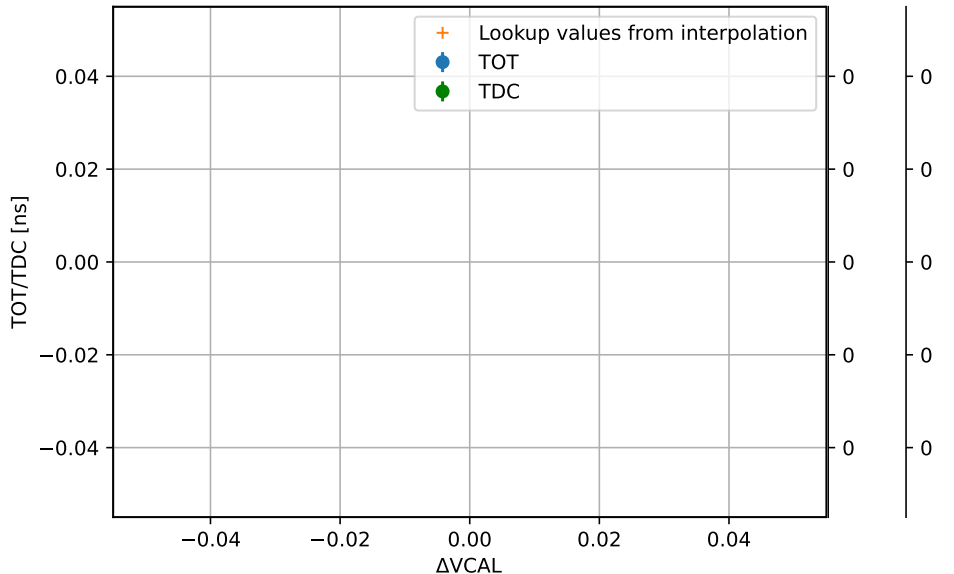




## Mean ToT/TDC for pixel (156, 175)

TDC

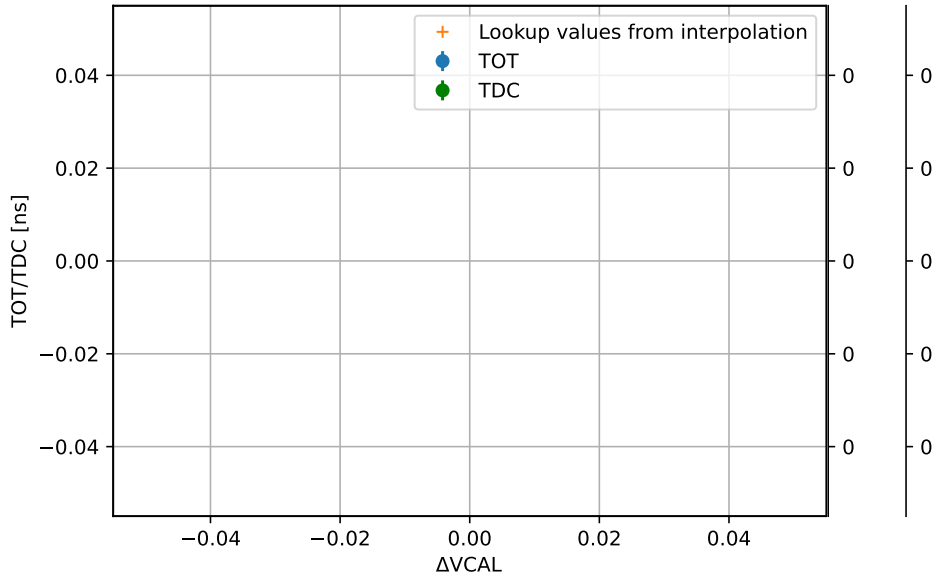
TOT

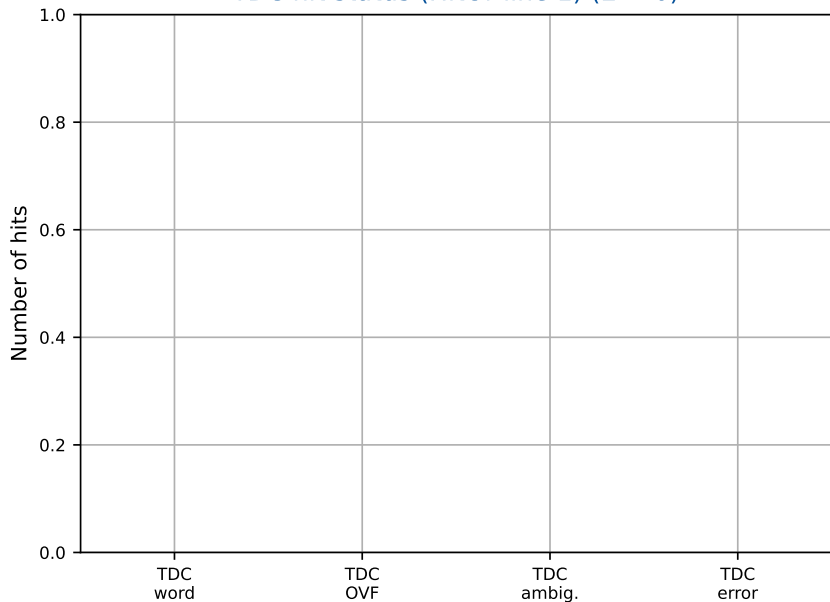


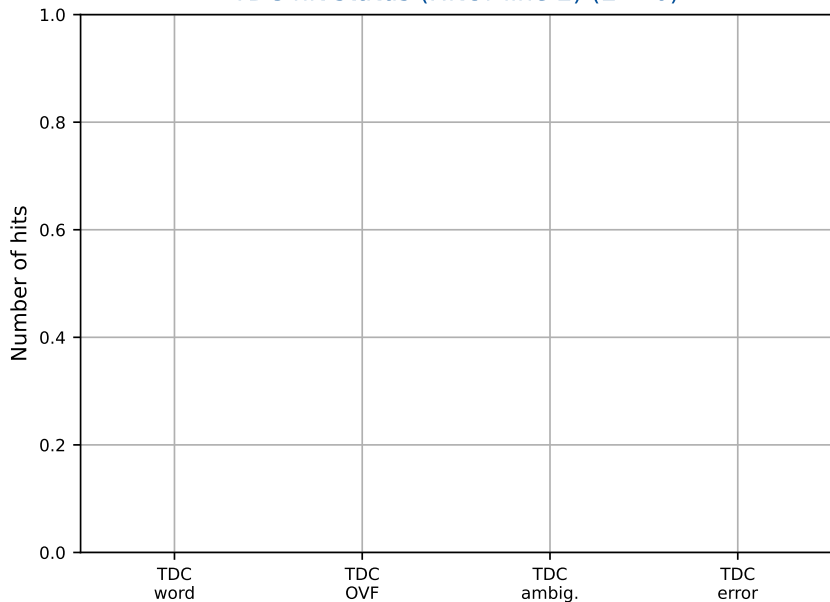
## Mean ToT/TDC for pixel (257, 82)

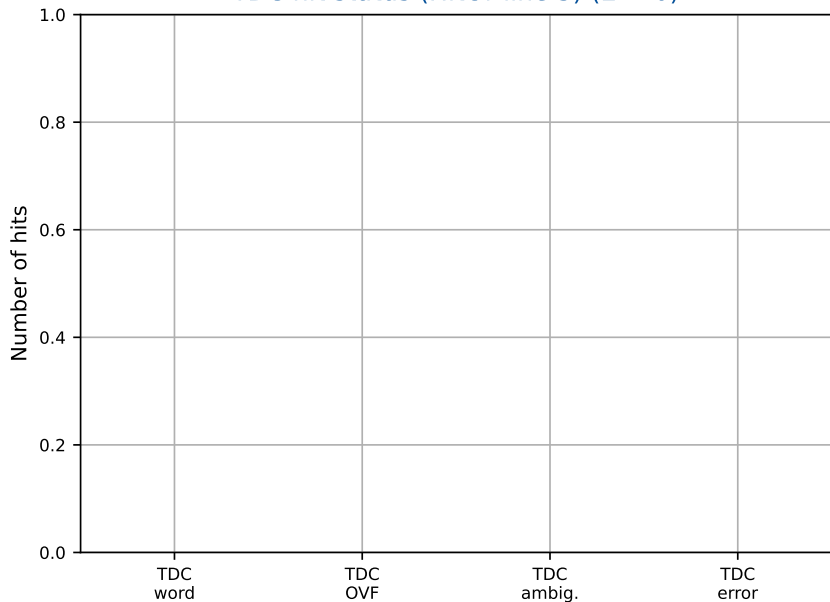
TDC

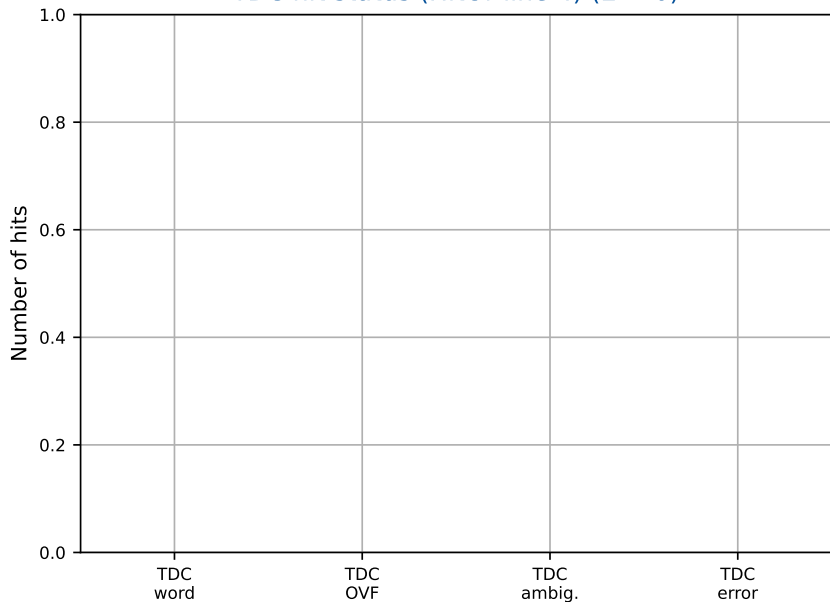
TOT



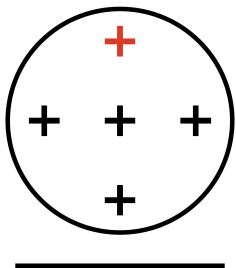
TDC hit status (HitOr line 1) ( $\Sigma = 0$ )

TDC hit status (HitOr line 2) ( $\Sigma = 0$ )

TDC hit status (HitOr line 3) ( $\Sigma = 0$ )

TDC hit status (HitOr line 4) ( $\Sigma = 0$ )

# Backup Slides

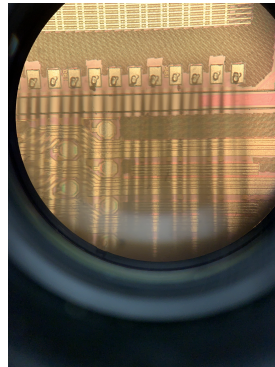
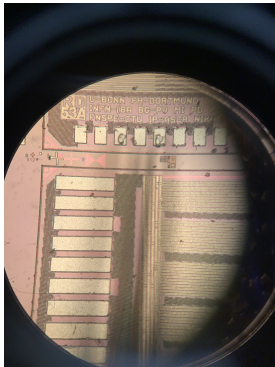


Point	Relative Height / $\mu\text{m}$	
	No Wafer	Wafer
Middle	290	250
Near	0	0
Far	220	160
Left	110	80
Right	320	320

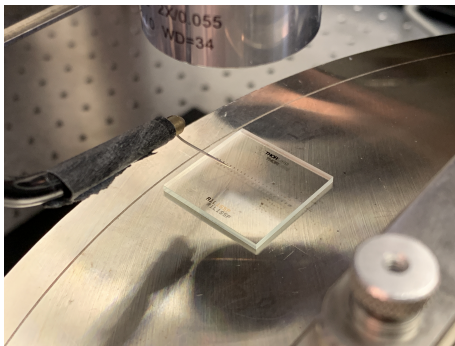
- Measured chuck height at 5 points with and without wafer to determine flatness of chuck and if wafer deforms to shape of chuck
- Dummy wafer conforms to shape of chuck with vacuum turned on
- Wafer levelled, but flatness only consistent within  $\sim 50 \mu\text{m}$ , and wafer no longer level after wafer replacement
  - **Rely on contact sensing**, with height map for safety



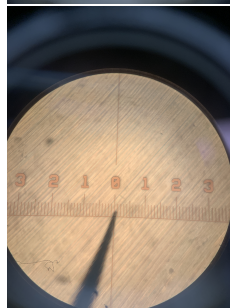
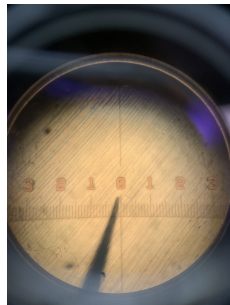
- Brought RD53a wafer into contact with its probe card
- Resulted in **acceptably even contact** marks to pads, despite lack of flatness

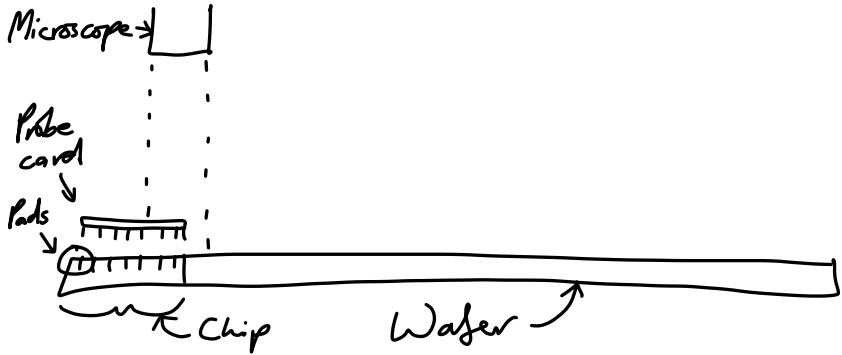


- Used dummy wafer and 2 stage micrometers (100  $\mu\text{m}$  precision) taped to chuck to test accuracy of horizontal stage movements
- Moved towards micrometers multiple times from different directions

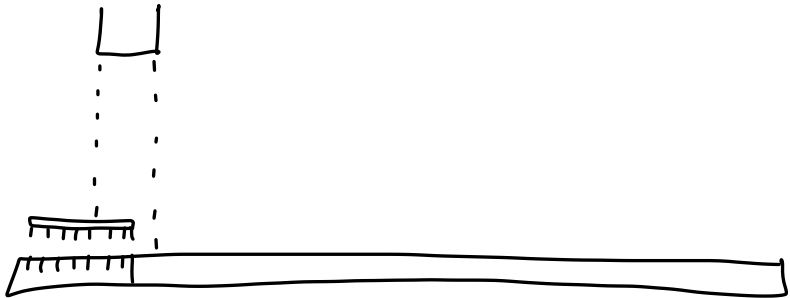


- Measurements using left stage micrometer seem roughly consistent with approach path
- Measurements using right stage micrometer differ with approach path by up to  $\approx 300 \mu\text{m}$  (see photos to right)
- **Resolved by moving from consistent direction of approach for both stages**

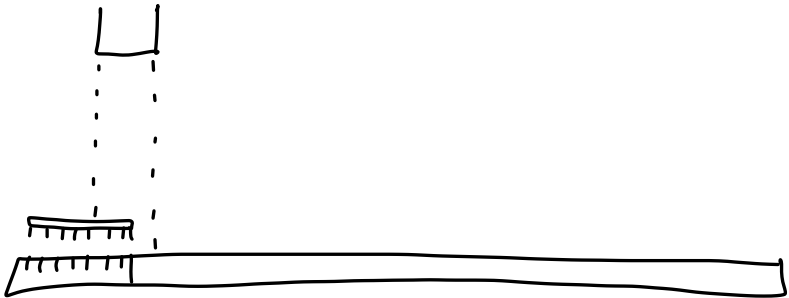


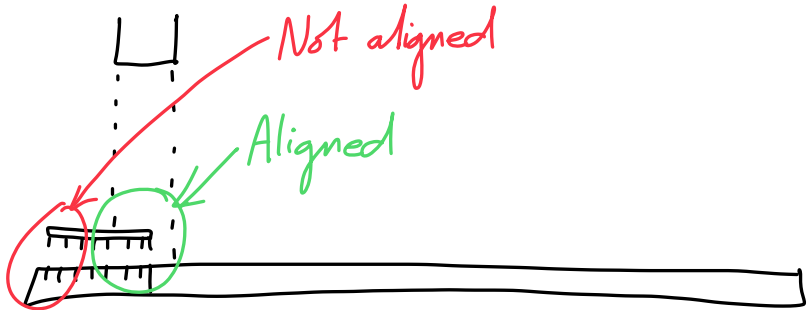


...Place wafer in traced outline...

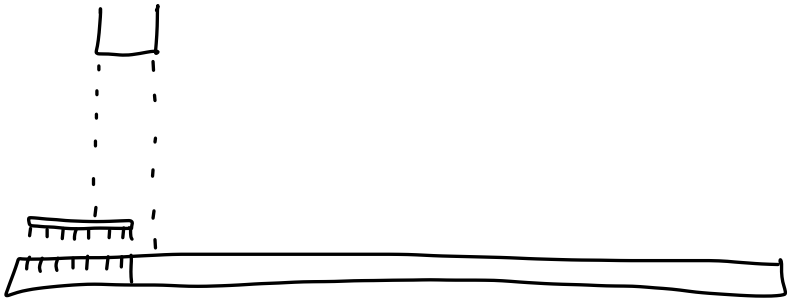


... Translate wafer ...



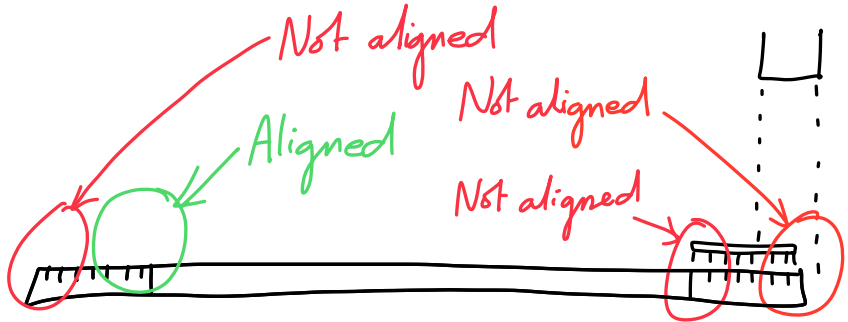


... Translate wafer ...

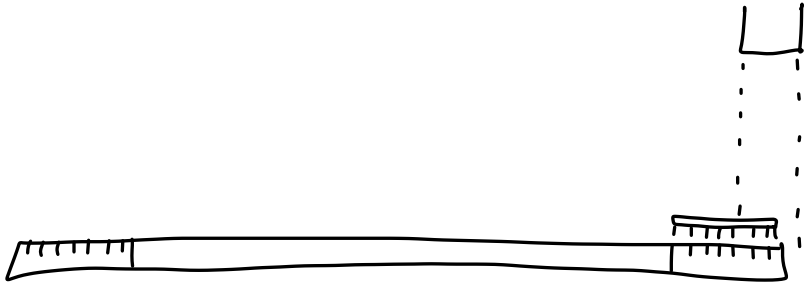




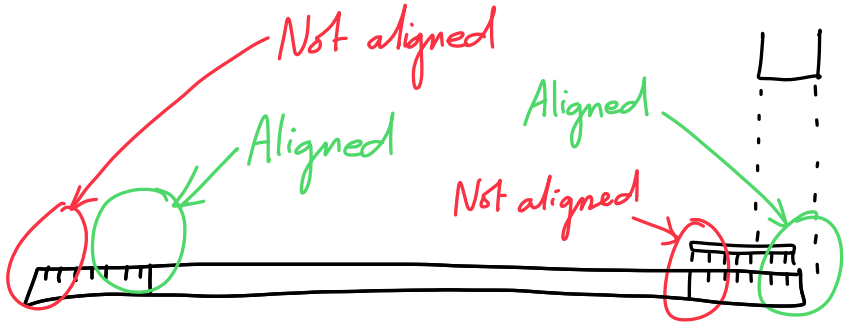
Chips, x-stage and probe card all misaligned



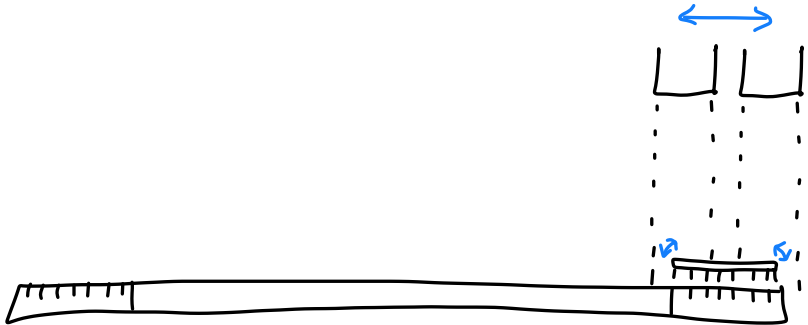
... Rotate and translate wafer ...



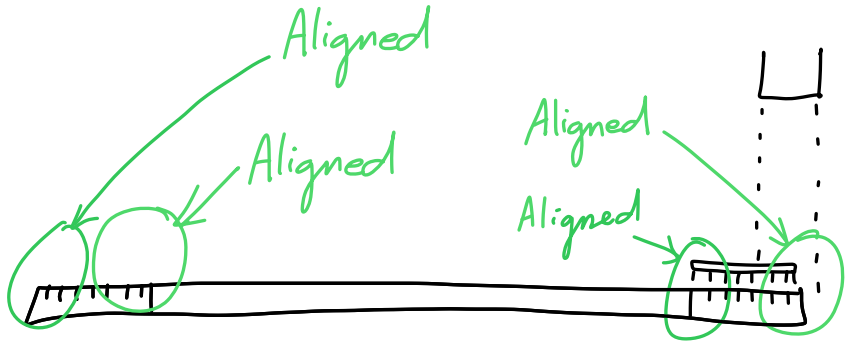
Chips and x-stage aligned  
Probe card not aligned



... Adjust probe card fit...



Chips, x-stage and probe card all aligned



- **Movement highly non-linear/orthogonal**, e.g. moving  $x$ -stage direction causes significant displacement in  $y$ -direction
- Designed **calibration**, to map “ideal”  $x$ - and  $y$ -positions to “true”  $x$ -,  $y$ - and  $z$ -positions
  - Used coordinates of the pads of every 3rd chip in  $x$ -direction and every 5th in  $y$ -direction
  - Calibrated missing corner chip locations by hand
- Replaced wafer before this test

