ITk Pixel TDAQ for HL-LHC using Optoboard-FELIX interface at LBL

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Weekly Instrumentation Meeting
Feb 24th, 2023

BERKELEY LAB

ATLAS EXPERIMENT

ITk Pixel TDAQ setup at LBL

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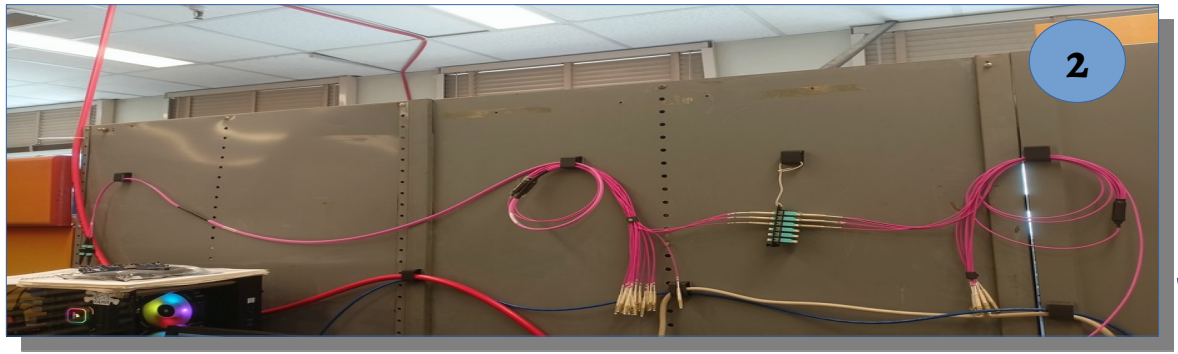
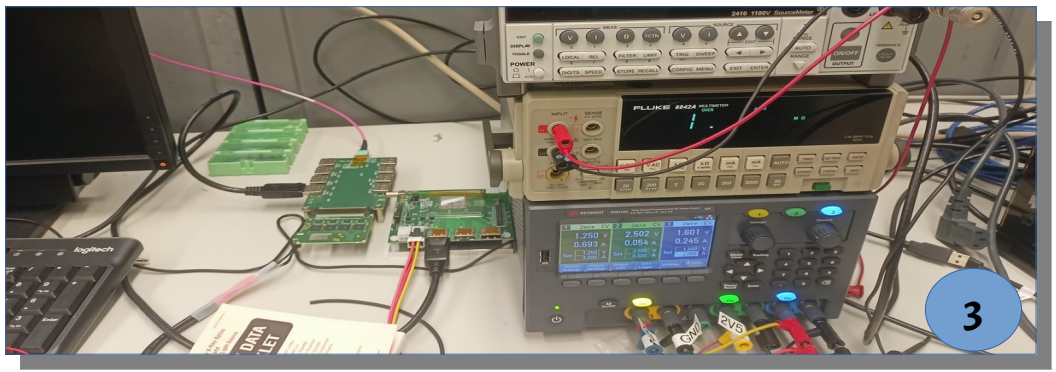
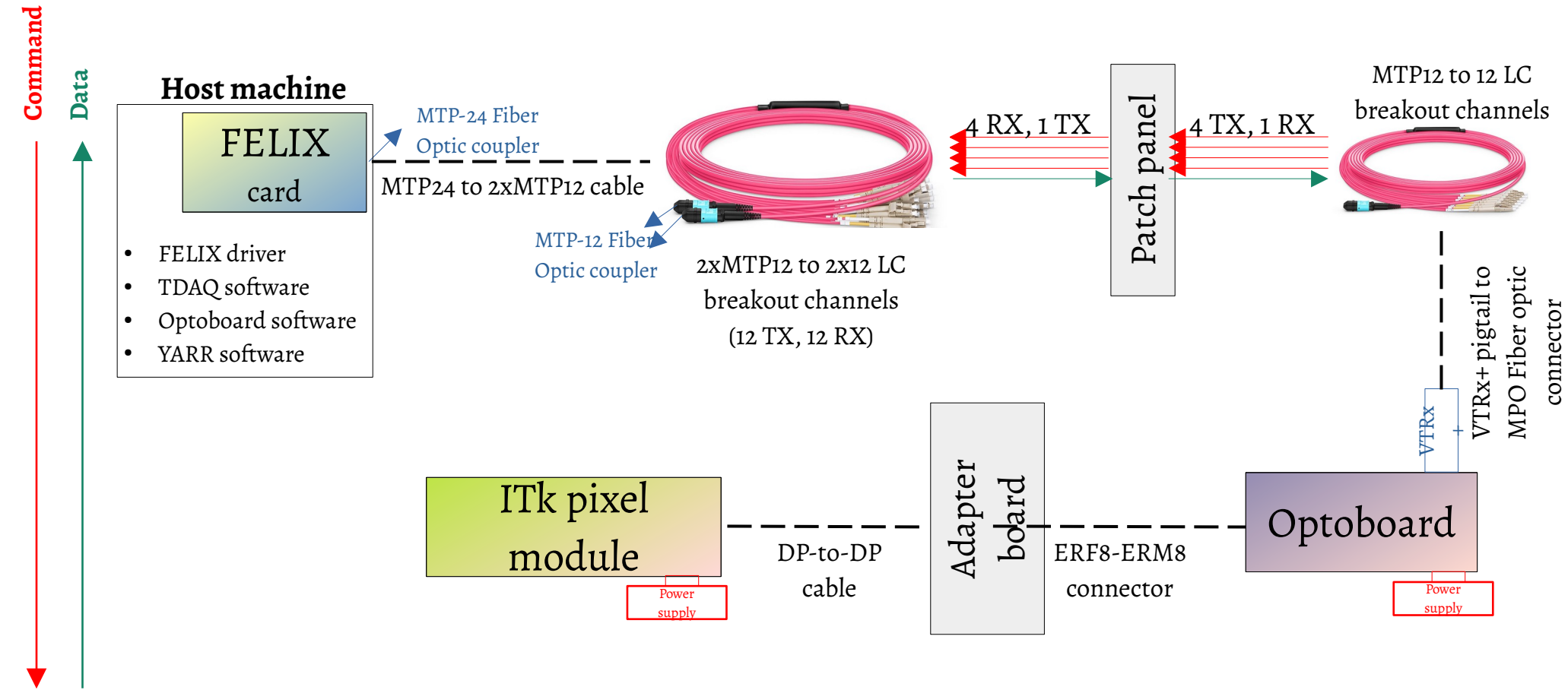




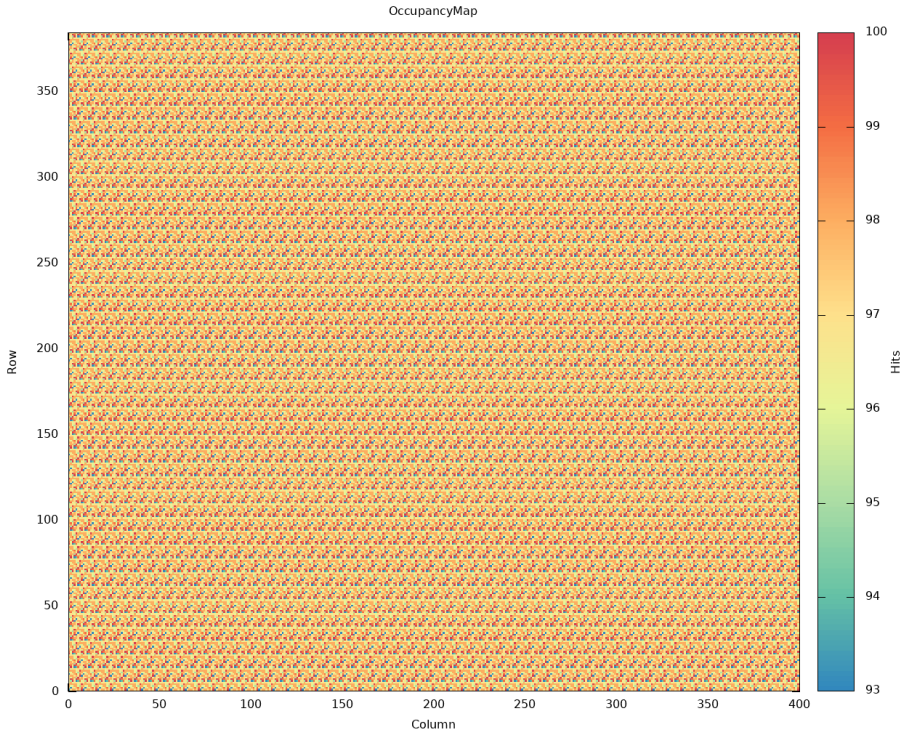
1. FELIX card
2. Optical fibers
3. Optoboard – ITk pixel module

50B-6038

Schematic of the setup



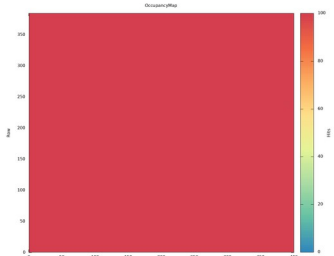
Recap: Digital scan



Link

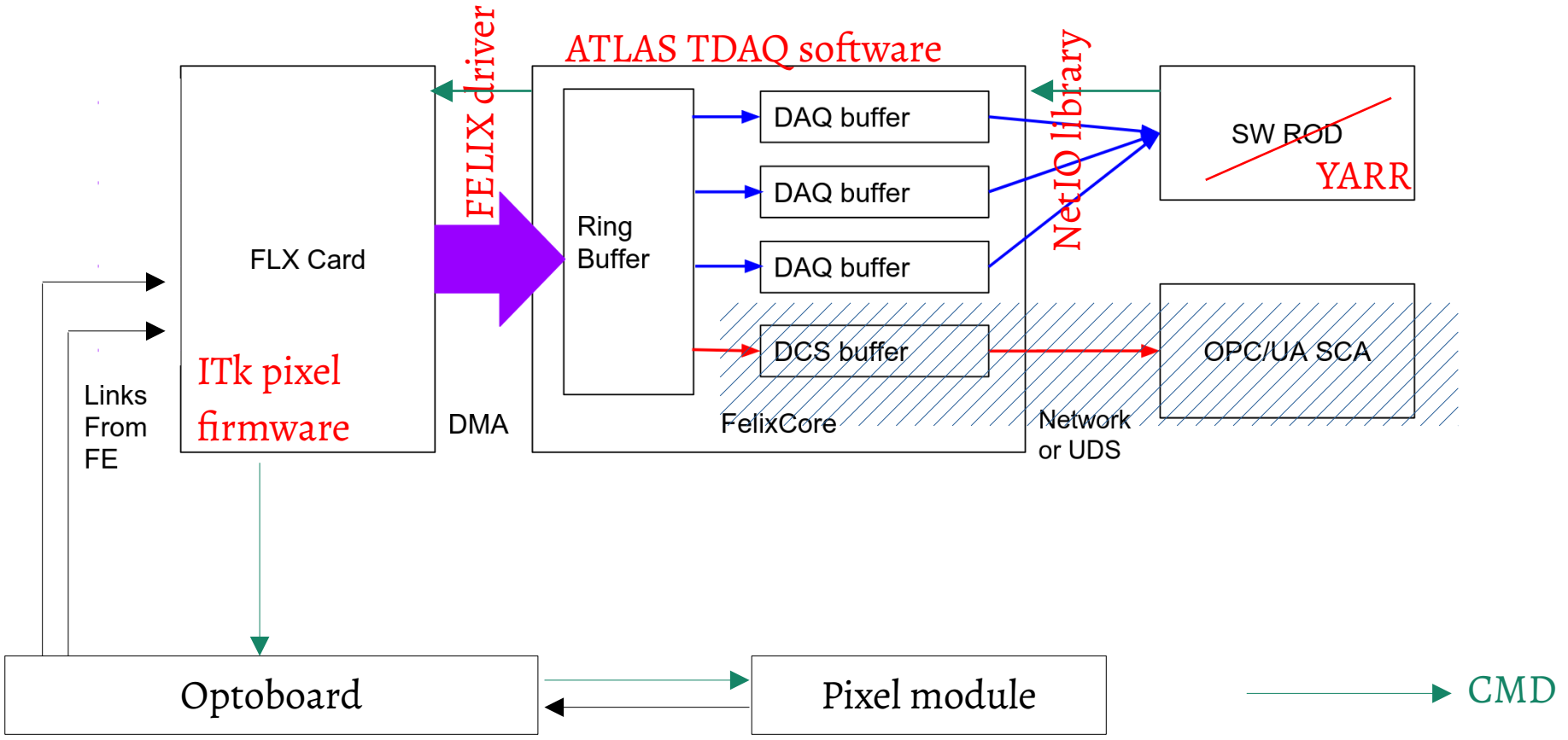
- Software-based trigger generation.
- Wait time of 1 second in StdDataLoop of YARR.
- Trigger frequency = 100 Hz
- Trigger count (injections) = 100
- Number of mask stages = 64

- Running the scans has been very unreliable, and is subjected to data losses.
- Felixcore server also crashes unexpectedly.

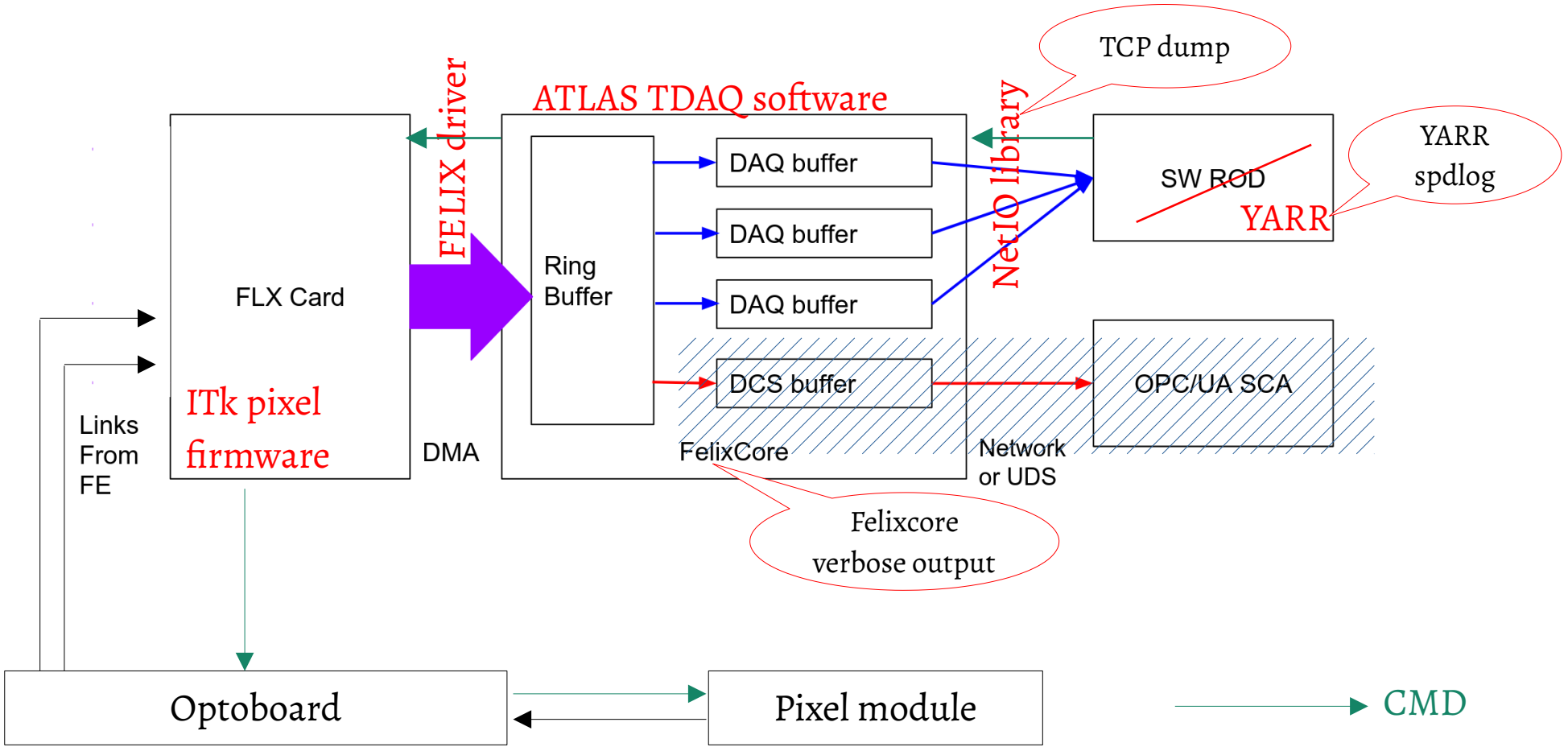


An example of a successful digital scan…

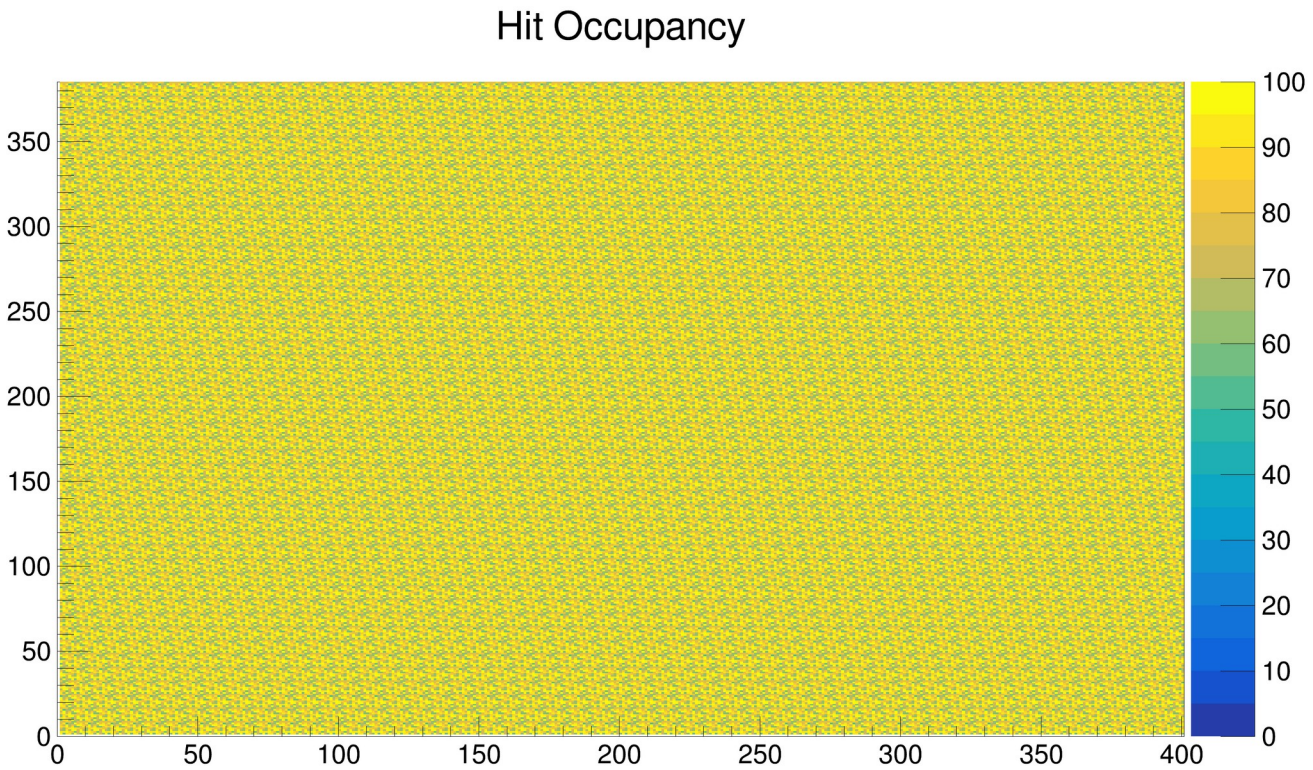
The heart of communication



Debugging

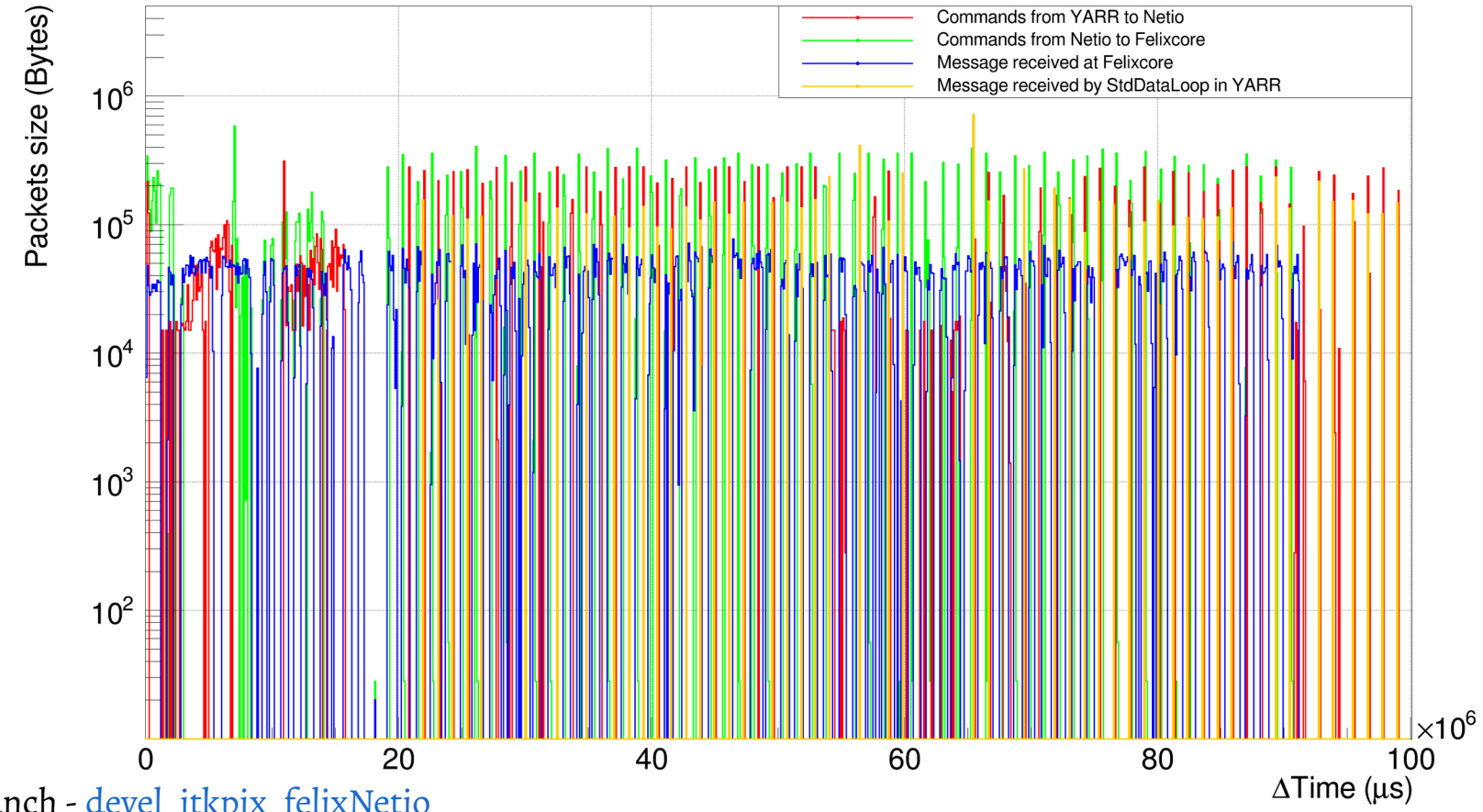

TCP dump
ATLAS TDAQ software
FELIX driver
NetIO library
YARR
spdlog
SW ROD
YARR
FLX Card
Ring
Buffer
DAQ buffer
DAQ buffer
DAQ buffer
DCS buffer
OPC/UA SCA
Links
From
FE
ITk pixel
firmware
DMA
FelixCore
Network
or UDS
Felixcore
verbose output
Optoboard
Pixel module
CMD

Investigating the digital scans

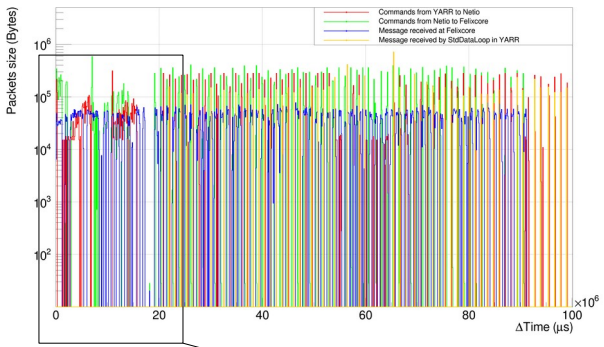


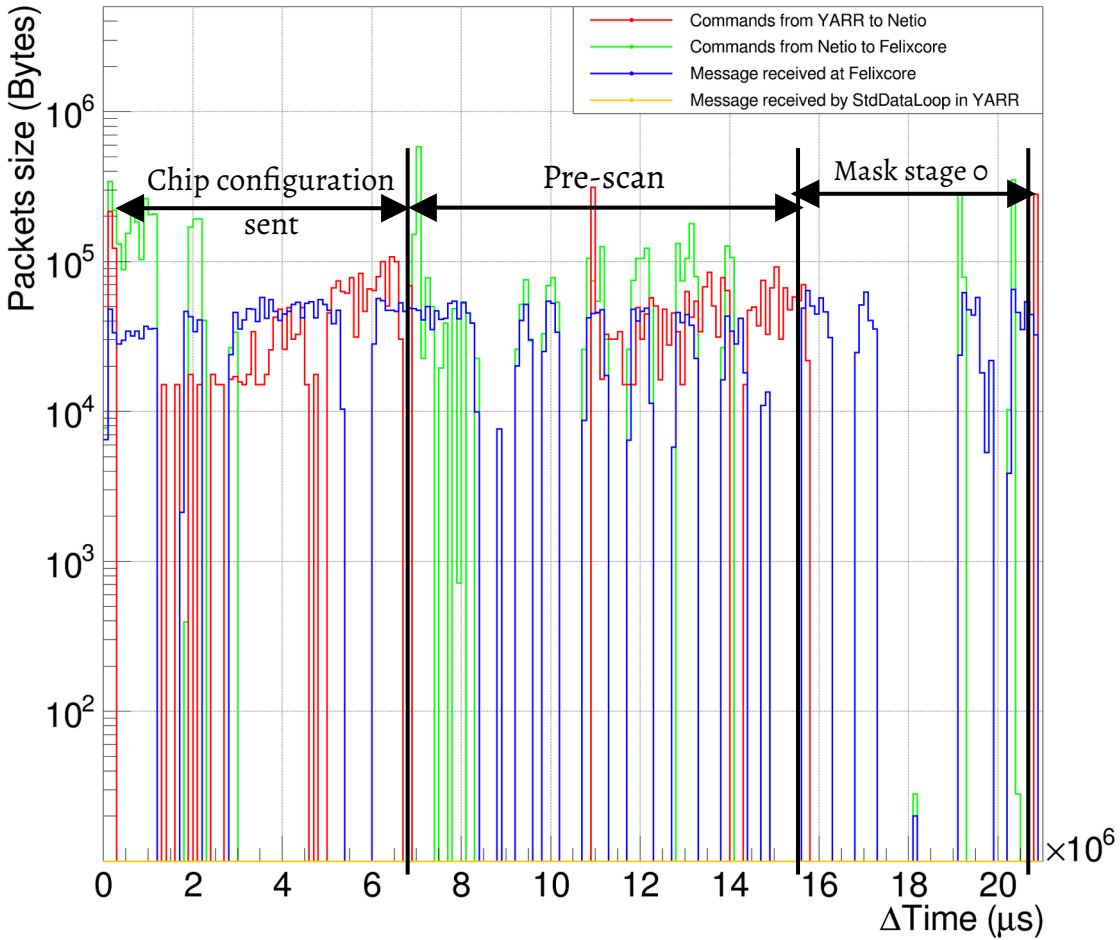
- Software-based trigger generation.
- Wait time of 1 second in StdDataLoop of YARR.
  Varied it up to 5 seconds at which point every mask stage has non-zero occupancy, but then felixcore crashes in between the scan.
- Trigger frequency = 5000 Hz
  Increasing the frequency otherwise felixcore server crashes in between the digital scan.
- Trigger count (injections) = 100
- Number of mask stages = 64

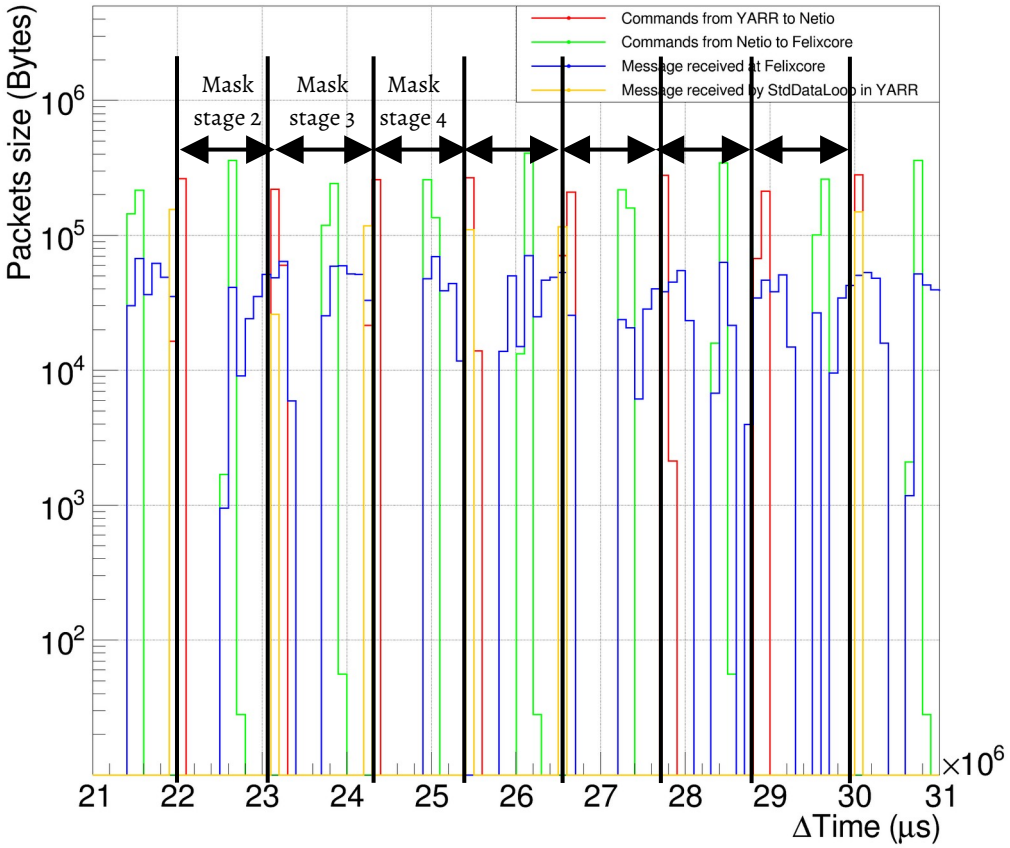
Timing vs packets: SW triggers

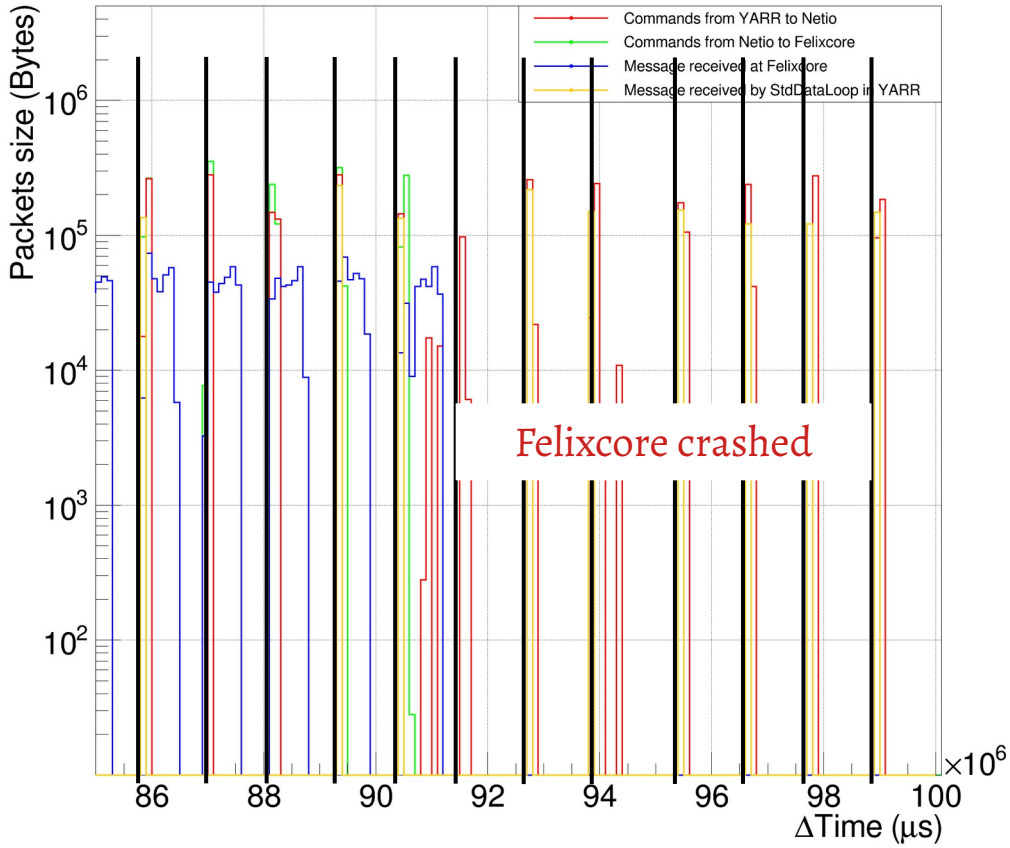


Default branch - devel_itkpix_felixNetio


Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Packets size (Bytes)
ΔTime (μs)
×10^6

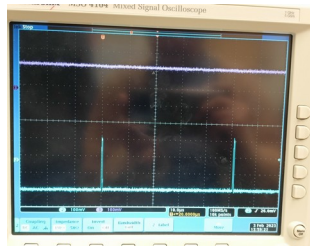

Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Chip configuration sent
Pre-scan
Mask stage 0
Packets size (Bytes)
ΔTime (μs)
×10^6


Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Mask stage 2
Mask stage 3
Mask stage 4
Packets size (Bytes)
10^6
10^5
10^4
10^3
10^2
21 22 23 24 25 26 27 28 29 30 31
$\times 10^6$
ΔTime (μs)

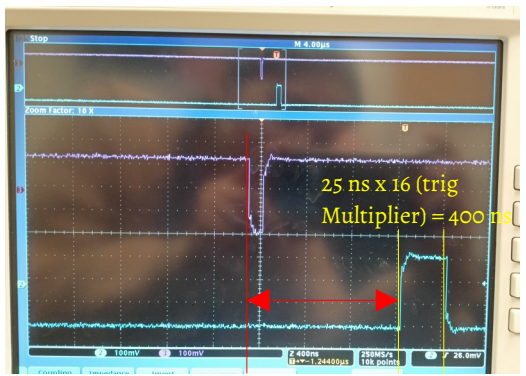

Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Packets size (Bytes)
10^6
10^5
10^4
10^3
10^2
Felixcore crashed
86 88 90 92 94 96 98 100
$\times 10^6$
ΔTime (μs)

Switching to FW triggers

- No raw data seen from the digital scan.
  - Packets with valid headers but no payload.
  - Varied the delay time and latency in the scan config to adjust the arrival of triggers, still nothing.



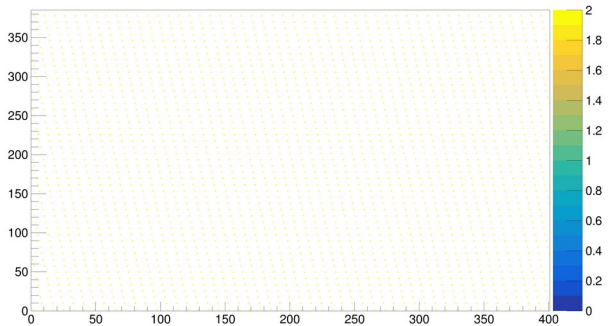
- Calibration injection, delay and trigger sequence not set in the FELIX firmware by default.
  - Raw data received after setting those registers.
  - No calibration injection+trigger sequence was seen in first few mask stages.



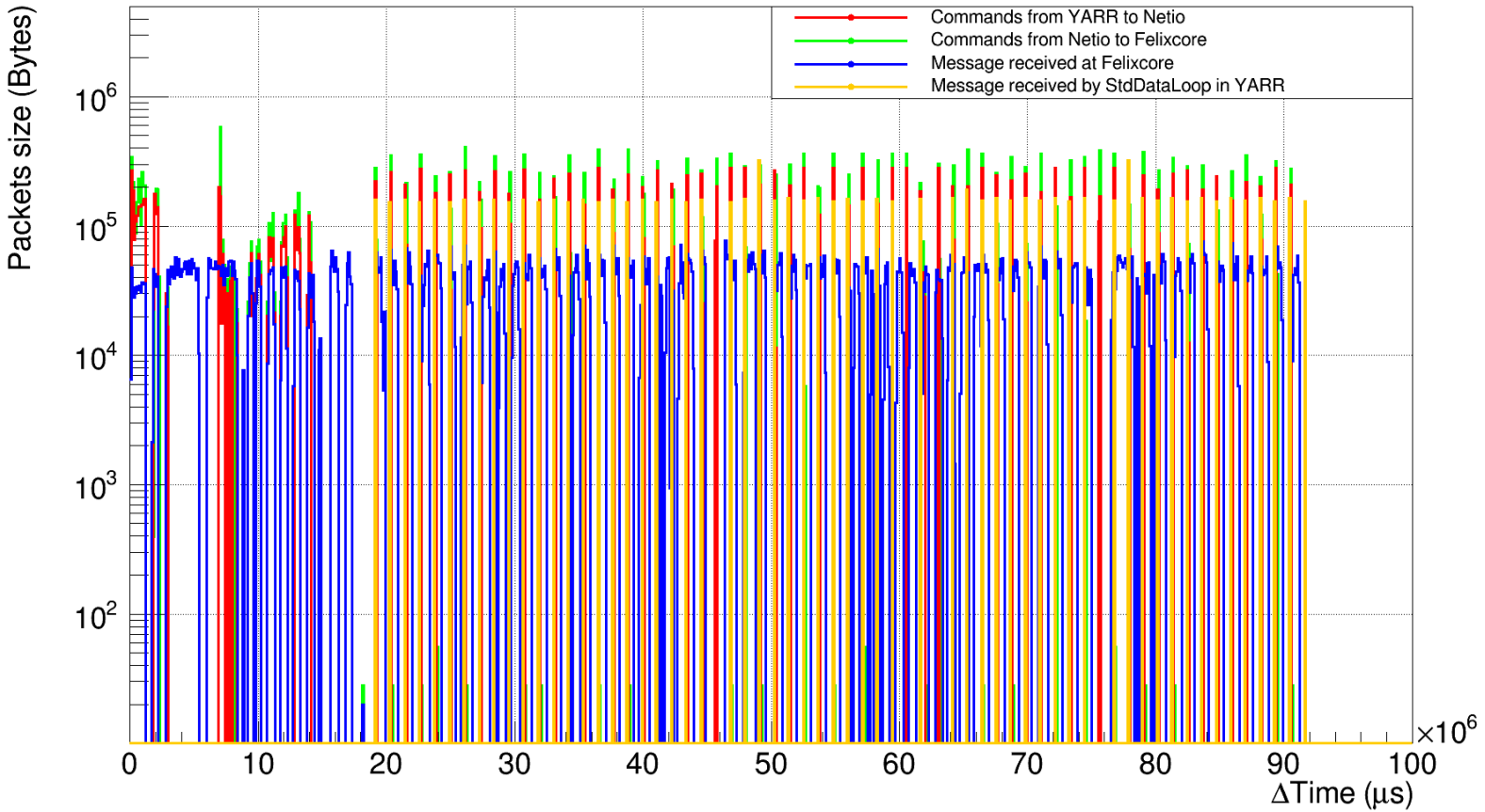
1460 ns ~ 58 BXs (Latency)

```
[06:41:08:269][  info  ][  ScanFactory  ][29462]: Entering pre scan phase ...
[06:41:08:269][  info  ][  ScanConsole  ][29462]: Starting histogrammer and analysis threads:
[06:41:08:269][  info  ][  ScanConsole  ][29462]:  .. started threads of Fe 0
[06:41:08:269][  info  ][Rd53bDataProcessor][29481]: Started raw data processor thread.
[06:41:08:269][  info  ][  ScanConsole  ][29462]: ################
[06:41:08:269][  info  ][  ScanConsole  ][29462]: ##  Run Scan  ##
[06:41:08:269][  info  ][  ScanConsole  ][29462]: ################
[06:41:08:395][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 0 (Activated 2400 pixels)
[06:41:13:467][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 913181 iterations!
[06:41:13:500][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 1 (Activated 2400 pixels)
[06:41:14:571][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 607014 iterations!
[06:41:14:588][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 2 (Activated 2400 pixels)
[06:41:15:659][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 818761 iterations!
[06:41:15:692][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 3 (Activated 2400 pixels)
[06:41:16:764][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 663088 iterations!
[06:41:16:797][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 4 (Activated 2400 pixels)
[06:41:17:869][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 629964 iterations!
[06:41:17:890][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 5 (Activated 2400 pixels)
[06:41:18:961][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 787887 iterations!
[06:41:18:982][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 6 (Activated 2400 pixels)
[06:41:20:053][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 722570 iterations!
[06:41:20:075][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 7 (Activated 2400 pixels)
[06:41:21:147][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 667551 iterations!
[06:41:21:184][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 8 (Activated 2400 pixels)
[06:41:22:256][  info  ][  StdDataLoop  ][29462]: --> Received 0 words in 299662 iterations!
[06:41:22:295][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 9 (Activated 2400 pixels)
[06:41:22:814][warning ][Netio::Handler ][29468]: WARNING: NetIO message is shorter than 8 bytes. It is 8 bytes.
[06:41:23:367][  info  ][  StdDataLoop  ][29462]: --> Received 160200 words in 308036 iterations!
[06:41:23:390][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 10 (Activated 2400 pixels)
[06:41:24:462][  info  ][  StdDataLoop  ][29462]: --> Received 152600 words in 409392 iterations!
[06:41:24:486][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 11 (Activated 2400 pixels)
[06:41:25:558][  info  ][  StdDataLoop  ][29462]: --> Received 160200 words in 746934 iterations!
[06:41:25:593][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 12 (Activated 2400 pixels)
[06:41:26:665][  info  ][  StdDataLoop  ][29462]: --> Received 152600 words in 674436 iterations!
[06:41:26:688][  info  ][ Rd53bMaskLoop ][29462]:  ---> Mask Stage 13 (Activated 2400 pixels)
[06:41:27:760][  info  ][  StdDataLoop  ][29462]: --> Received 160200 words in 858122 iterations!
```

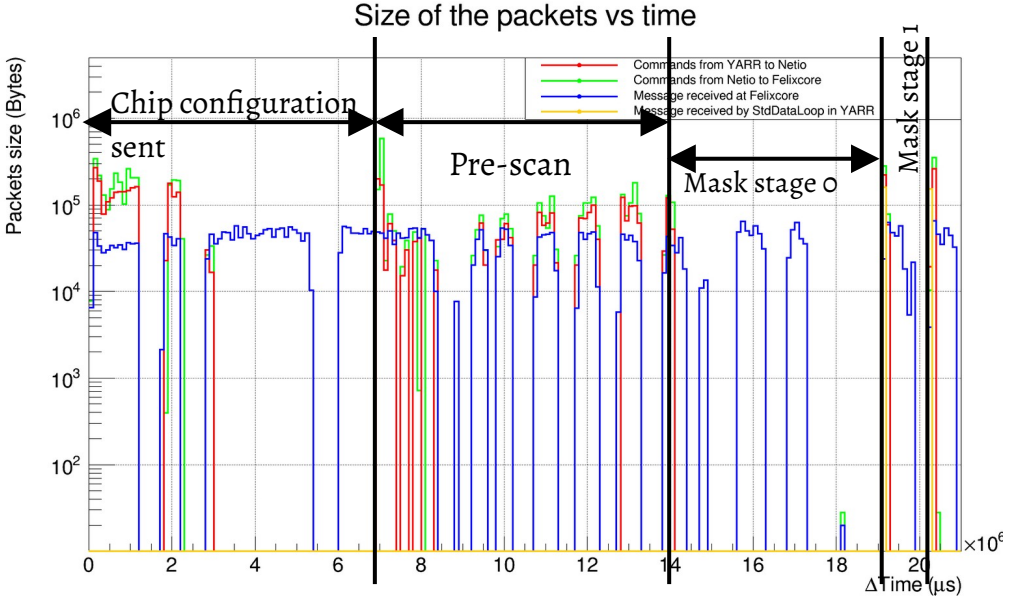
First event in raw data ~ Matches with first mask stage pattern.

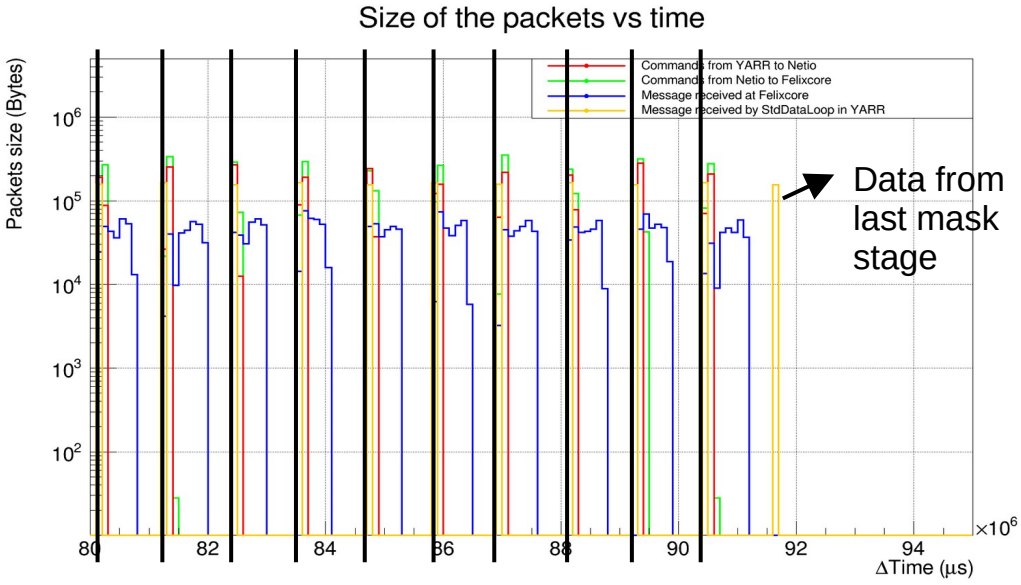


Timing vs packets: FW triggers



Default branch - devel_itkpix_felixNetio


Size of the packets vs time
Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Chip configuration sent
Pre-scan
Mask stage 0
Mask stage 1
Packets size (Bytes)
ΔTime (μs)
×10^6


Size of the packets vs time
Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Data from last mask stage
Packets size (Bytes)
ΔTime (μs)
×10^6

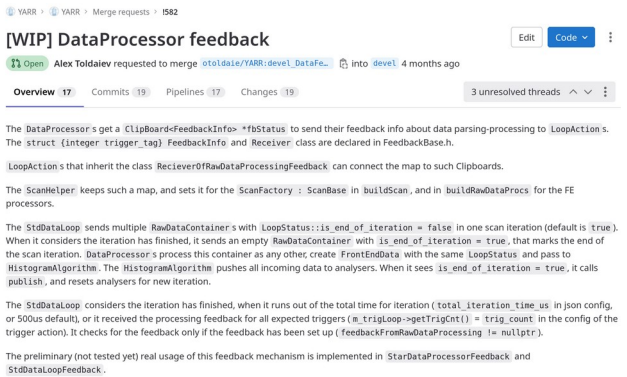
- Command takes a long time to reach the chip. Also, many many encoded packets per command are sent out from YARR to Felixcore.
  - Consequences: Felixcore buffer is flushed only after its full, hence takes a long time, and the scan time for that mask stage runs out.

- To resolve this,
  i. Wait longer to collect data back from chip in **StdDataLoop**: less efficient, also very system-dependent. Works only partially in the beginning and then Felixcore crashes.
  ii. No size check for the **NetioTxCore** buffer from YARR exists in the current version. Instead of sending out messages from YARR FiFo to Felixcore constantly, we can aggregate the messages so that command reaches the chip faster and in its entirety.

  iii. Can also add a maximum wait time in **NetioRxCore** to get the non-null raw data pointers for every mask stage. Same issues as i.

  Instead, a different implementation of this exists from the strip side – to continue reading out more data by using a feedback from the DataProcessor for approximate size of incoming data.

  MR - otoldaie/YARR:devel_DataFeedback



Fix for FW triggering

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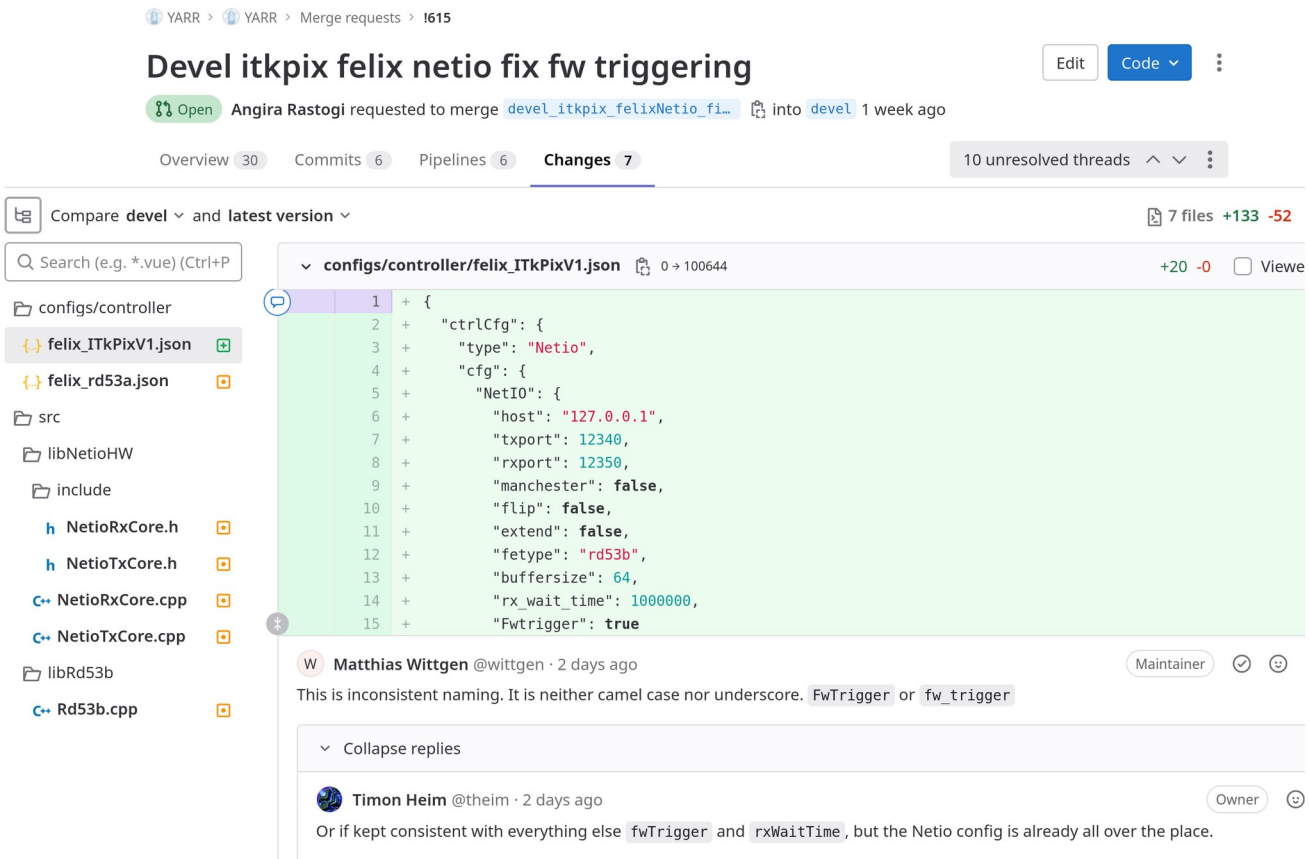
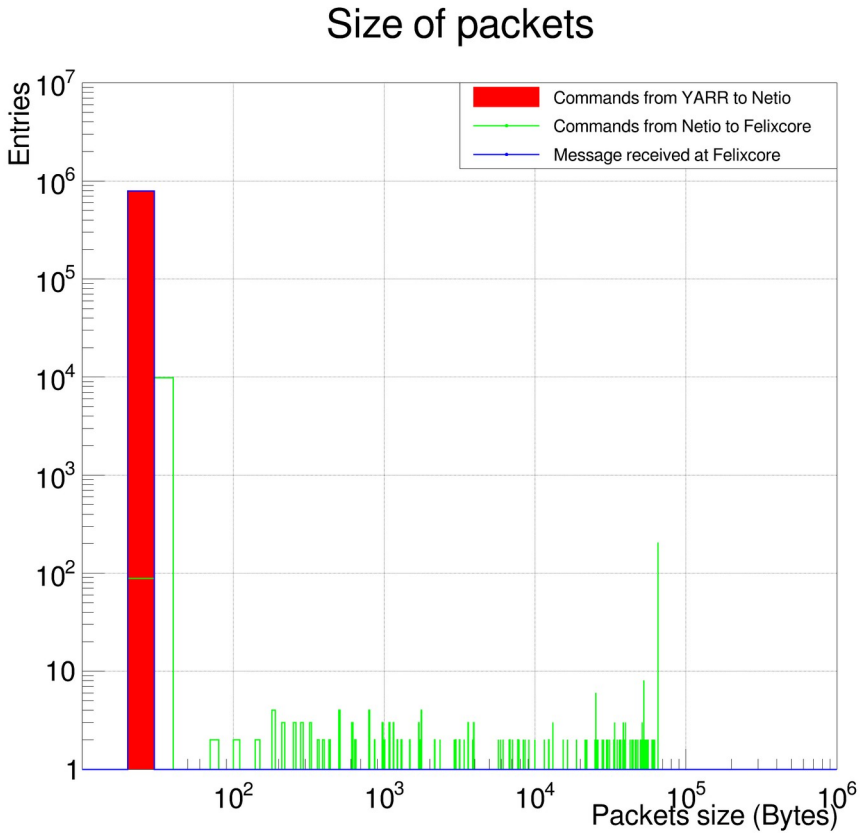
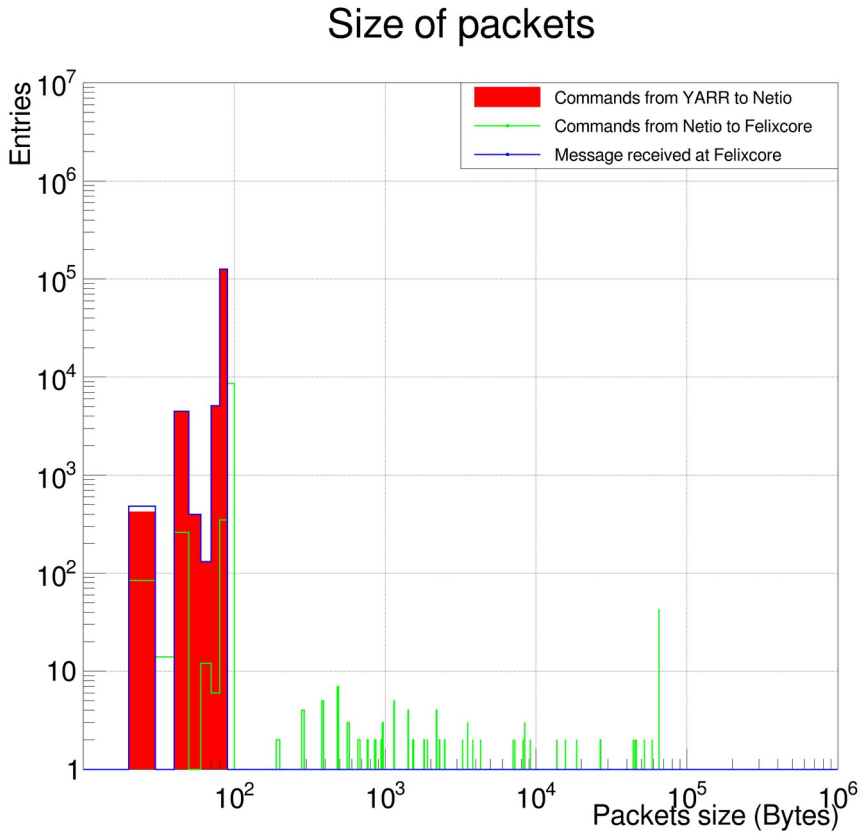
Link



- Through releaseFifo(), sending out longer command messages from YARR to felixcore.
- Using IsCmdEmpty() to flush the buffer, if not found empty in the end.

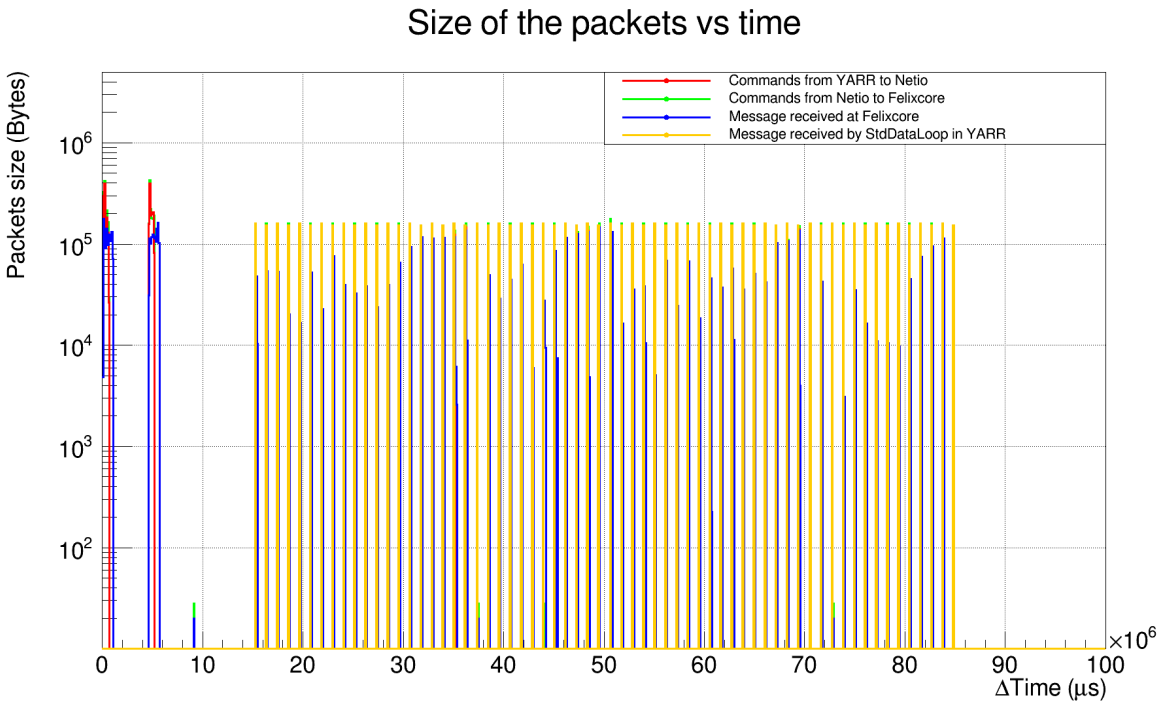


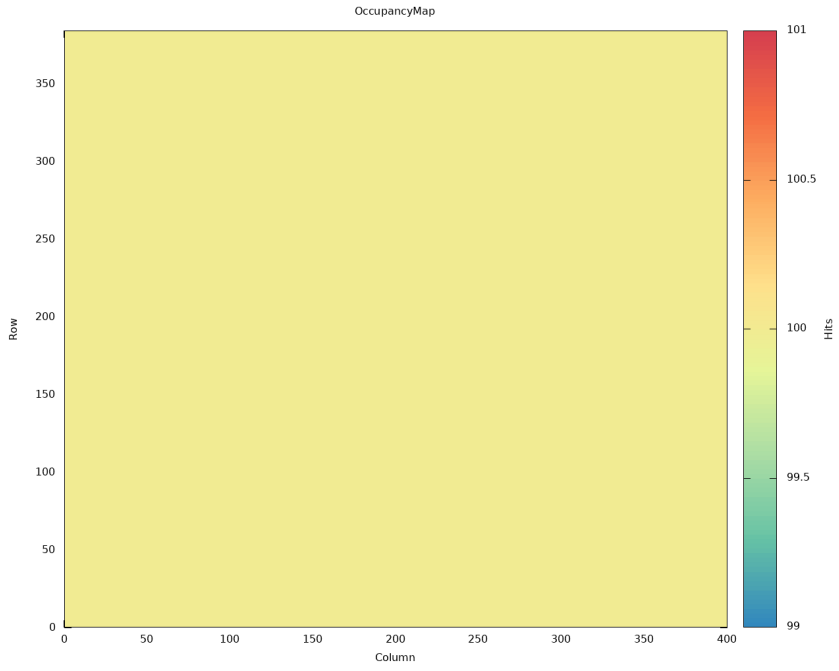
Default branch - devel_itkpix_felixNetio



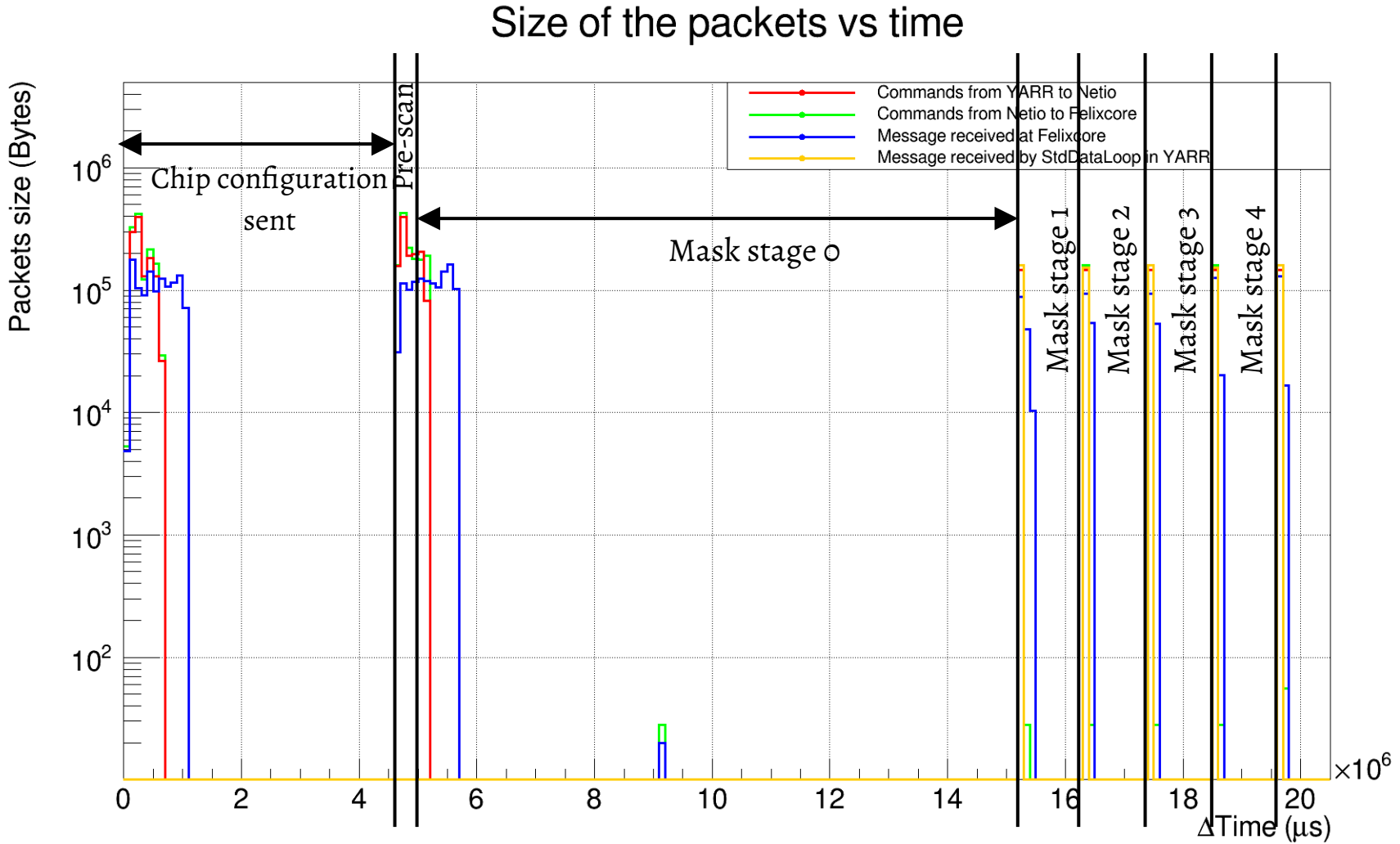
New branch - devel_itkpix_felixNetio_fixFWtrigger

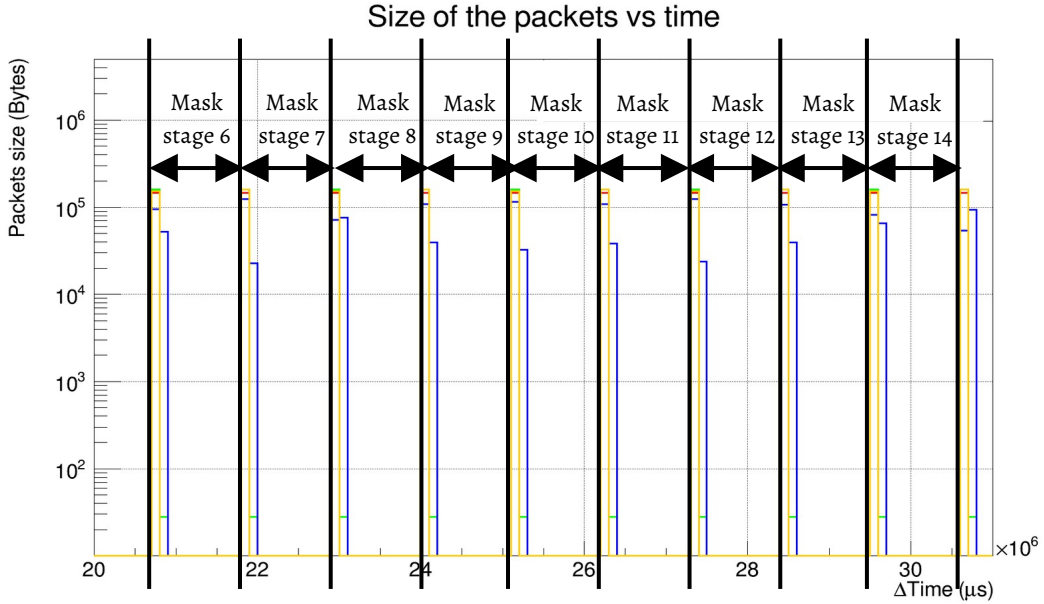
FW triggers: New results

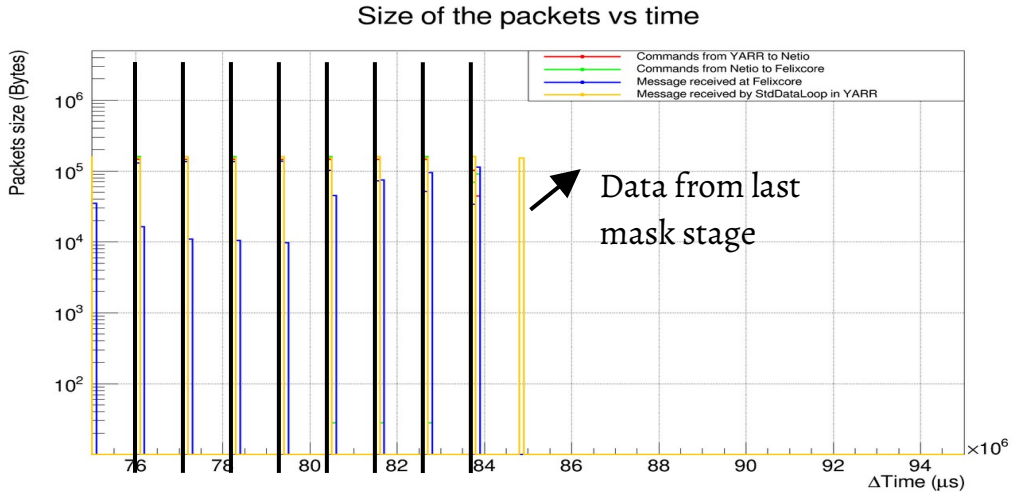




New branch - devel_itkpix_felixNetio_fixFWtrigger


Size of the packets vs time
Packets size (Bytes)
Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Chip configuration sent
Pre-scan
Mask stage 0
Mask stage 1
Mask stage 2
Mask stage 3
Mask stage 4
ΔTime (μs)
×10^6


Size of the packets vs time
Packets size (Bytes)
Mask stage 6
Mask stage 7
Mask stage 8
Mask stage 9
Mask stage 10
Mask stage 11
Mask stage 12
Mask stage 13
Mask stage 14
×10^6
ΔTime (μs)


Size of the packets vs time
Commands from YARR to Netio
Commands from Netio to Felixcore
Message received at Felixcore
Message received by StdDataLoop in YARR
Packets size (Bytes)
Data from last mask stage
×10^6
ΔTime (μs)

Next steps

- Cross verifying the merge request which fixes the firmware trigger, especially changes done in the NetioTxCore, with the strips community.
- Verify the other hidden latencies which could cause delays in sending out the commands – such as with network, ethernet or with the host machine.
- Check with other pixel SCCs, if the changes work.
- Understand the timing plots, try to optimize the limit on the buffer size and wait time in StdDataLoop.

- Enable FELIX firmware to read the chip configuration registers (right now its bypassed through the ServiceEnable=0).
- To implement the data processor feedback changes for ITk pixel DAQ.

- Finally, move to using quad modules.