Module QC results

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on behalf of Module QC developers

Instrumentation meeting Feb 10 2023

BERKELEY LAB

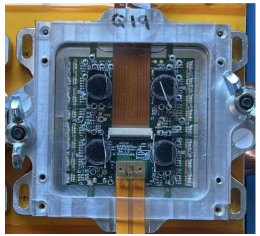
UNIVERSITY OF OREGON

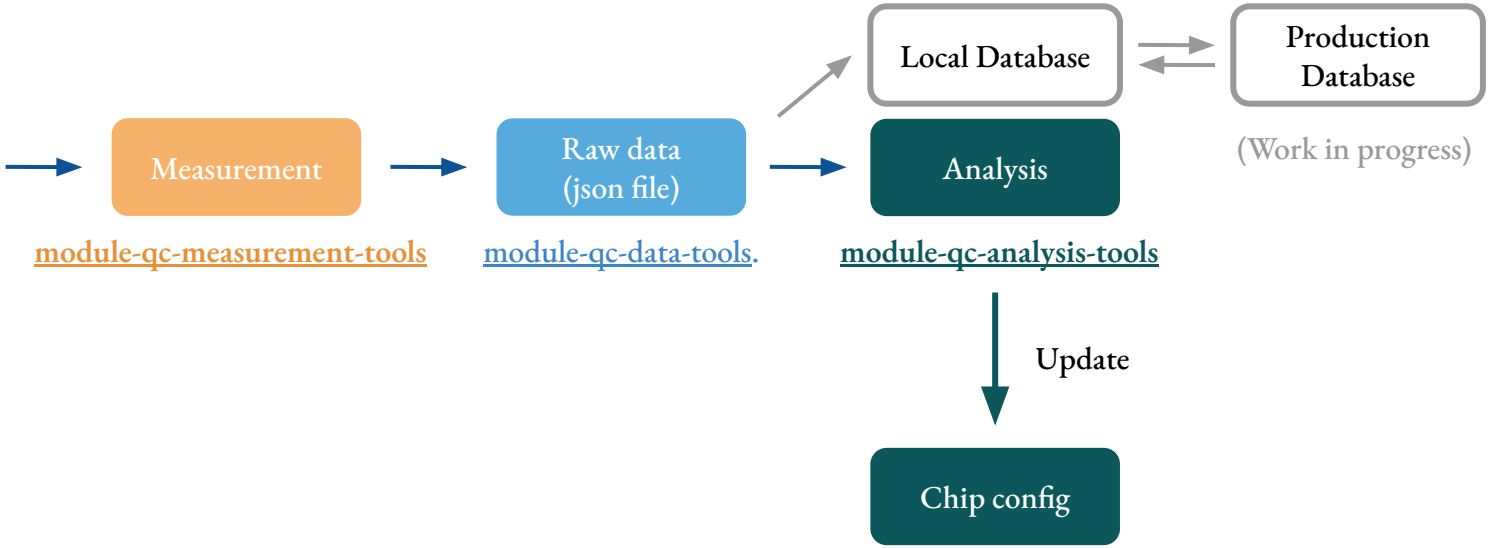
Module QC tools

Electrical quality control (QC) testing procedures of ITkPixV1.1 modules.

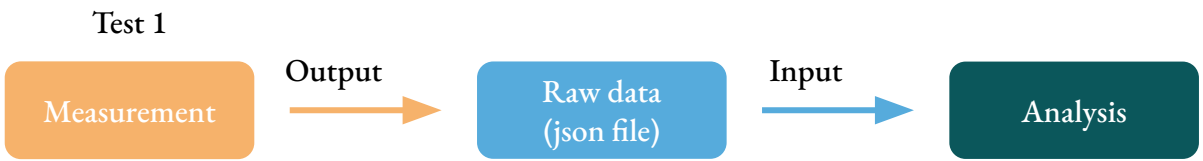
We released the first version (V1) of the tools for digital module test qualification!

ITkPixV1.1 Module





Workflow



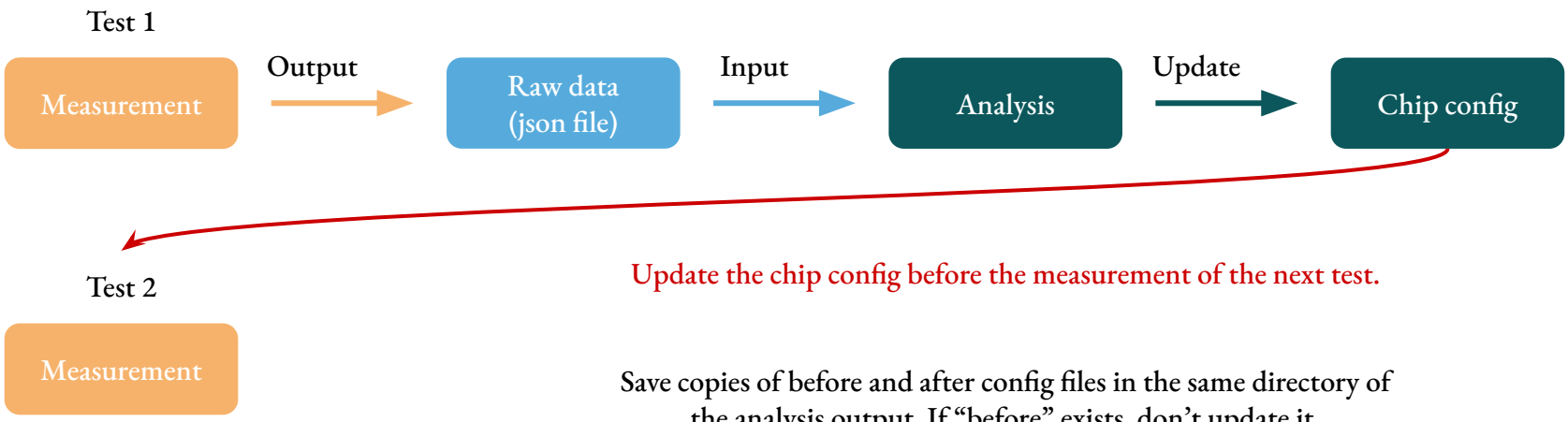

```
<modulde_uid>
|__ <modulde_uid>_<tag>.json
|__<tag>
    |__ <chip_uid1>_<tag>.json
    |__ <chip_uid2>_<tag>.json
    |__ <chip_uid3>_<tag>.json
    |__ <chip_uid4>_<tag>.json
|__ Measurements
    |__ <test_name>
    |__ VCAL_CALIB
        |__ <timestamp>
            |__ <chip_name/module_serial_number>.json
            |__ <sym link to analysis result>
    |__ SLDO_IV
```

```
|__ Analysis
    |__ <test_name>
    |__ VCAL_CALIB
        |__ <timestamp>
            |__ <chip_name/module_serial_number>.json
            |__ <sym link to measurement>
```

Folder structure

The **test name** is part of the output path.

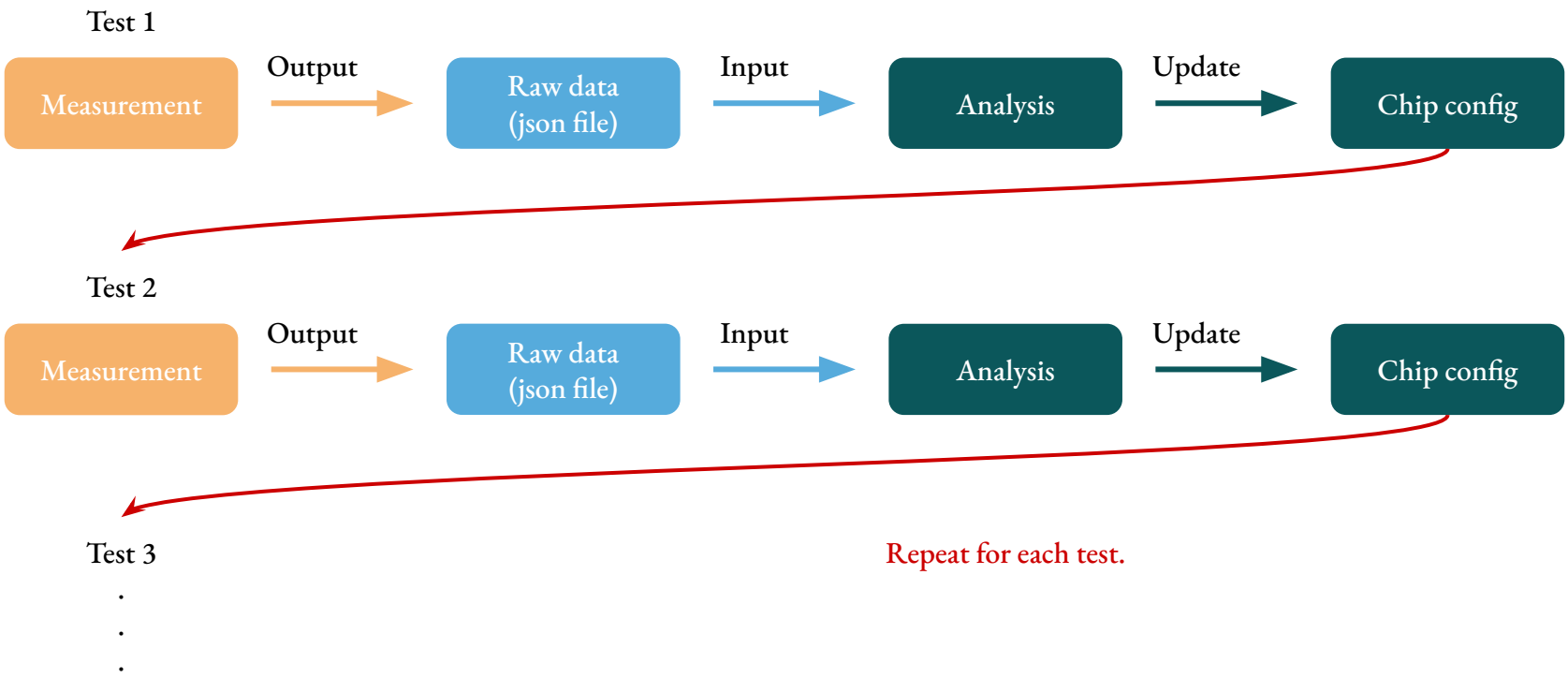
Workflow



Update the chip config before the measurement of the next test.

Save copies of before and after config files in the same directory of the analysis output. If "before" exists, don't update it.

Workflow


Test 1
Measurement
Output
Raw data (json file)
Input
Analysis
Update
Chip config
Test 2
Measurement
Output
Raw data (json file)
Input
Analysis
Update
Chip config
Test 3
.
.
.
Repeat for each test.

Electrical QC tests

ADC Calibration

- Calibrate Analog to Digital Converter (ADC) so that all voltages and currents can be measured through ADC.

Analog Readback

- Measure all internal biases, chip temperature, and VDDA/VDDD vs Trim.
- Give access to the status of the chip during module QC, and after modules being loaded on to local support.

VCal Calibration

- Calibrate DACs that generate the injection voltages, and compare to wafer probing.

Injection Capacitance

- Measures the capacitance of the front-end injection capacitor.

SLDO

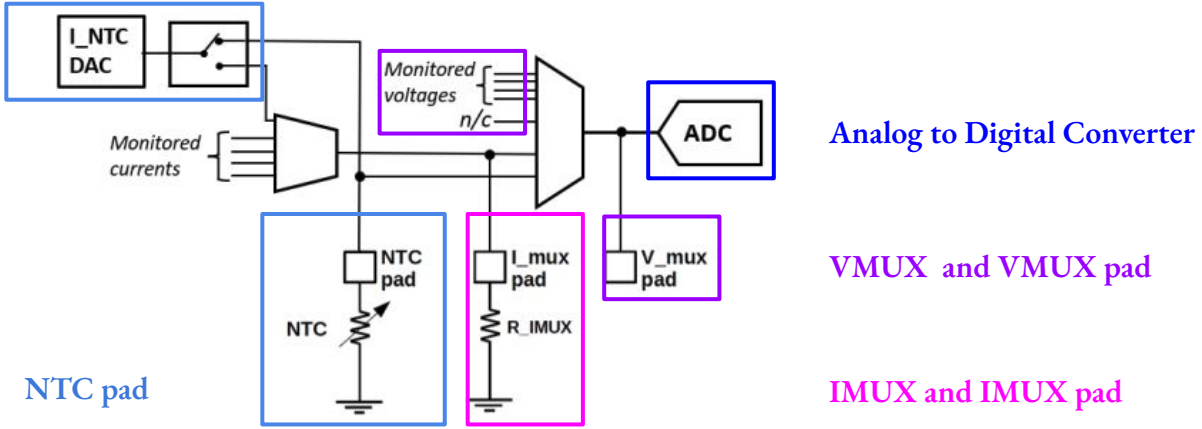
- Check if the Shunt LDO regulator (SLDO) is working as expected.

Chip sensing and monitoring

Monitoring block:

- Analog current multiplexer (IMUX)
- Analog voltage multiplexer (VMUX)
- Analog to Digital converter (ADC)
- VMUX pad, IMUX pas, and NTC pad.

Current and voltage multiplexers feed the input of the ADC, and are available on the VMUX pad.



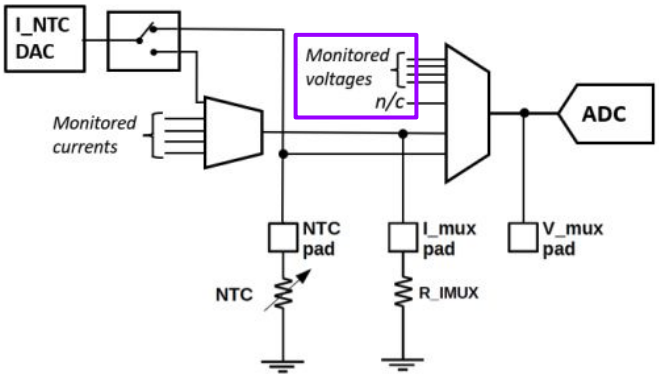
Voltage multiplexer (VMUX)

- Voltages: VINA, VIND, VDDA, VDDD, ...
- Temperature: MOS Sensors & Poly Sensors, external NTC (More on this later).
- Radiation sensor

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	Vref_ADC (GADC)	10	DIFF FE VTH1 Main array	31	Vref_CORE
1	I_mux pad voltage	11	DIFF FE VTH1 Left	32	Vref_PRE
2	NTC_pad voltage	12	DIFF FE VTH1 Right	33	VINA / 4
3	VCAL_DAC / 2 (Sec. 6.3)	13	RADSENS Ana. SLDO	34	VDDA / 2
4	VDDA / 2 from capmeasure	14	TEMPSENS Ana. SLDO	35	VrefA
5	Poly TEMPSENS top	15	RADSENS Dig. SLDO	36	VOFS / 4
6	Poly TEMPSENS bottom	16	TEMPSENS Dig. SLDO	37	VIND / 4
7	VCAL_HI	17	RADSENS center	38	VDDD / 2
8	VCAL_MED	18	TEMPSENS center	39	VrefD
9	DIFF FE VTH2	19-30	Ana. GND	40-62	not used
				63	high Z

Table 27: Voltage multiplexer (V_mux) assignments for ATLAS chip.

Analog voltage multiplexer



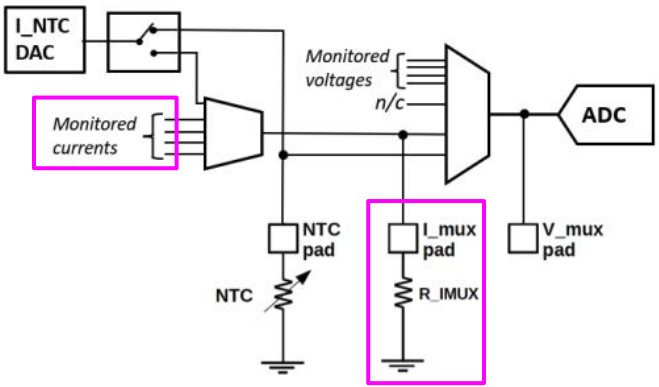
Current multiplexer (IMUX)

- Internal biases for PLL (CDR), data output driver (CML), and analog front-end (DIFF FE)
- Internal chip currents: input current & shunt current.
- The output of IMUX is measured as voltage through connection of an external resistor to ground.

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	IREF main ref. current	11	Capmeasure parasitic	22	DIFF FE Preamp Top-Left
1	CDR VCO main bias	12	DIFF FE Preamp Main array	23	DIFF FE VTH1 Right
2	CDR VCO buffer bias	13	DIFF FE PreComp	24	DIFF FE Preamp Top
3	CDR CP current	14	DIFF FE Comparator	25	DIFF FE Preamp Top-Right
4	CDR FD current	15	DIFF FE VTH2	26	not used
5	CDR buffer bias	16	DIFF FE VTH1 Main array	27	not used
6	CML driver tap 2 bias	17	DIFF FE LCC	28	Ana. input current/21000
7	CML driver tap 1 bias	18	DIFF FE Feedback	29	Ana. shunt current/21600
8	CML driver main bias	19	DIFF FE Preamp Left	30	Dig. input current/21000
9	NTC_pad current	20	DIFF FE VTH1 Left	31	Dig. shunt current/21600
10	Capmeasure circuit	21	DIFF FE Preamp Right	32-62	not used
				63	high Z

Table 26: Current multiplexer (I_mux) assignments for ATLAS chip.

Analog current multiplexer



ADC Calibration → Analog Readback → VCal Calibration → Injection Capacitance → SLDO

- Compare the same voltage measured through VMUX pad by external multimeter vs through ADC (digital readout from YARR).
- Obtain the slope and offset, and update the **ADCcalPar** setting in the chip configuration.

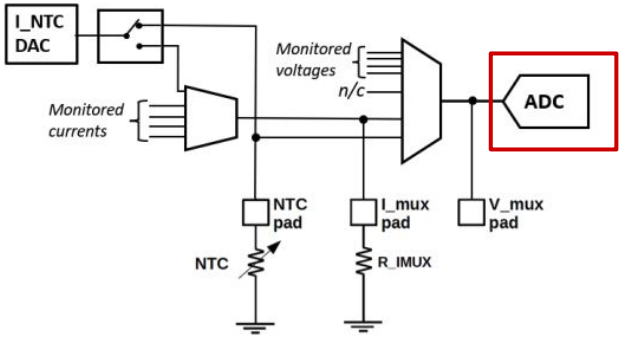
ADC Calibration output

"ADC_CALIBRATION_SLOPE": 0.198,
"ADC_CALIBRATION_OFFSET": 4.67,

→

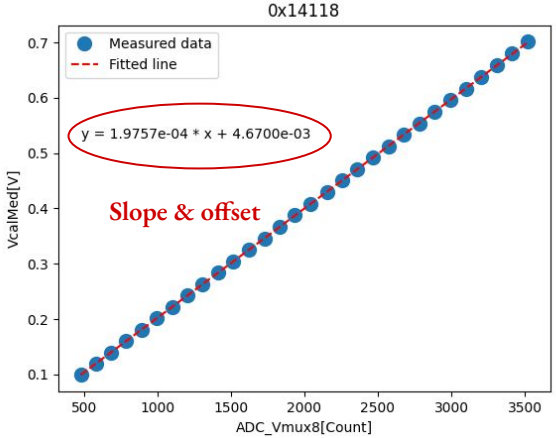
Chip config setting

"ADCcalPar": [4.67, 0.198, 4990.0]



Analog to Digital Converter

Read out voltages from the monitoring multiplexer (MUX).



- Measure all internal biases, NTC sensors, internal temperature sensors, and VDDA/VDDD vs Trim.
- From VDDA/VDDD vs Trim measurement, find the trim values that gives the VDDA/VDDD closest to 1.2V.
- Use the optimal trim setting to update **SldoTrimA** and **SldoTrimD** in the chip configuration.

Analog Readback output

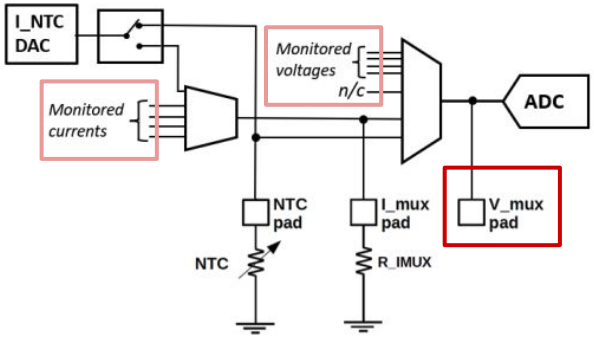
```
"AR_VDDA_VS_TRIM": [1.1023, 1.121, ..., 1.1963, ..., 1.3605, 1.379]
"AR_VDDD_VS_TRIM": [1.086, 1.104, ..., 1.1995, ..., 1.3536, 1.3595]
```

→

Chip config settings

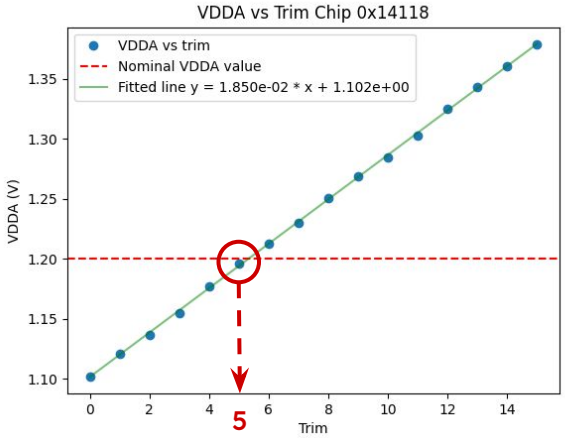
```
"SldoTrimA": 5,
"SldoTrimd": 6,
```

32 IMUX, 40 VMUX, and NTC temperature



VMUX pad

Read out all internal biases form the VMUX pad.



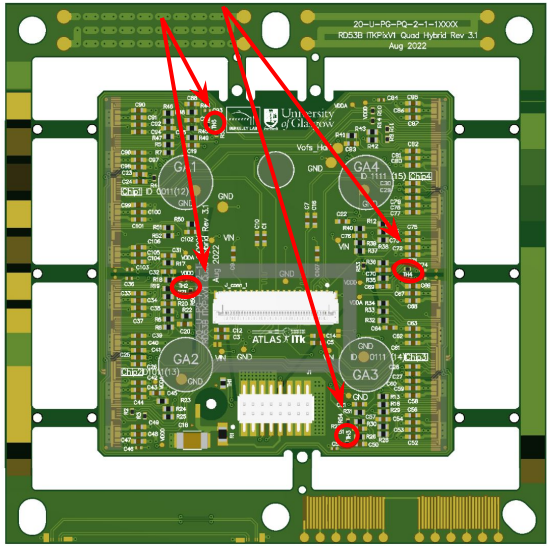
Measure T from External NTC

- External NTC: one per chip on the flex.
  - Each NTC is routed to its chip via wire bond pad.
  - Chip sources a known current through the NTC, which can be measured through IMUX.
  - The voltage at NTC pad is is measured via VMUX, and can be converted into T using Steinhart–Hart equation.

NTC parameters are taken from the chip config.

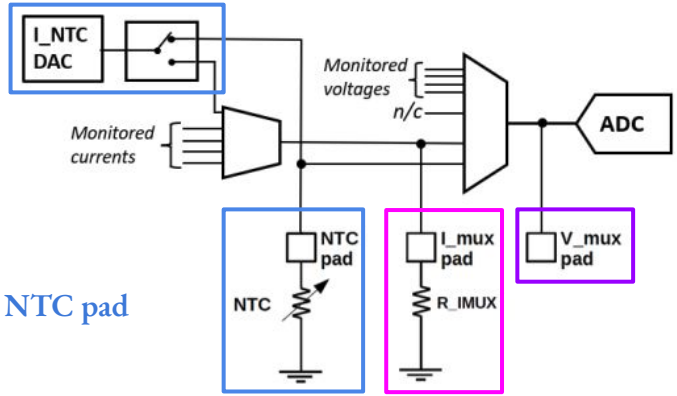
Detailed procedure see backup.

4 Ext NTC (one per chip)



Vmux 2	NTC_PAD voltage
Imux 9	NTC_PAD current

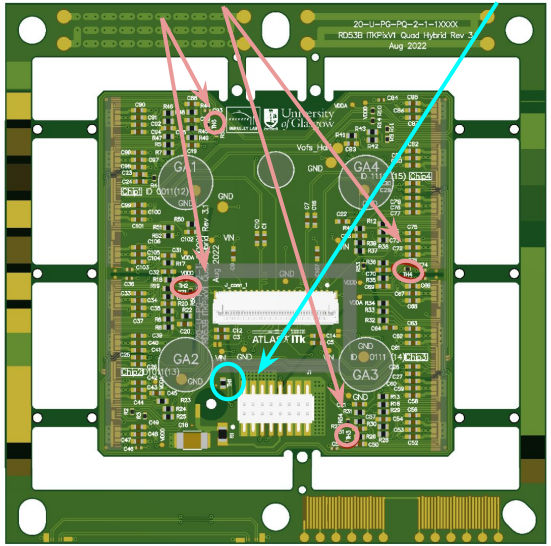
NTC pad



Measure T from DCS Ext NTC

- External NTC: one per chip on the flex.
- Detector Control System (DCS)/Interlock External NTC: connected externally via the power connector.

4 Ext NTC (one per chip) 1 DCS Ext NTC per flex



- During module QC, connect an external multimeter to pin on the power adaptor board.
- Directly measure the resistance of the NTC.
- Convert R to T using the Steinhart-Hart Equation.

$$T = 1/(A + B \ln R + C (\ln R)^3)$$

- Implemented as a tool in labRemote.

Precision limitations: multimeter resolution and ADC resolution.

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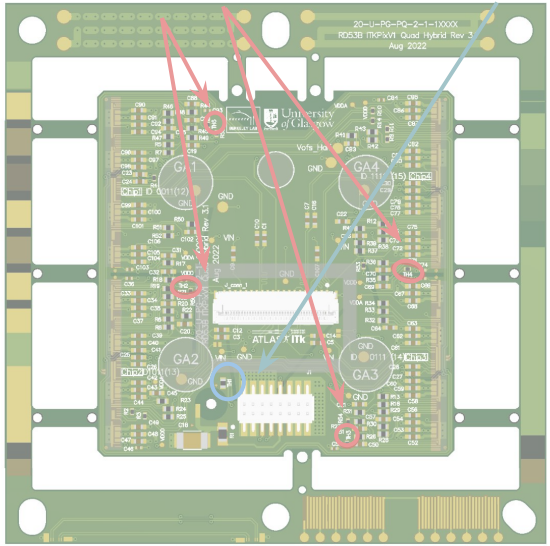
Measure T from MOS sensors

- External NTC: one per chip on the flex.
- Detector Control System (DCS)/Interlock External NTC: connected externally via the power connector.
- Internal MOS sensors: 3 transistor sensors inside the chip - proved internal temperature sensing.

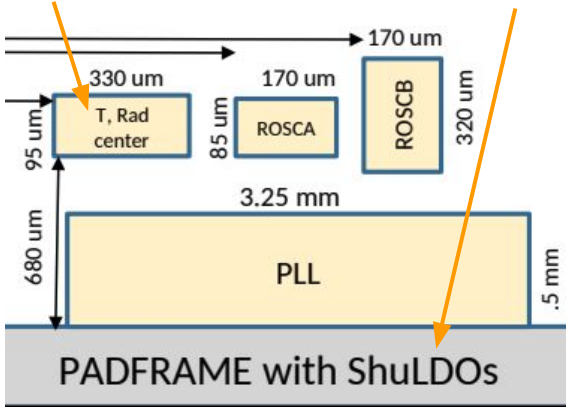
4 Ext NTC (one per chip) 1 DCS Ext NTC per flex



MOS sensor at the center of the analog chip bottom

MOS sensors at the analog & digital SLDO

Vmux 14	SLDO Analog
Vmux 16	SLDO Digital
Vmux 18	ACB center



Measure T from MOS sensors

Motivation

- NTC sensors are very precise, easy to measure, but external to the chip.
- MOS sensors are closer to the regulators (main heat source), but more complicated to measure.
- MOS sensors are in theory very precise, but constrained by the ideality factor.

MOS sensors

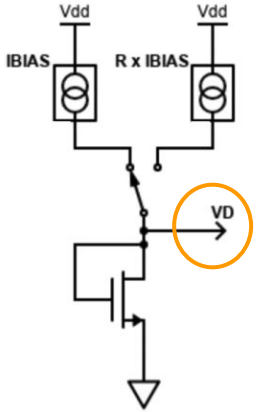
The voltage difference VD shows a Complementary-To-Absolute Temperature variation.

$$T = \Delta VD \times q / (Nf \times kB \times \ln(R))$$

Read from VMUX

R=15 fixed ratio

ideality factor from wafer probing



Precision limitations: measurement of the ideality factor Nf.

T measurement results

Results are fairly consistent from different T sensors.

	Ext NTC	Ana. SLDO Mos	Dig. SLDO Mos	ACB center MOS
T (℃)	59.1	67.6	67.7	67.6

```
"AR_TEMP_NTC": 59.1,
"AR_TEMP_EXT": 0.0,
"AR_TEMP_ASLDO": 67.6,
"AR_TEMP_DSLDO": 67.7,
"AR_TEMP_ACB": 67.6,
```

- Compare the measured injection voltages with the DAC settings.
- Obtain the slope and offset, and update **VcalPar** in the chip configuration.

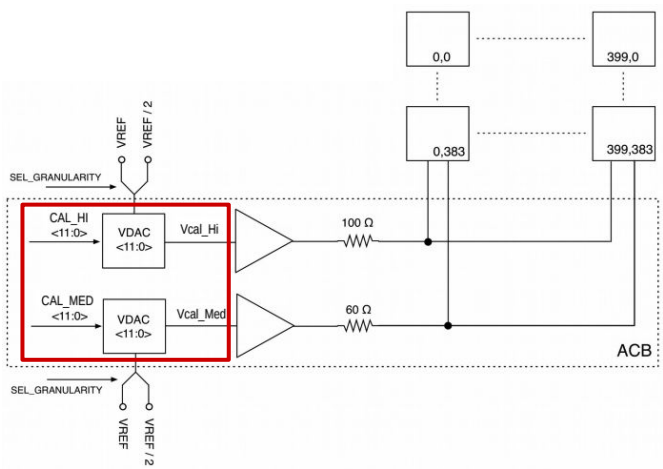
VCal Calibration output

```
"VCAL_HIGH_SLOPE": 0.209,
"VCAL_HIGH_OFFSET": -3.81,
```

→

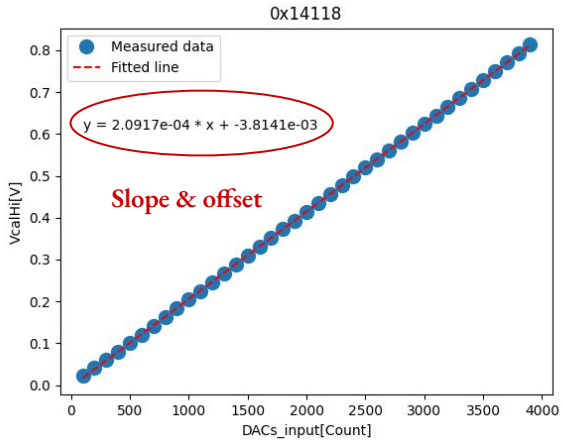
Chip config setting

```
"VcalPar": [ 0.209, -3.81 ]
```



Injection voltage

Generated by digital to analog converters (DACs).



- Measures the capacitance of the front-end injection capacitor.
- Update **InjCap** in the chip configuration to the output of the analysis.

Injection Capacitance output

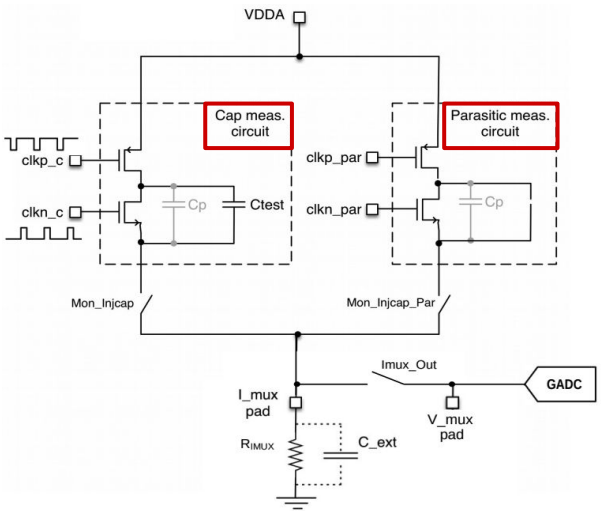
"INJ_CAPACITANCE": 7.407

→

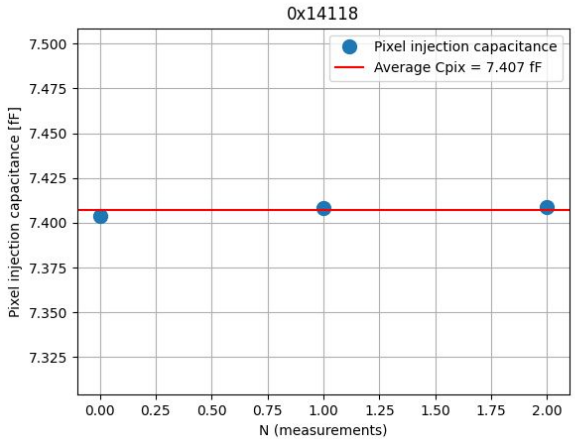
Chip config setting

"InjCap": 7.407

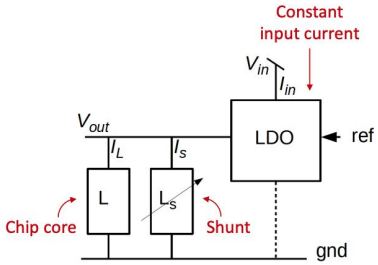
But wafer probing measures ~ 8fF!

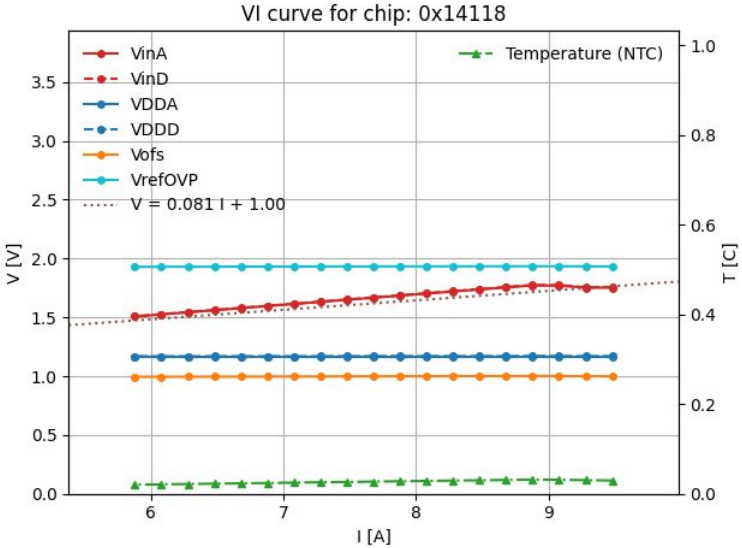


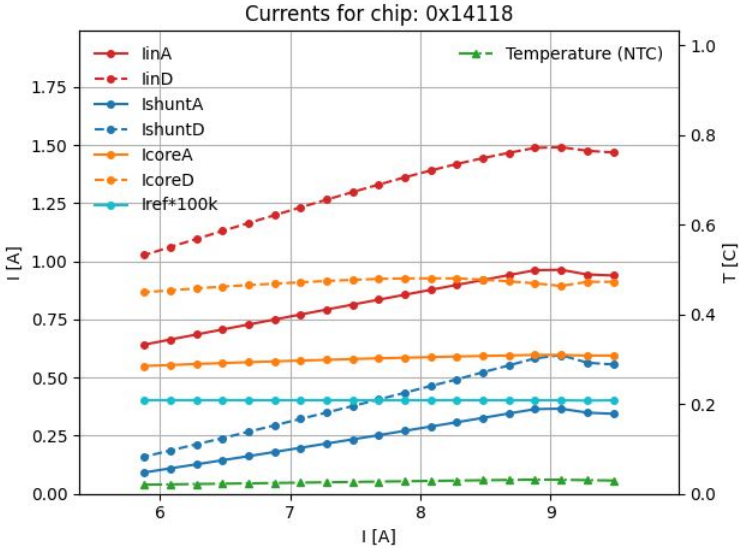
Capacitance measurement circuit



- Provides constant current operation with multiple chips connected in parallel.







Summary

- We released V1.
- We got feedback from users.
- It's working.
- We are still developing and adding new features, scans, and tests.

Backup

Workflow

Test 1

Measurement → (Output) → Raw data (json file) → (Input) → Analysis → (Update) → Chip config

update_chip_config.py

cmd:

```
analysis-update-chip-config -i <path/to/analysis/output/directory> -c <path/to/YARR/config/directory>  -t <config-type>
```

```
|__ Analysis
    |__ <test_name>
    |__ VCAL_CALIB
        |__ <timestamp>
            |__ <chip_name/module_serial_number>.json
            |__ <sym link to measurement>
```

The script identifies the test type from the -- input-dir, and updates the corresponding chip settings in the Yarr config.

Workflow

Test 1

Measurement → (Output) → Raw data (json file) → (Input) → Analysis → (Update) → Chip config

update_chip_config.py

cmd:

```
analysis-update-chip-config  -i <path/to/analysis/output/directory> -c <path/to/YARR/config/directory> -t <config-type>
```

config-path

config-type

```
<modulde_uid>
|__ <modulde_uid>_<tag>.json
|__<tag>
    |__ <chip_uid1>_<tag>.json
    |__ <chip_uid2>_<tag>.json
    |__ <chip_uid3>_<tag>.json
    |__ <chip_uid4>_<tag>.json
```

Yarr config directory contains the chip configs for all chips in a quad module. The script searches through the output files from the analysis according to the chip serial number to update the config settings.

```python
test_type = self.get_test_type()
if test_type == "ADC_CALIBRATION":
    self.set_ADCcalPar(chip_data, config_file)
elif test_type == "ANALOG_READBACK":
    self.set_trim(chip_data, config_file)
elif test_type == "VCAL_CALIBRATION":
    self.set_VcalPar(chip_data, config_file)
elif test_type == "INJECTION_CAPACITANCE":
    self.set_InjCap(chip_data, config_file)
else:
    raise KeyError(
        f"No test type found in the input directory {self.input_path}! Please check the input path."
    )
```

/module_qc_analysis_tools/src/module_qc_analysis_tools/cli/update_chip_config.py