The Microelectronics Initiative and the HEP Community

An opportunity for cutting-edge use-inspired research on technologies of interest for HEP

A. Dragone,

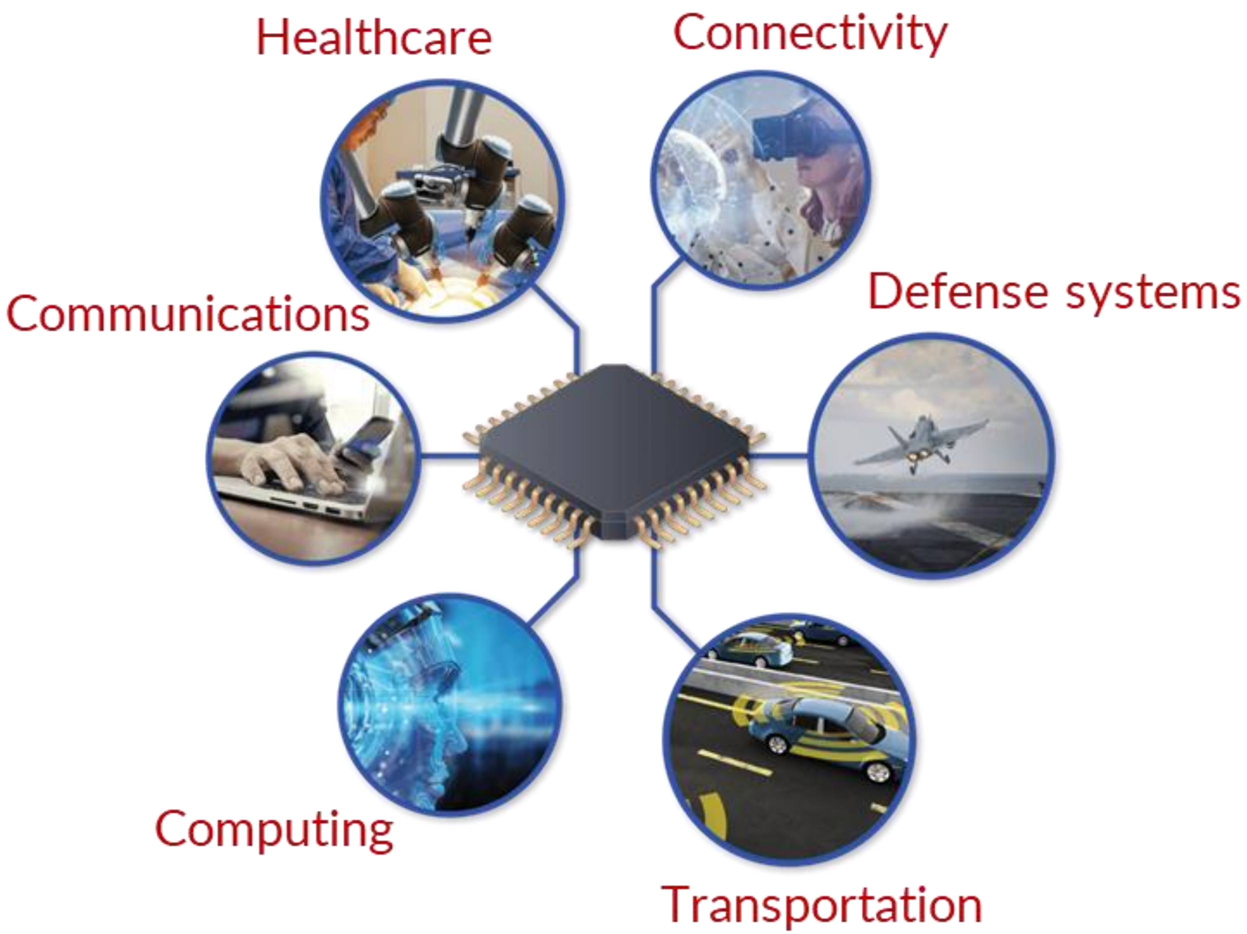
22 February 2023

P5 Town Hall - LBNL

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

U.S. and the Semiconductor Industry



- Semiconductors are critical to the U.S. economy, national security, and technology leadership.

- The current shortage of chips highlights the vital role of semiconductors throughout the entire economy – including aerospace, automobiles, communications, defense systems, information technology, manufacturing, medical technology, and countless others, including instrumentation for our experiments

The U.S. semiconductor leadership is at risk

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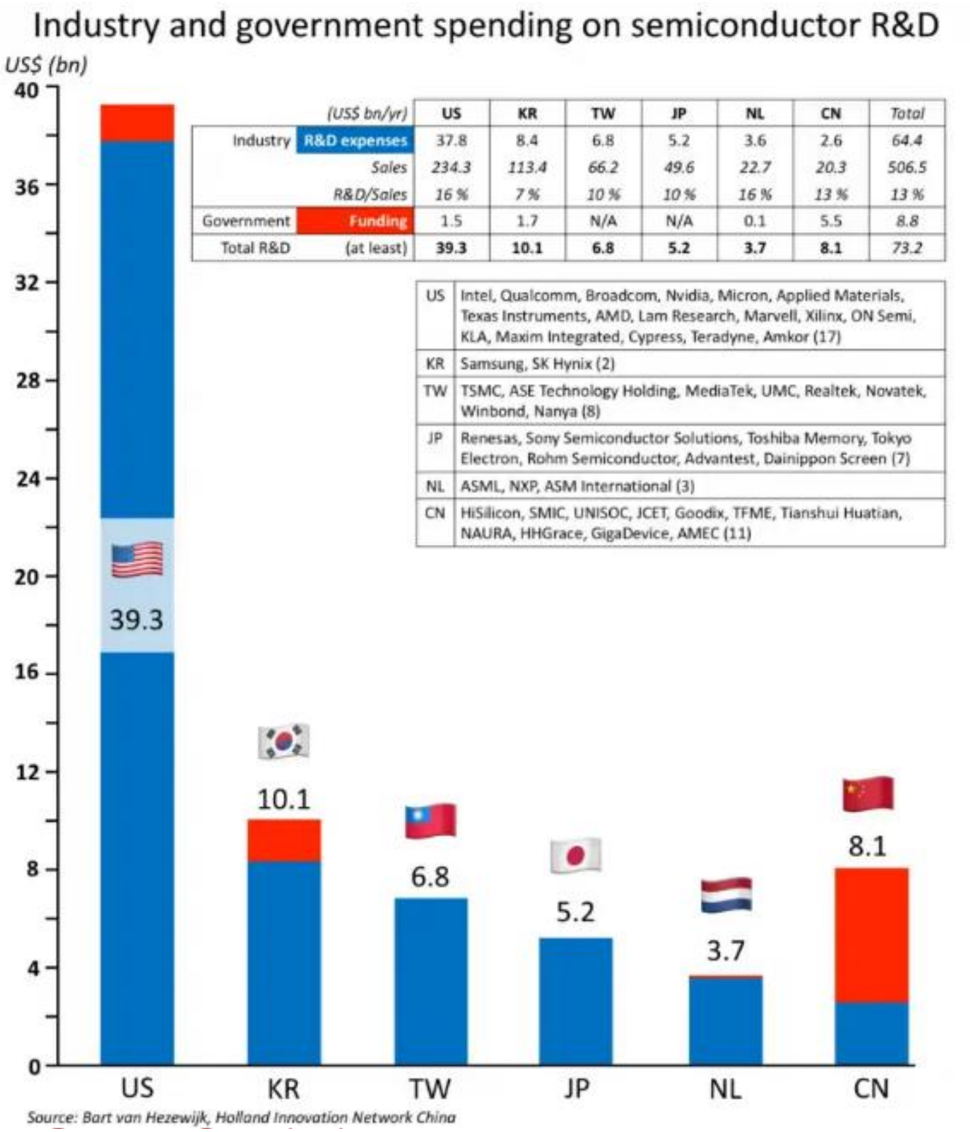


Industry and government spending on semiconductor R&D

	(US$ bn/yr)	US	KR	TW	JP	NL	CN	Total
Industry	R&D expenses	37.8	8.4	6.8	5.2	3.6	2.6	64.4
	Sales	234.3	113.4	66.2	49.6	22.7	20.3	506.5
	R&D/Sales	16 %	7 %	10 %	10 %	16 %	13 %	13 %
Government	Funding	1.5	1.7	N/A	N/A	0.1	5.5	8.8
Total R&D	(at least)	**39.3**	**10.1**	**6.8**	**5.2**	**3.7**	**8.1**	73.2

US	Intel, Qualcomm, Broadcom, Nvidia, Micron, Applied Materials, Texas Instruments, AMD, Lam Research, Marvell, Xilinx, ON Semi, KLA, Maxim Integrated, Cypress, Teradyne, Amkor (17)
KR	Samsung, SK Hynix (2)
TW	TSMC, ASE Technology Holding, MediaTek, UMC, Realtek, Novatek, Winbond, Nanya (8)
JP	Renesas, Sony Semiconductor Solutions, Toshiba Memory, Tokyo Electron, Rohm Semiconductor, Advantest, Dainippon Screen (7)
NL	ASML, NXP, ASM International (3)
CN	HiSilicon, SMIC, UNISOC, JCET, Goodix, TFME, Tianshui Huatian, NAURA, HHGrace, GigaDevice, AMEC (11)

Source: Bart van Hezewijk, Holland Innovation Network China

Research and Development challenges

- To maintain global technology leadership, the U.S. semiconductor industry invests approximately 16% of revenue in research.

- Government funding generally supports lower TRL discovery and high-risk/high-reward research compared to industry R&D funding. The low US government funding of this sector over the past few decades has reduced our capacity to launch and sustain new research directions related to semiconductors.

- To ensure U.S. leadership in future technologies, the U.S. needs to increase its investments in semiconductor research.

Opportunities

CHIPS Act – $52B package to revitalize U.S. Semiconductor Industry and support for R&D on advanced manufacturing and sustainability, Metrology, Energy efficiency, and workforce training

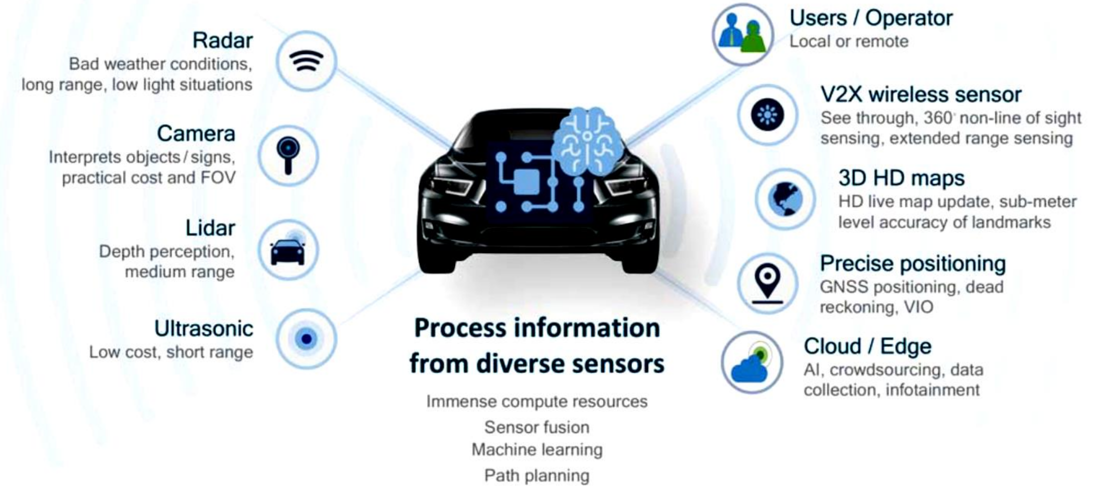
- DOC Research and Development (“R&D”): $11 billion for DOC research and development. authorized and appropriated
  - National Semiconductor Technology Center (“NSTC”): Advanced semiconductor manufacturing R&D and prototyping, expand workforce training and development opportunities.
  - National Advanced Packaging Manufacturing Program: A Federal R&D program to strengthen advanced assembly, test, and packaging (“ATP”) capabilities, in coordination with the NSTC.
  - Microelectronics Metrology R&D: A NIST research program to advance measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities.

- CHIPS for America Defense Fund: $2 billion for the DoD to implement the Microelectronics Commons, a national network for onshore, university-based prototyping, lab-to-fab transition of semiconductor technologies—including DoD-unique applications—and semiconductor workforce training. authorized and appropriated
  - 9 Reginal Hubs ($35M/yr, 5+5 years) – Proposal Deadline February 28, 2023

- Micro Act – DoE SC funds for 4 Microelectronics Centers ($25M/yr, 5+5 years) and RD funds at the level of $100M/yr for six years in areas where SC Labs and Institutions could contribute to the Microelectronics industry (material science synthesis and characterization, new devices, circuits and architectures for sensing and operation in extreme environments, computational methods for big data, co-design methodologies for efficiency, translation lab-to-fab by system scaling, workforce development) – authorized not yet appropriated

The 5 key challenges for Microelectronics - SRC Decadal Plan

Smart Sensing	The Analog Data Deluge
Memory & Storage	The Growth of Memory and Storage Demands
Communication	Communication Capacity vs. Data Generation
Security	ICT Security Challenges
Energy Efficiency	Compute Energy vs. Global Energy PRoduction



Radar
Bad weather conditions, long range, low light situations

Camera
Interprets objects / signs, practical cost and FOV

Lidar
Depth perception, medium range

Ultrasonic
Low cost, short range

Users / Operator
Local or remote

V2X wireless sensor
See through, 360° non-line of sight sensing, extended range sensing

3D HD maps
HD live map update, sub-meter level accuracy of landmarks

Precise positioning
GNSS positioning, dead reckoning, VIO

Cloud / Edge
AI, crowdsourcing, data collection, infotainment

Process information from diverse sensors

Immense compute resources
Sensor fusion
Machine learning
Path planning

A world of interconnected devices

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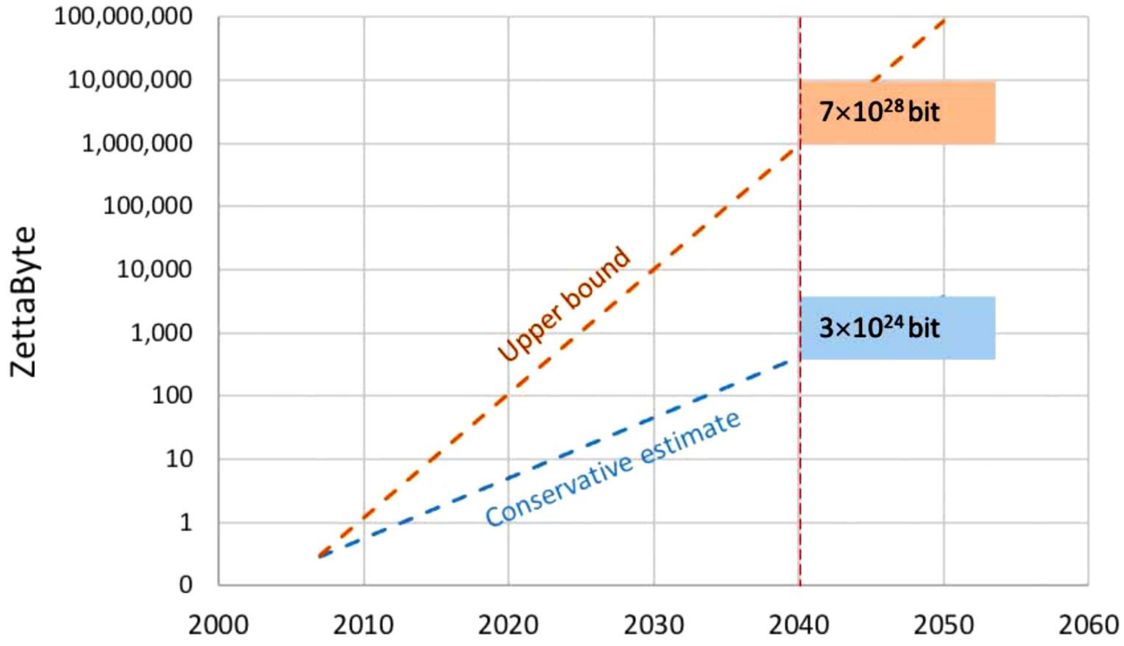

Global demand for memory and storage
(utilizing silicon wafers) is projected to exceed the amount
of global silicon that can be converted into wafers.

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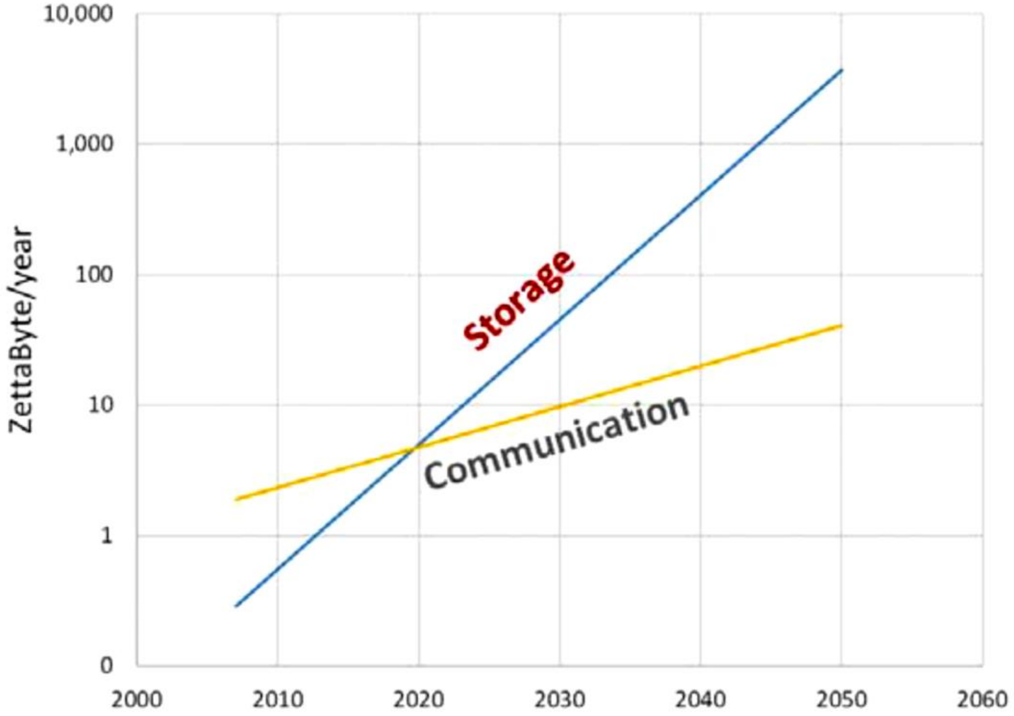


The Global Communication Data Generation Crossover occurs when the data generated exceeds the world's technological information storage and communication capacities creating limitations to transmission of data.

The 5 key challenges for Microelectronics - SRC Decadal Plan

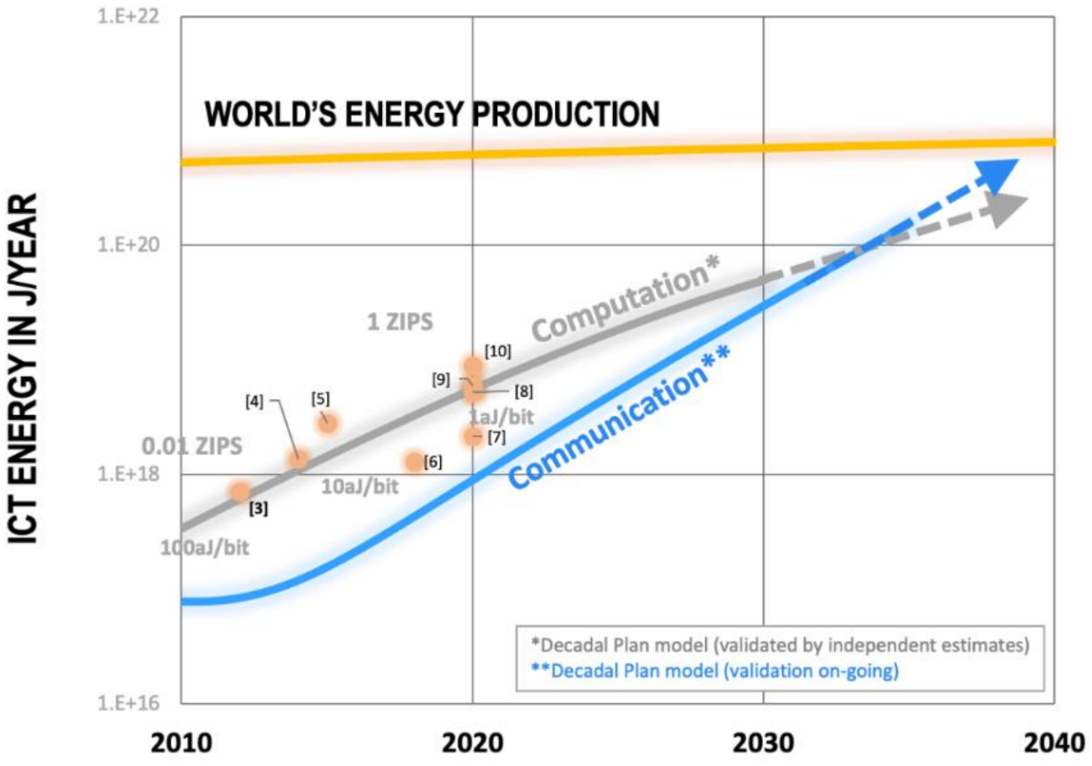
Smart Sensing — The Analog Data Deluge

Memory & Storage — The Growth of Memory and Storage Demands

Communication — Communication Capacity vs. Data Generation

Security — ICT Security Challenges

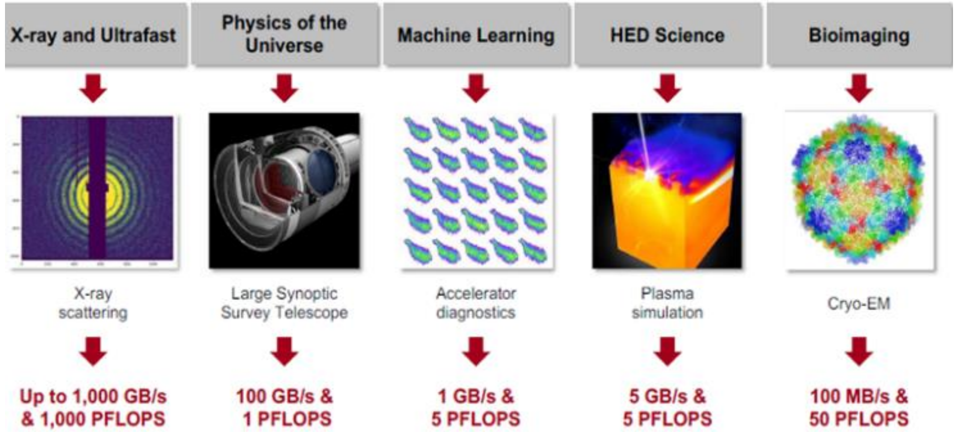
Energy Efficiency — Compute Energy vs. Global Energy PRoduction



Energy consumption trend in computing vs. the world energy production.

The Data Deluge Problem in Scientific Experiments and Beyond

In Science:



X-ray and Ultrafast	Physics of the Universe	Machine Learning	HED Science	Bioimaging
X-ray scattering	Large Synoptic Survey Telescope	Accelerator diagnostics	Plasma simulation	Cryo-EM
Up to 1,000 GB/s & 1,000 PFLOPS	100 GB/s & 1 PFLOPS	1 GB/s & 5 PFLOPS	5 GB/s & 5 PFLOPS	100 MB/s & 50 PFLOPS

Detectors = Network of high precision independent sensing units densely distributed with local and exa-scale computing

e.g., a 2Mpix MHz detector for LCLS would generate 5 Terabytes/s. Equivalent to ~75 Zettabytes/year (assuming 6 months operation per year)

e.g. just 1 detector at HL LHC can produce up to few PB/s data (same rate as average internet traffic in all of North America)

In Society:

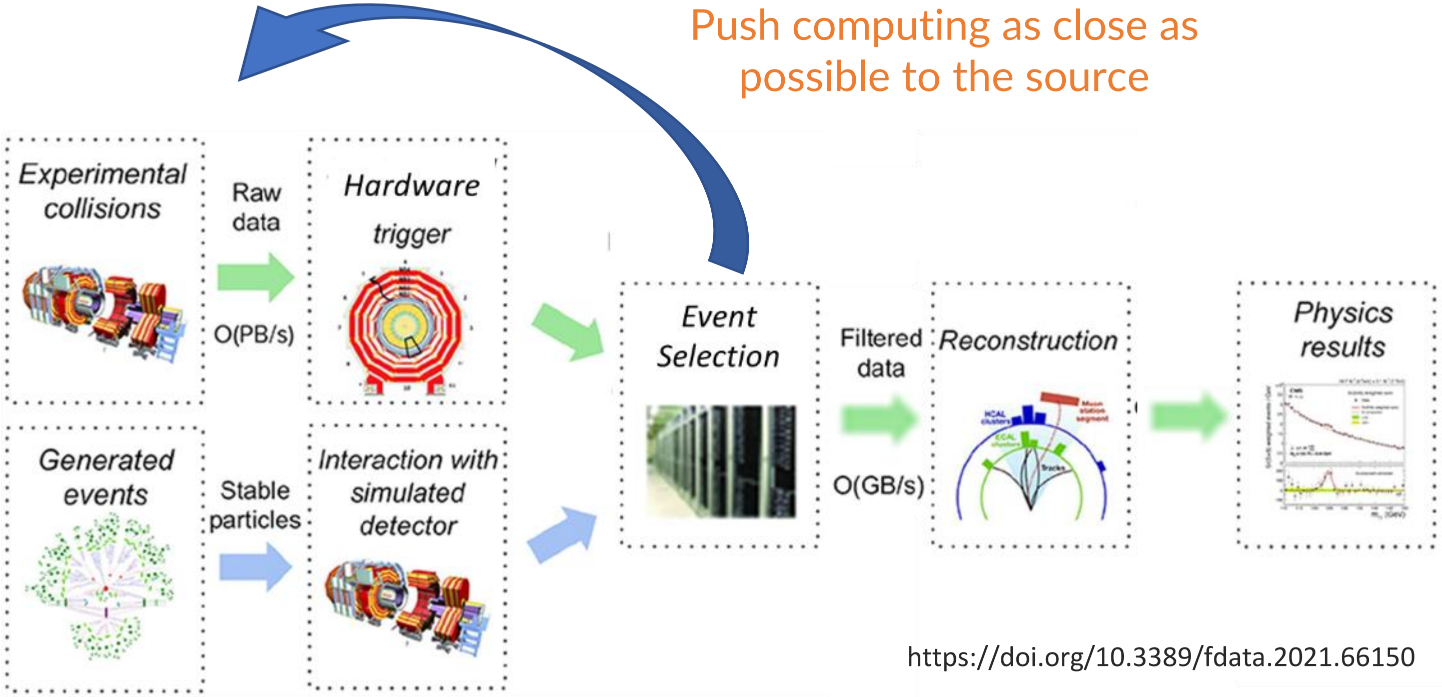
IoT = Network of low precision independent sensing units widely distributed with Cloud computing

> 30 billion connected devices generating ~100 Zettabytes/year

What’s the path forward for HEP?

Pushing microelectronics technology boundaries and add additional design elements to the traditional HEP detector workflow

- Distributed processing for efficiency (energy, information)
- Leverage AI/ML for triggering & data reduction
- Develop adaptive data driven readout architectures
- Develop supporting technology for high bandwidth on detector communication
- Adopt beyond CMOS technologies with heterogenous integration
- Co-design and integration of new materials and devices with standard technologies



Push computing as close as possible to the source

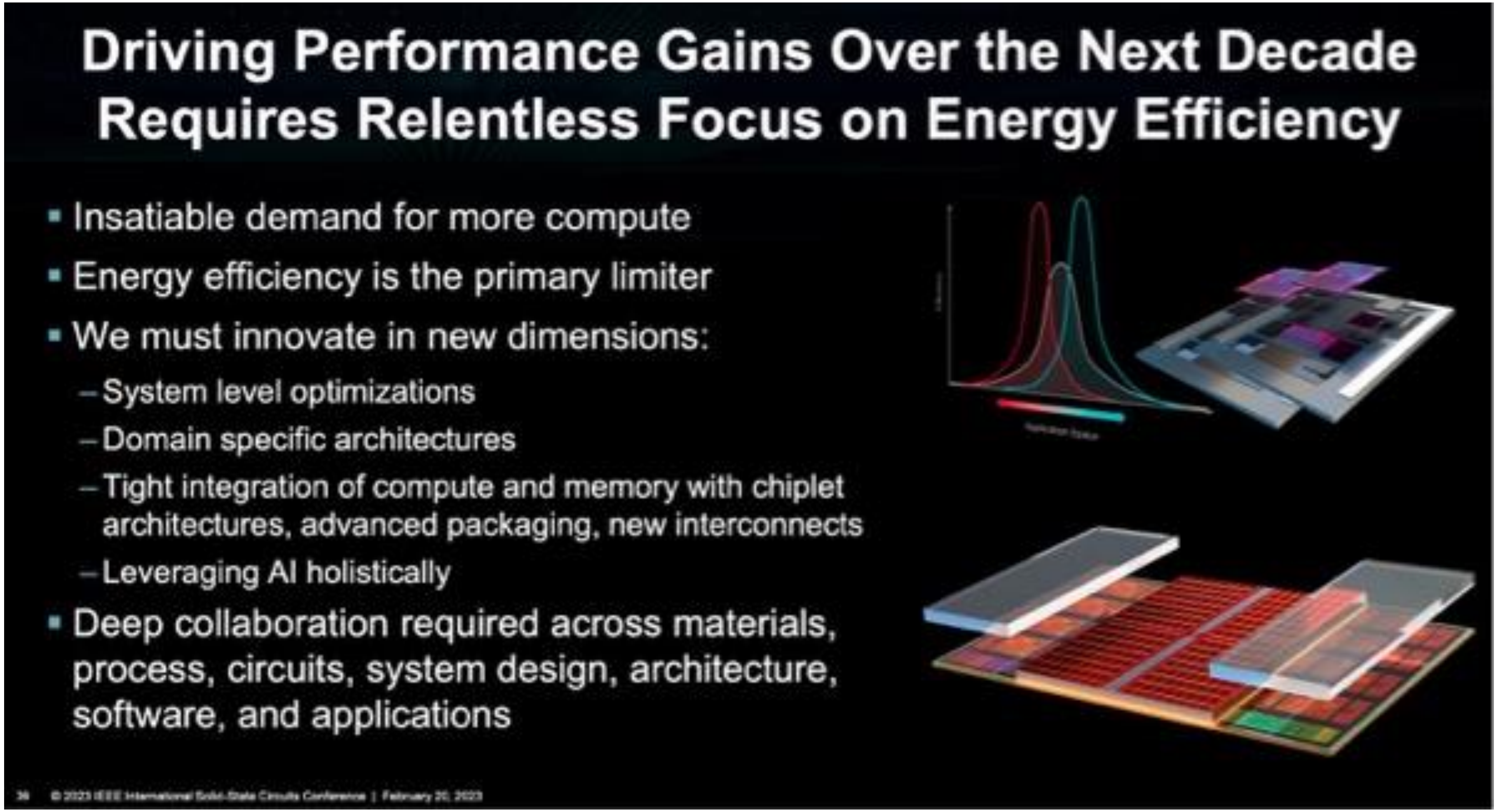
https://doi.org/10.3389/fdata.2021.66150

EL-ASIC **TDAQ** **MIC** **ML**

PRD10, PRD16, PRD17, PRD18, PRD19, PRD20, PRD21, PRD22

Where is industry going?

Lisa Su, CEO of Advanced Micro Devices, keynote speaker at the 2023 IEEE International Solid State Circuits Conference (ISSCC), in San Francisco



Driving Performance Gains Over the Next Decade Requires Relentless Focus on Energy Efficiency

- Insatiable demand for more compute
- Energy efficiency is the primary limiter
- We must innovate in new dimensions:
  - System level optimizations
  - Domain specific architectures
  - Tight integration of compute and memory with chiplet architectures, advanced packaging, new interconnects
  - Leveraging AI holistically
- Deep collaboration required across materials, process, circuits, system design, architecture, software, and applications

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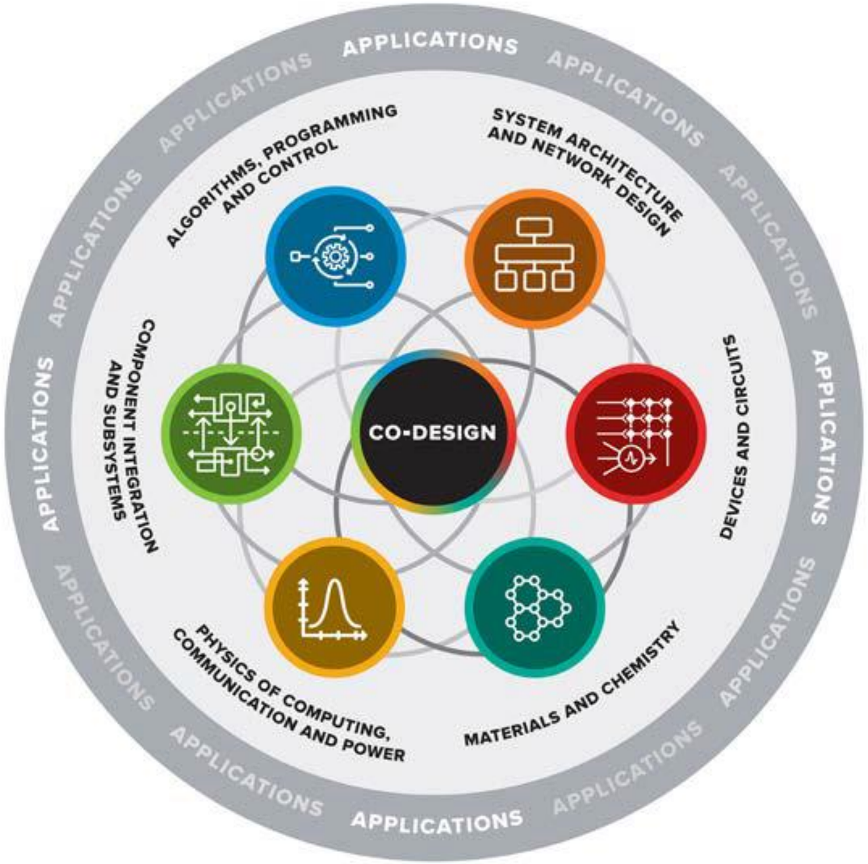
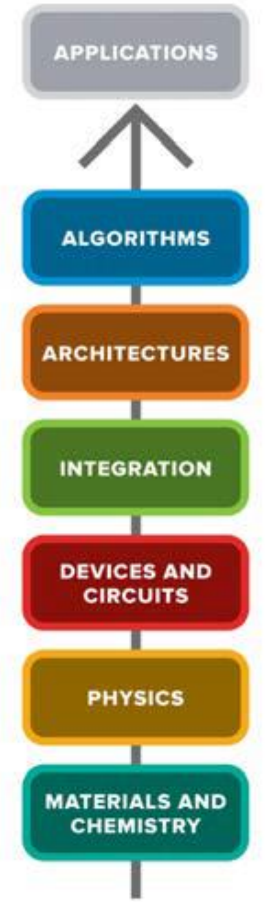
Co-Design as a key principle for Microelectronics R&D





Science

ASCR

HEP, NP Instrumentation

BES, FES

DOE SC has the capabilities to contribute across the entire microelectronics stack including manufacturing

We have been early adopters of new technology and we have prototyping and scaling capabilities

Take away

- Microelectronics Technologies are essential for HEP Detectors and advances are required for HEP future needs.

- HEP can play an important role in driving microelectronics innovation in synergy with industry in particular in the area of microelectronics for sensing, communication and edge computing.
  - We share similar challenges and intend to pursue similar R&D directions in our systems
  - National Labs and their infrastructure can offer prototyping capabilities facilitating lab to fab transition

- Opportunities in Microelectronics can increase foundational (not only applied) R&D on technologies for future experiments
  - Critical given the few generic R&D funding opportunities available in HEP

- Opportunities in Microelectronics can attract and retain workforce in technology fields (currently at risk)
  - Cutting-edge problems feed the passion of microelectronics engineers that are researchers in their own field while serving the HEP mission