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FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades

FE65_P2: a mixed-signal ASIC test chip produced in 65nm CMOS as part of an R&D effort by the RD53 collaboration is presented here.
RD53 was established to design the next generation of readout chips for hybrid pixel detectors to cope with the demanding conditions in the HL-LHC at CERN and implementations of its findings will be used in the ATLAS and CMS detector upgrades.

The FE65_P2 establishes the efficacy of several candidate concepts for the first major prototype in the collaboration, these include:

- A synthesized digital sea with analog 'islands'
- A 50x50 micron pixel matrix
- And more!

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