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HIPSTER: A 24-channel low-noise digitizer ASIC with multi-Gb/s serial data interface

HIPSTER (High-Speed Image Processing System Targeted for Electron Readout) is a noise-optimized digitizer ASIC primarily intended for reading out low-noise, high-speed detectors while reducing physical interconnect. The front end of the ASIC comprises 24 analog channels each with programmable gain and a 12-bit, 75 MS/s ADC. The back end of the ASIC comprises six 4.5 Gb/s serial transmitters that conform to the JESD204B data communications standard. The ASIC also includes an integrated frequency synthesizer to generate the required multi-GHz clocks. HIPSTER was implemented in 180 nm CMOS technology.

Chip functionality has been demonstrated. Performance tuning and evaluation are ongoing.

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