Sensor Creations

Development of a Radiation Hard, Fully Depleted CMOS Monolithic Active Pixel Sensor (MAPS) on 50micron thick High Resistivity Silicon Using SBIR Funding

Stefan Lauxtermann

LBNL Project Presentation, October 1 2015

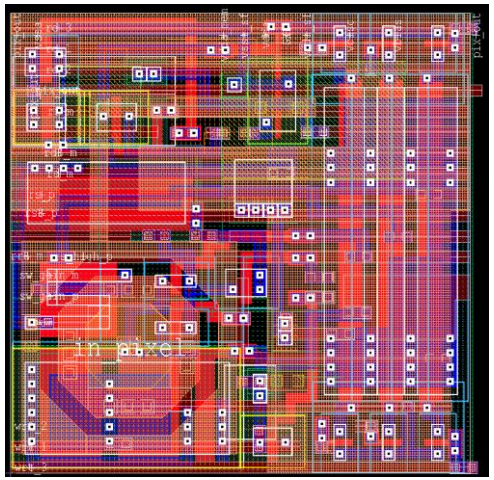
Outline

- About SCI
- SCI' deep depletion process
- Overview of SBIR Project
- SCI camera

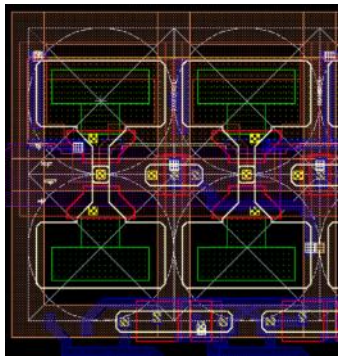
About Sensor Creations, Inc. (SCI)

- Founded by Stefan Lauxtermann in 2010
- Located in Southern California
- Affordable, ROIC and image sensor design
  - Design (in house)
  - Fabrication (through CMOS fab partner)
  - Test (in house)
  - Prototype and low volume packaging (in house)
- Extensive suite of silicon proven IP blocks available today
  - Low noise snapshot shutter pixels with multi frame storage
  - Low noise readout chain programmable
  - Serial interface (SPI)
  - 14bit high speed, low power column parallel ADC (measured)
  - High speed I/O port with 1Gbit/sec (measured)
- Fully depleted backside illuminated CMOS imagers
  - Custom designs
  - Products
- Prototype Cameras

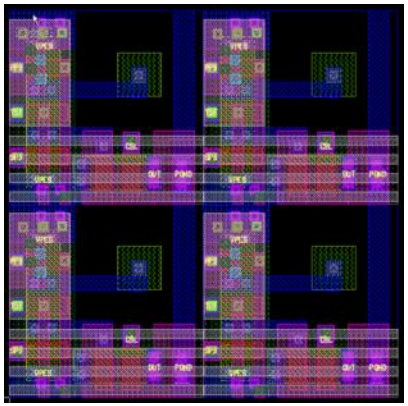
Pixel IP for Monolithic and Hybrid Imagers



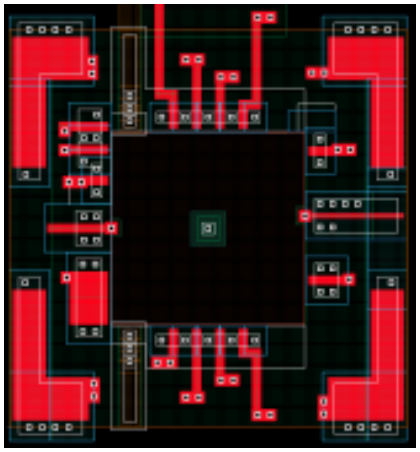
15 µm ROIC Pixel



2.7 µm 4T pixel with CFA and micro lens (FSI, 2x2)



5.8 µm 5T pixel (BSI, 2x2) Test array

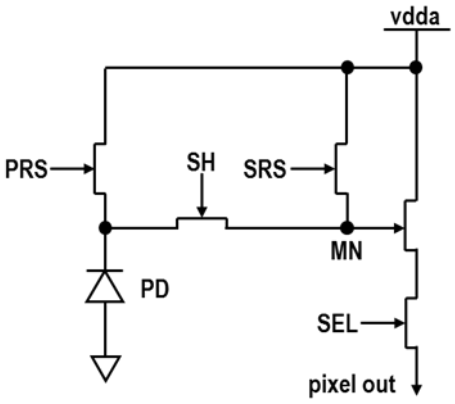


15 µm Mutiframe BSI Pixel

SCI's Custom Pixels Typically Provide Functionality Beyond Classical Intensity Measurement

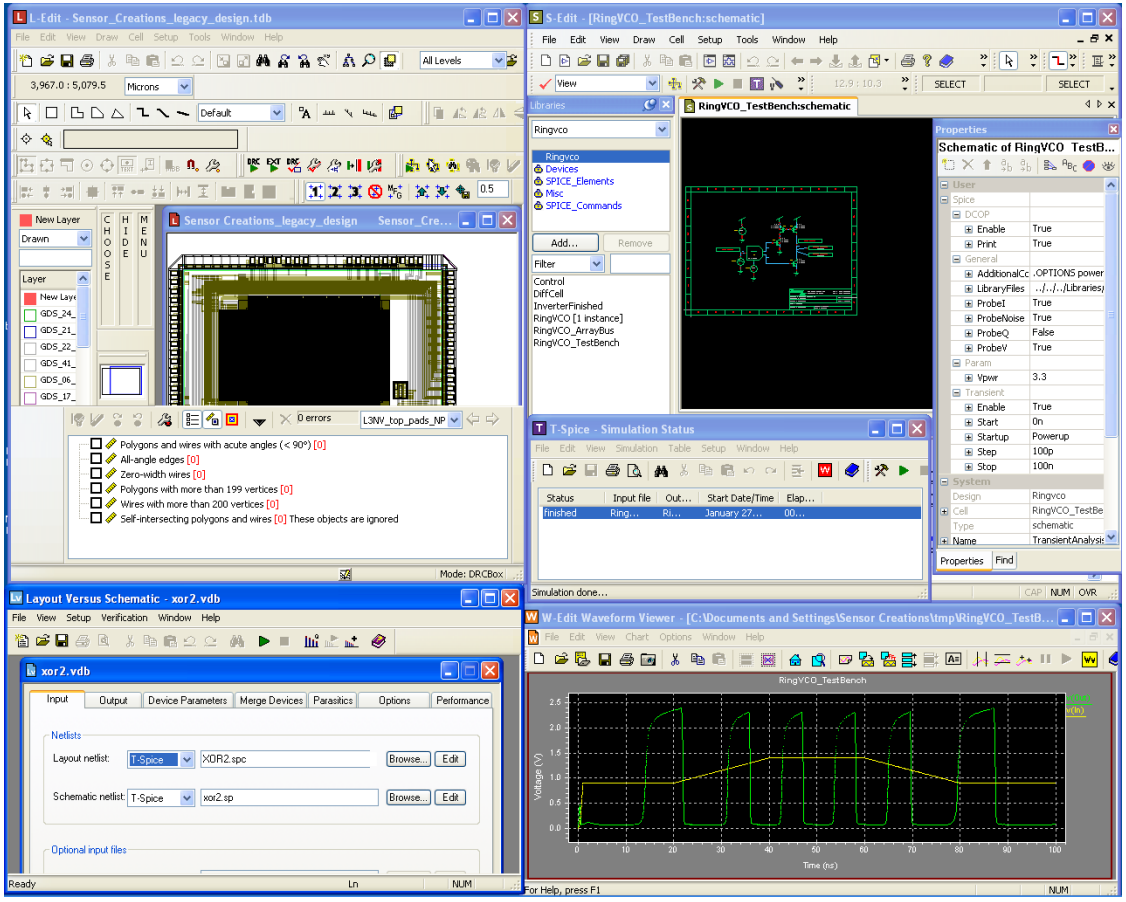
Examples of added functionality:

- Binning
- Multi Frame Sampling
- Signal discrimination
- <100nsec exposure time control

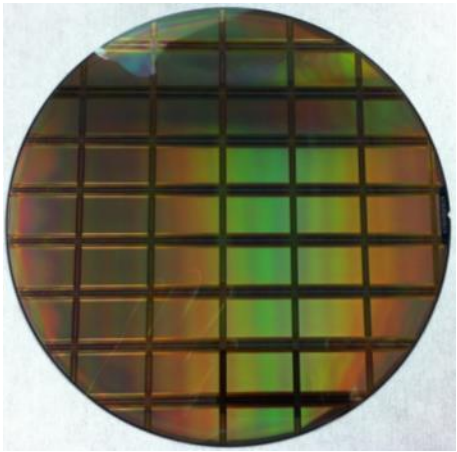


Conventional 5T pixel

SCI uses Tanner EDA Design System



1. Schematic entry
2. Simulation
3. Layout
4. Block level verification
5. 2D/3D parasitic extraction
6. Top level verification



8” wafer with large format ROIC designed by SCI, (MacDougal et al, DSS 2012)

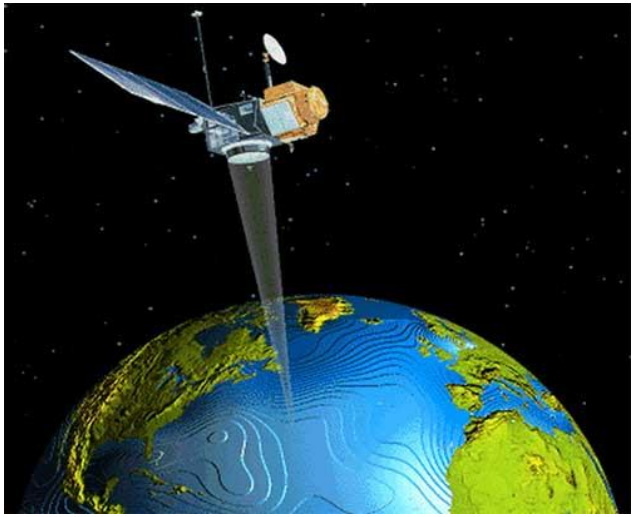
Designs with > 45M Transistors and Layout Area >22 x 32 mm^2 have been realized successfully

Advantages of Deep Depletion CMOS Technology

- High NIR response
  - Up to 40% at λ = 1069 nm (with 500µm thick silicon)
- High UV response
  - > 30% at λ = 300nm
- High broad band response
  - peak QE > 90%
- Direct detection of high energy radiation
  - X-ray < 20k eV
  - MIP (Minimum Ionizing Particle) for tracking
- Suited for very large format arrays
  - High yield compared to Hybrid FPAs
  - High data rate compared to CCD
  - Small pixel pitch (Nyquist MTF: 200µm thick silicon, 100V bias: 4.5µm)
- High Snapshot Shutter Efficiency
- Manufactural in standard CMOS foundry

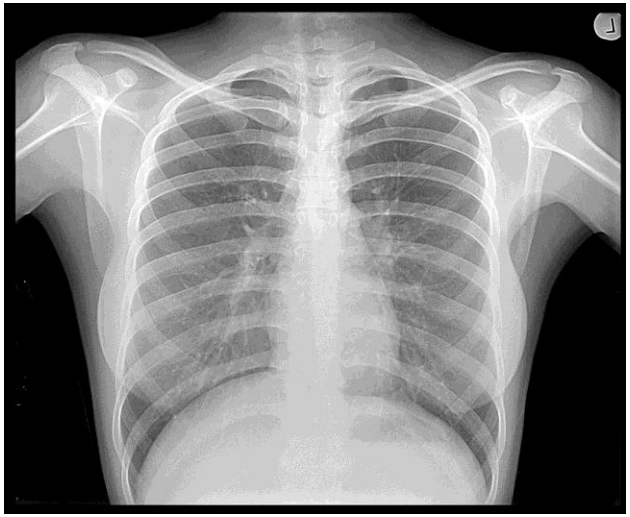
Deep depletion CMOS Imagers Provide Scientific Sensor Performance with a Fabrication Price of a Mobile Phone Camera

Application for Deep Depletion CMOS Imagers

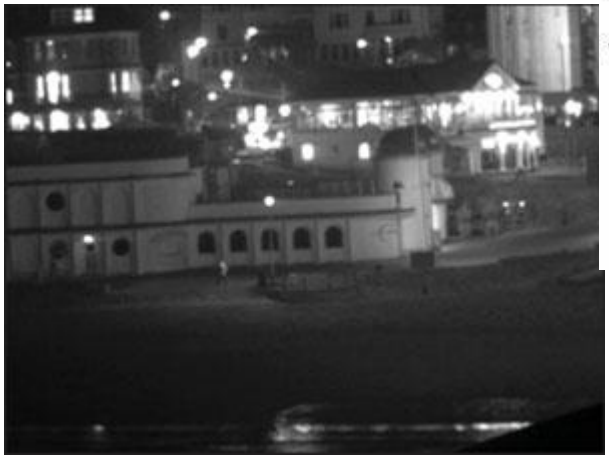


Hyperspectral Imaging in Remote Sensing Applications

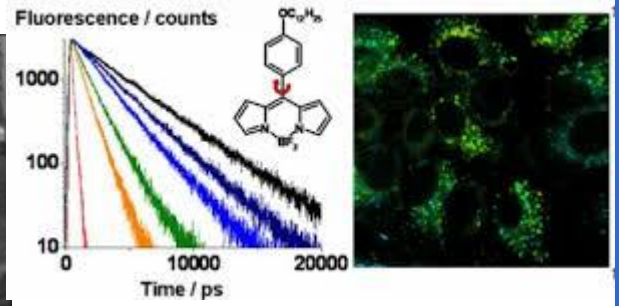
NIR Laser Ranging



Direct X-Ray Detection



NIR Night Vision

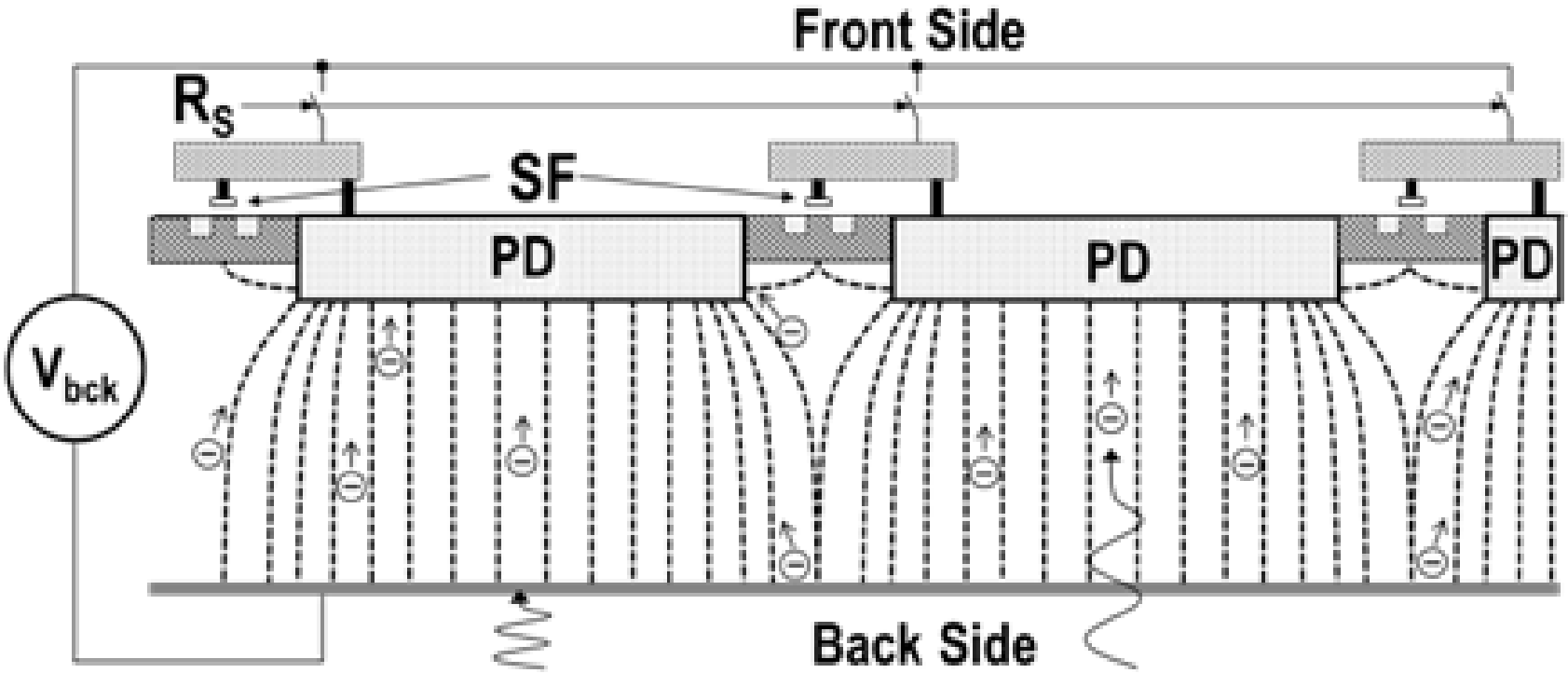


Nsec Fluorescence Lifetime imaging

Benefits of DD-CMOS

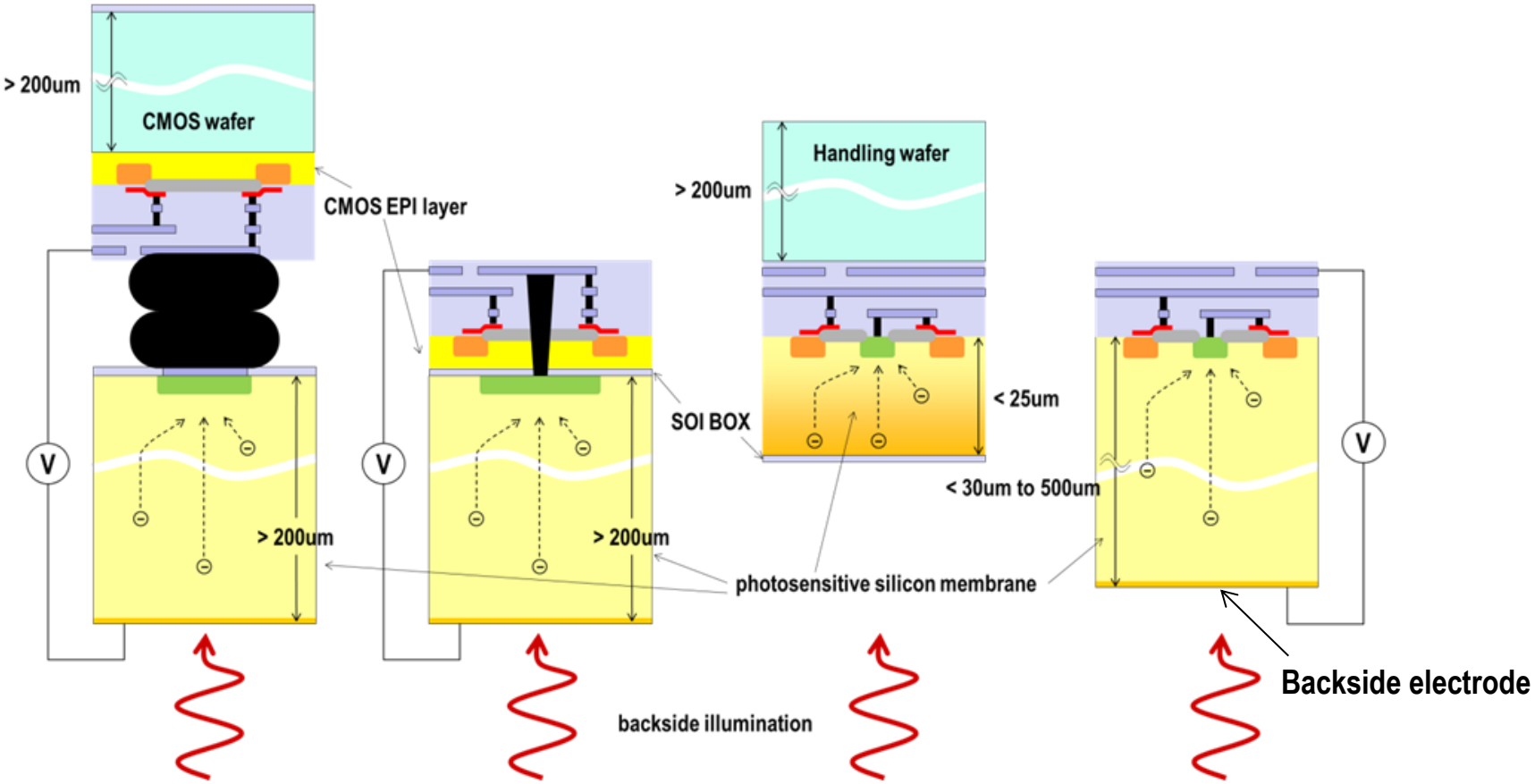
- High NIR sensitivity
- nsec response time
- High X-ray sensitivity
- Low noise at high speed

Cross Section of Fully Depleted CMOS Technology

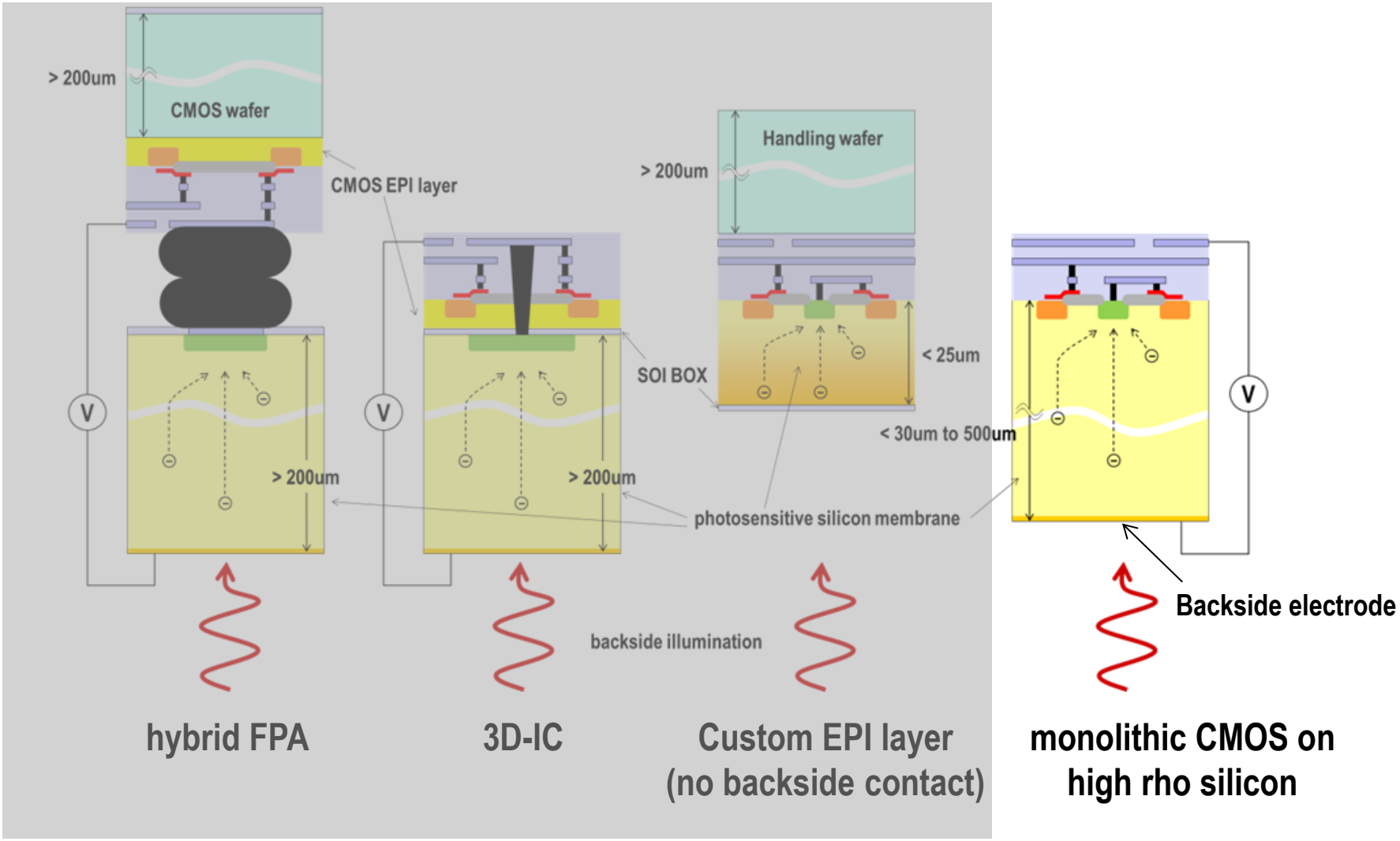


Charge Collection Region Defined by Lateral and Vertical Depletion

Comparison of Deep Depletion MAPS Technology



Comparison of Deep Depletion MAPS Technology



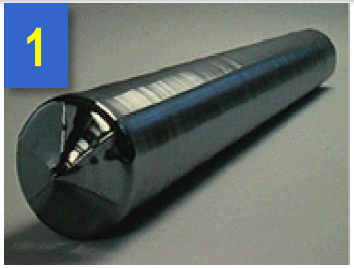
SCI's Approach Combines Excellent Performance with Highest Manufacturability

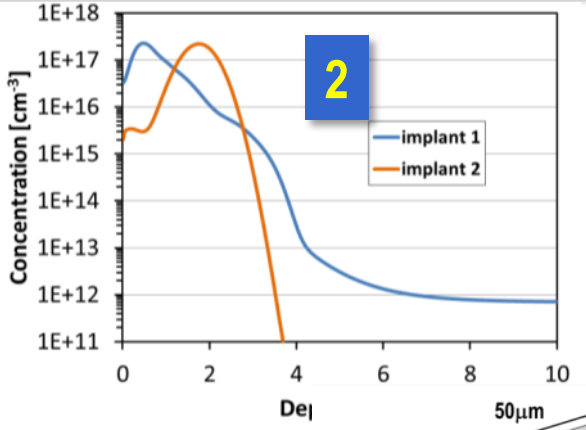
Comparison Summary of MAPS Technologies

	Hybrid FPA (a)	3D-IC (b)	EPI on SOI (c)	SCI technology (d)
Detector material	high ρ_{Si} wafer	high ρ_{Si} wafer	high ρ_{Si} EPI	high ρ_{Si} wafer
Detector thickness	<500 μm	<500 μm	~ 25μm	<500 μm
Backside Electrode	Yes	Yes	No	Yes
Photodiode speed	high	high	medium	high
Volume fabrication	poor	good	good	good
CMOS fab compatibility	poor	medium	good	good
Achievable noise	medium	low	low	low
Volume fabrication cost	high	high	medium	low

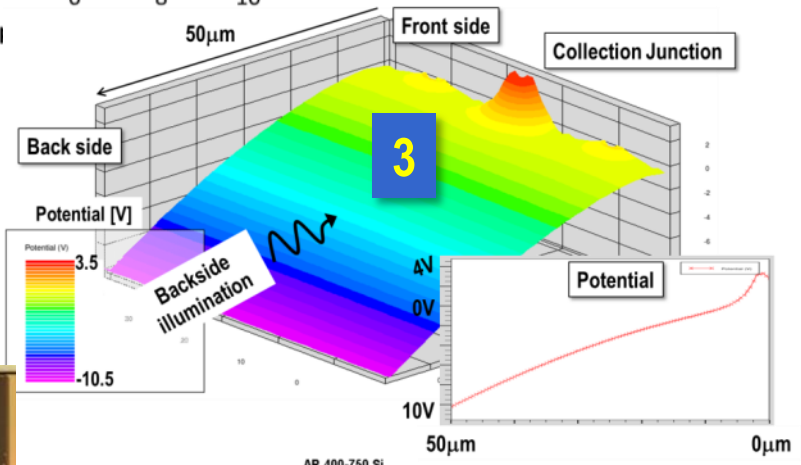
Monolithic MAPS on High Resistivity Bulk Silicon Promise Best Overall Performance but is the Least Developed Technology

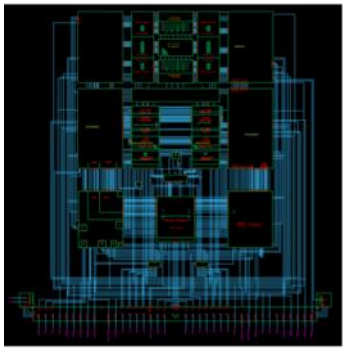
Deep Depletion Sensor Development

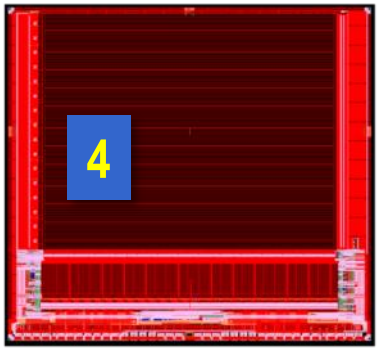




1. Selection of silicon material
2. Development of Process Recipe
3. Verification of Device Functionality
4. IC Design
5. CMOS Fabrication and wafer thinning
6. Definition of AR coating layers on backside

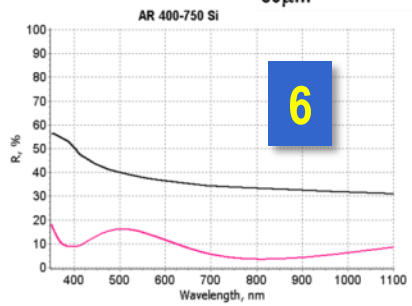



schematic



layout

chip micrograph

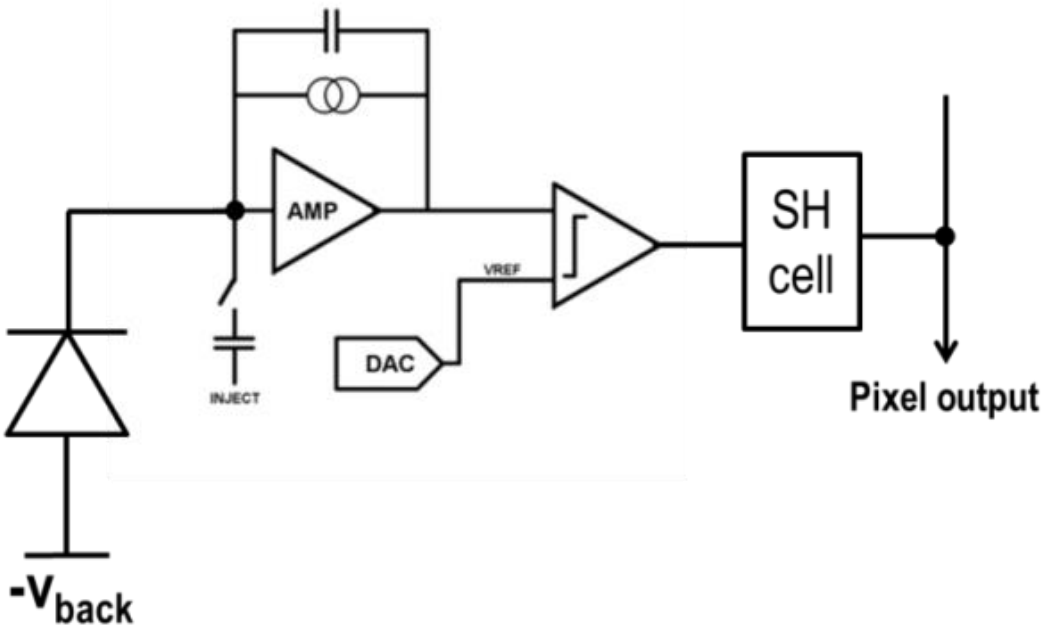


Deep Depletion CMOS Development is a Very Interdisciplinary Effort

SBIR Project Objectives

- Develop active Minimum Ionizing Particle (MIP) detector using one of SCI's Existing Monolithic Deep Depletion Sensors
  - This is the equivalent of a MAPS
- Develop passive MIP detector array in SCI's deep depletion CMOS technology
  - Will be connected to FE-I4 readout for independent verification
- Characterize Detection Efficiency of active and passive detector arrays
  - To be done with 10GeV e^- from SLAC test beam facility (LBNL)
- Propose full size MAPS detector arrays to be developed in phase 2 of the SBIR project

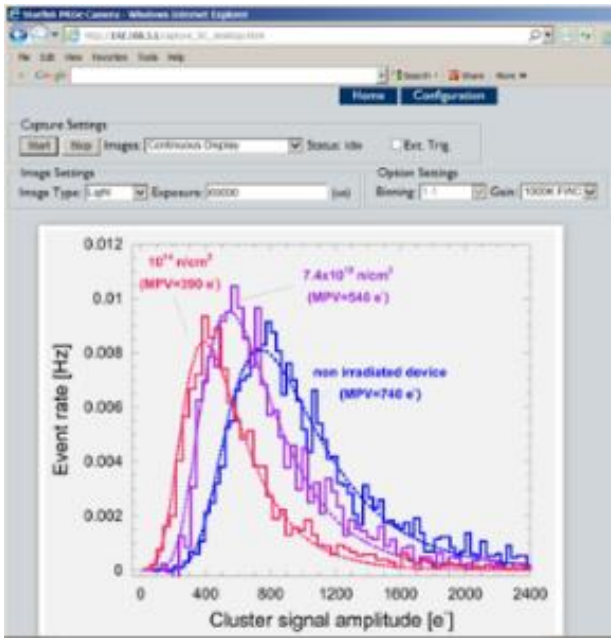
Functionality of Monolithic MAPS



- Charge amplification
- Signal discrimination

MAPS Demonstrator will Provide Functionality of Classical MIP Detector

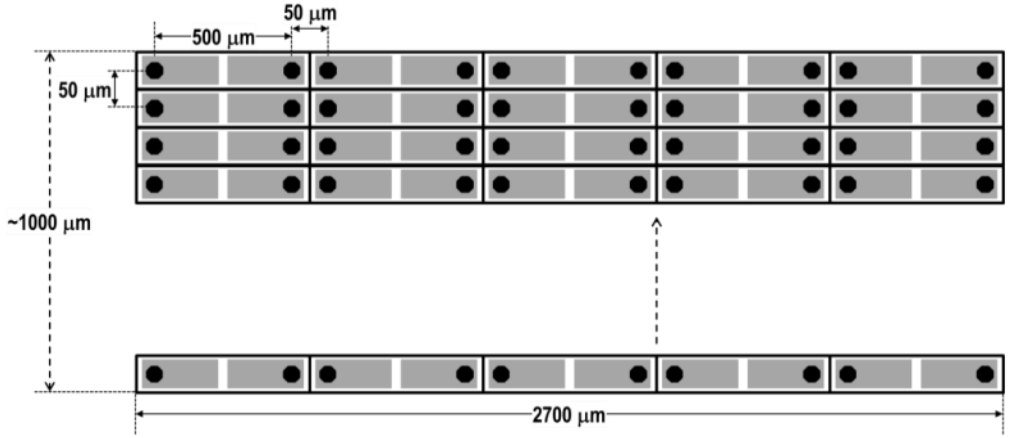
MAPS Detection System



- **SCI technology demonstration camera with deep depletion sensor (left) will be converted into particle detection system**

All Hard- and Software Required for Technology Characterization will be Developed during phase 1 of the SBIR project

Passive Detector Array for FE-I4 Readout



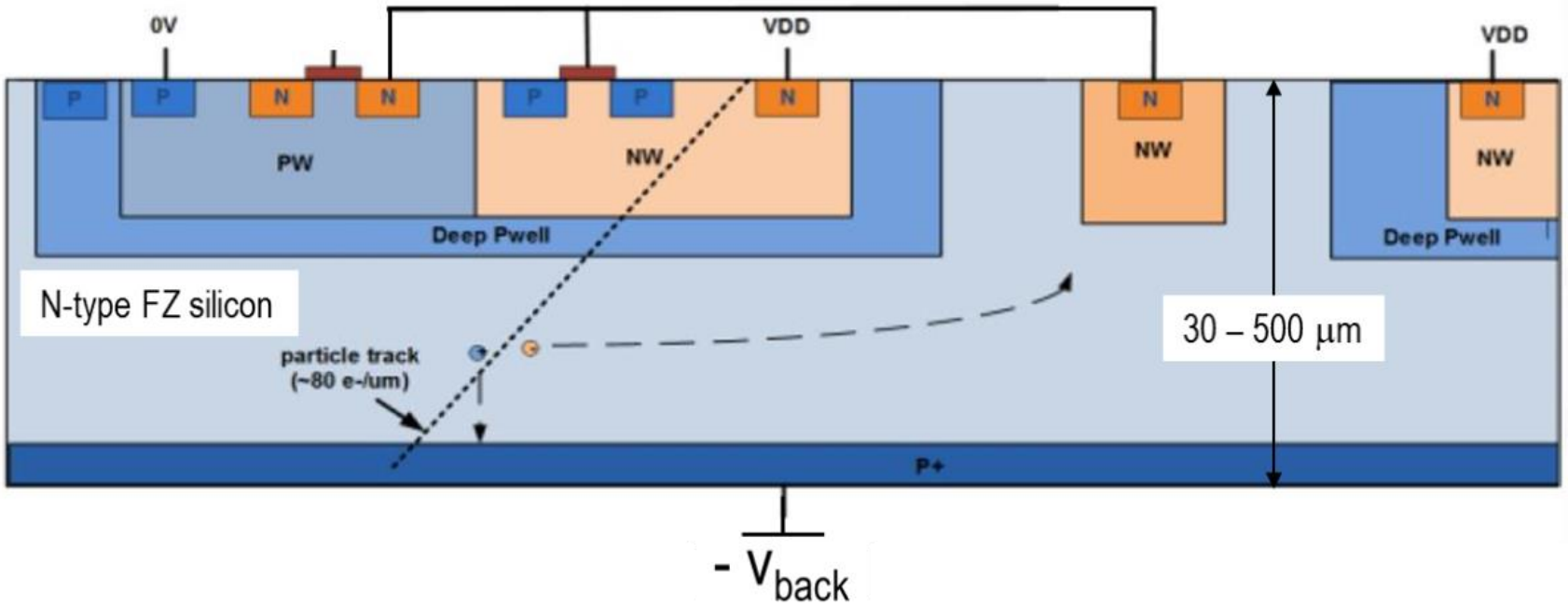
- **Independent verification of SCI's deep depletion technology for MIP particle tracking applications using the well characterized FE-I4 readout system.**

Sensor Performance Aspects of Deep Depletion CMOS Technology can be Characterized Independent of Readout Circuitry

What are the Challenges?

- Thick bulk detector layer must be completed depleted without punch through to backside
- Photodiodes must not short out laterally
  - Note: Electrons are collected in N type material

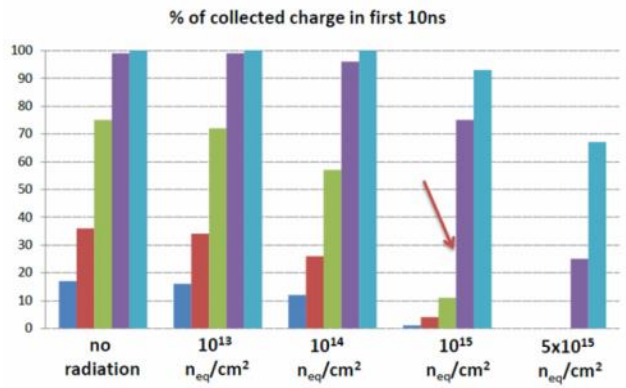
SCI's Deep Depletion CMOS Technology Well Structure



A single deep pwell is used to isolate circuitry from the high resistivity silicon sensing membrane. Electrons are collected very fast by lateral and vertical drift fields.

Deep Depletion Sensor is 3D structure with vertical and lateral Parasitic Bipolar Transistors

Radiation Damage Reduces Detection Efficiency



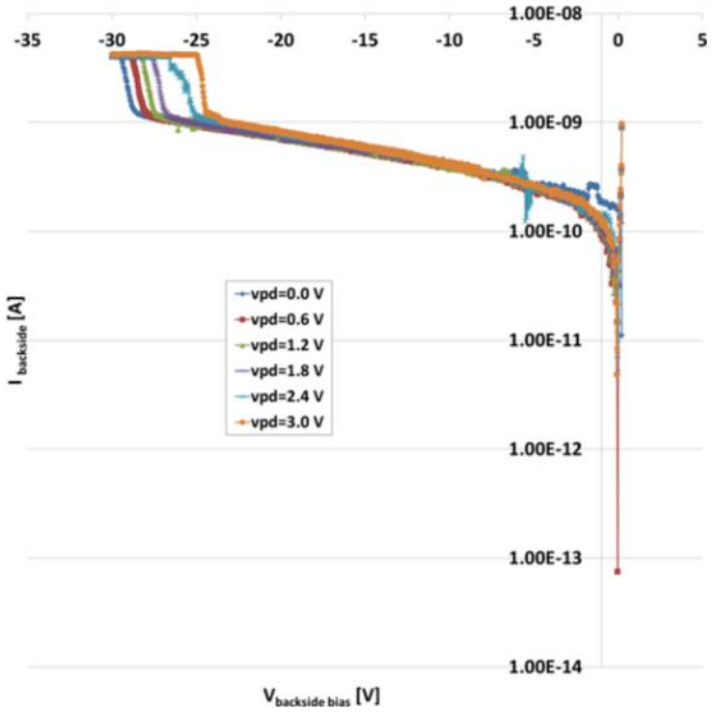
substrate resistivity [Ohm cm]	Bias [V]	Fill Factor [%]
10	1	15
10	20	15
2k	1	15
2k	20	15
2k	20	75

Published by
Tomasz Hemperek
CPIX 2014

Detection Efficiency for a collection time of 10nsec as a function of accumulated neutron irradiation for a 20μm thick detector. Charge Collection decreases with increasing radiation damage but can be compensated in high rho silicon by increasing detector backside bias

MIP Detectors Require High Resistivity Silicon and Backside Bias

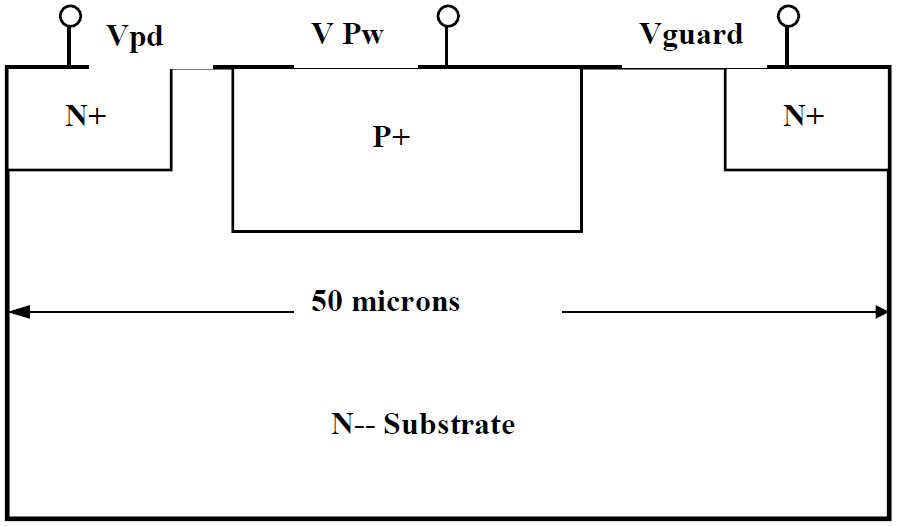
Back to Front Side Detector I-V Characteristic

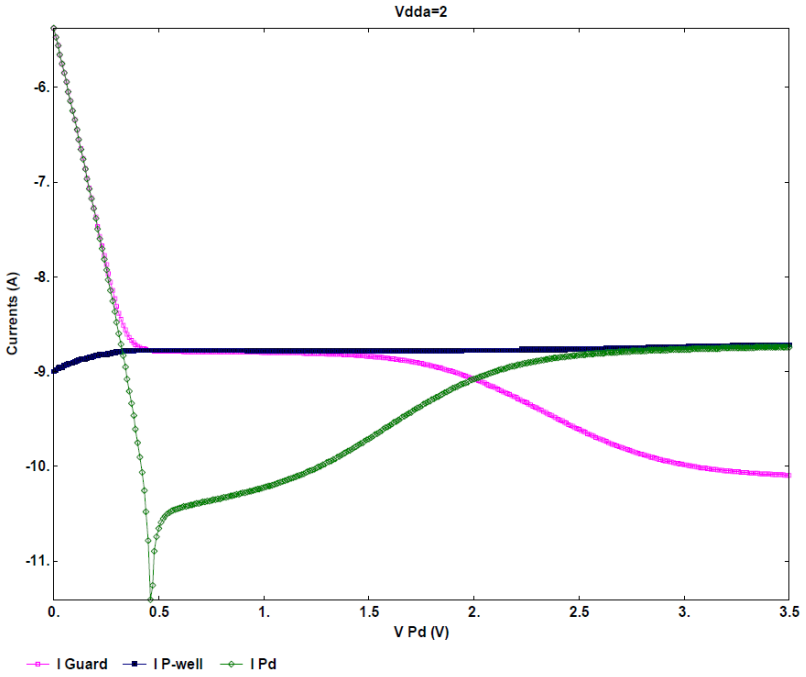


Reverse bias IV characteristic measured on one of our 50 µm thick, 1mm^2 large test structures fabricated in SCI's high rho silicon CMOS process.

Monolithic Detectors Can Be Reverse Biased with < -25V

How to Collect electrons in N-- Substrate?

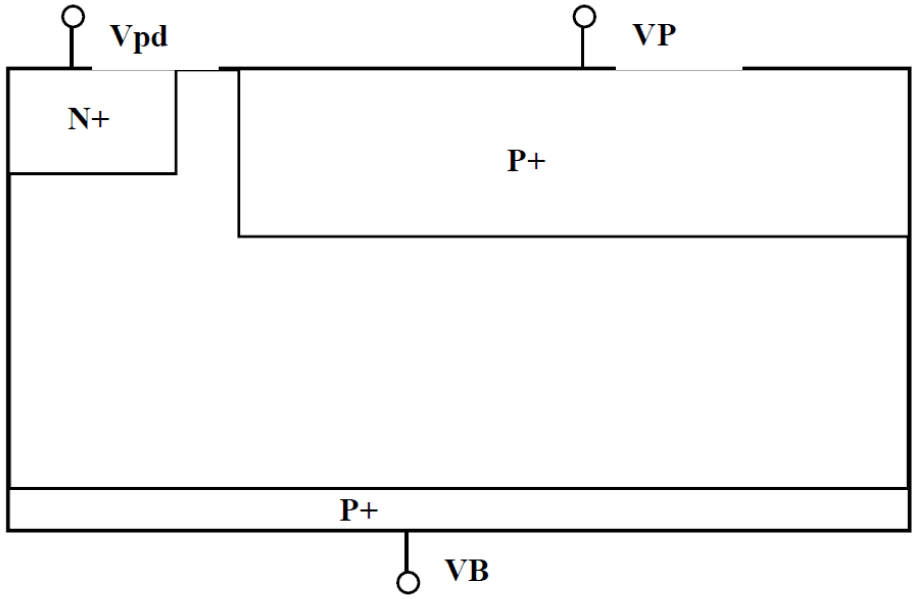


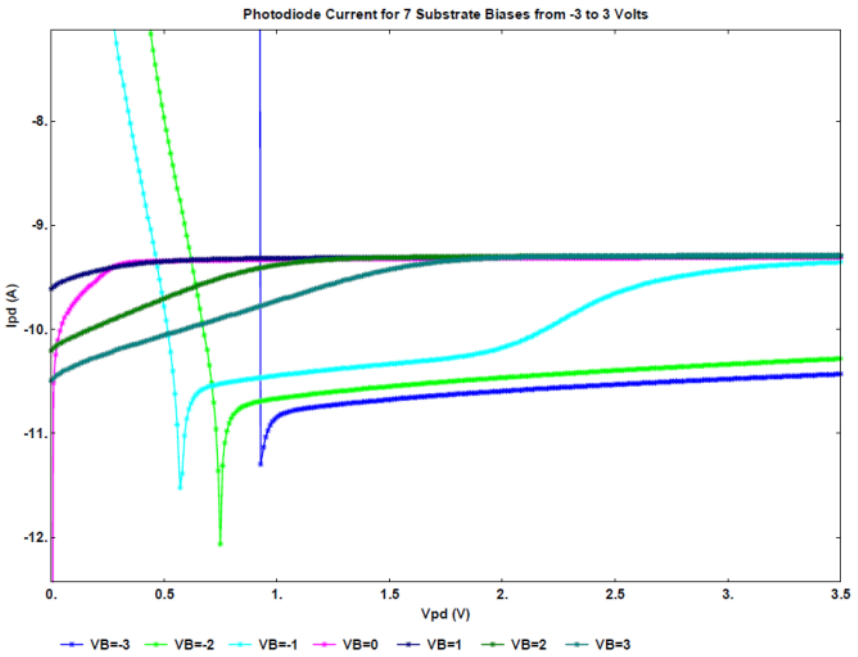


- **Neighboring N^+ regions with different potential can easily short in high rho silicon**

N^+ regions must be Sufficiently Isolated Through Implants or/and Bias to Avoid Lateral Breakdown

Negative Backside Bias Suppressed Lateral Shorts

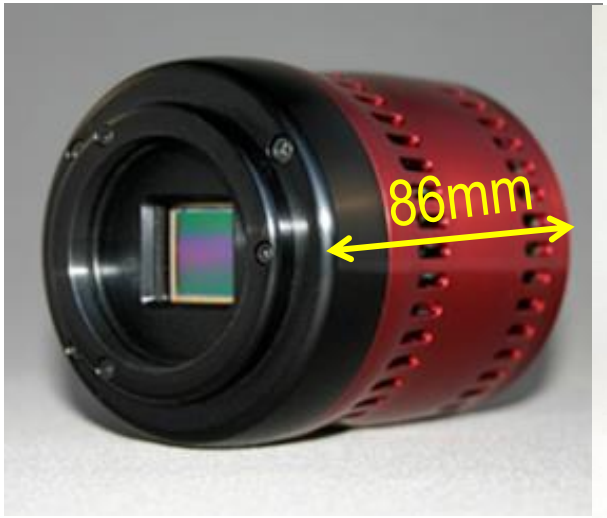




- **Current on IPD decreases when VB is decreased**
  - **Stronger reverse bias decrease of VB is also required to compensate for radiation damage**

Negative Backside Bias Suppressed Lateral Shorts

SCI Deep Depletion BSI Camera

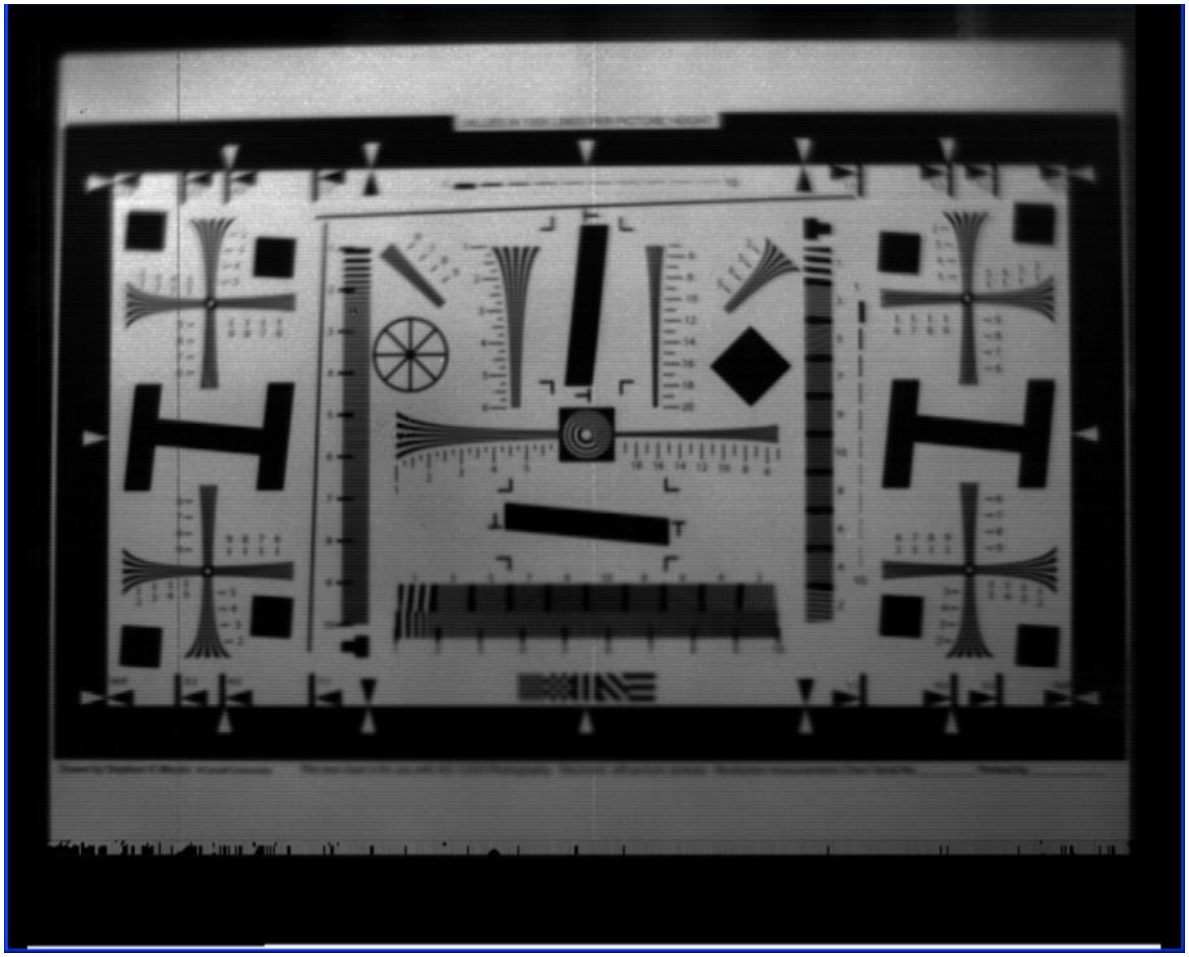


- GigE or WiFi Interface
- C- or F- mount
- CameraLink available upon request
- Internet browser for display and camera control
  - No driver installation required

Sample image taken with this camera (raw data)

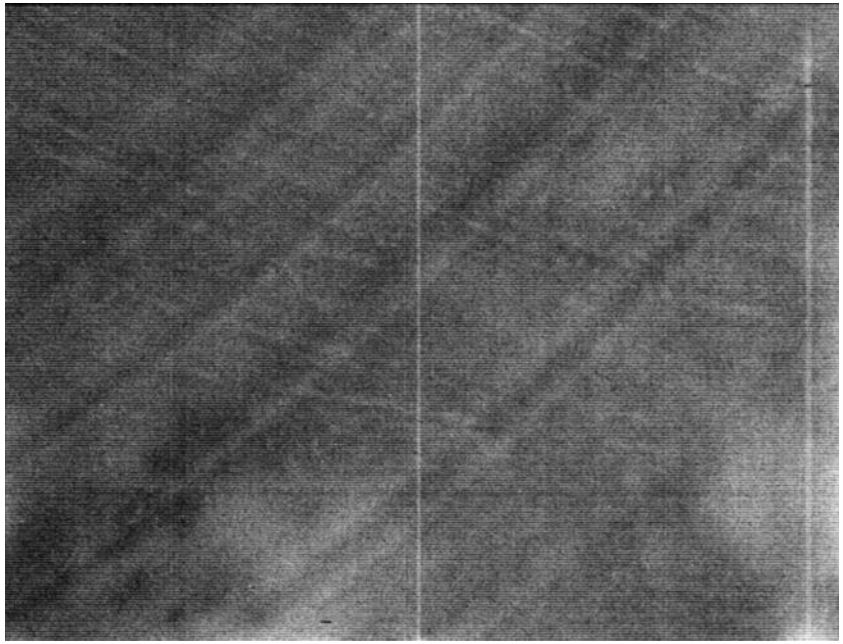
Camera provides easy access to this new image sensor technology for early adopters

First Images, 50um thick sensor – Example 1



- **Correction : 2 point NUC**
- **Integration time: 15.11 msec (66Hz frame rate)**
- **F/#: 5.6**

Phenomenon in Deep Depletion Silicon Sensors



- **Curved line pattern under flat field illumination**
  - **Reported before in deep depletion CCDs → tree rings**
    - **Steve Holland et al., LBNL**
- **Caused by inhomogeneity in silicon resistivity during crystal growth**
  - **Phenomenon in all deep depletion sensors**

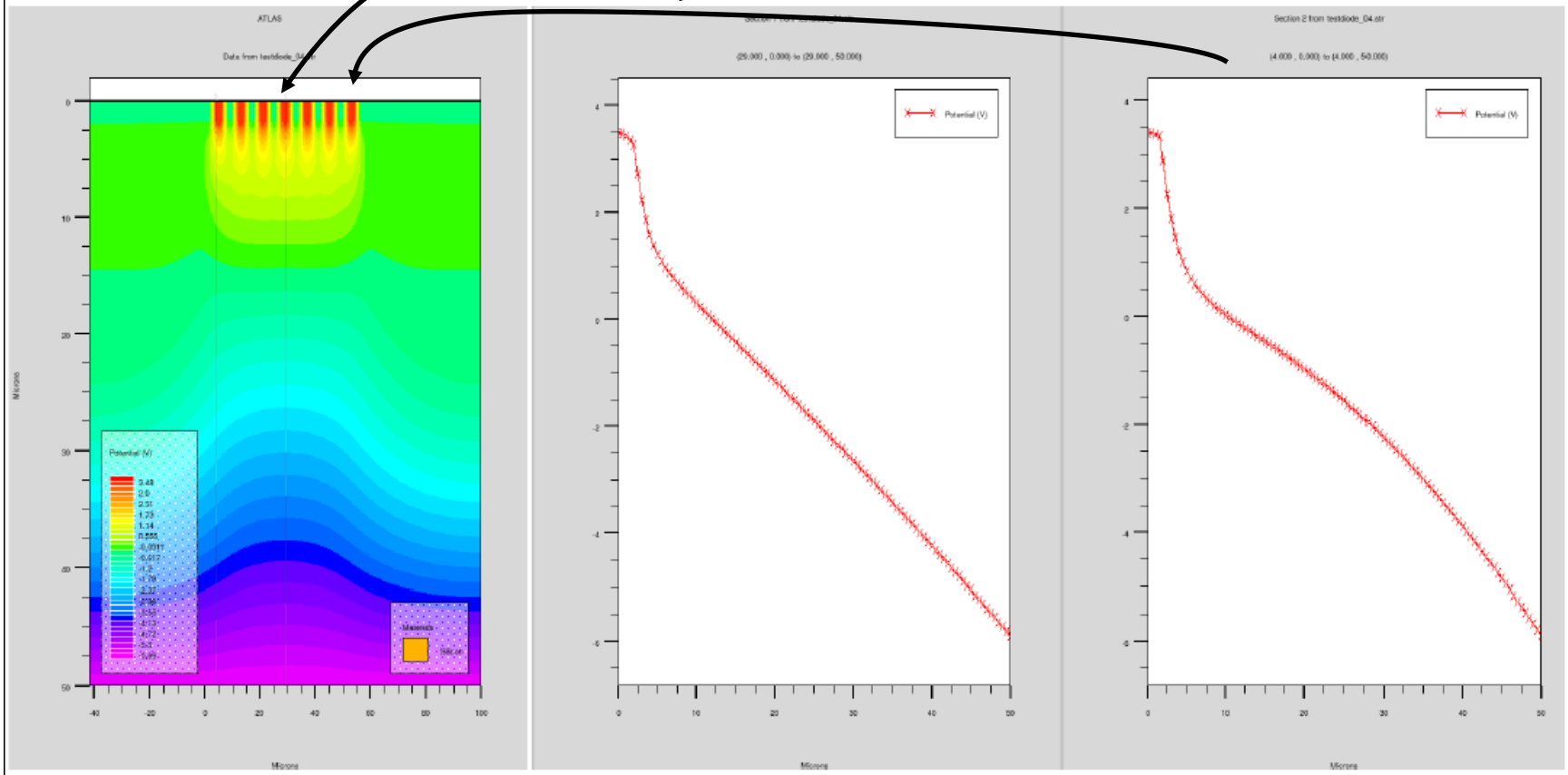
Tree Rings Disappear when Reverse Bias is Increased

Deep Depletion Sensor Camera Performance Targets

Parameter	Value
Array Format	640 X 512
Pixel Size	15 μm
Die Size	11.2 X 12.2 mm^2
Die Thickness	50 μm, 100 μm, 200 μm
Exposure time control	snapshot shutter: ITR, IWR, NDR
Charge Capacity	programmable
minimum	10k e^- (high gain)
medium	60k e^- (high gain)
maximum	500Ke (low gain)
Input Referred Noise	
high gain	10e^-
medium gain	30e^-
low gain	130e^-
Windowing	horizontal center to outsides, bottom to top
minimum	1 rows x 24 columns minium
increments	1 rows, 24 columns
Integration Time range	100nsec to 30 msec
Output	analog (through 1,2, 4 or 8 output ports)
Frame Rate	1000 Hz (when using all 8 output ports)
Output data rate	5MPixel/sec - 41MPixel/sec
Number of output channels	1, 2, 4 or 8 (programmable)
Master Clock	2.5 - 20.5 MHz
Binning	2x2, 2x1, 1x2
Power (120Hz, 60Hz, 30Hz)	60mW @ 60Hz frame rate
Supply voltage	3.3/1.8
Logic I/O levels	0.0V/3.3V
Serial Interface	3 wire (multiple long word of different length)
Operating Temperature	300K

Thank You for your attention!

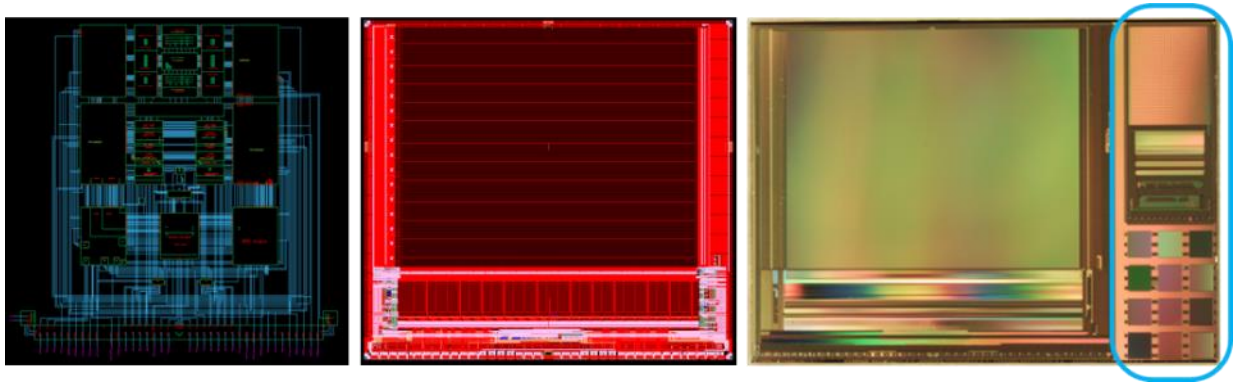
Potential Underneath 50 micron thick Photodiode Array



- **Full Depletion and Pixel isolation on front side achieved**

#	Parameter	Value	Comment
1	Type of Detector	high rho MAPS	Monolithic Active Pixel Sensor (MAPS on high resistivity silicon
2	CMOS process	180nm	this is the technology node but a modified process flow applies
3	Silicon material	FZ	FZ - Float Zone silicon
4	Pixel resolution	50 x 60	equidistant in x and y direction
5	Pixel pitch [μm]	50	this is the pixel to pixel spacing
6	Detector thickness [μm]	50	no support substrate
7	Frame rate [Hz]	100,000	all pixel will be read out, no token based readout
8	Chip size [μm]	3000 x 6600	size is defined by our existing test chip dimensions
9	Output data rate [MPix/sec]	300	data from all pixels will be transferred off-chip, data stream not sparse
10	Clock rate [MHz]	150	output is double data rate (DDR)
11	Supply voltages [V]	1.8, 3.3	CMOS logic at 1.8V; analog circuits and CCD at 3.3V
12	Backside bias voltage [V]	-20	only ~-10 V is required to achieve full depletion
13	Output format	single bit data stream	data from all pixels will be transferred off-chip, data stream not sparse
14	Number of digital output pins	1	CMOS
15	I/O frame	single sided	all pads are arranged along bottom edge of chip over distance of 3000 μm

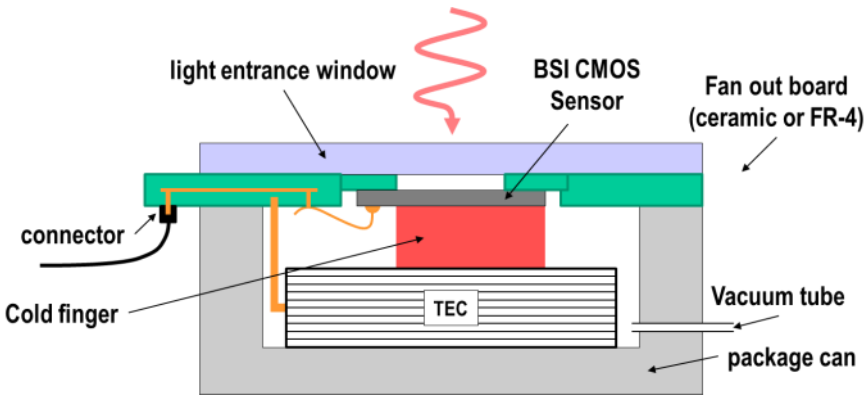
- **Summary of specifications for the proposed SBIR phase 1 MAPS demonstrator**

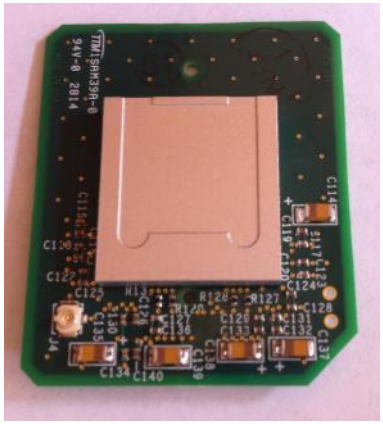


- **Screen shot of top level schematic (left) and layout (middle) of SCI's 640x512 deep depletion CMOS imager. A photograph of the chip cell comprising this imager, a test chip for evaluation of novel pixel designs (top in blue boundary box) and 12 1mm^2 large test**

Thank You for your attention!

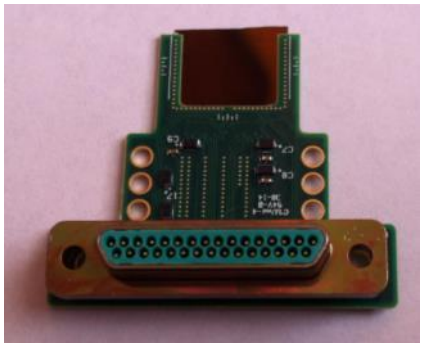
SCI Packaging Approach

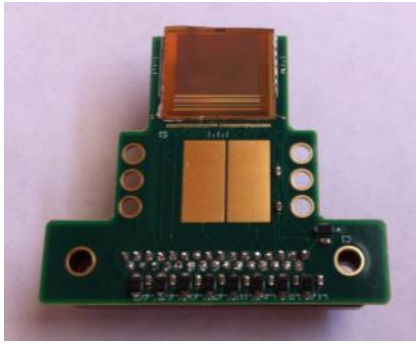




Package 1: Cold finger directly attached against CMOS circuits

- **Wire bonding**
- **Chip on board**
- **Cold finger attached**
  - **Also guarantees planarity**
- **Backfill or vacuum seal**
  - **With ceramic board**

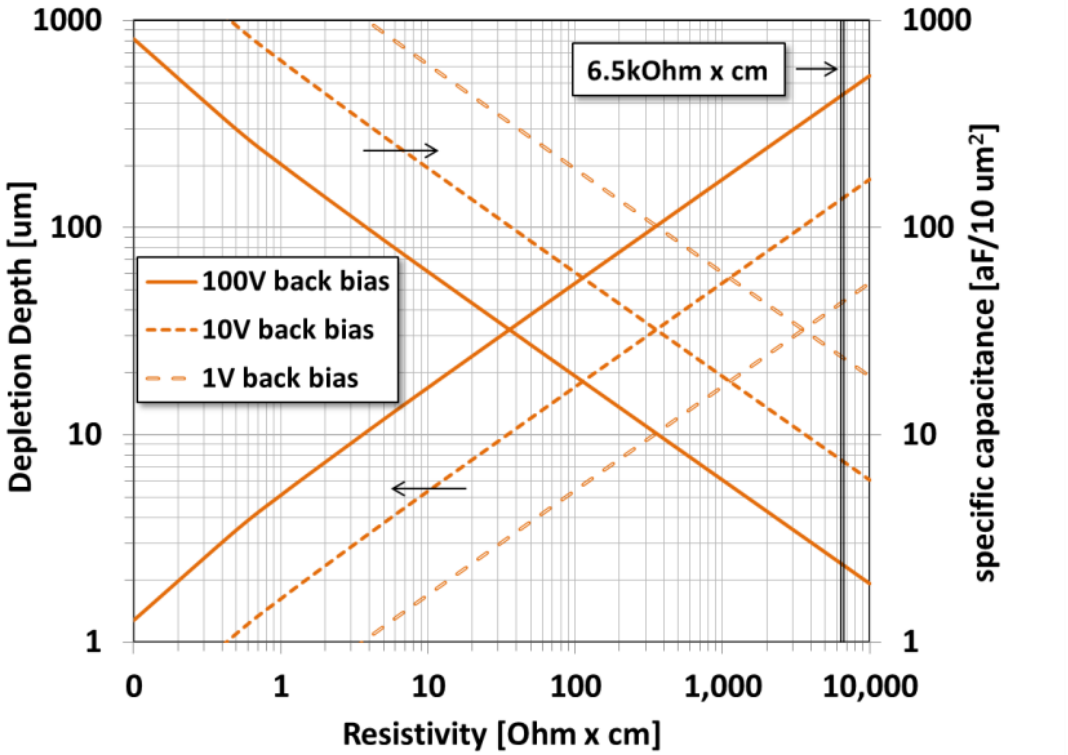




Package 2: Sensor freely suspended with support on sides only (⇒ only 50µm thick silicon membrane in beam path)

Low cost Package for High End Applications with Low Volume

Estimate of Depletion Layer Versus Si Resistivity

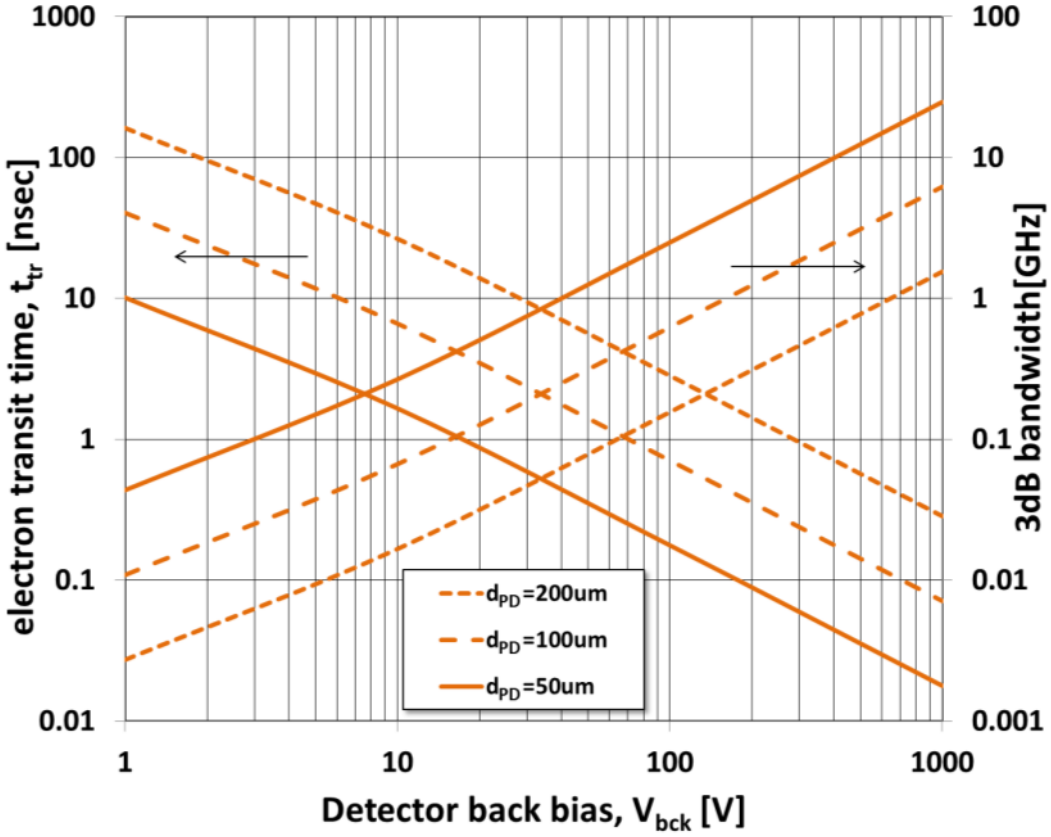


For best performance a backside bias must be applied

Our 6.5 kOhm x cm material can be depleted to a thickness of 50um with a backside bias of less than 5V

High Resistivity Silicon Must be Used to Achieve Deep Depletion

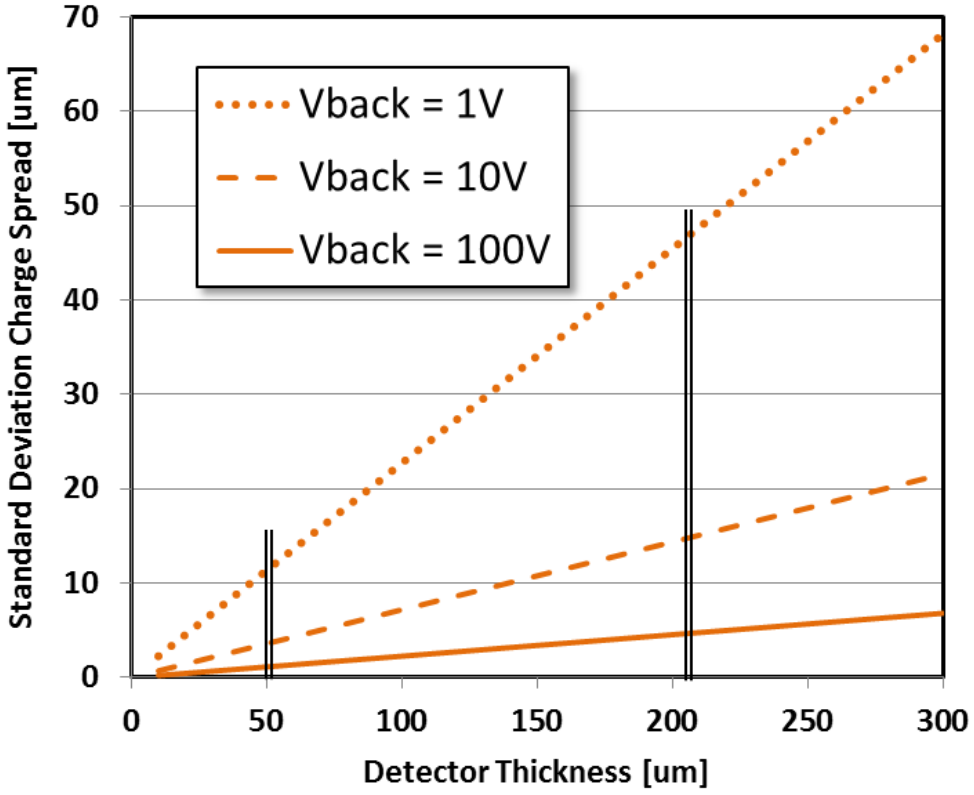
Predicted FD PIN Diode Response Time



- **Transit time of photo generated charge carriers in 100um FD CMOS imager with 100V backside bias < 1nsec, corresponding to a 3dB bandwidth > 1GHz**

Fully Depleted Imager is Suited to Support Nanosecond Integration Time Windows

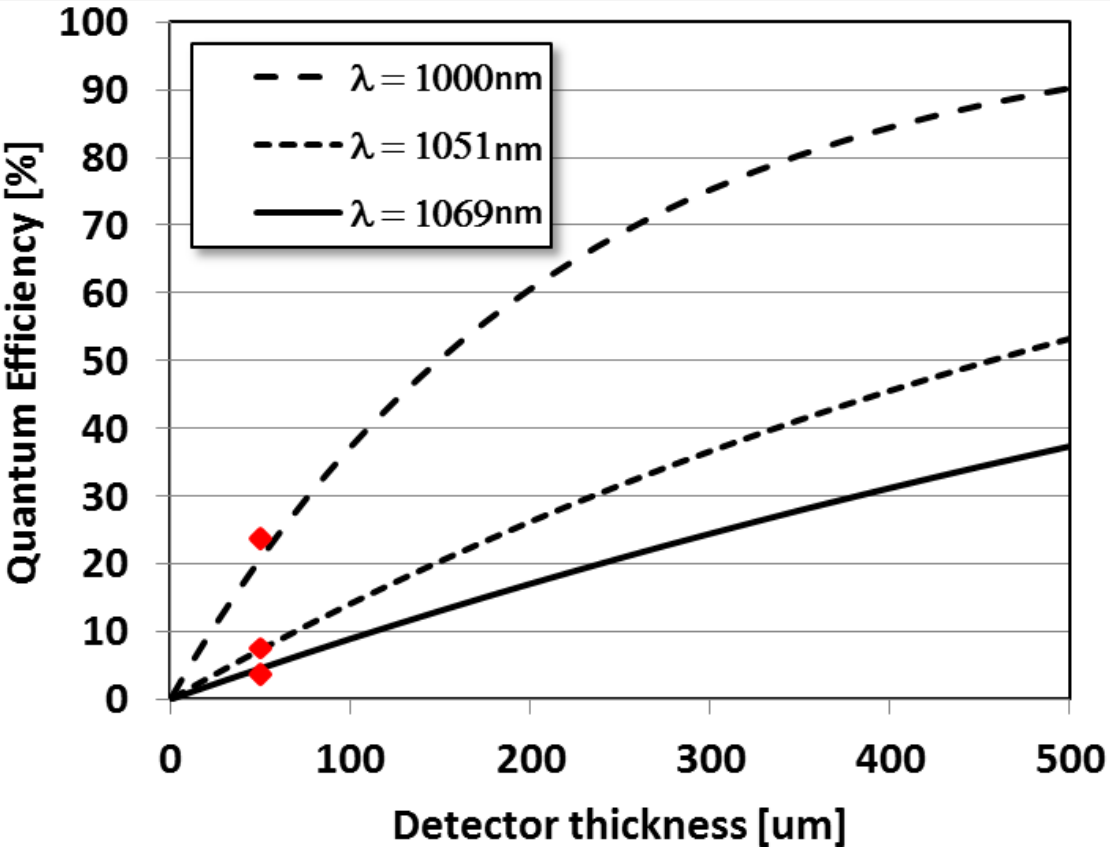
Predicted Charge Spread Versus Detector Thickness

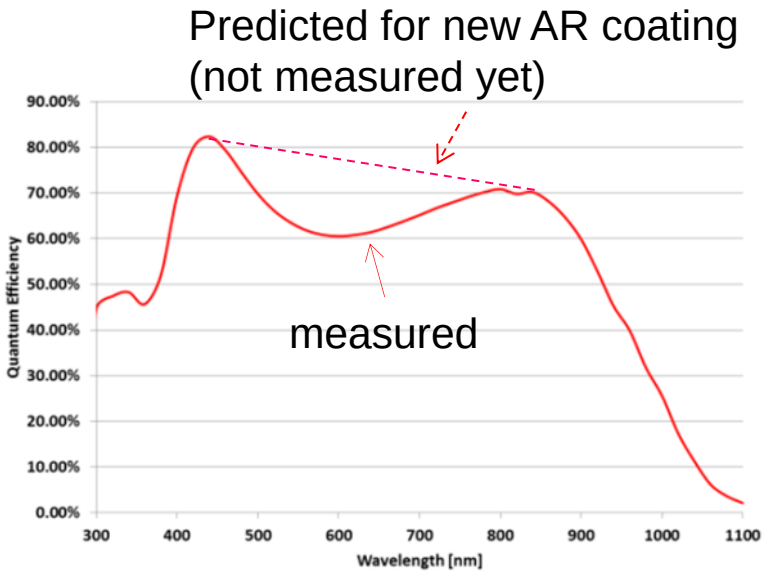


For a 200um thick FD CMOS imager with 100V backside bias, photo generated charge carriers can spread up to 4.5 um before reaching the front side collection junction

MTF Performance Limited Pixel Pitch of FD imager: < 4.5um

Quantum Efficiency

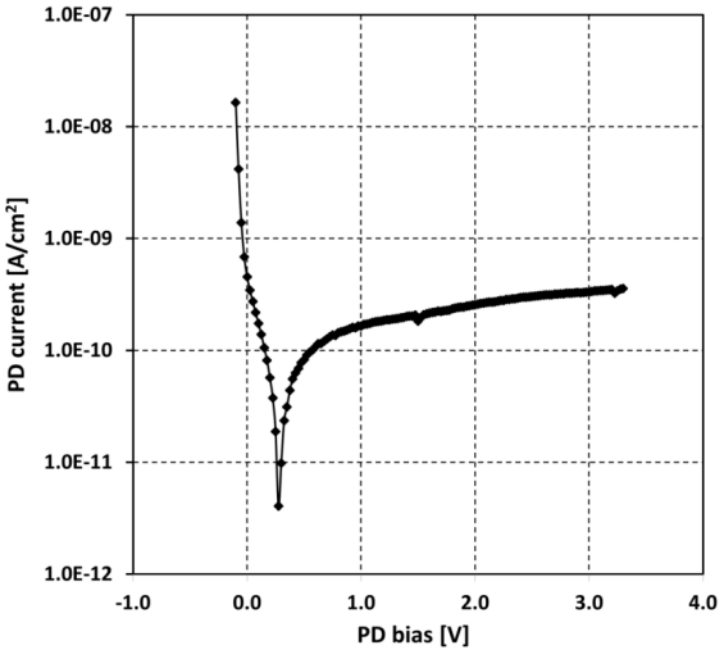


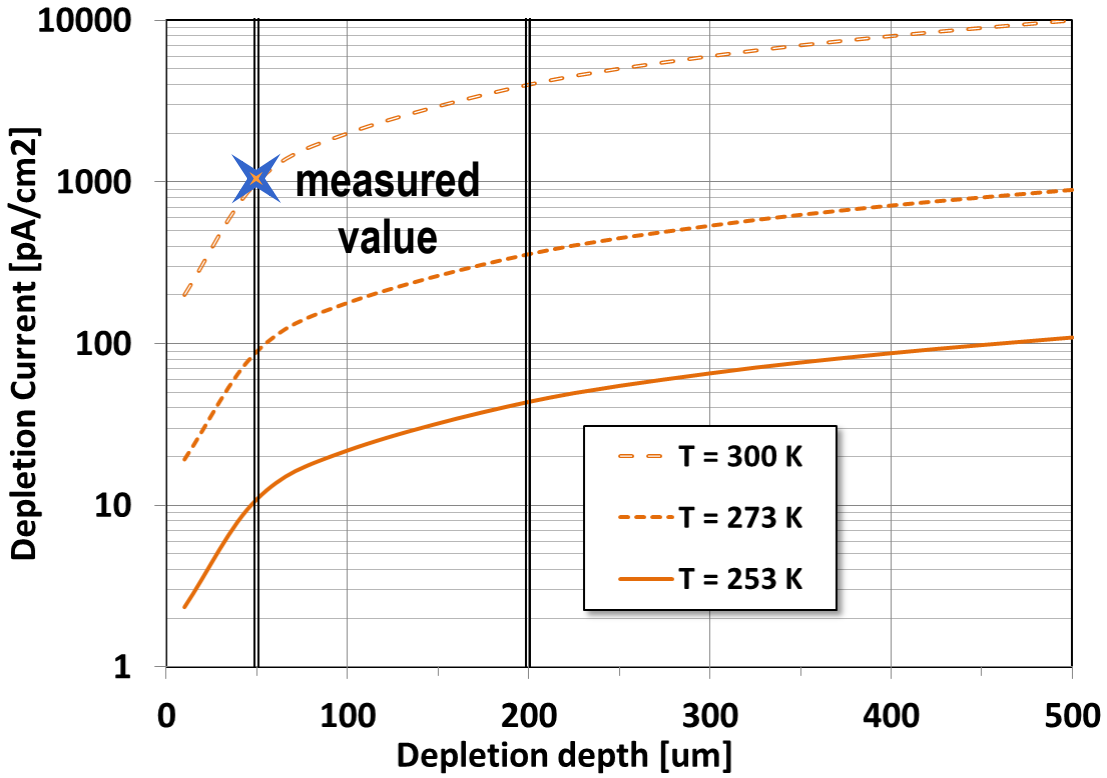


- High Broadband response
- High and stable UV response
- Peak QE > 90% can be customized with AR coating

Quantum Efficiency Comparable to that of Fully Depleted BSI CCDs

Dark Current on 50um Thick Silicon



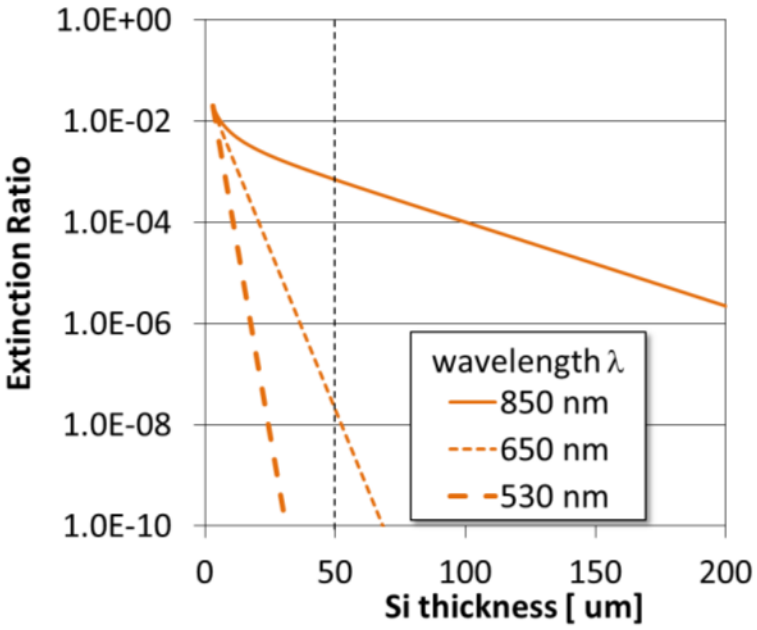


- Measured on 1mm^2 large test pixel arrays, on wafer level, at room temperature
- 1V back bias was applied

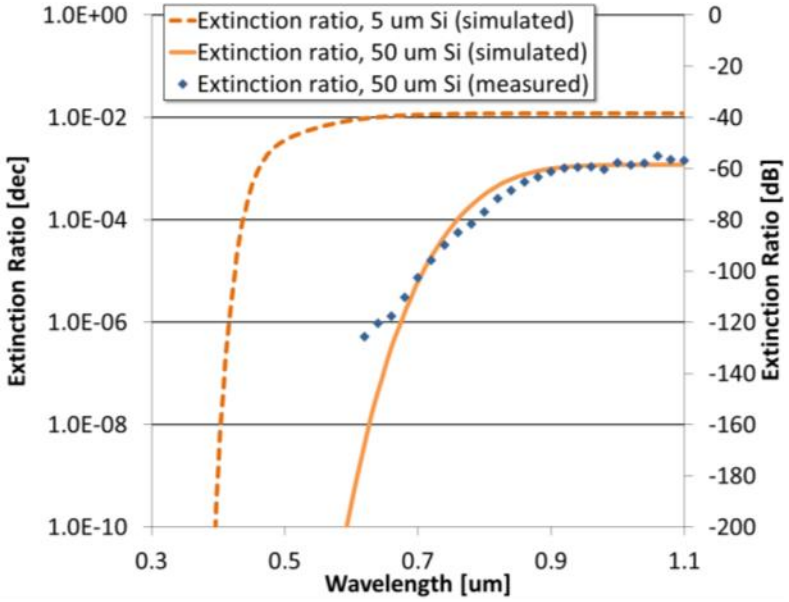
Measured Dark Current is Close to Predicted Depletion Current

Predicted and Measured Snapshot Shutter Performance

Extinction Ratio as a function of detector thickness (simulated)

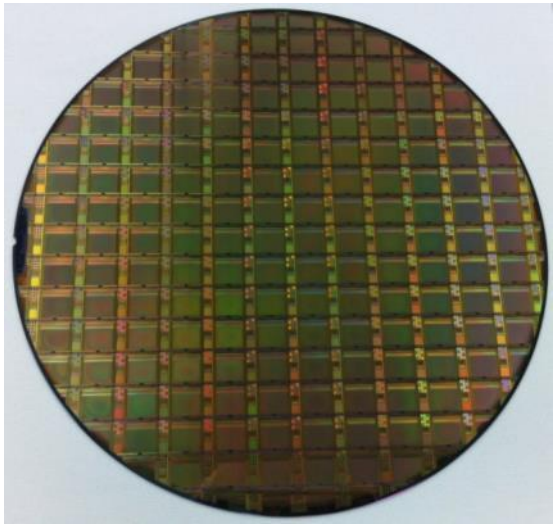


Extinction Ratio as a function of wavelength (simulated + measured)

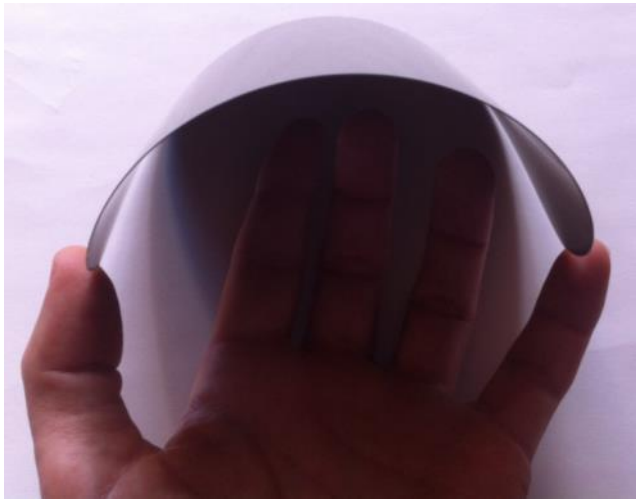


>120dB Extinction Ratio in Visible Domain for $\lambda \leq 640$nm

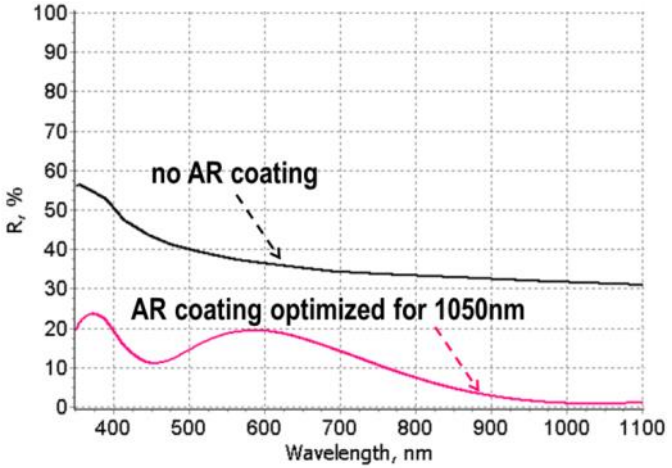
Backside Processing of 640x 512 Imager



High rho silicon wafer with completed CMOS process

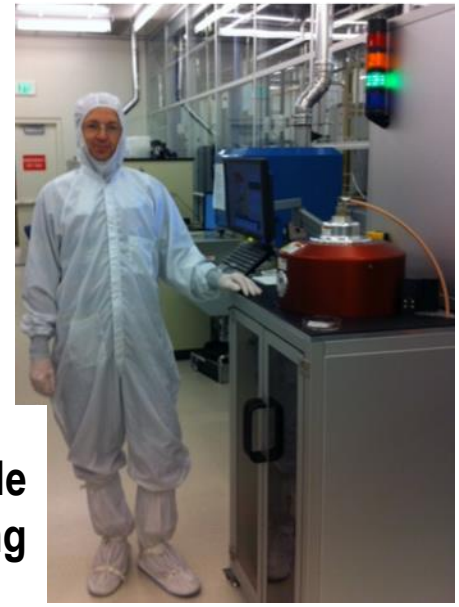


Wafer thinned to 50um

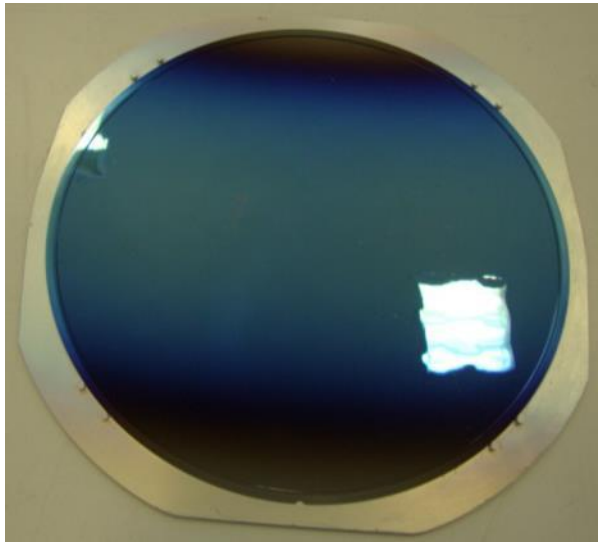


Thin film simulation of AR coating

Backside Process defines Optoelectronic Device Characteristics and can be Optimized for Different Applications



in-house backside processing



50um thick wafer with AR coating