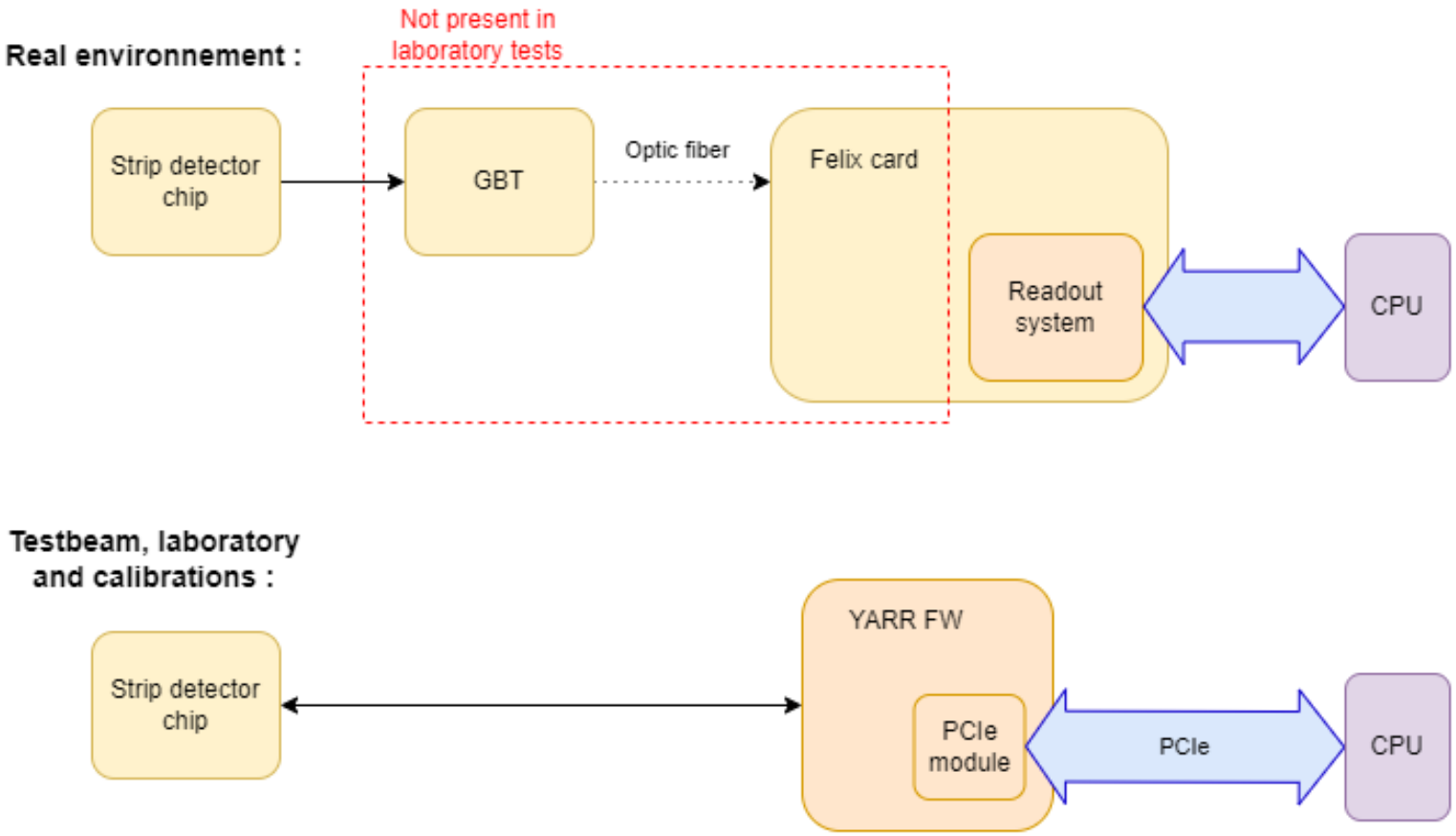
YARR PCIe Firmware optimisation

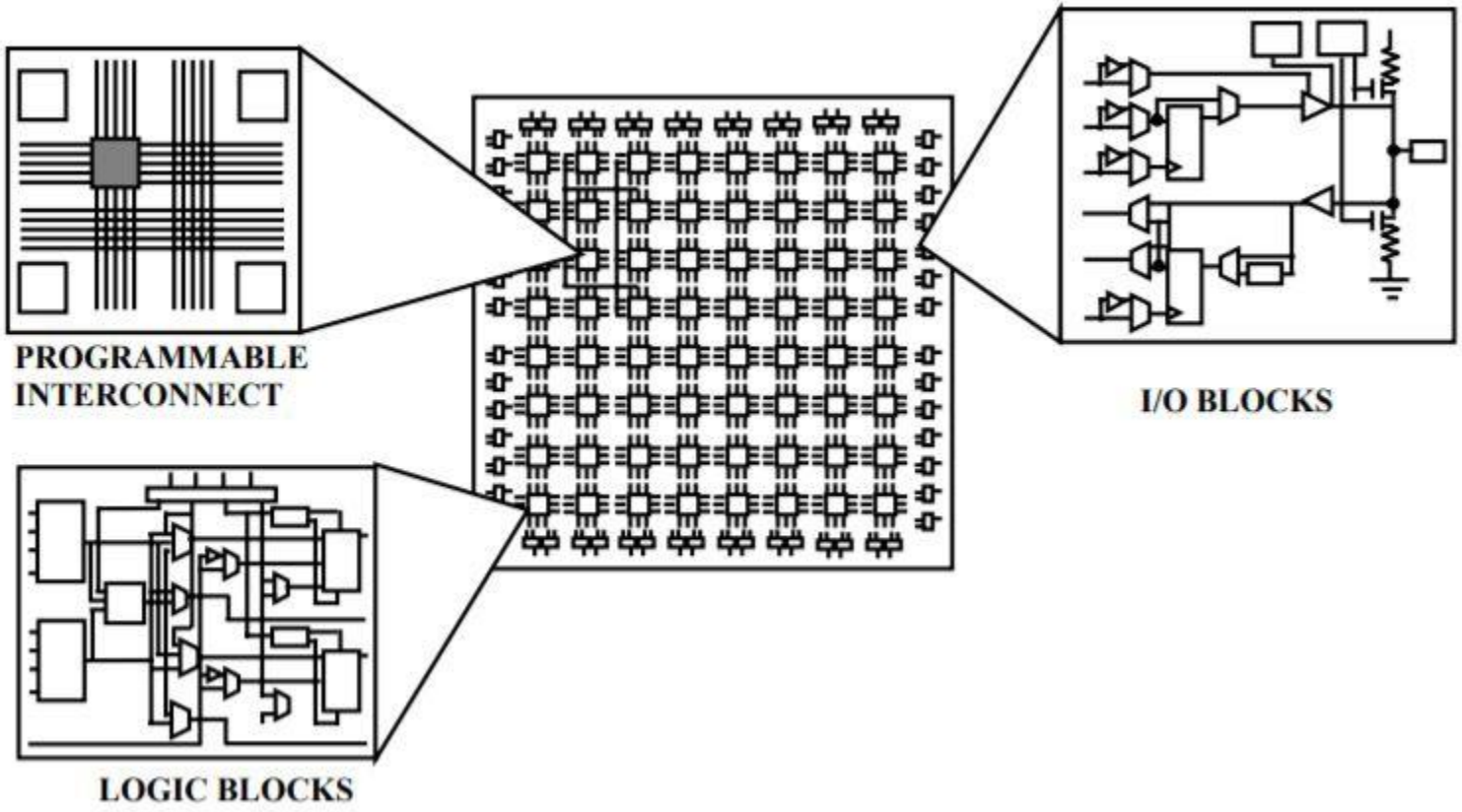
MASTER OF SCIENCE IN ENGINEERING

BERKELEY LAB

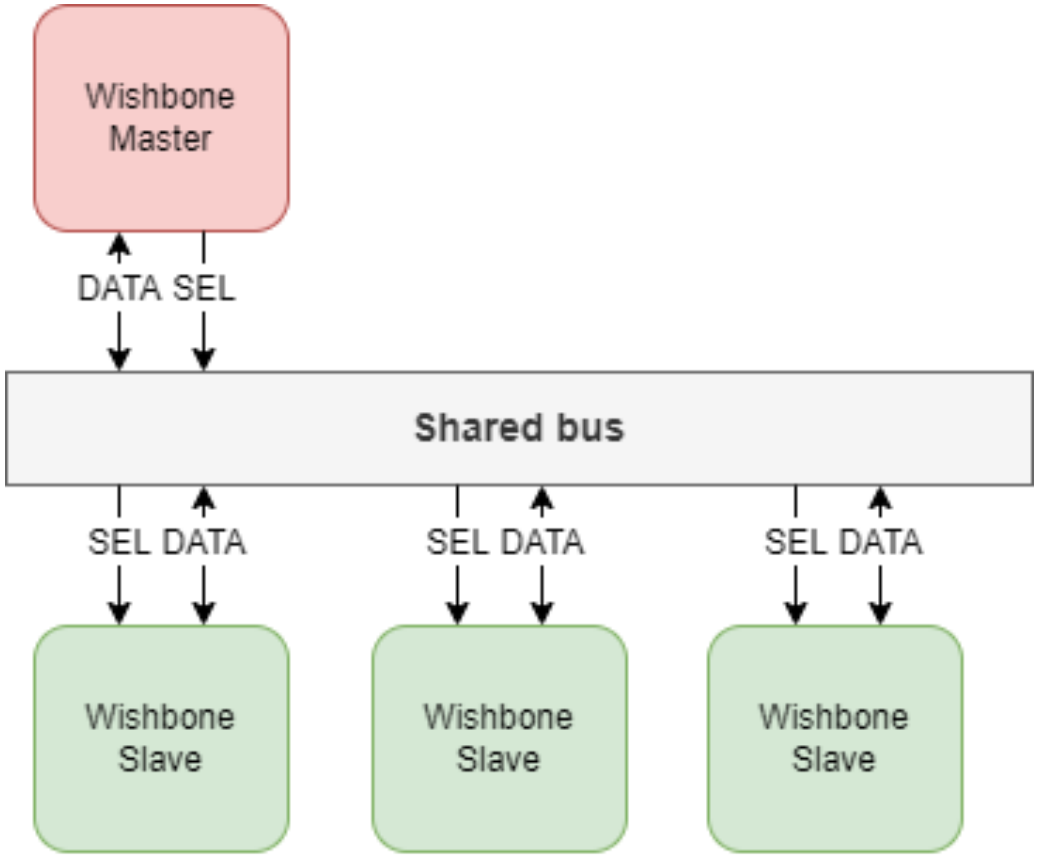
YARR


Real environnement :
Not present in laboratory tests
Strip detector chip
GBT
Optic fiber
Felix card
Readout system
CPU
Testbeam, laboratory and calibrations :
Strip detector chip
YARR FW
PCIe module
PCIe
CPU

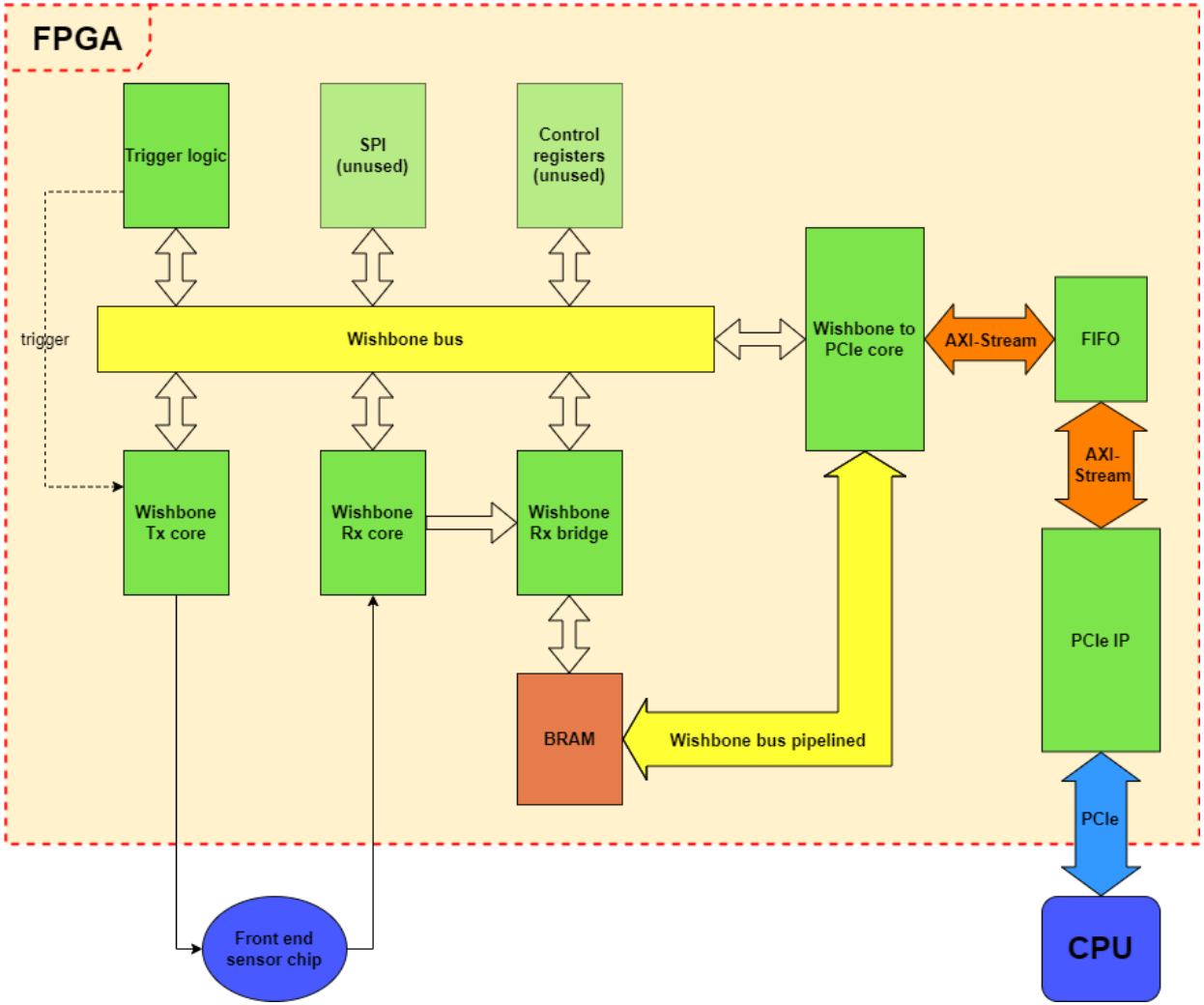
FPGA



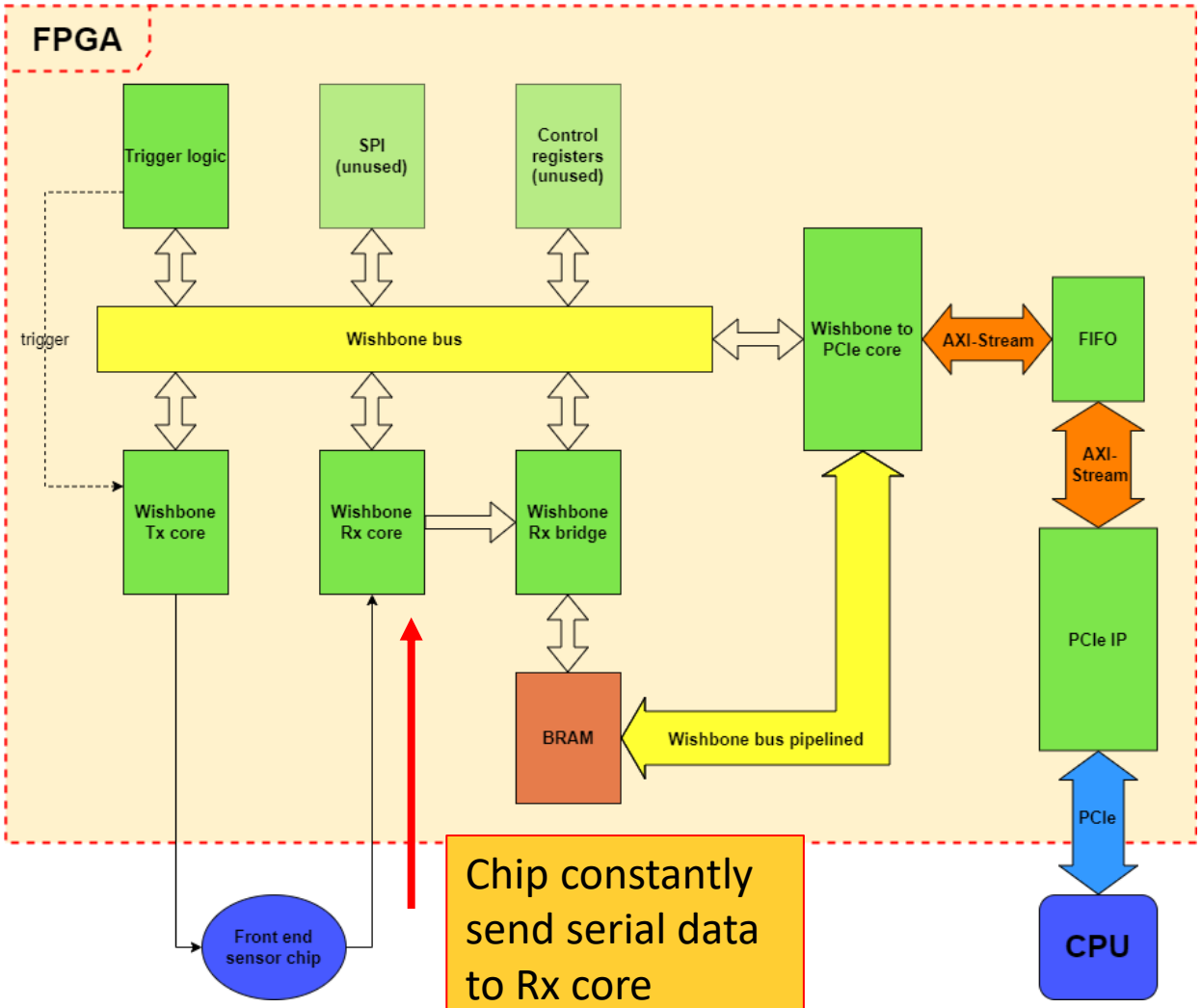
Wishbone bus



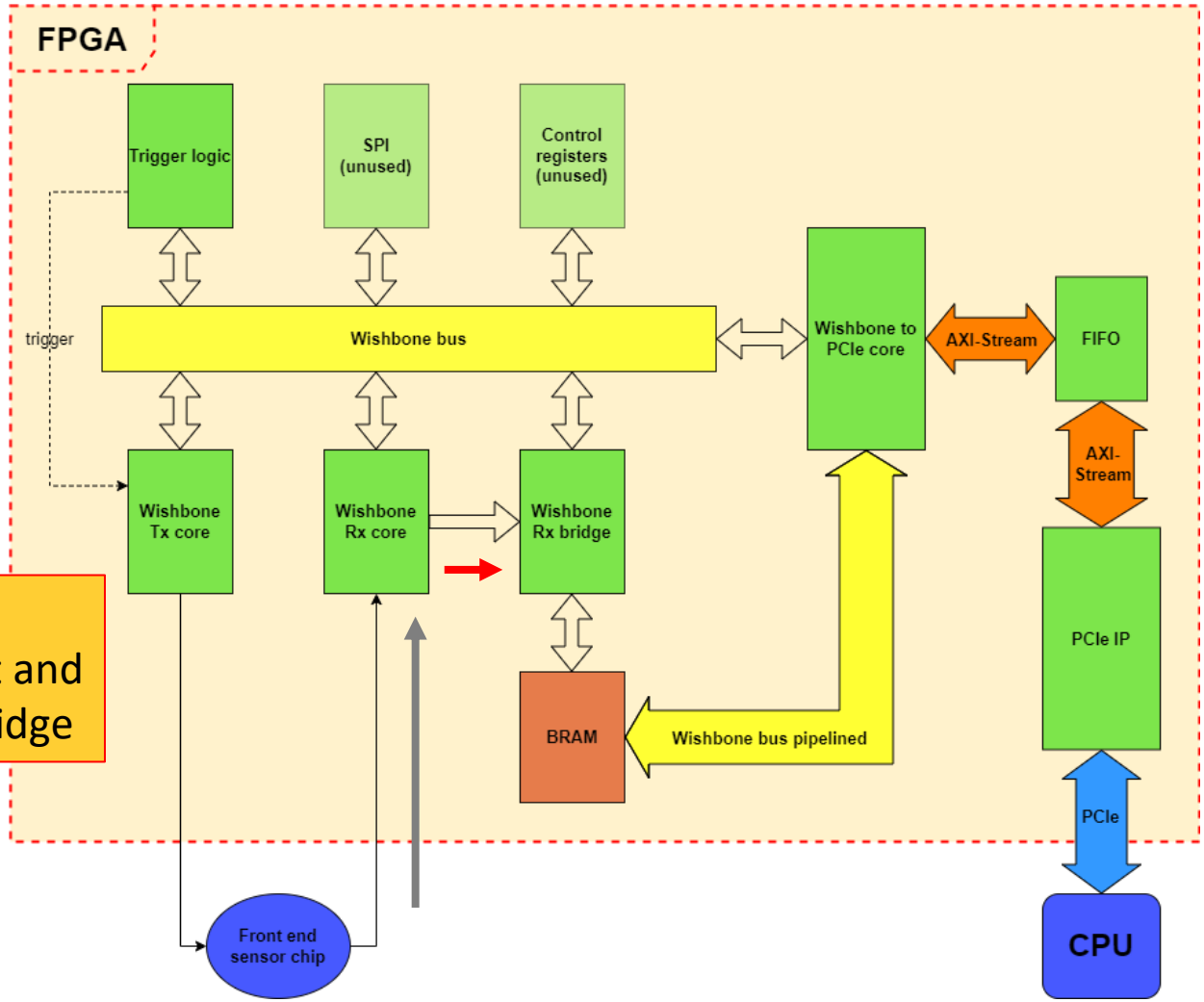
Firmware architecture



Data flow

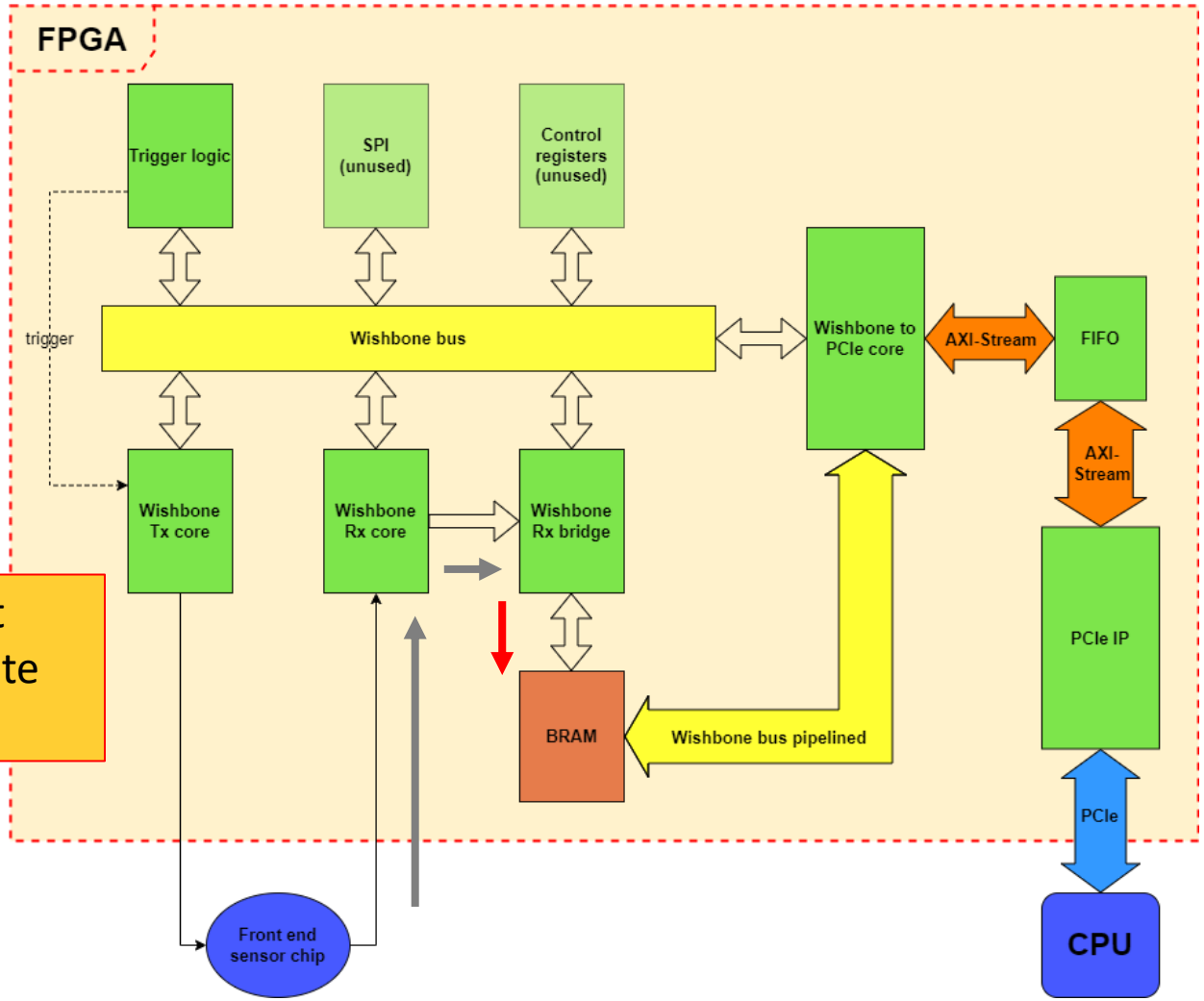

FPGA
Trigger logic
SPI (unused)
Control registers (unused)
trigger
Wishbone bus
Wishbone to PCIe core
AXI-Stream
FIFO
AXI-Stream
Wishbone Tx core
Wishbone Rx core
Wishbone Rx bridge
PCIe IP
BRAM
Wishbone bus pipelined
PCIe
Front end sensor chip
CPU
Chip constantly send serial data to Rx core

Data flow



Rx core deserialize it and send it to bridge

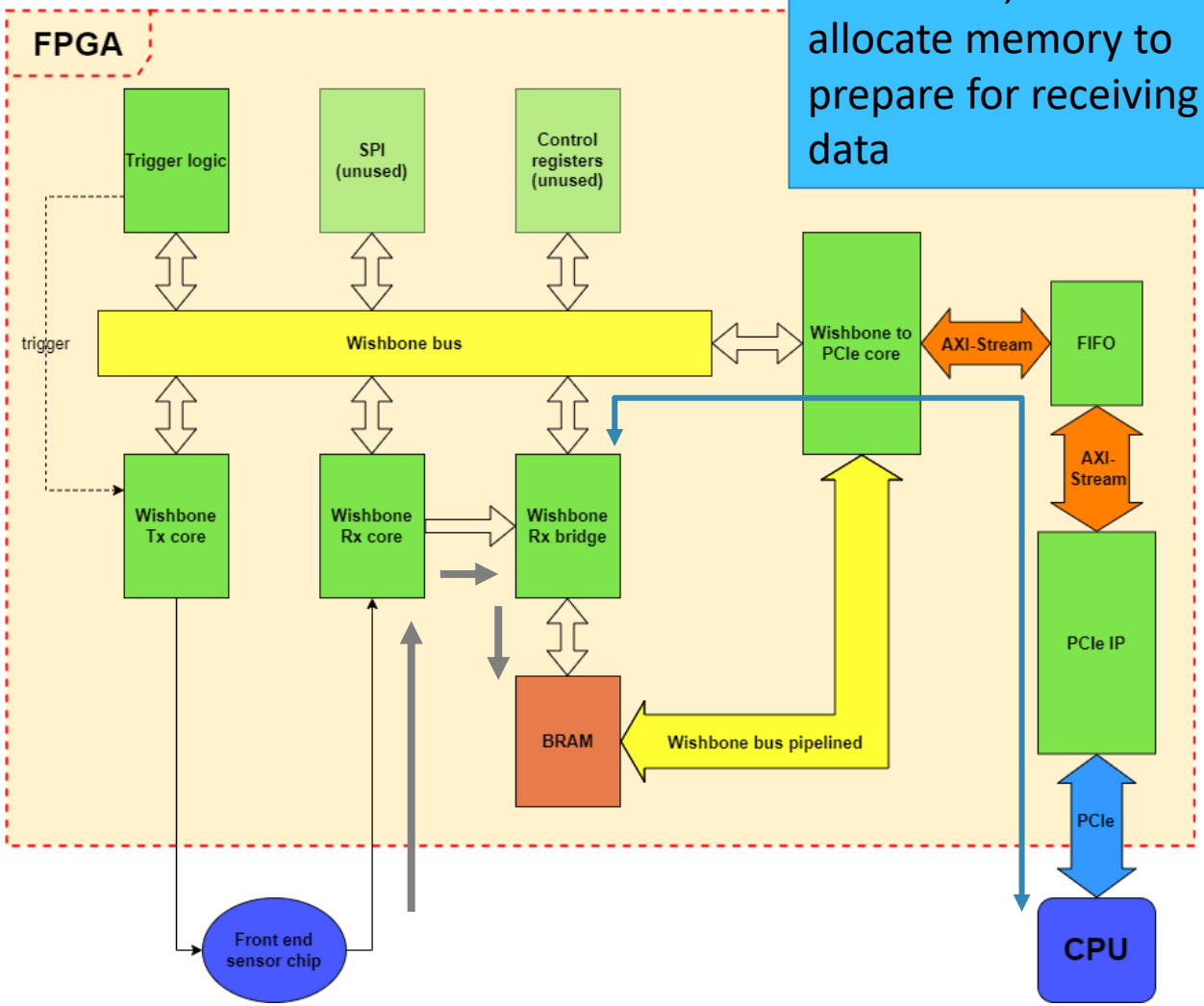
Data flow



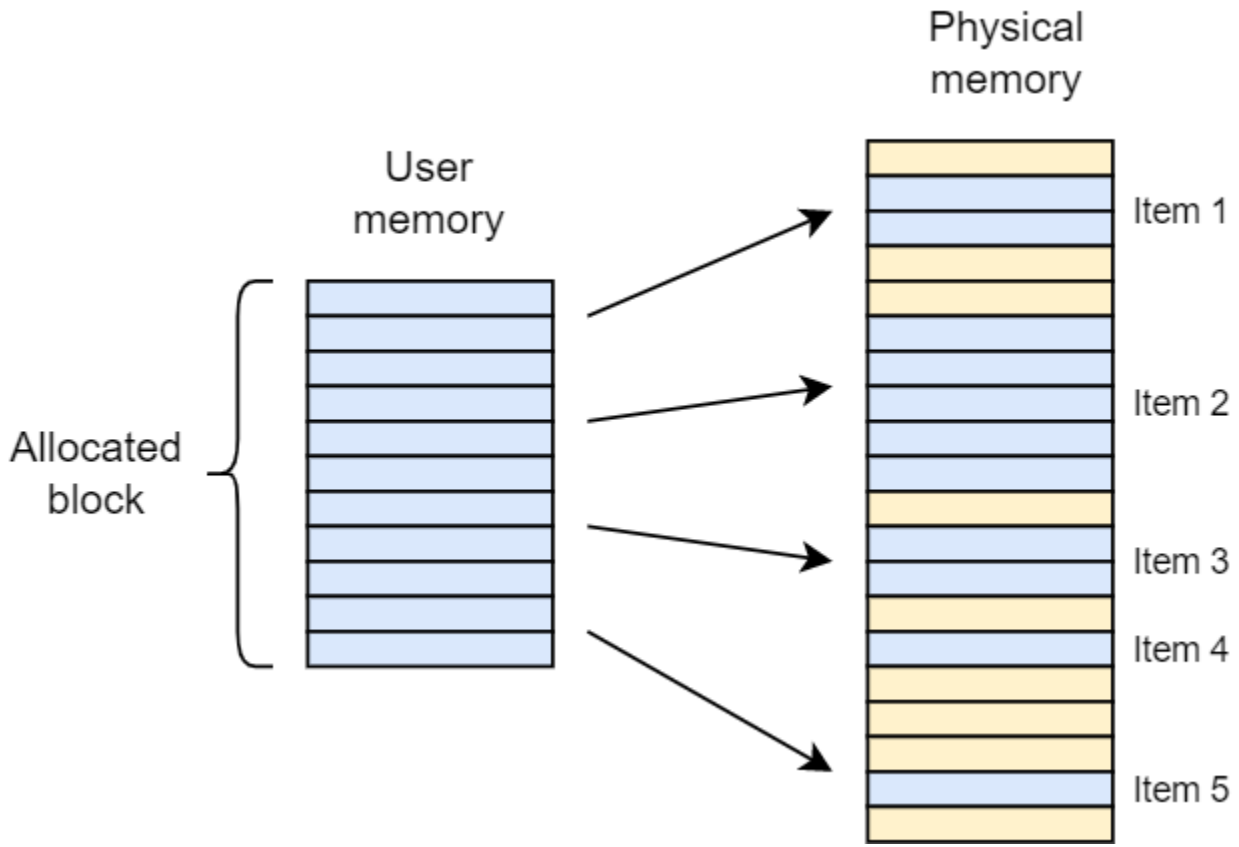
Bridge count data and write into BRAM

Data flow

When the BRAM is almost full, the CPU allocate memory to prepare for receiving the data

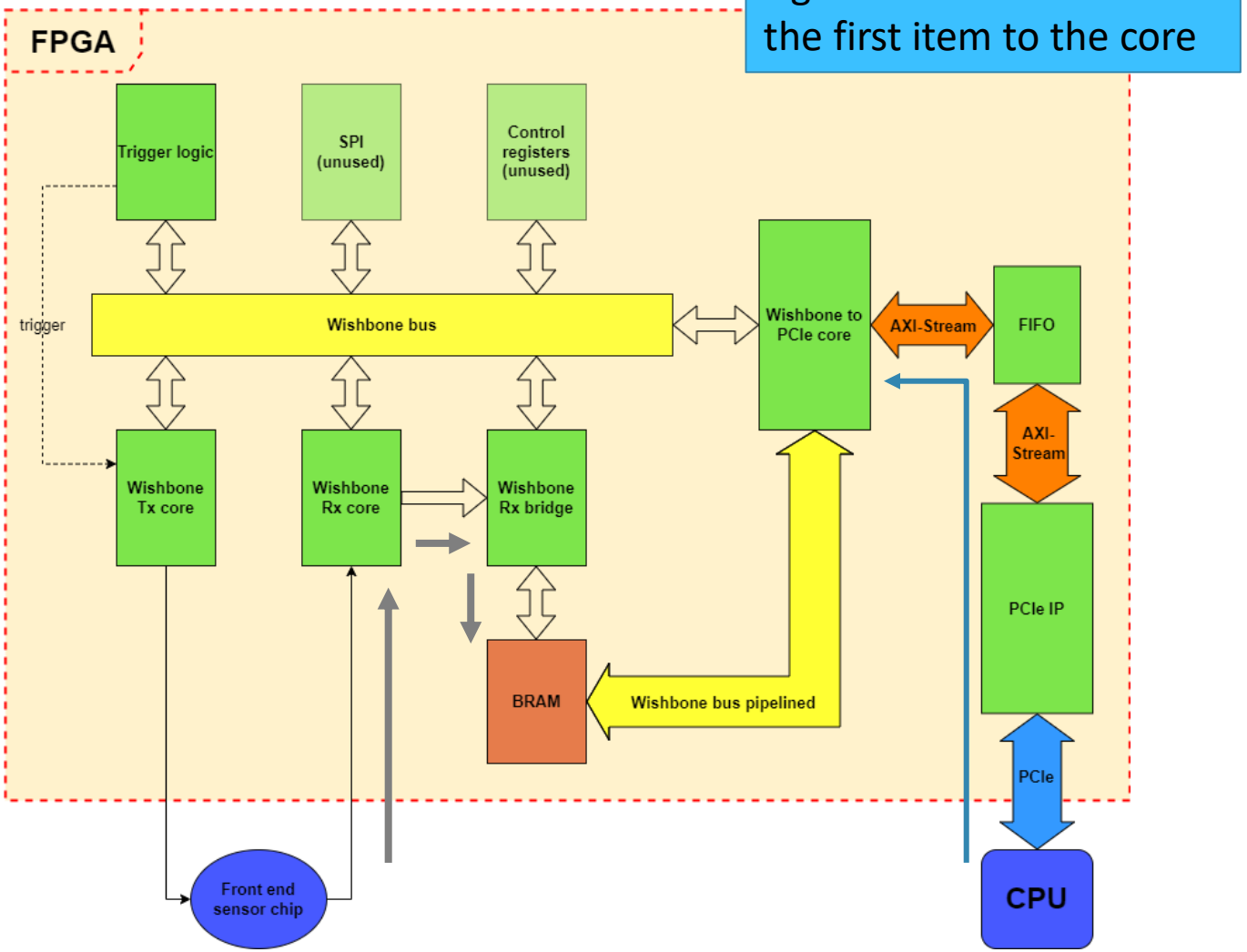


Memory allocation

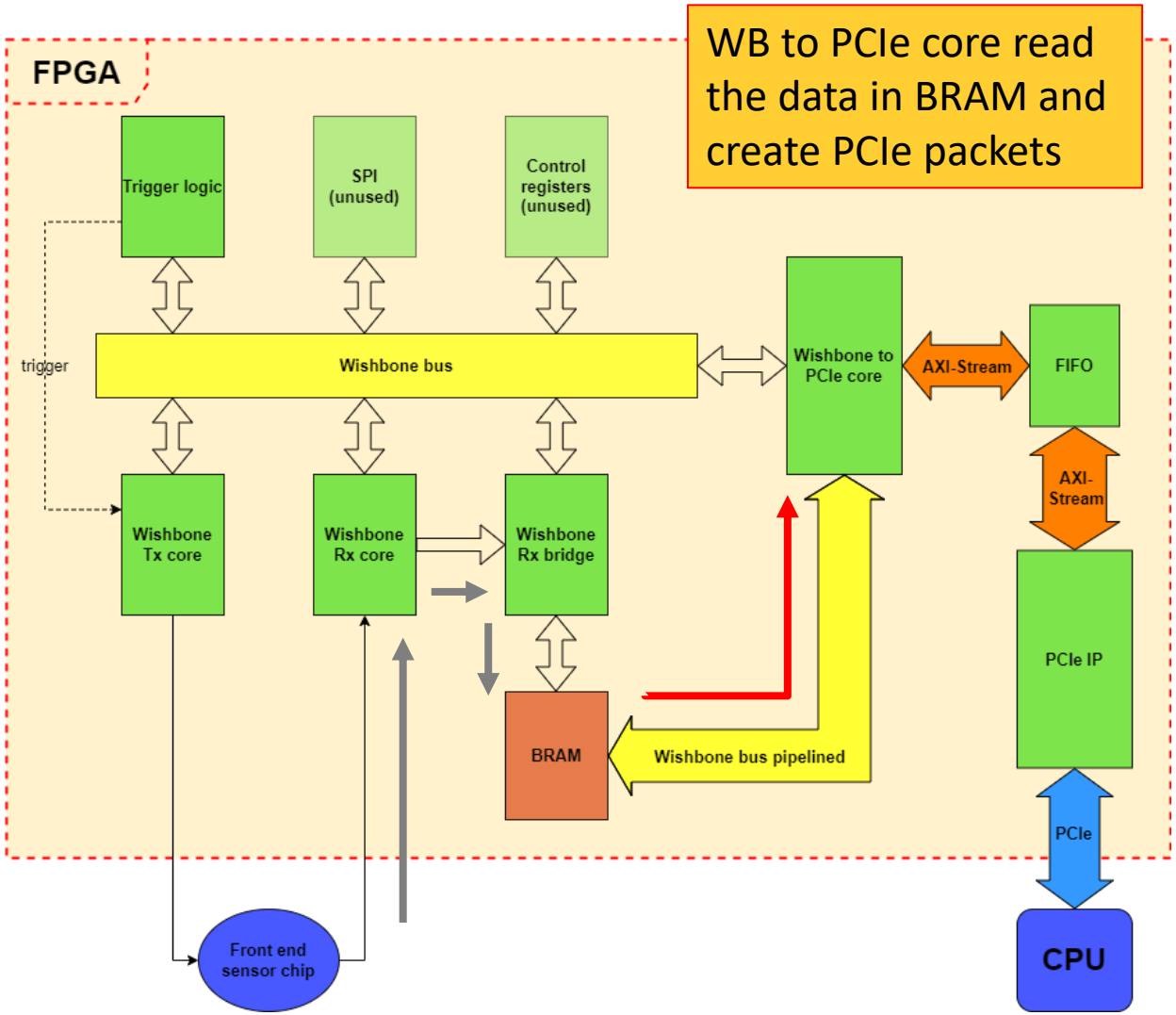


Data flow

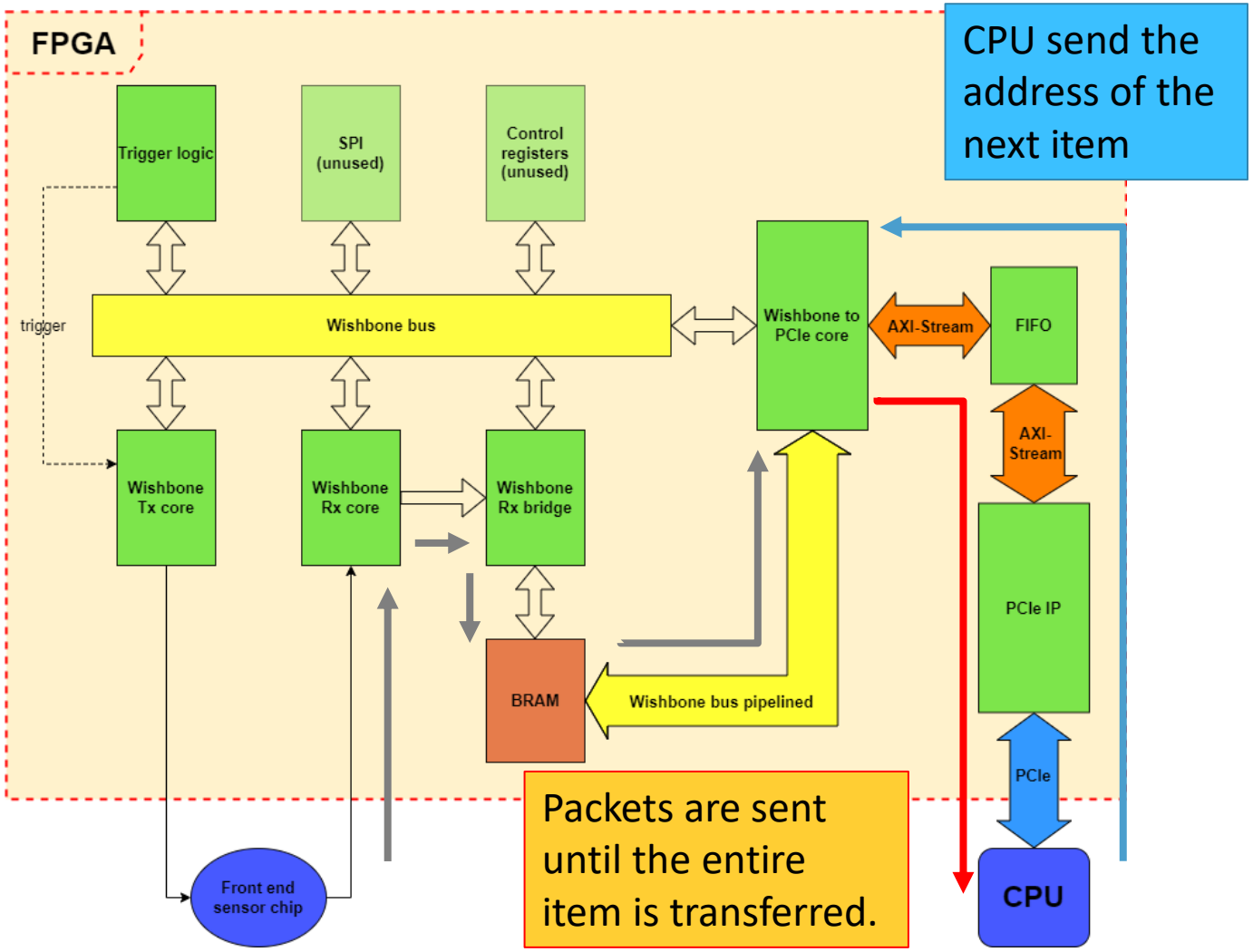
The CPU send the start signal and the address of the first item to the core



Data flow


FPGA
WB to PCIe core read the data in BRAM and create PCIe packets
Trigger logic
SPI (unused)
Control registers (unused)
trigger
Wishbone bus
Wishbone to PCIe core
AXI-Stream
FIFO
AXI-Stream
Wishbone Tx core
Wishbone Rx core
Wishbone Rx bridge
PCIe IP
BRAM
Wishbone bus pipelined
PCIe
Front end sensor chip
CPU

Data flow


FPGA
CPU send the address of the next item
Trigger logic
SPI (unused)
Control registers (unused)
trigger
Wishbone bus
Wishbone to PCIe core
AXI-Stream
FIFO
AXI-Stream
Wishbone Tx core
Wishbone Rx core
Wishbone Rx bridge
PCIe IP
BRAM
Wishbone bus pipelined
PCIe
Front end sensor chip
CPU
Packets are sent until the entire item is transferred.

Issues

- Important delay between the request of the next item by the FPGA and its reception. Solution -> Request the whole list adresses at once and store them
- Wishbone bus cannot go higher than 160Mhz without having timing issues. Solution -> Figure out what's wrong and fix it

Goals of my project

- Analysis of the bottlenecks
- Improvement of the readout speed
- Documentation of the system

Questions ?