Highlights of TWEPP2022
Topical Workshop on Electronics for Particle Physics

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LBNL

Oct 14, 2022

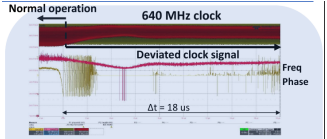
TWEPP2022

- One week workshop of electronics for particle and astro-particle physics experiments:
  - ASIC, FPGA, optoelectronics, power, trigger, system
  - Radiation tolerant systems
  - Status and experience of existing experiments's upgrade (production, testing, installation, commissioning and running)
  - R&D for future experiments
- Indico agenda: https://indico.cern.ch/event/1127562/
  - About 200 attendees
  - 72 oral + 100 poster presentations, 6 invited talks, 3 hours tutorial (on high speed PCB design)
- This talk: highlights of a few selected presentations, mostly about ASIC

Status of Existing Upgrades

RD53: pixel chips for ATLAS and CMS

- Final chips to be submitted soon (ATLAS: Q4 2022, CMS: Q1 2023)
- Currently focusing on verification: SEU/SET verification at RTL and gate level



- ❑ Readout link dropouts caused frequent DAQ-chip re-sync and hit/event loss
- ❑ Projected time between link dropouts in the inner layer? 0.2s (plus DAQ needs time to re-sync.)
- ❑ SET sensitivity of which biasing circuit is causing this? How to find the sensitive part of that circuit?

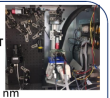
Two-Photon Absorption (TPA) laser setups

@ KU Leuven, Campus Geel

PULSCAN
- Wavelength 1550 nm
- Pulse duration 450 fs
- Pulse energy up to 50 nJ

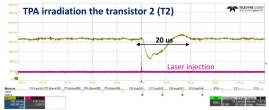
@ CERN

Many thanks to the SSD lab of the EP-DT group (CERN)



FYLA
- Wavelength 1550 nm
- Pulse duration 430 fs
- Pulse energy up to 2.2 nJ

- ➢ Injection into a single known node
- ➢ Near-infrared imaging
- ➢ Beam focused through the substrate
- ➢ Allows spatial and temporal resolution
- ➢ Charge collection occurs only at the beam focus
- ➢ Requires optical access to the backside of the chip



- Problem is reproduced in the SET SPICE simulations
- SEE Compensating capacitors are added (VGATE1 to GDNA, VGATE2 to GNDA)
- SET simulations show that the revised design mitigates previous SET sensitivity
- RD53C is now expected to have a much lower cross-section of the link dropout

The critical IPs in the analog chip bottom are all characterized against SETs by the TPA irradiation and the expected SET robustness is confirmed.

Talk(s): R. Beccherle, J. Lalic

DC-DC converters for CMS MTD and ECAL

- Few interesting observations from them:
  - Low frequency (about 20 kHz) oscillation of output voltage (up to 20mV amplitude) at a small range of load current

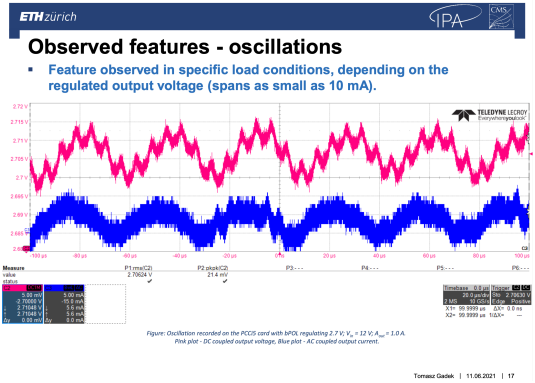


Figure: Oscillation recorded on the PCCI5 card with bPOL regulating 2.7 V; V_{in} = 12 V; A_{out} = 1.0 A.
Pink plot - DC coupled output voltage, Blue plot - AC coupled output current.

Table: Low frequency oscillations measured at the output of the DC-DC converters. Measurements performed with 10 mA step load scan. (green field – no oscillations observed). Current values denote range in which oscillations are present.

input voltage / converter	7 V	8 V	9 V	10 V	11 V	12 V
PCCi1_FEAST_X_1v8	530 – 600 mA 7.5 – 11.2 kHz	560 – 630 mA 8.3 - 11.6 kHz	580 – 650 mA 8.5 – 11.6 kHz	600 – 670 mA 8.7 – 11.7 kHz	620 – 680 mA 9.0 – 11.8 kHz	630 – 700 mA 9.3 – 12.0 kHz
PCCi1_FEAST_Y_1v2						
PCCi1_FEAST_W_2v5						
PCCi1_FEAST_Z_1v8						
PCCi2_FEAST_X_1v8						
PCCi2_FEAST_Y_1v2						
PCCi2_FEAST_W_2v5						
PCCi2_FEAST_Z_1v8			620 - 630 mA 15.8–16.4 kHz	650 – 670 mA 16.4–16.7 kHz	660 – 690 mA 16.4–19.2 kHz	670 – 700 mA 16.2–18.8kHz
PCCi3_bPOL_X_1v8						
PCCi3_bPOL_Y_1v2	500 – 570 mA 19.7–26.5 kHz	510 – 590 mA 19.7-26.3 kHz	520 – 610 mA 19.5–26.5 kHz	530 – 610 mA 20.1–22.2 kHz	540 – 630 mA 20.9–27.5 kHz	550 – 640 mA 21.7–28.5 kHz
PCCi3_bPOL_W_2v5					800 – 810 mA 31.9–41.9 kHz	820 – 850 mA 39.9–42.7 kHz
PCCi3_bPOL_Z_1v8						
PCCi4_bPOL_X_1v8						
PCCi4_bPOL_Y_1v2	410 – 520 mA 15.9–19.9 kHz	420 – 540 mA 16.1–22.9 kHz	420 – 560 mA 16.1–23.5 kHz	420 – 580 mA 16.3–24.6 kHz	430 – 580 mA 16.5–25.6 kHz	430 – 590 mA 16.5–27.4 kHz
PCCi4_bPOL_W_2v5	750 – 800 mA 20.1–27.6 kHz	800 – 870 mA 20.5–28.6 kHz	840 – 920 mA 21.3–30.6 kHz	870 – 950 mA 22.3–28.7 kHz	900–1010 mA 23.3–33.6 kHz	920–1040 mA 23.5–35.3 kHz
PCCi4_bPOL_Z_1v8						
PCCi5_bPOL_X_1v8						
PCCi5_bPOL_Y_1v2	420 – 560 mA 16.0–22.4kHz	430 – 560 mA 16.0–22.6 kHz	440 – 580 mA 16.2–23.6 kHz	440 – 610 mA 15.4–26.9 kHz	450 – 610 mA 16.2–27.2 kHz	450 – 620 mA 15.4–29.3 kHz
PCCi5_bPOL_W_2v5	740 – 840 mA 19.5–31.6kHz	800 – 900 mA 21.3–33.0 kHz	840 – 970 mA 21.9–34.5 kHz	870–1010 mA 22.6–36.3 kHz	900–1060 mA 23.8–38.2 kHz	920–1080 mA 24.2–39.1 kHz
PCCi5_bPOL_Z_1v8	540 – 670 mA 13.8–22.2kHz	560 – 700 mA 14.2–23.4 kHz	590 – 730 mA 15.4–24.9 kHz	610 – 750 mA 16.0–26.4 kHz	620 – 770 mA 16.4–26.9 kHz	630 – 780 mA 16.4–27.6 kHz

Talk(s): T. Gadek

DC-DC converters for CMS MTD and ECAL

- Few interesting observations from them:
  - Efficiency drop in a narrow input voltage span (around 8 V)

Observed features – efficiency drops

- **Feature observed in a very narrow input voltage span of 250-300 mV.**

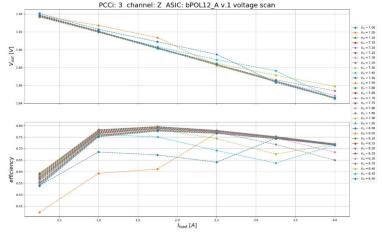


Figure: PCC3 channel Z, efficiency decrease problem reminder, target plot at V_{in} = 8 V

Table: Input voltage regions causing efficiency drops in DC-DC converters measured at 0.25 – 4 A load (green field - none observed)

converter \ input voltage	7 – 8.5 V	8.5 – 10 V	10 – 12 V
PCCi1_FEAST_X_1v8			
PCCi1_FEAST_Y_1v2			
PCCi1_FEAST_W_2v5			
PCCi1_FEAST_Z_1v8			
PCCi2_FEAST_X_1v8			
PCCi2_FEAST_Y_1v2			
PCCi2_FEAST_W_2v5			
PCCi2_FEAST_Z_1v8			
PCCi3_bPOL_X_1v8	8.10 – 8.35 V		
PCCi3_bPOL_Y_1v2	7.95 – 8.20 V		
PCCi3_bPOL_W_2v5	7.95 – 8.25 V		
PCCi3_bPOL_Z_1v8	7.80 – 8.05 V		
PCCi4_bPOL_X_1v8	8.05 – 8.25 V		
PCCi4_bPOL_Y_1v2	8.20 – 8.40 V		
PCCi4_bPOL_W_2v5	8.20 – 8.45 V		
PCCi4_bPOL_Z_1v8	8.15 – 8.40 V		
PCCi5_bPOL_X_1v8	7.00 – 7.25 V		
PCCi5_bPOL_Y_1v2	7.85 – 8.10 V		
PCCi5_bPOL_W_2v5	7.85 – 8.15 V		
PCCi5_bPOL_Z_1v8	7.50 – 7.75 V		

Talk(s): T. Gadek

Selected R&D Progress

TimeSPOT: ASIC for 4D-Tracking with 28 nm CMOS

- TimeSPOT1: 32x32 channels with in pixel TDC; σ_t ~50 ps; ~20 μW/pixel

Timespot1: Analog Front End

Inverter core amplifier with double Krummenacher FB

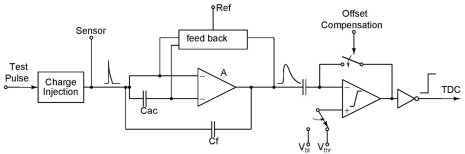
Inverter-based Charge Sensitive Amplifier (CSA) with DC current compensation.

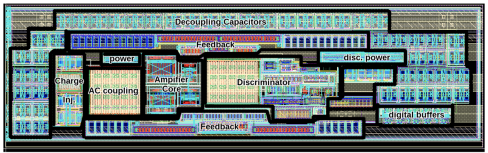
Leading Edge Discriminator with Discrete-time Offset-Compensation for threshold uniformity

OC procedure: 250 ns every ≤800 µs

Pwr regime	nominal	high
Pwr/channel [µW]	18.6	32.9
Slew rate [mV/ns]	250	360
Z_{in} [Ω] in BW	23k	23k
Gain [dB]	93	93
RMS noise [mV]	3.9	3.8
BW [MHz]	311	455
Jitter [ps]	15.6	10.5

Expected performance @ 2 fC (post-layout simulation)



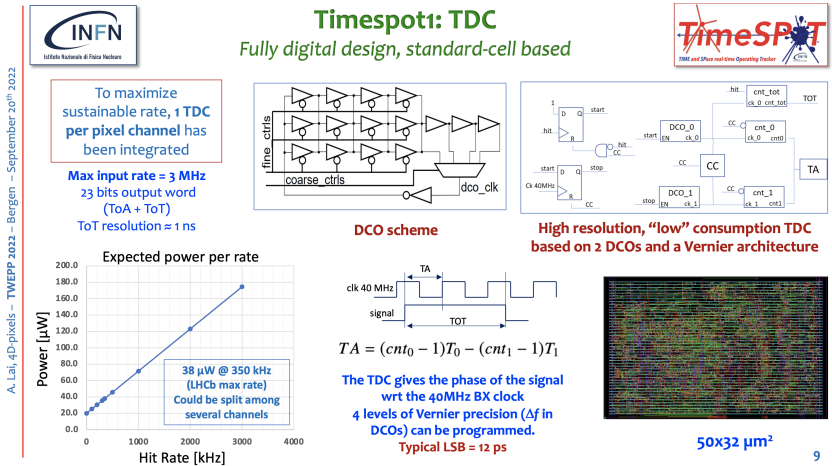


50x15 µm²

Talk(s): A. Lai

TimeSPOT: ASIC for 4D-Tracking with 28 nm CMOS

- TimeSPOT1: 32x32 channels with in pixel TDC; σ_t ~50 ps; ~20 μW/pixel



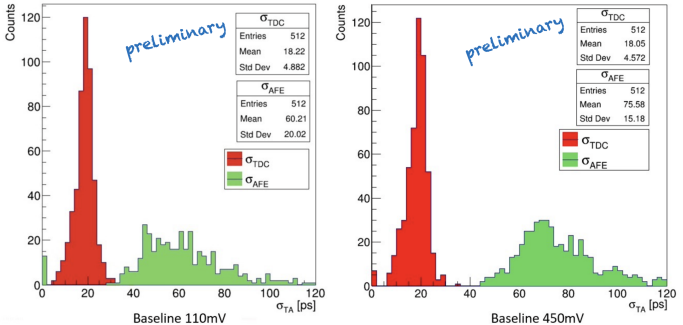
Talk(s): A. Lai

TimeSPOT: ASIC for 4D-Tracking with 28 nm CMOS

- TimeSPOT1: 32x32 channels with in pixel TDC; σ_t ~50 ps; ~20 μW/pixel

First hybridized devices

time resolution (2 fC pulses) – 2



Same behaviour with slight worsening of timing performance

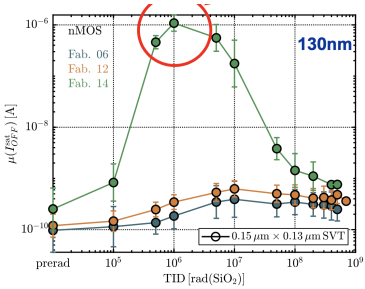
$\sigma_t \propto \sigma_n, C_{in}, vt_r, 1/Q_{in}$

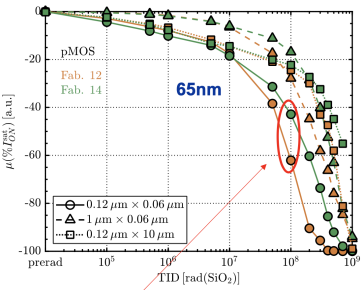
16

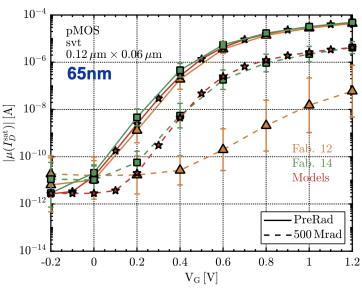
Talk(s): A. Lai

Fab-to-fab and run-to-run variation of TID

- Large variability observed in the radiation response of 130/65nm CMOS technologies: different fabrication plants, different runs within one fab.
- An effort in the past 8 years: 22 chips from 3 different fabs in 130nm and 10 chips from 2 different fabs in 65nm were measured.
- Conclusion: small device has larger variation and not well modeled.



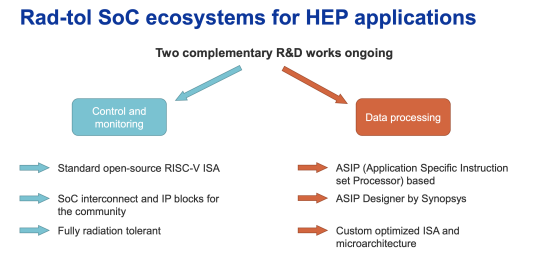


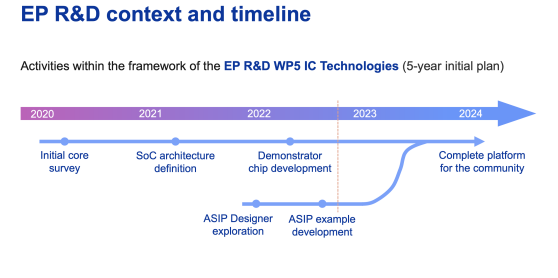


Talk(s): G. Termo

Rad-hard SoC and ASIP

- SoC: useful for slow control and monitoring on detector chips. CERN is working towards a flexible, standardized and open platform to build your own custom SoC.
- ASIP: allow to add on-chip data processing capabilities to your chips.





Talk(s): M. Andorno

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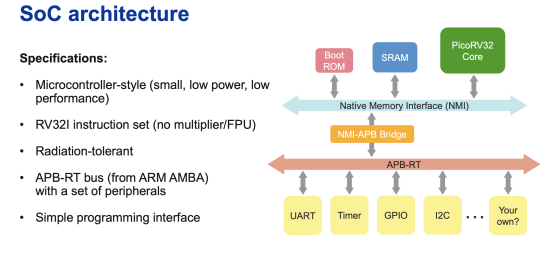
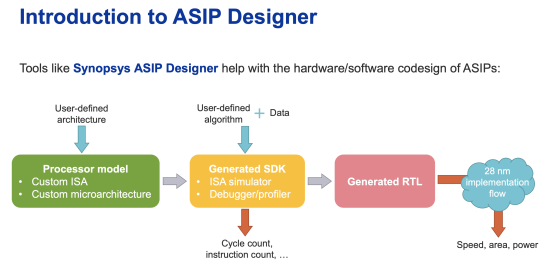




Talk(s): M. Andorno

Developments with 28 nm CMOS

- CERN IP blocks: a few rad-hard analog IP blocks are being developped within the 3-way NDA

IP Block Library (Design Finished)

Circuits to share	Notes
Bandgap voltage reference and temperature monitor	Block submitted in January 2022. Development lead by **G. Traversi (Bergamo/Pavia) collaboration with the INFN Falaphel project** with support from CERN engineers.
Digital to Analog Converter (8-bit)	Core block submitted in January 2022. Development lead by M. Piller
Differential line drivers and receivers	Block submitted in January 2022. Development lead by F. Bandi.
Rail to Rail Operational Amplifier	Completed. To be submitted in 2022. Development lead by J. Kaplon.

Design followed guidelines for radiation hardness from the initial technological characterization[1].

[1] Giulio Borghello, "Advantages of 28nm technology in ultra-high-TID environments", *Forum on 28nm CMOS (CERN), Login and access required., 2020.*

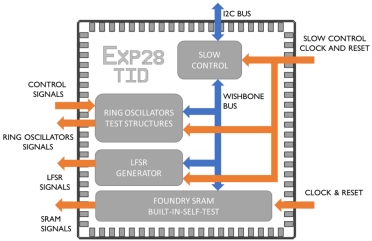
IP Block Library (Work In Progress)

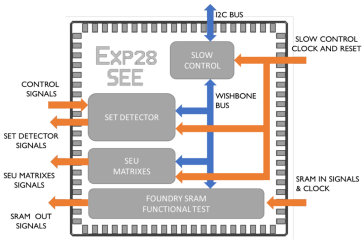
Circuits to share	Notes
Analog to Digital Converter for monitoring (12b incremental 16b free running; Volt/curr mode)	In progress. Development lead by T. Hofmann. Collaboration with University of Ulm.
Rail to Rail Operational Amplifier (slow/low power (e.g. monitoring in unity gain))	In progress. To be submitted in 2022. Development lead by M. Piller.
Digital to Analog Converter (10-bit)	Development lead by V. Sriskaran.
Digital PLL	Discussion on specifications ongoing, collaboration with WP6.
DCDC converter	In progress. Development lead by S. Michelis and G. Ripamonti
LDO	In progress. Development lead by TU Graz, supervised by S. Michelis
Shunt LDO (SLDO) for serial powering solutions (mainly inner tracker pixels)	In progress. Development lead by M. Karagounis (FH Dortmund)

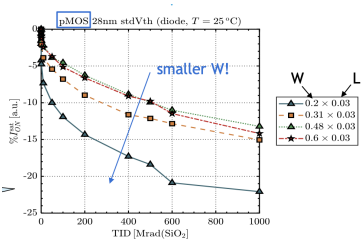
Talk(s): F. Bandi, G. Bergamin

Developments with 28 nm CMOS

- EXP28: chips suite to evaluate radiation effects of 28 nm: TID, SEE, analog IP blocks



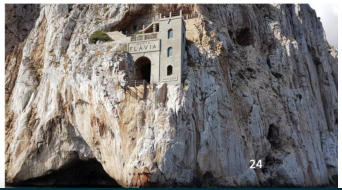




Talk(s): F. Bandi, G. Bergamin

TWEPP 2023...


Looking forward to see you all
in Sardinia in October 2023 for
TWEPP2023!
Screenshot


24

Backup slides