MOSIS Roadmap

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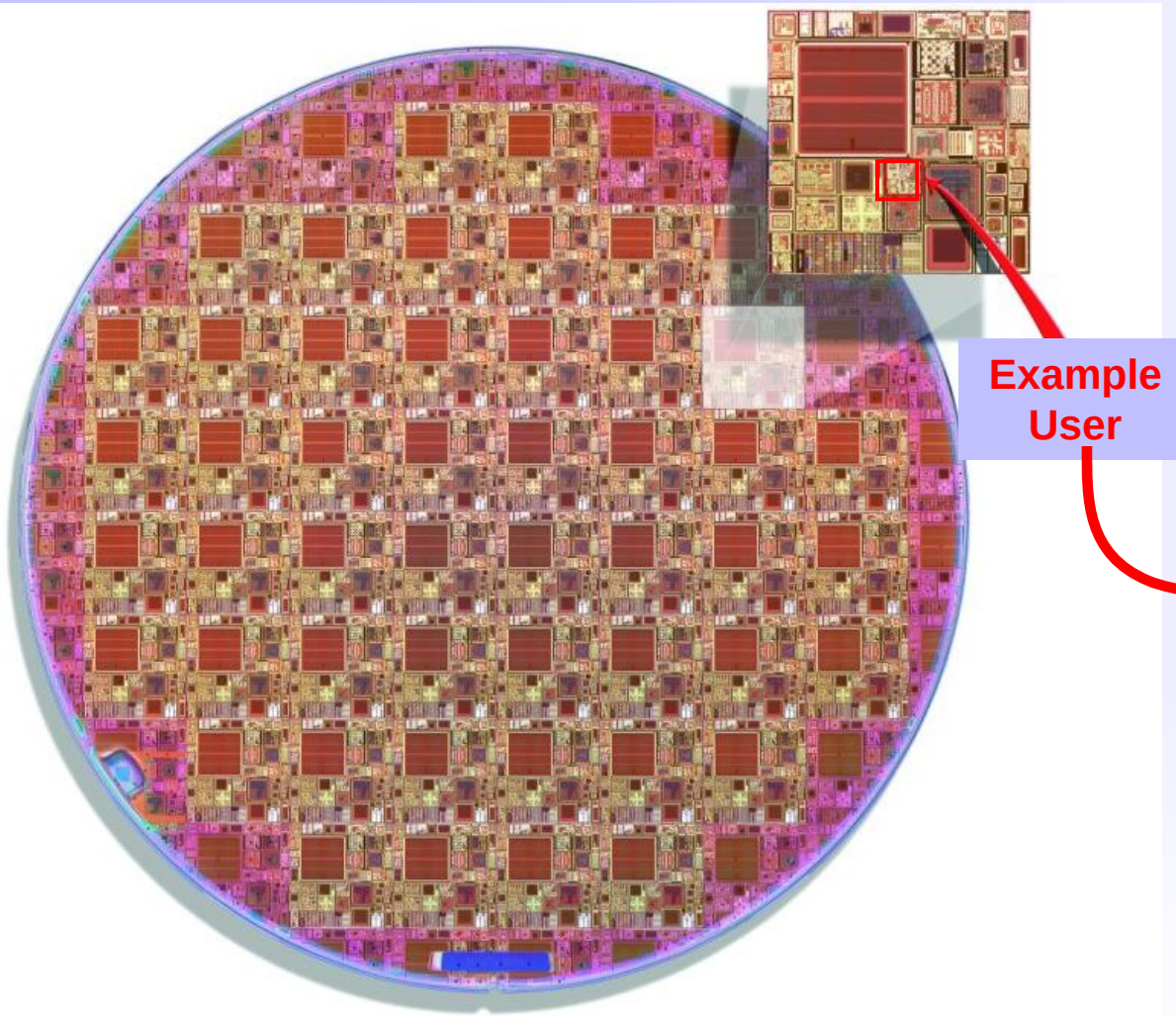
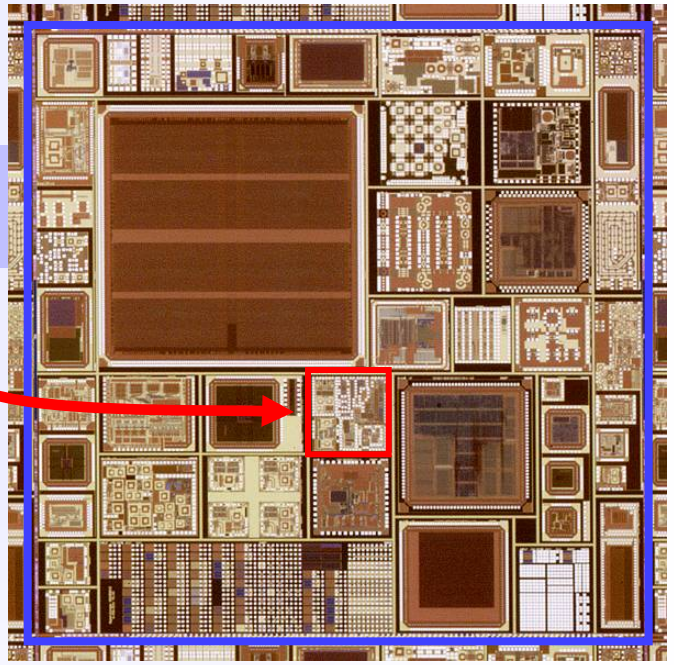
Overview

- MOSIS is Dedicated to Provide:
  - Low Cost Engineering Samples of IC Designs
    - Multi-Project Wafers (MPWs) – Quantities of Small to Medium
  - Production Service (COT/dedicated)
    - From 2 Wafers Only to 500+ Wafers/Yr
  - Support
    - Technical, e.g. Design Kits, Modeling, IP
    - Business, e.g. Pricing, Logistics
  - Single Point of Interface to Customers for Additional Services or Products Offered by Partner Vendors
  - Access to Production Proven Technologies
- Experience – 30+ Years of Providing Fabrication
  - Staff of 30 People – Design, Test, Admin, etc.
  - Long History with HEP Community (USA, Intl)

MOSIS Multi-Project Wafer

Many
Dedicated
Runs





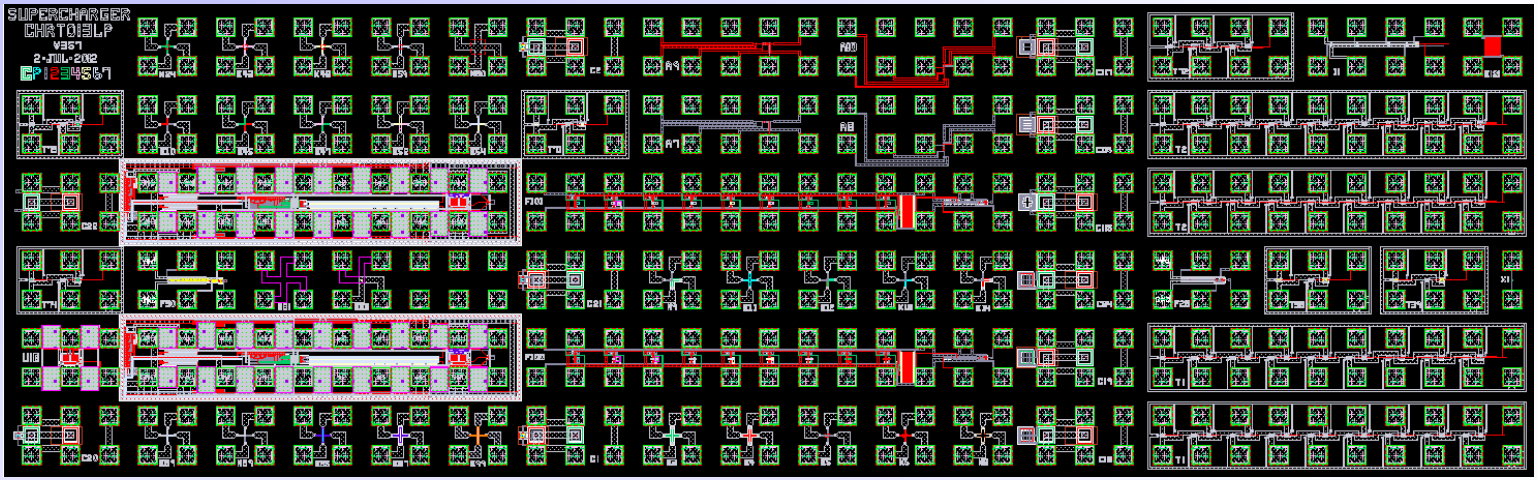
Multi-Project Reticule
~ 50 Different Designs

<u>Shared Costs:</u> Mask, Wafer, Foundry and Packager Interface

PDK & Library Support

- PDKs Available
  - Generated By Foundry
  - Multiple Design Tools Supported
    - Cadence, Mentor, Synopsys
    - Other Needed?
- Foundry Libraries
  - e.g. TSMC 65, 90, 130, 180nm
  - Standard Cells, IOs, etc.
- ARM/Artisan Libraries for Universities
  - GF 65nm LPe
  - IBM 8RF
  - TSMC 65, 130, 180 & 250 nm

MOSIS Process Monitor



- Sheet Resistance - 15 layers
- Via/Contact Resistance - 12 vias
- Inverters - 5 sizes
- Transistors- N/P* Enhancement - 34 sizes
- Transistors- N/P Thick Enhancement - 3 sizes
- Transistors- N zero Vt common - 3 sizes
- Transistors- Extended N Enhancement - 5 sizes
- Transistors- N/P Low Vt common - 3 sizes
- Capacitors - 27
- Ring Oscillators - Thin and Thick oxide
- Operational Amplifiers - 3

Develop run specific Spice model for MOSIS lead MPWs

Assembly and Test Options

- MOSIS Offers a Variety of Packaging Options
- Packages - QFPs, BGAs, etc. - Plastic, Ceramic
- Flip Chip Wafer Bumping (e.g. Third Party Vendors)
- Work with US-Based Medium Volume Vendors in Addition to High Volume Offshore Partners
- Functional Testing Available
- Optional – Most Customers WANT To Do Testing (Debug Designs)
- Work with Partners for Functional Testing
- Digital Testers – Advantest, etc.
- Mixed-Signal Testers - Teradyne, etc.

MOSIS
HEP Community Roadmap

IBM 130 nm
TSMC 250 nm

IBM SiGe
TSMC 65 nm

GF/TSMC 28 nm
GF/TSMC 24 nm
GF/TSMC 20 nm
GF/TSMC 10 nm

Today → Near → Future

GlobalFoundries Processes

Vendor	Feature Size	Process
GLOBALFOUNDRIES	28 nm	Future
	40 nm	Limited Access
	65 nm	Logic, RF
	0.13 µm	Logic, RF, HV
	0.18 µm	Logic, RF, HV, Memory
	0.35 µm	Logic, RF, HV, Memory

Supported GF Processes

Technology	Base Logic	Low Power Enhanced	RF CMOS	High Voltage	SiGe BiCMOS	Memory	2013 Schedule
28 nm	Future						
40 nm	Limited Access Currently						
65 nm	X	X					7 MPW runs
0.13 µm	X		X	X			8 MPW runs
0.18 µm	X		X	X	X	X	10 MPW runs
0.35 µm	X		X	X	X	X	4 MPW runs

IBM SiGe BiCMOS

Vendor	Feature Size	Process
IBM SiGe BiCMOS	90 nm	9HP (mid-2014)
	0.13 µm	8XP, 8HP, 8WL
	0.18 µm	7WL, 7HP
	0.25 µm	6HP, 6DM, 6WL
	0.35 µm	5HPE, 5PAe
	0.5 µm	5HP, 5AM, 5DM, 5PA

Also RF CMOS
8RF – 0.13
9RF – 90nm

Supported IBM Processes
SiGe BiCMOS

Technology	Process	Availability
90 nm	9HP	Mid 2014
0.13 µm	8XP, 8HP, 8WL	8HP MPWs - 6 per year
0.18 µm	7WL, 7HP	7WL MPWs - 6 per year
0.25 µm	6HP, 6DM, 6WL	No MPW runs
0.35 µm	5HPE, 5PAe	Some MPW runs
0.5 µm	5HP, 5AM, 5DM, 5PA	No MPW runs

SiGe vs. RF CMOS

- Maximum Application Frequency
  - SiGe Increased Operating Speed than RF CMOS
- Reduced Electronic Noise
- Lower Power Consumption
- Wafer Costs
  - Fewer Masks Required for RF CMOS Resulting in Lower Wafer Costs
  - As Geometry Scaling Decreases,

    # Masks for RF CMOS Increases

    Bringing Wafer Costs of RF CMOS Closer To SiGe

Current TSMC Processes

Vendor	Feature Size	Process
TSMC	40/45nm	Logic/MM
	65nm	Logic/MM
	90nm	Logic/MM
	130nm and up	Logic/MM

Supported TSMC Processes

Technology	Standard Logic	RF CMOS	Mixed Mode	MiM	Low Voltage	High Voltage	Low Power	ESD 5.0 V
28 nm	Future							
40 nm	Restricted Access Currently							
65 nm	X	X	X	X				
90 nm	X	X	X	X				
0.13 µm	X	X		X	X	X		
0.18 µm	X	X	X	X	X	X	X	
0.25 µm	X	X	X	X				
0.35 µm	X	X	X			X		X

Community Access

- Work With HEP Community in Regard to Minimum Quantity Orders
- Remain Flexible to HEP Community Needs
- Address All Levels Needed
  - Prototype – MPW
  - Medium – MPW / Taxi
  - Dedicated – Continued Availability
- Suggestions
  - HEP-MOSIS User Group (Web Based)
  - Workshops

Current & Future IC Design Organization

- MOSIS Education Program (MEP)
  - Seeding Future Designers Across USA
- Collaborations With Other International Programs
  - i.e., CIC, CMC, CMP, Europractice, IDEC, VDEC, etc.
- MOSIS Here For 30+ Years
- Will Continue For Many More

MOSIS Summary

Working with MOSIS As Their Fabrication Partner,

HEP Designers Speed Their Route to Design Implementation:

- **Access to Broad Range of Production Services**
  - MPWs → Low Volume Production
  - Foundry/Test/Packaging
  - Leverage Network of IP/Design Partners
- **Strong technical support**
  - 30+ Years Experience (50,000+ Designs Managed)
  - Can Provide Direct Answers to 98% of Technical Questions
- **Build On Long Term Relationship With HEP Community**
  - Future Access
  - Workshops, Web Forums, Training, etc.
  - Help Us Help You

HEP-MOSIS Dialogue

- Open To Further Dialogue
- How Can MOSIS Best Support the HEP Community?

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