IC processes currently in use & projection into the future

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U.S. DEPARTMENT OF ENERGY

Fermilab

Outline

- Transition of μelectronics to nanoelectronics
  - A few facts from industry
  - Scaling or something else?
  - μElectronics for radiation detectors
    - More tasks
    - Scaling in HEP
- Issues in HEP μelectronics
  - Legal
  - Budgetary
  - Organizational
- Current nodes
- μ / nElectronics 2 options: 3D-IC, V(V)DSM
- Integration readout+sensor SOI
- Conclusions

~~µElectronics~~ nanoElectronics Industry

- Typing in Google a query: *"10 nm CMOS process"*

Update: Intel to build fab for 14-nm chips

Mark Lapedus

2/18/2011 3:01 PM EST

EE Times News & Analysis

Intel Corp. announced plans to invest more than $5 billion to build a new chip manufacturing facility at its site in Chandler, Ariz. SAN JOSE, Calif. - Continuing its aggressive fab expansion efforts, Intel Corp. on Friday (Feb. 18) announced plans to invest more than $5 billion to build a new chip manufacturing facility at its site in Chandler, Ariz.

Initially, Intel's new Arizona factory, designated Fab 42, will be a 300-mm plant. It will also be compatible for 450-mm-if or when that wafer size is ready, according to the chip giant. Fab 42 will process wafers at the 14-nm node-and perhaps beyond. This is said to be the world's most advanced fab. Construction of the new fab is expected to begin in the middle of this year and is expected to be completed in 2013.

"The investment positions our manufacturing network for future growth," said Brian Krzanich, senior vice president and general manager of manufacturing and supply chain at Intel, in a statement. "This fab will begin operations on a process that will allow us to create transistors with a minimum feature size of 14 nanometers."

- HEP, photon science, medical imaging communities – front-end ICs for radiation detectors - are a few generations behind of the industry edge;
- Needs, targets, money are different in science comparing to consumer electronics
- Not developing new processes but cleverly leveraging searching for optimum

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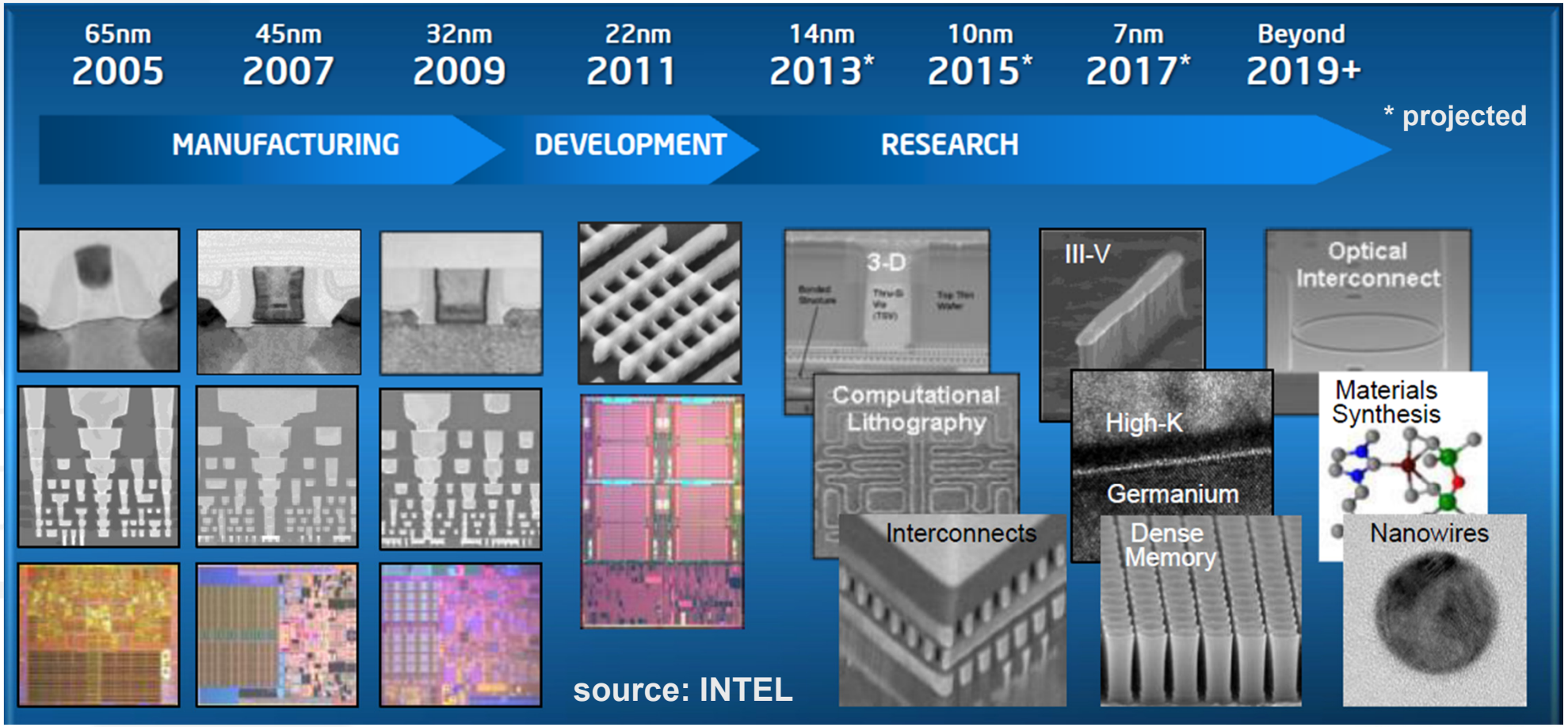
- Moore's Law is not a law of nature; it is just an expectation of ceaseless innovation – innovation stimulated by customers' needs
- Industry is expected to continue through focused research, rapid development and through exorbitant investments in production
- Name of the game is scaling and it is ever more about materials research



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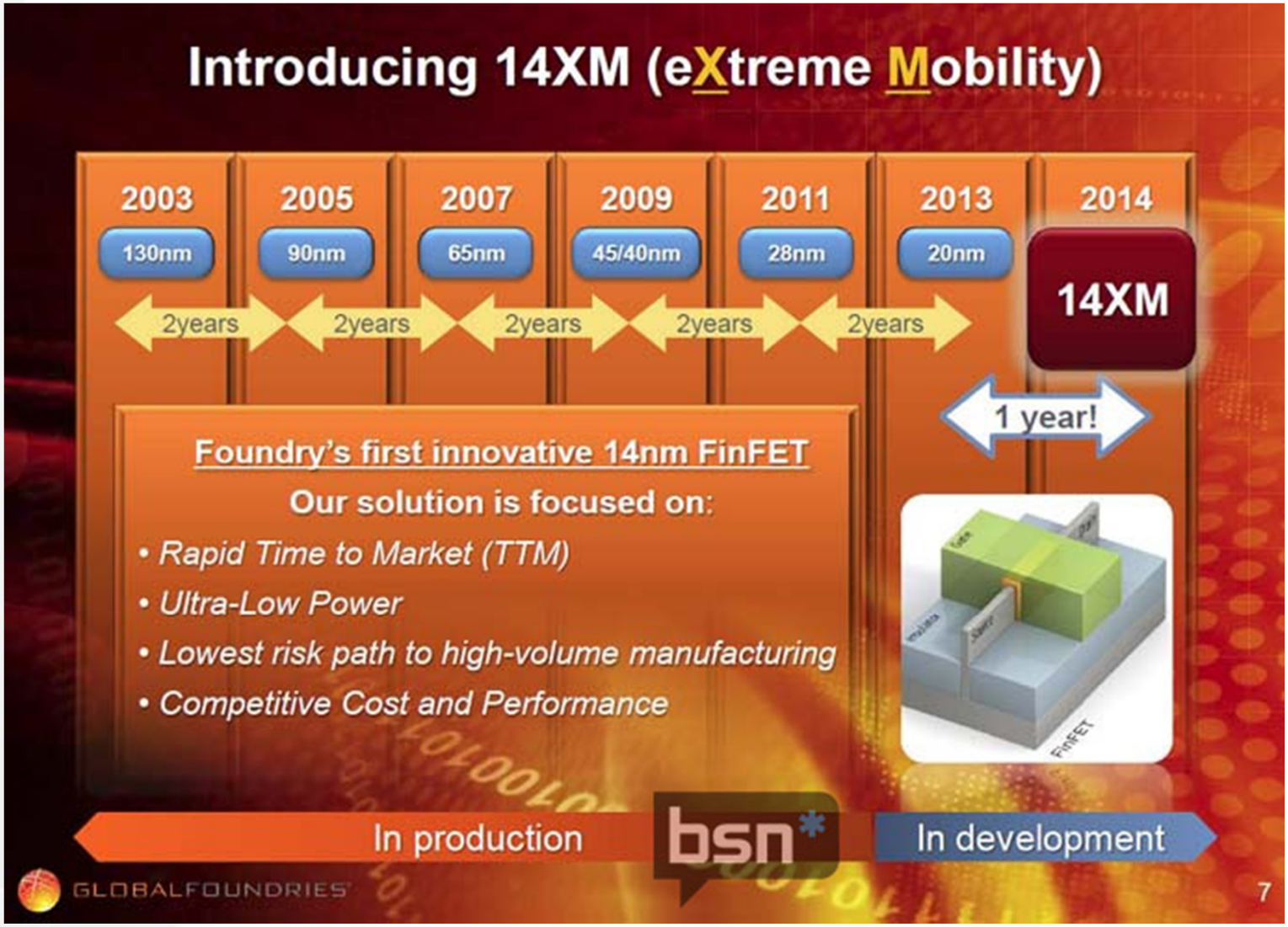
- at the head of the race, only a few players are present because only a few are able to withstand the imposed pace and costs, but they go head to head



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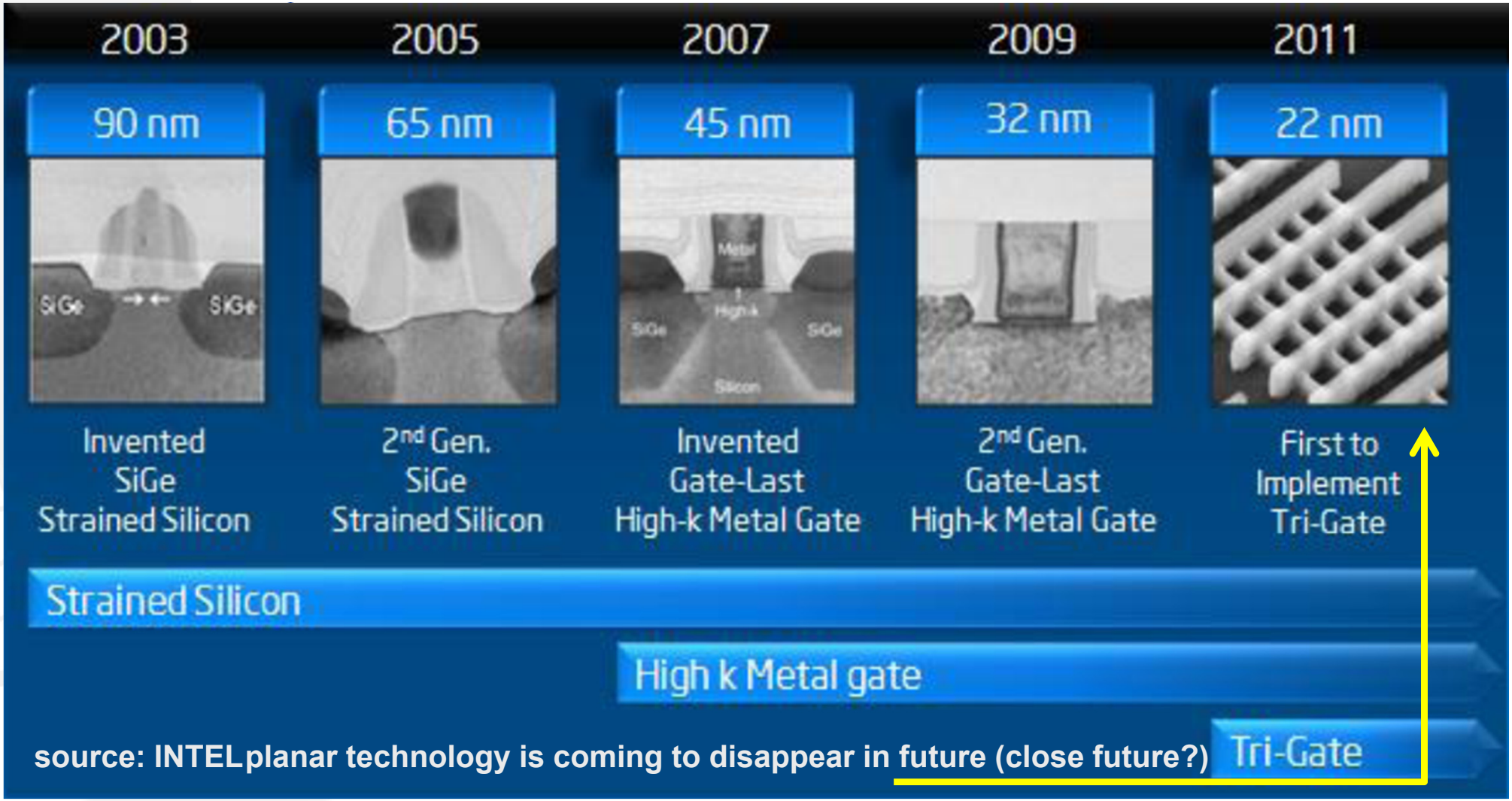
- around year 2004 scaling started breaking apart; now advancing through innovation
- with a reduction of node size is getting harder on a good quality performance of



source: INTEL planar technology is coming to disappear in future (close future?)

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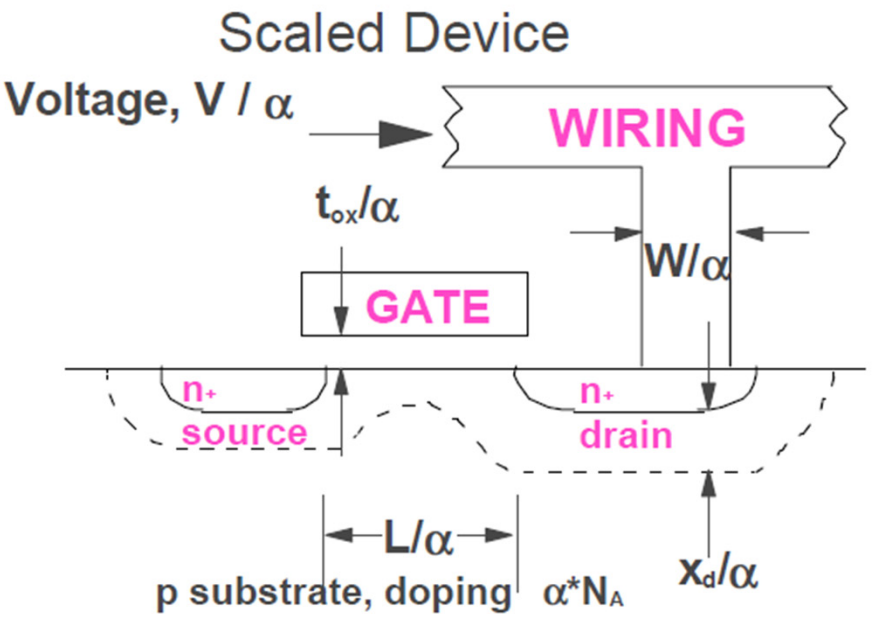
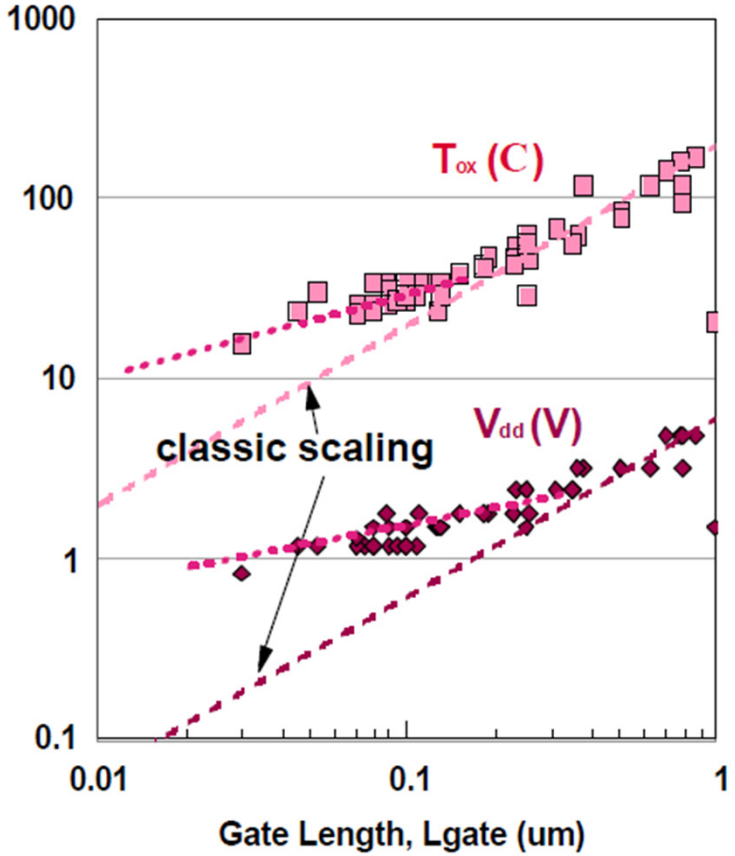
- It is not really classical scaling… is it saving analog?





SCALING:		*RESULTS:*	
Voltage:	V/α	Higher Density:	~α^2
Oxide:	t_{ox}/α	Higher Speed:	~α
Wire width:	W/α	Power/ckt:	~$1/\alpha^2$
Gate width:	L/α		
Diffusion:	x_d/α	**Power Density:**	**~Constant**
Substrate:	$\alpha * N_A$		

- Why deviate from "ideal" scaling
  - unacceptable gate leakage/reliability
  - additional performance at higher voltages
- What is the consequence of this deviation?
  - **a dramatic rise in power density**

from Bernard S. Meyerson, IBM

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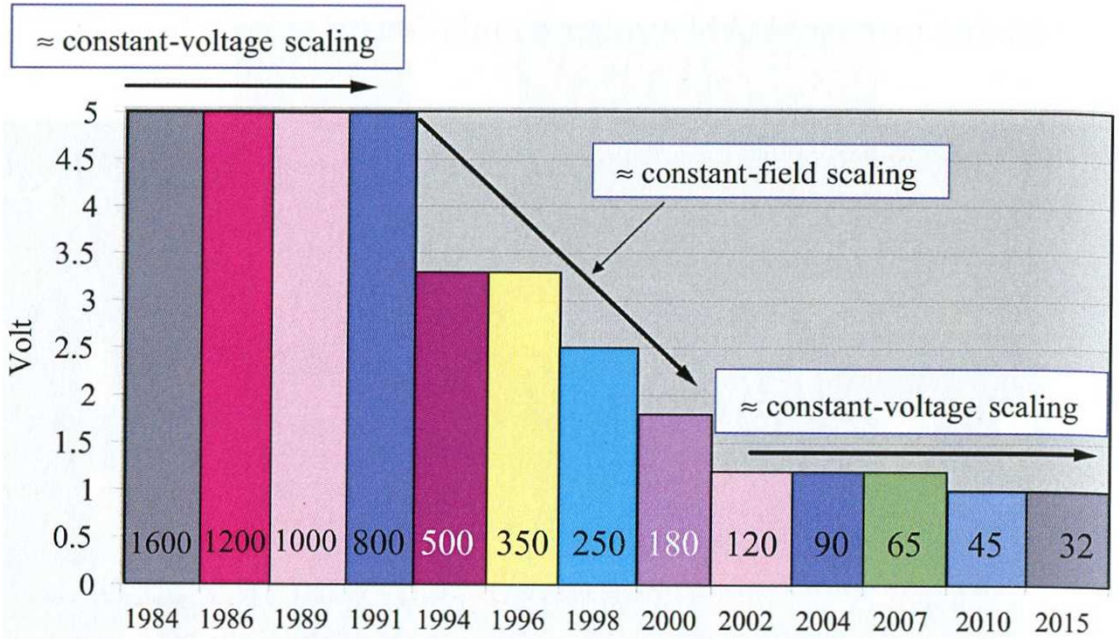
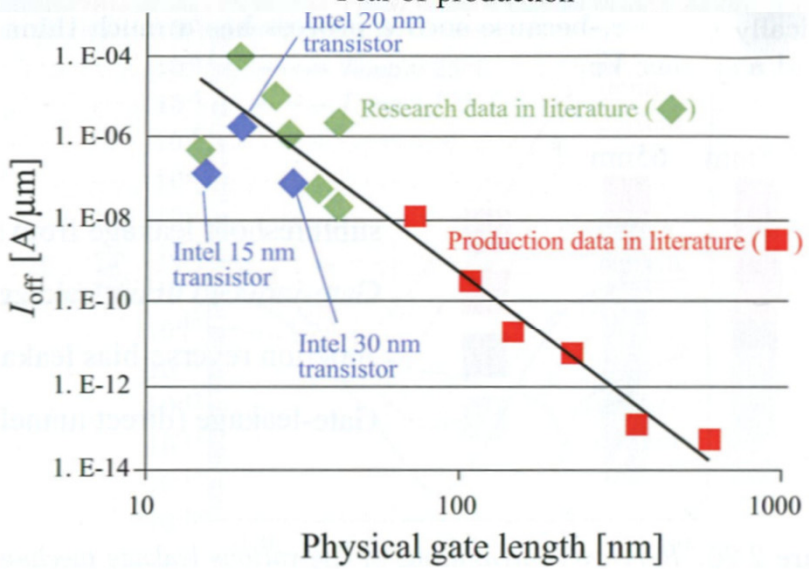
- Scaling driven by const. voltage or field?



* projected

- Unwanted results of scaling = leakage currents



from H. Veendrik, Nanometer CMOS ICs

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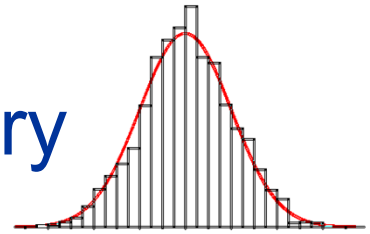
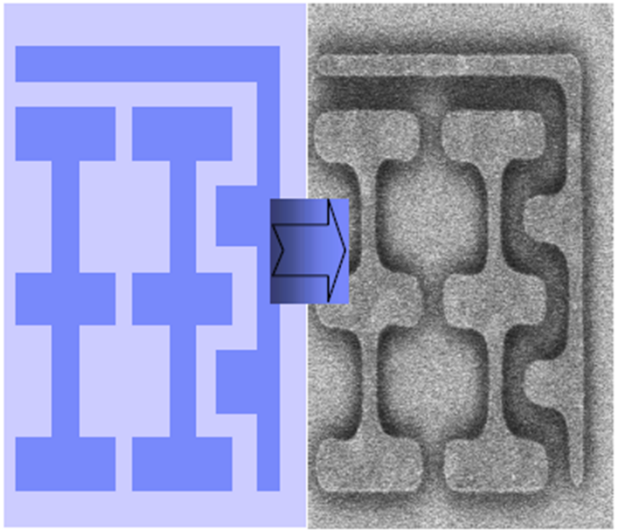
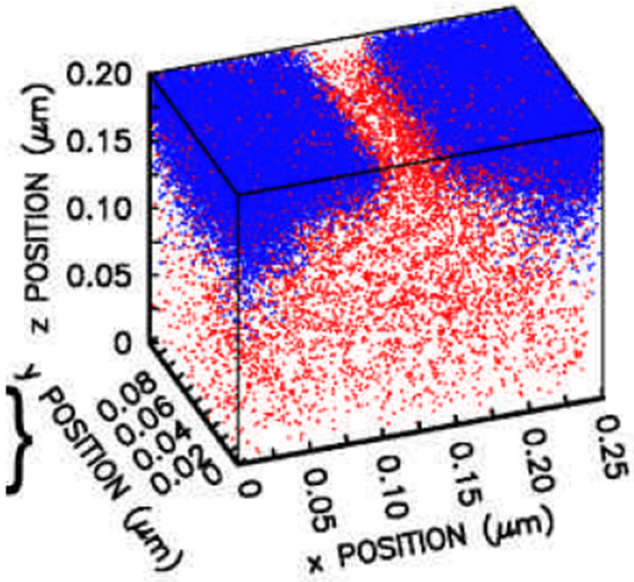


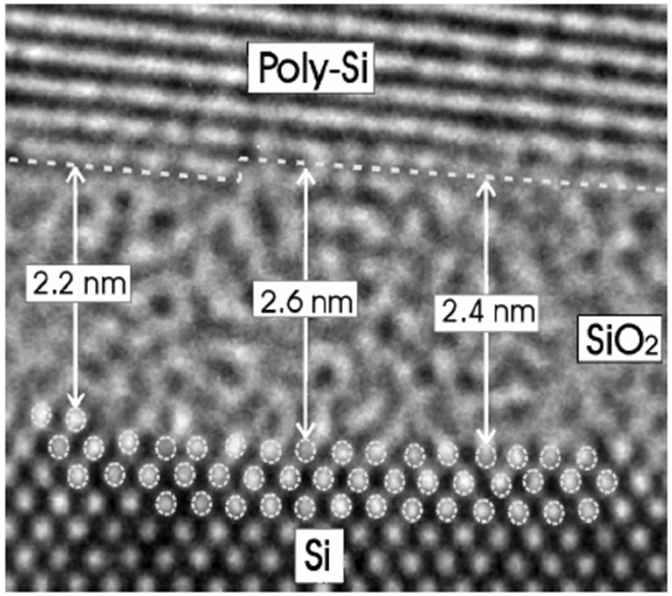
- Exposure to increasing and unavoidable VARIABILITY



Litho-induced variability



Random dopant effects



Oxide thickness

Interconnect CMP effects

*D. J. Frank et al, Symp. VLSI Tech., 1999

µElectronics for radiation detectors

- at nodes L<100nm how front-end designs will be made is changing: digital systems including redundancy and capabilities of corrections at various levels with embedded analog blocks (necessitated by the need to automate and comply with complex rules)

- Can analog still be achieved?

	250nm RF	130nm RF	90nm LP (low power)	65 nm RF
t_{OX} physical/effective	5nm/6.2nm	2.2nm/3.12nm	2.1nm/2.8nm	??/2.6nm
K_a $(C_{OX} \cdot \mu)$ NMOS	330 uA/V^2	720 uA/V^2	800 uA/V^2	740 uA/V^2
Vdd	2.5V	1.2V (1.5V)	1.2V	1.2V (1.0V)
g_m/g_{ds} Weak Inv.	70	30	18	14
Peak ft	35 GHz	94 GHz	105 GHz	120 GHz

…….. oxynitride ……..

from Pierpaolo Valerio, CERN

µElectronics for radiation detectors

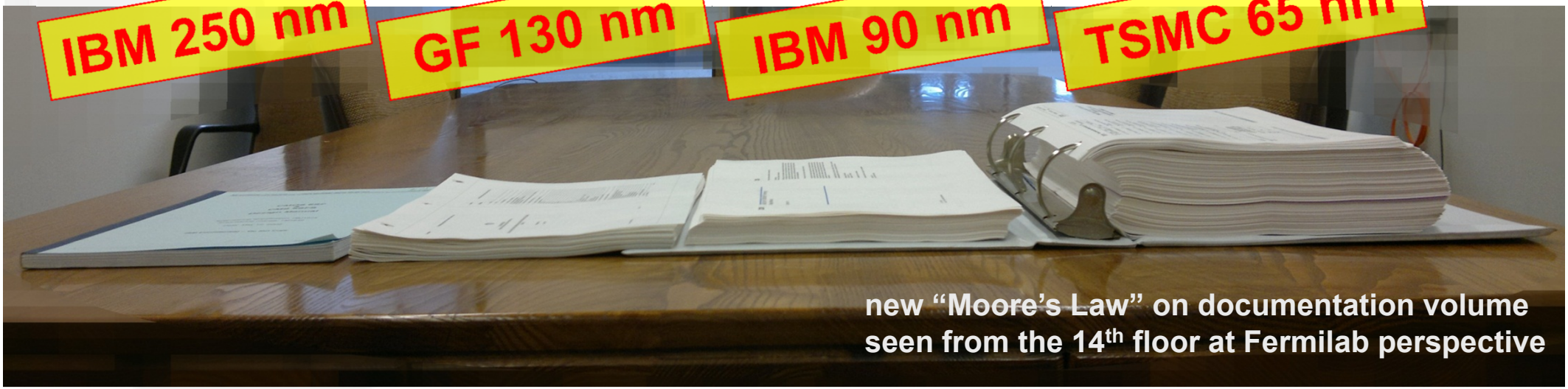
costs

Costs of engineering run		
Technology	node 130nm (8”)	node 65nm (12”)
“foundry A” – planar 2D	$500k	$1,900k
“foundry B” – planar 2D	$250k	$600k
3D-IC	$350k	?

My remarks towards smaller ‘L’:

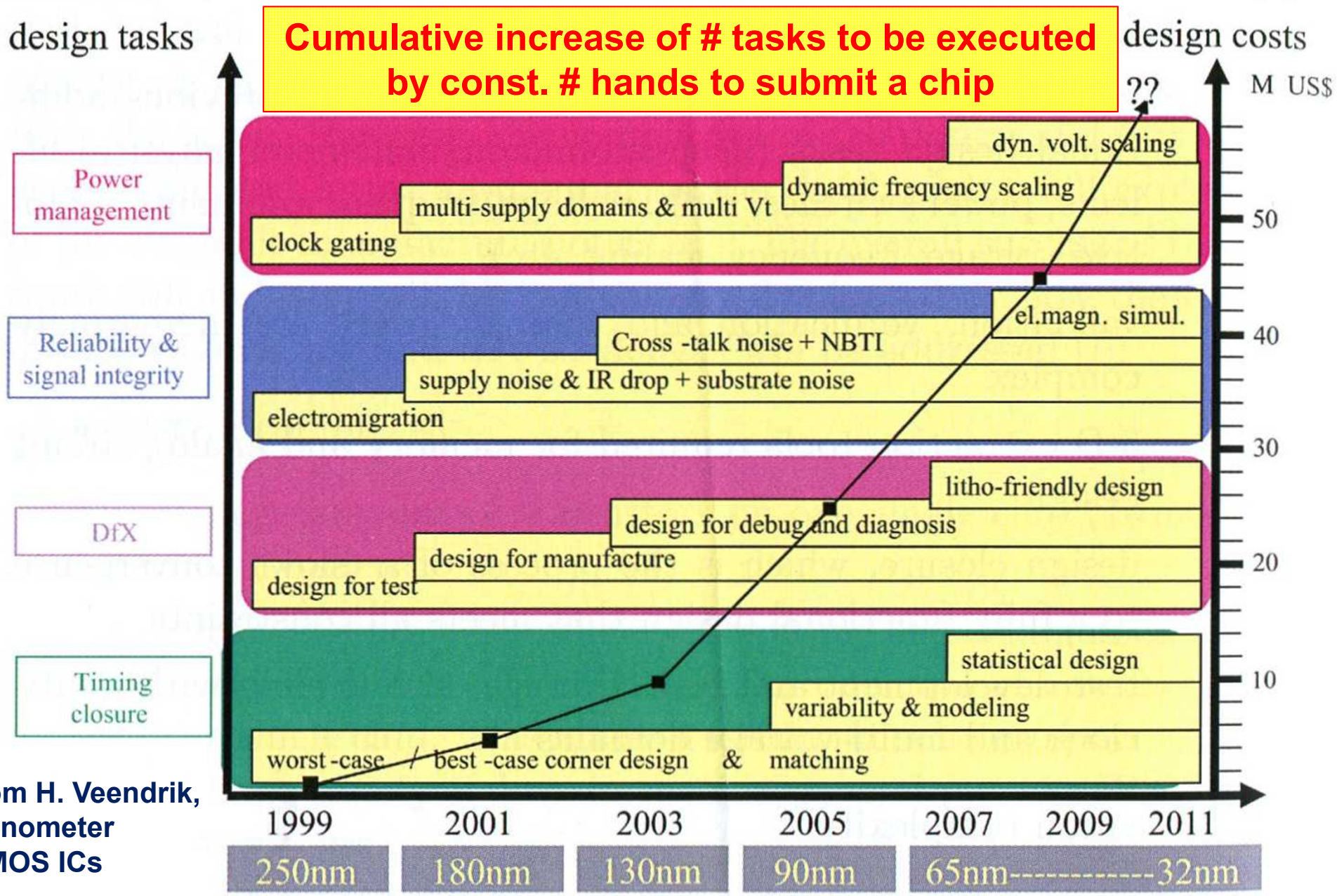
- Much more complicated structures
- Increasing number of design tasks
- Higher cost
- Imposing increasing demands of people’ skills
- Impossible designing without specialized and expensive CAD/EDA tools

and learning



new “Moore’s Law” on documentation volume seen from the 14th floor at Fermilab perspective

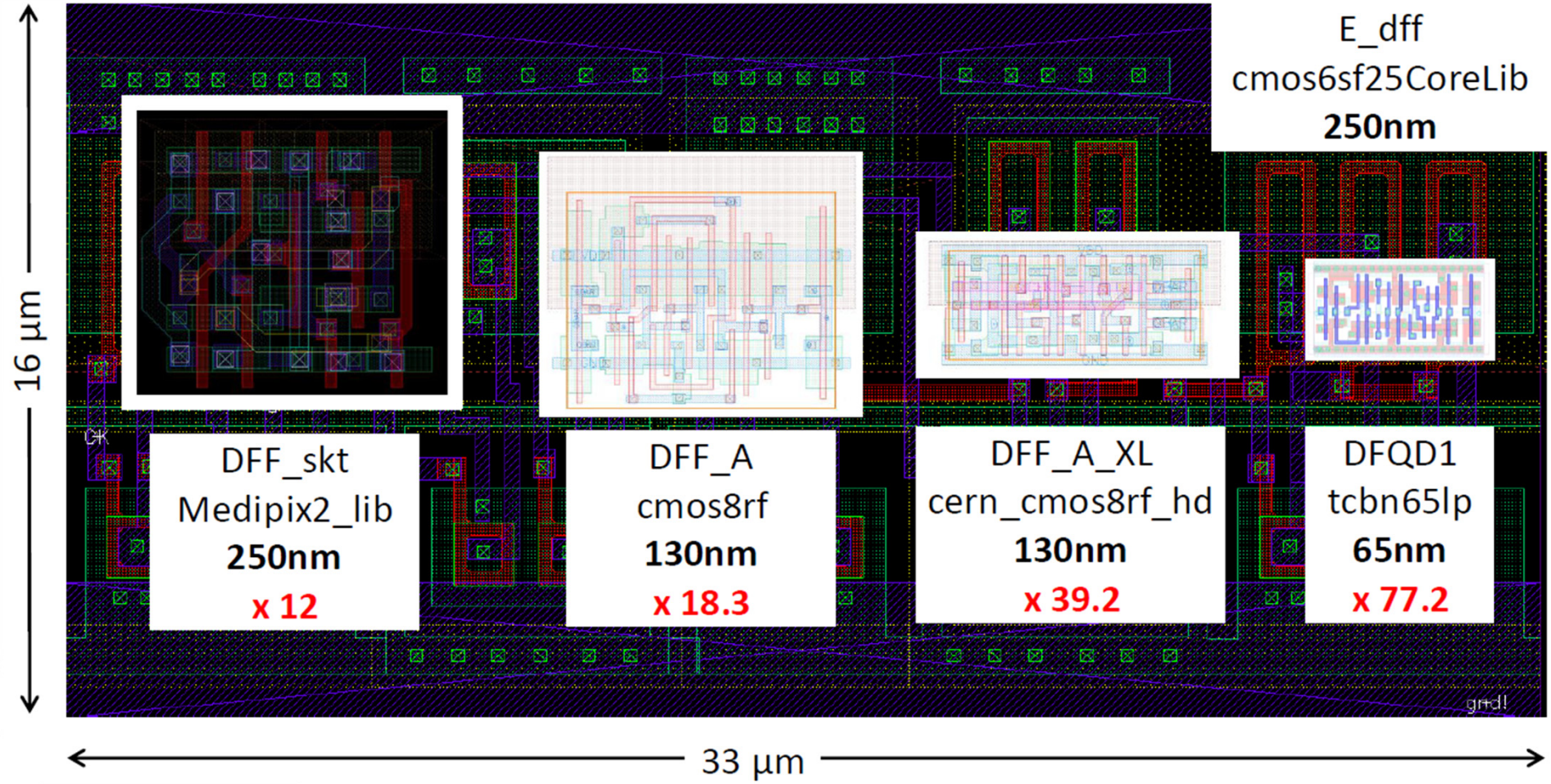
µElectronics for radiation detectors



from H. Veendrik, Nanometer CMOS ICs

µElectronics for radiation detectors

Technology scaling in HEP constrained criteria other than just size



Radiation hardness in 250nm was limiting achievable functionality
In 130nm + 65 nm we gained - we need to learn how to use the real estate

from Xavier Llopart, CERN

Issues in HEP μElectronics

Ability of coping with technology scaling in US HEP is constrained by:

- **Indemnification (legal paralysis for using commercially developed but offered free of charge IPs mainly standard cells) – not counter-matched by resources to develop necessary components in-house**
  - **Full library of standard cells probably 0.5 FTE / node/process (*risk*)**
  - **Characterization of standard cell libraries for RTL - $20k-$40k if done by CAD vendor or buy licenses for Encounter characterization in-house**
- **Affordability of tools - tools budgets of ASIC groups from national labs are >$500k/year/group for mixture of Cadence/Mentor tools and is not buying all what is available elsewhere**
  - **On one hand: to cope with more advanced designs forces getting licenses for new sets of tools (*vendor politics is muddy and often misleading*) - *where is time for learning?***
  - **On second hand tools for which licenses were required often don't work with smaller L nodes, ex. parasitics extraction in 130nm works with ASSURA 300 – in 65nm ASSURA 330 (or XL) is needed, which translates to new $$ - *patching hole rather than building a new road***
- **Spinning wheels on ice - efforts going to catch up, maintain, etc. without being able to deliver new designs**
  - **Underinvestment in tools, scattered resources not reaching critical mass required for full project or exploration a few variants to chose best at the end – *can you do this project with 0.5 FTE?***

Legal paralysis together with costs of CAD/EDA tools increases costs and may lead to exclusions of US labs from forefront international projects

Issues in HEP μElectronics

Continuation: ability of coping with technology scaling:

- **Export control (legal uncertainty and barriers are unknown to ASIC developers but consequences of breaching the rules can be severe)**
  - **Actually all circuits designed with processes L ≤ 130nm can be subject of export control restrictions, unless "fuse circuits" are implemented – can you imagine reticle size ROIC for edgeless and seamless detectors with TSVs for no waste of chip area with radiation blast fuses?**
  - **What was designed to protect is becoming a barrier - experiments are located world-wide (less in the US) and chips must pass across the boarders**
- **Inter laboratory collaborations – costs of projects are high (advanced nodes + sensors + technology development gets quickly to $M)**
  - **Added complexity of designing in VDSMs asks either increasing group sizes or strngthening inter-laboratory collaboration and/or work for others**
  - **Overheads on manpower makes dedication of reasonable resources on projects for other labs unaffordable – thus projects may face either underfunding or abandonment**
- **Non-HEP and share developed libraries (returning questions)**
  - **non-HEP projects based on HEP-gained experience are crucial to maintain groups and their skills**
  - **Multiple attempts for HEP IP of common use libraries of blocks – not too much of success except when working in collaboration on active projects**

- **Missing services capable of handling export control issues: "here you have ITAR classification, what is your number?" - I don't know, I want to design ASICs…**
- **Typical legal office help: "you cannot do that" *(there are exceptions)***

Issues in HEP μElectronics

Continuation: ability of coping with technology scaling:

- **Mentality of "*full custom, mixed mode*", incorporation of IP blocks – sensitive subject - HEP chips are proud to be full custom - is it still possible to maintain this scheme under current situation: low projects budgets, short deadlines, overload of groups?**
  - **reservation, because often special needs due to extreme environments: radiation, cryogenic reliability, low power, etc.**
  - **there are some examples, I interviewed a group who did it:**

    1) Purpose of the block, its size, and major terms of the contract:

    High-speed SerDes for serialized IO with data rate up 2.4Gbps

    2) Technology for the block and its portability to other processes nodes:

    Acquired for 65nm technology only

    3) Terms of the contract:

    Single use license with an additional price/chip for large production

    4) What happens if the implementation doesn't work:

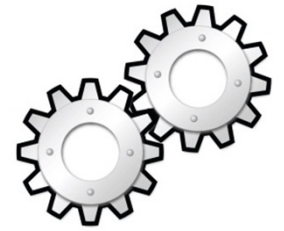
    IP provider guarantees working implementation

    5) Why did you decide to buy IP and not to develop it on your own?

    Because the cost of internal development would be incredibly higher and because the project schedule would not allow for internal development. The acquired IP is a typical IP that requires a long and careful design. This was the main motivation for acquiring it.

Ironically, to be able to work with IPs – tools allowing floor-planning, automated P&R, timing sign-off tools

Current nodes



US HEP ICs: designs current in 2013 and R&D

Node	Process	BNL	FNAL	LBNL	SLAC	SMU/U. Penn	Comments
350nm	AMS CMOS, SiGe BiCMOS and HV		X	X			MOSIS / Europractice
250nm	TSMC	X		X	X		MOSIS
	IBM			X			MOSIS
180nm	TSMC	X			X		MOSIS
	UMC CIS			X	X		Europractice
130nm	TSMC				X		MOSIS
	IBM	X		X		X	CERN / MOSIS
	IBM SiGe		X				MOSIS
	GF		X				Shuttle MPW
65nm	TSMC		X	X	X		MOSIS
40nm	TSMC		X				Europractice
28nm	TSMC				X		MOSIS
250nm	Peregrine SOS					X	MOSIS
200nm	LAPIS FDSOI		X	X			KEK MPW
800nm	Telefunken HV			X			

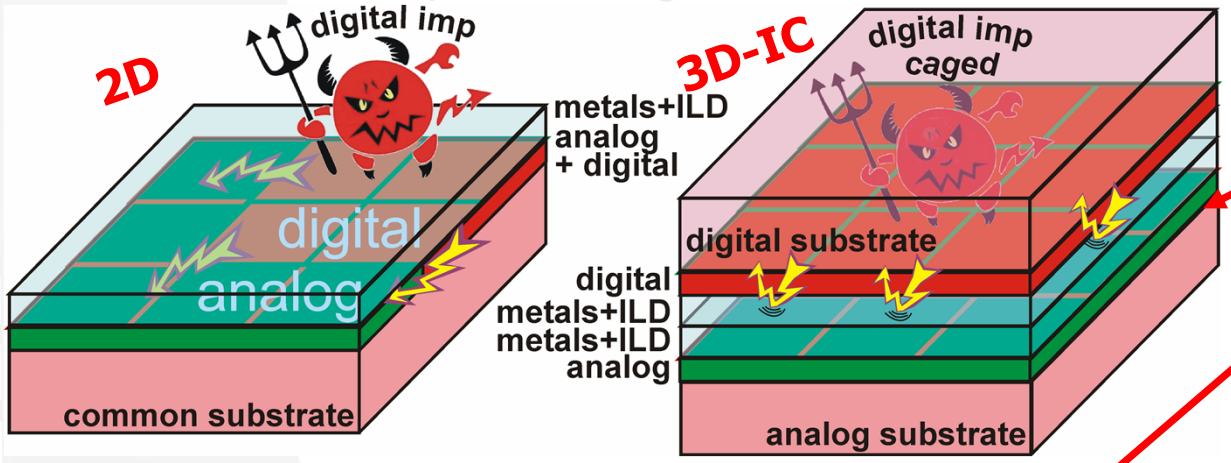
Table may be incomplete but concentration 250nm-130nm

option 1: 3D-IC

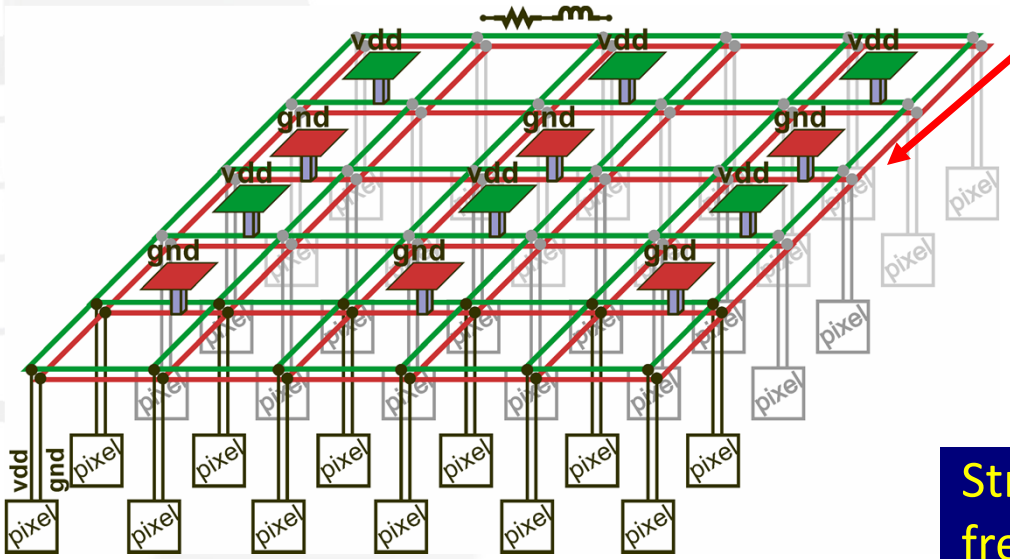
µ/nElectronics: 2 possible directions

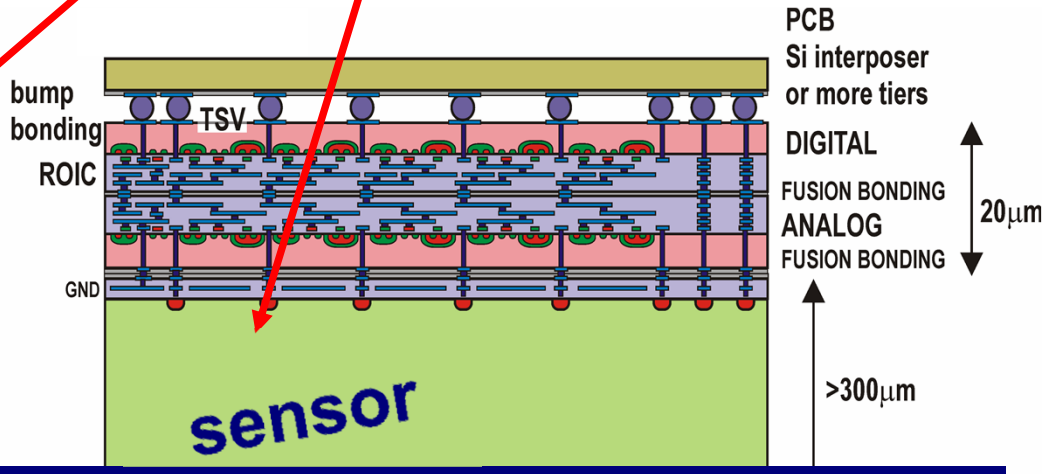
Why?

- 3D-IC offers a transformational change to address current road-blocks in advancing fine-grained detector, and with in-situ processing



- 3D ROICs - complete separation of digital activity from low-noise analog parts
- 3D ROICs - uniform distribution of power supply and I/O pads on the back side
- ROICs can be integrated with sensors without bump-bonds





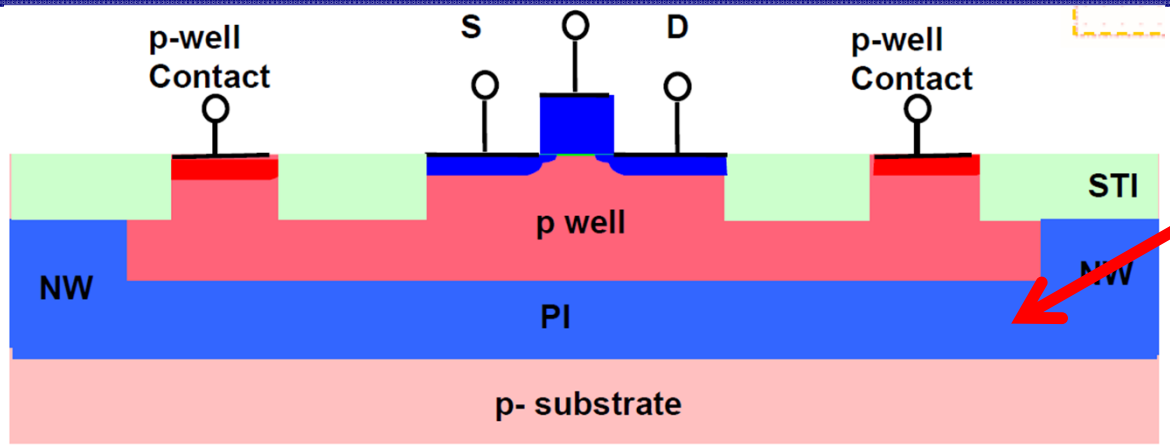
Strategic direction: 4 side buttable, dead-area-free detectors

Comparing 3D-IC isolation to options in 2D

Why?

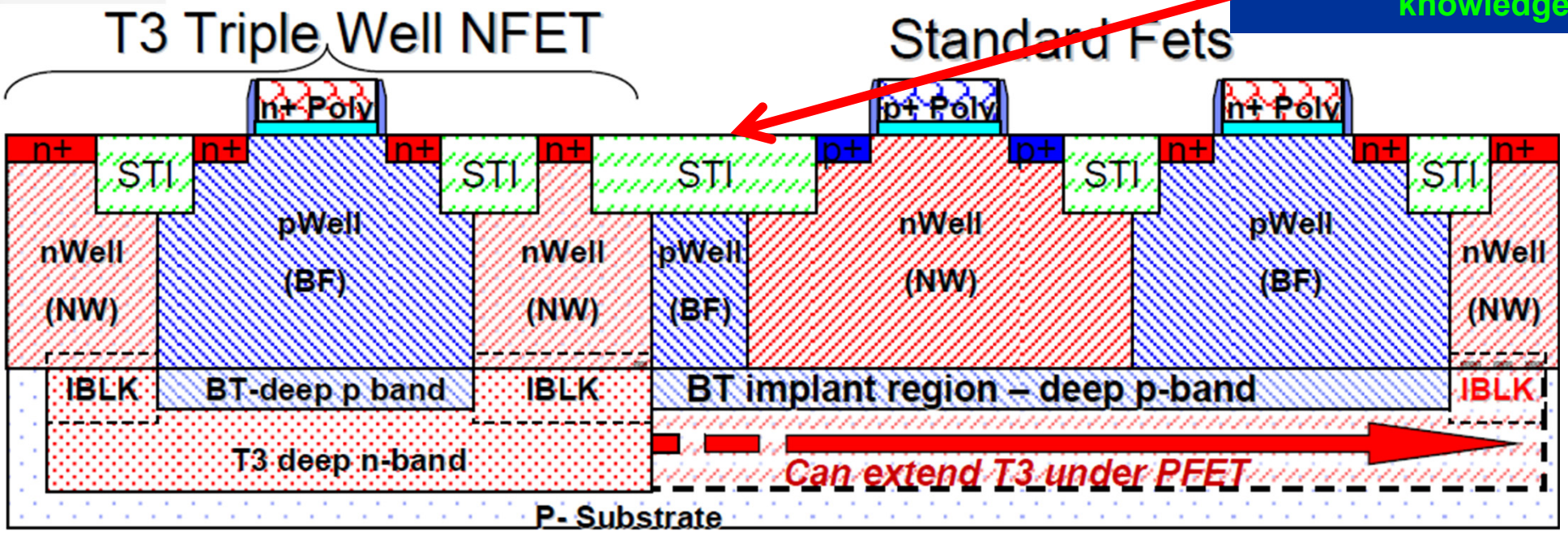
- Designing heavily digitally loaded large area Mixed-Mode front-end chips without good isolation may be challenging

Isolation of Analog from Digital



Triple-well isolation offered in most of planar technologies 250nm, 130nm, 65nm,…

Quad-well isolation offered in only in IBM 130nm (to my knowledge



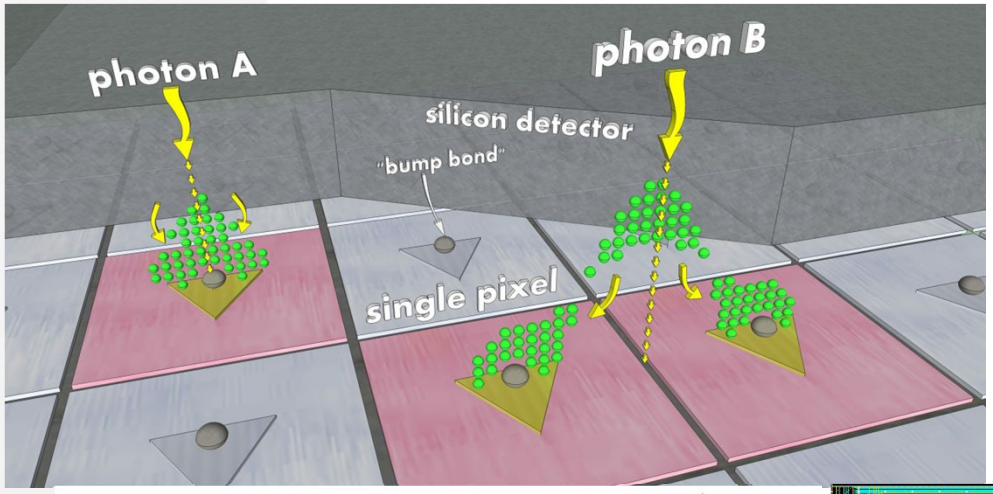
option 2: VVDSM

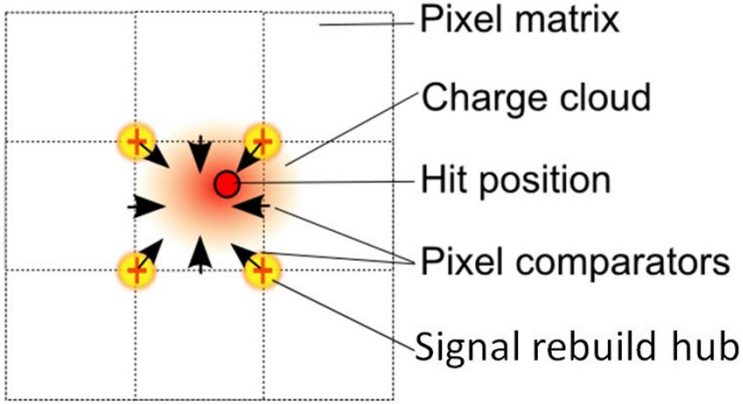
µ/nElectronics: 2 possible directions

A Pixel Readout Chip in 40 nm CMOS Process for High Count Rate Imaging Systems with Minimization of Charge Sharing Effects

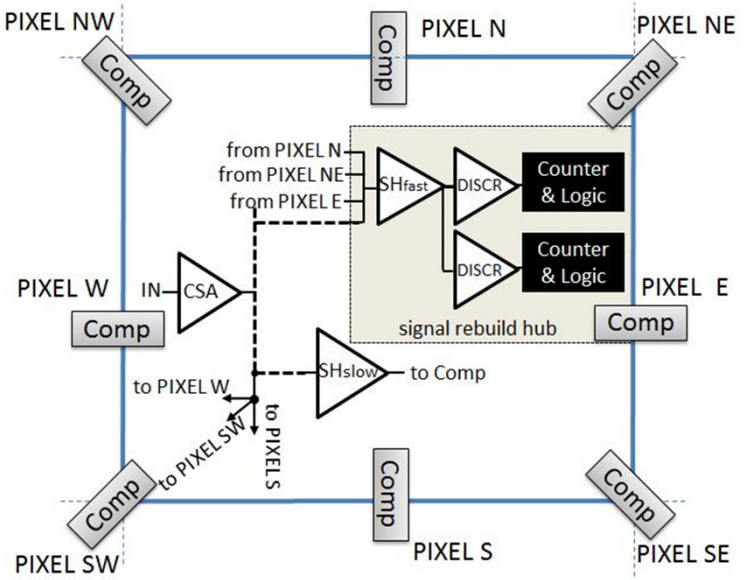
P. Maj, P. Grybos, R. Szczygiel, P. Kmon and G. Deptuch

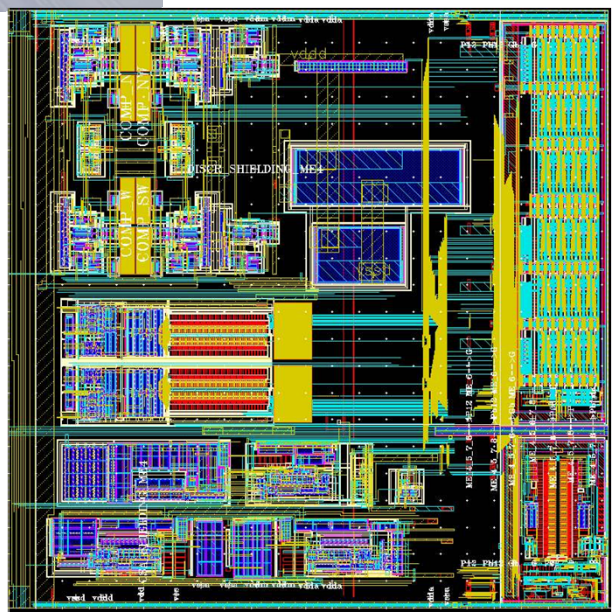
NSS 2013 – if accepted





C8P1 algorithm





Single pixel: front-end electronics diagram and layout - layers up to MET2 (100x100µm^2)

Complicated algorithm + test structures – still a lot of free space in single pixel !

which VDSM?

Costs:

TSMC 65nm CMOS 1PM9 - $6.9k / mm²

GF 130nm CMOS 1P8M - $1.1k / mm²

-----o----

TSMC 40nm CMOS = $\sqrt{2}$ ×TSMC 65nm

cost difference between 65nm and 40nm is moderate
performance of 40nm is better and more towards future

- **increases density of transistors /μm² and more in small space ("intelligence in- situ)**
- **follows industry trend (design heavily tools aided), necessary for links and w-sampling**
- **is attractive (research) for younger designers**
- **is not itself a transformational change, and to be used really when necessary**

40nm:

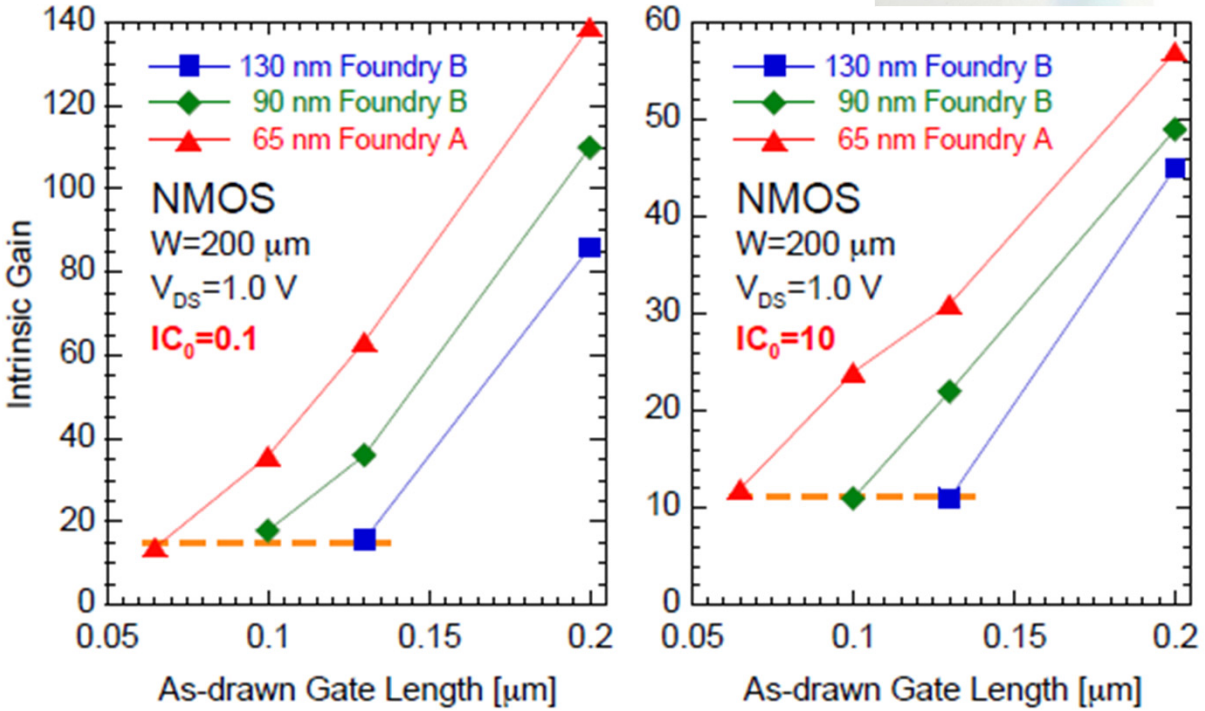
- **193nm immersion photolithography, performance-enhancing silicon strains, and extreme low-k (ELK) inter-metal dielectric (still oxynitride gate dielectric and poly gate – but some processes high-K and metal gate)**
- **doubles the gate density of the 65nm process with significantly lower power and cost /die.**
- **provide more than twice the density at the same leakage and more than a 40 percent speed improvement compared to TSMC's 65nm process.**
- **difficulty for designers: transistors on grids, layout for lithography … but not much worse than 65nm,**

µElectronics in radiation detectors

- It represents the maximum gain obtainable from a single transistor

$$Intrinsic\ Gain = \frac{g_m}{g_{ds}} \propto \alpha L$$

  - g_m channel transconductance
  - g_{ds} output conductance
  - α scaling factor

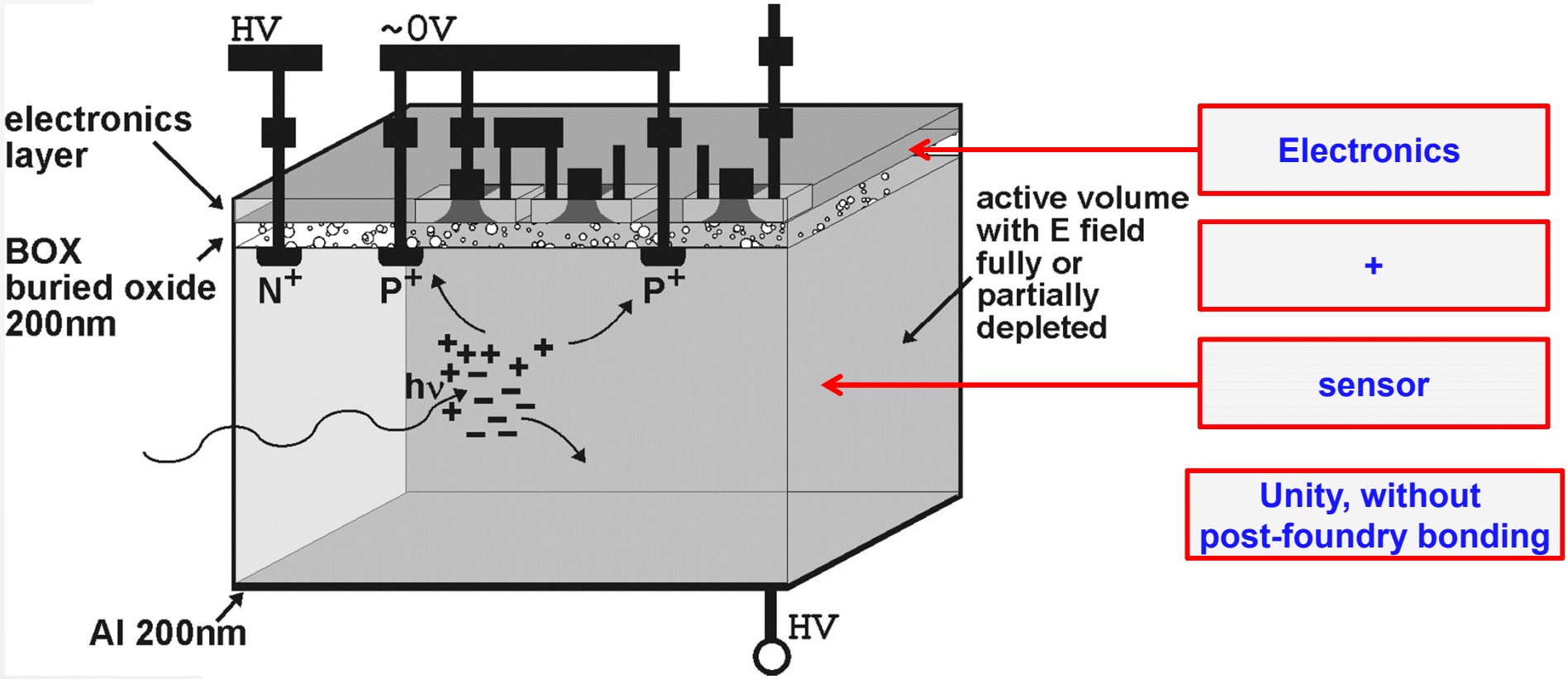


- Devices in the plot are biased at the same inversion level expressed by the Inversion Coefficient $IC_0 = I_D/(I_Z^* W/L)$ where I_Z^* is the characteristic normalized drain current
- The intrinsic gain (for LP and GP devices)
  - is proportional to the channel length
  - is maintained across technology nodes (L_{min} scales by the same factor α)

from Massimo Manghisoni, INFN

Silicon On Insulator (SOI) pixels

- Collaboration established with KEK and under a Japan-US agreement (MoU 2007) on monolithic SOI devices + OKI/LAPIS (industrial partner).
- SOI pixels are a kind of naturally 3D integrated, ready for further stacking



process was modified from a commercial FD SOI process to get shielding (nested wells and double SOI)

Other, now matured, MAPS technologies are available, e.g. based on quad well Towers Semi.

Conclusions

- **Access to processes is easy through Si brokers,**
- **Organized, standardized access through negotiated agreements is worth attempting, but more important is to remove various barriers and create friendly environment,**
- **Under current, very quickly changing circumstances (economy driven) special agreements may not result in more security than through brokers,**
- **Going into 65nm is not aggressive – it is unavoidable – but it is expensive for the HEP community (costs of fabrication – but also people, groups accumulating know-how, x-boundaries collaborations!),**
- **HEP getting to 65nm in 2013 is 3-4 generation behind industry (250nm in 2000 was 1 generation behind),**
- **There are some groups looking at 40nm nodes for readouts (EU funding),**
- **3D-IC is becoming viable and accessible – it is actually unavoidable – we may not need multi-stack chips but 3D-IC techniques for achieving detector assemblies are obvious,**
- **Is VDSM really the only solution? 180nm, 130nm allow satisfying a lot of HEP needs with more efficient costs – visible through the HEPIC workshop,**
- **Will lagging behind industry be attractive for young designers?**