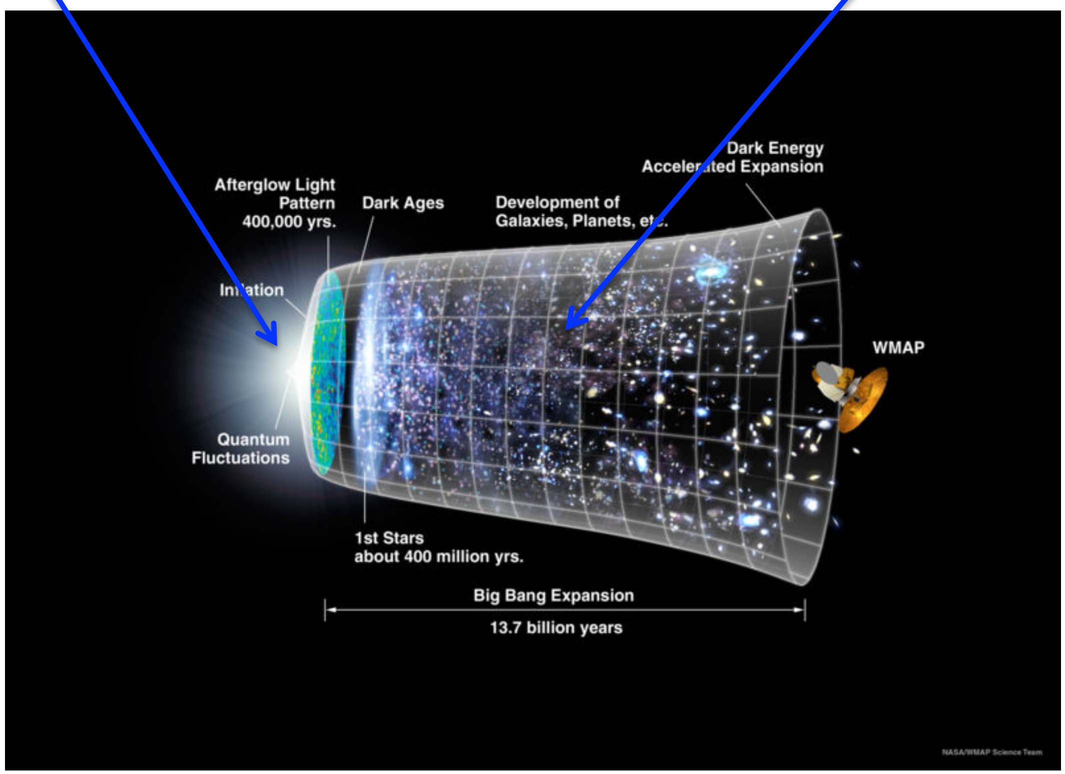
ASICS for Cosmic Microwave Background Experiments

Adrian T. Lee
Physics Department, U.C. Berkeley
Physics Division, LBNL

Two Science Goals

Signature of Inflation

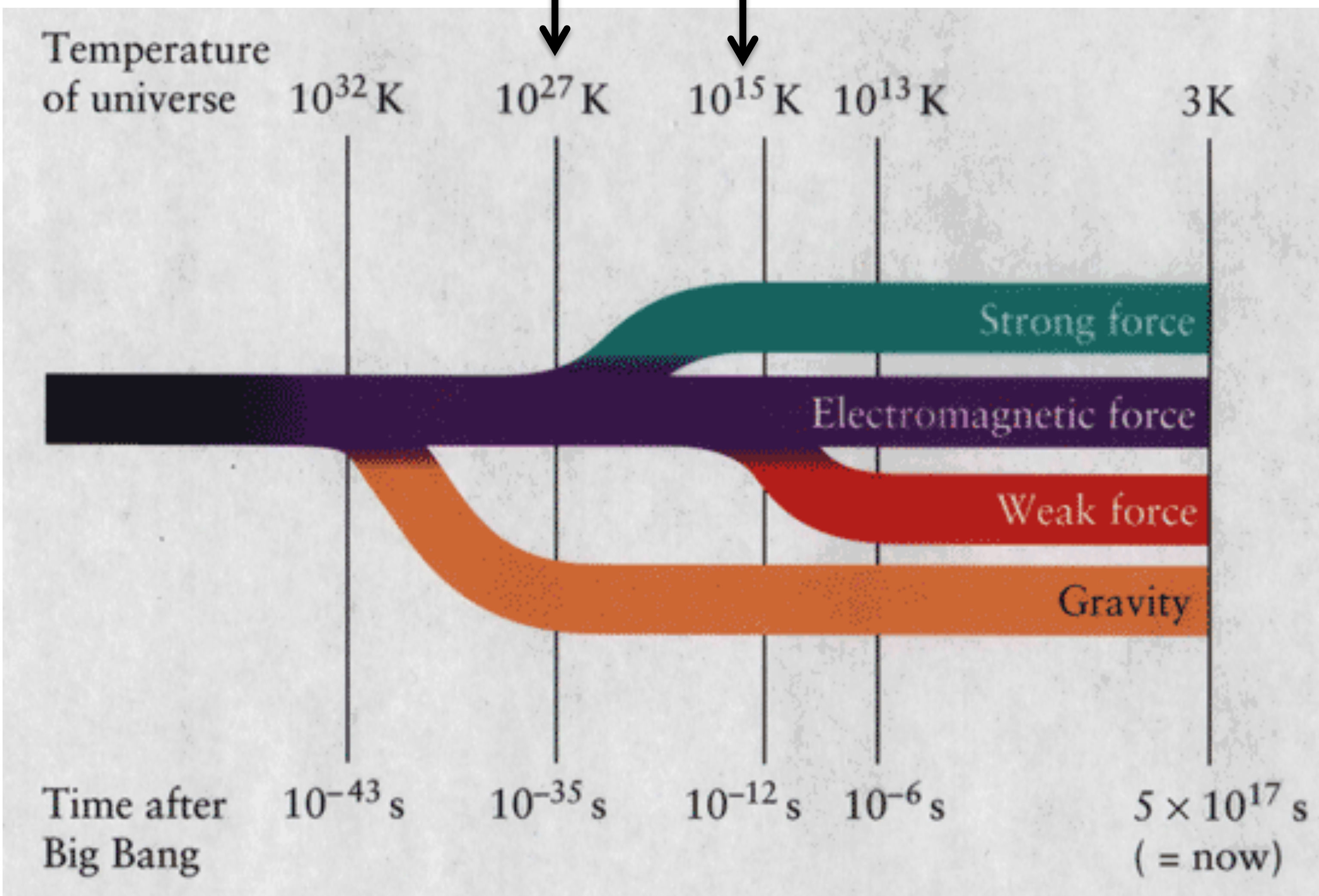
Gravitational Lensing of CMB



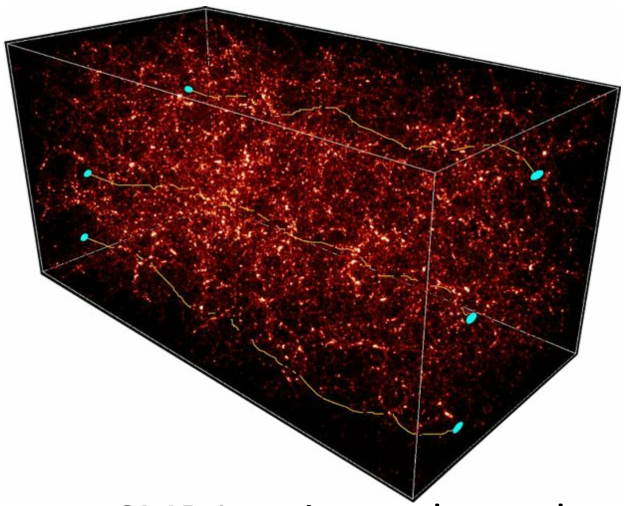
Early Time = High Energy

Gravitational Waves Emitted (10^{16} GeV)

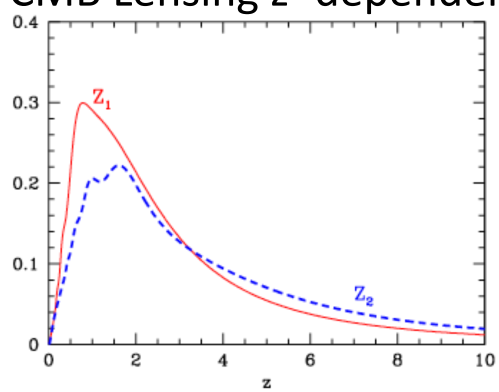
Present Accelerators

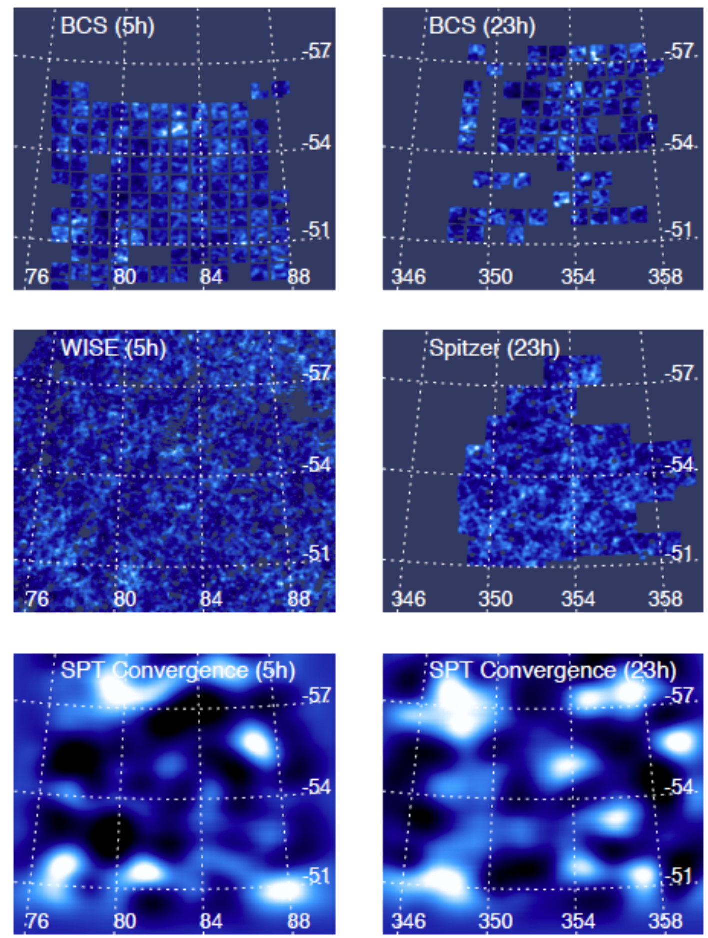


CMB Lensing: Higher z than optical

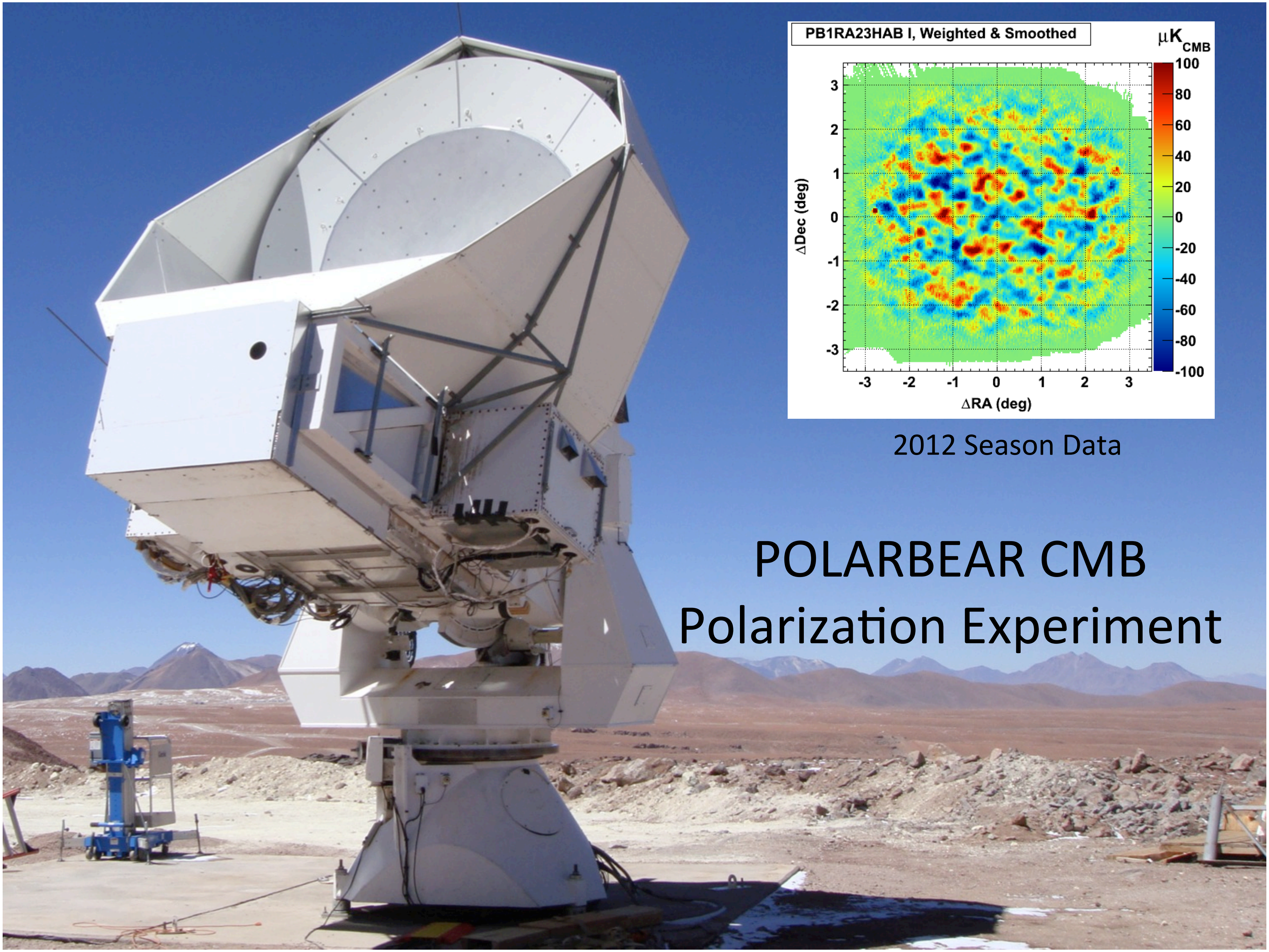


CMB Lensing z -dependence





- Lensing Source at z = 1100
  - Probes higher z than optical lensing and BAO
- Sum of Neutrino Masses
- Detect early Dark Energy



2012 Season Data

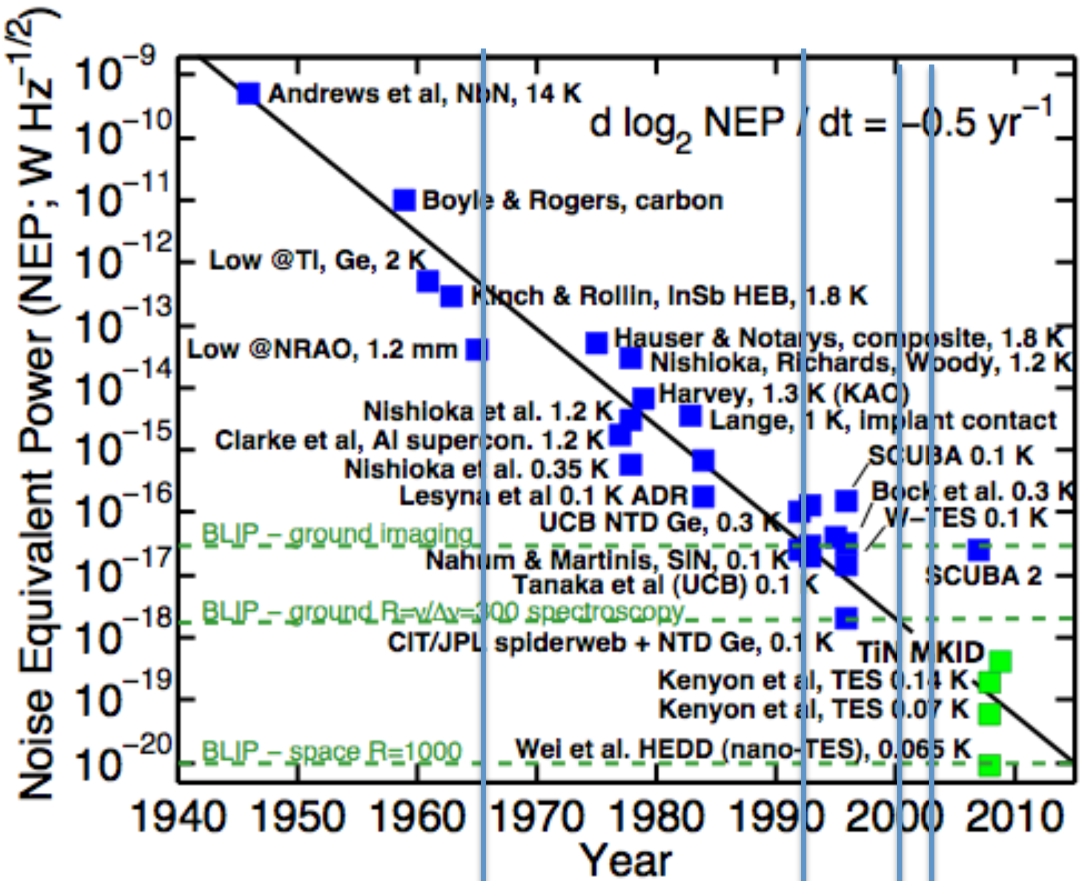
POLARBEAR CMB Polarization Experiment

CMB Detector Development

CMB Science driven by detectors

- Possible "direct" detection of Inflation
  - 10^{16} GUT energy scale – window to ultra high energy.
  - Current limit r ~ 0.7 (Polarization)
  - Experimental limit ~ 0.001
- Gravitational Lensing
  - CMB+BAO Neutrino masses present limit ~ 230 meV (95% C.L.)
  - Long term possibility: Δm ~ 20 meV (need O[10^5 - 10^6] detectors)
  - Constrain Early Dark Energy models

Richards' Law (like Moore's Law)



?

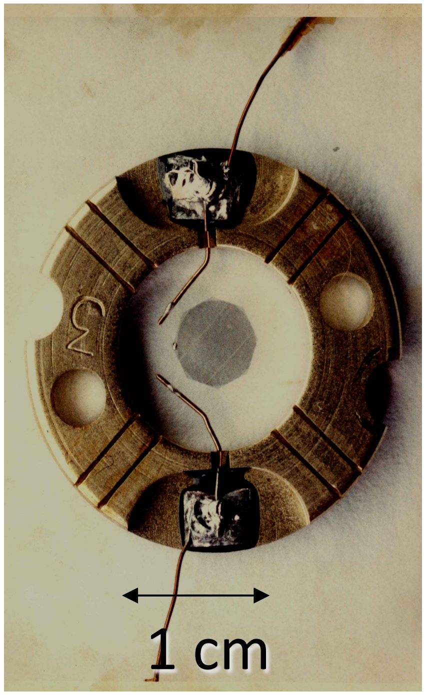
Discovery of CMB polarization

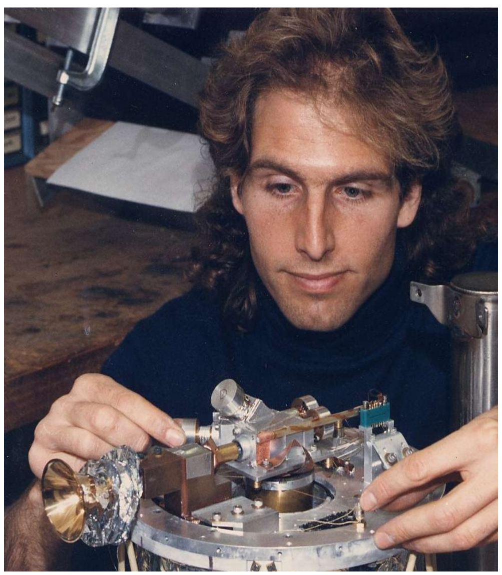
Discovery of Acoustic Peaks

Discovery of CMB fluctuations

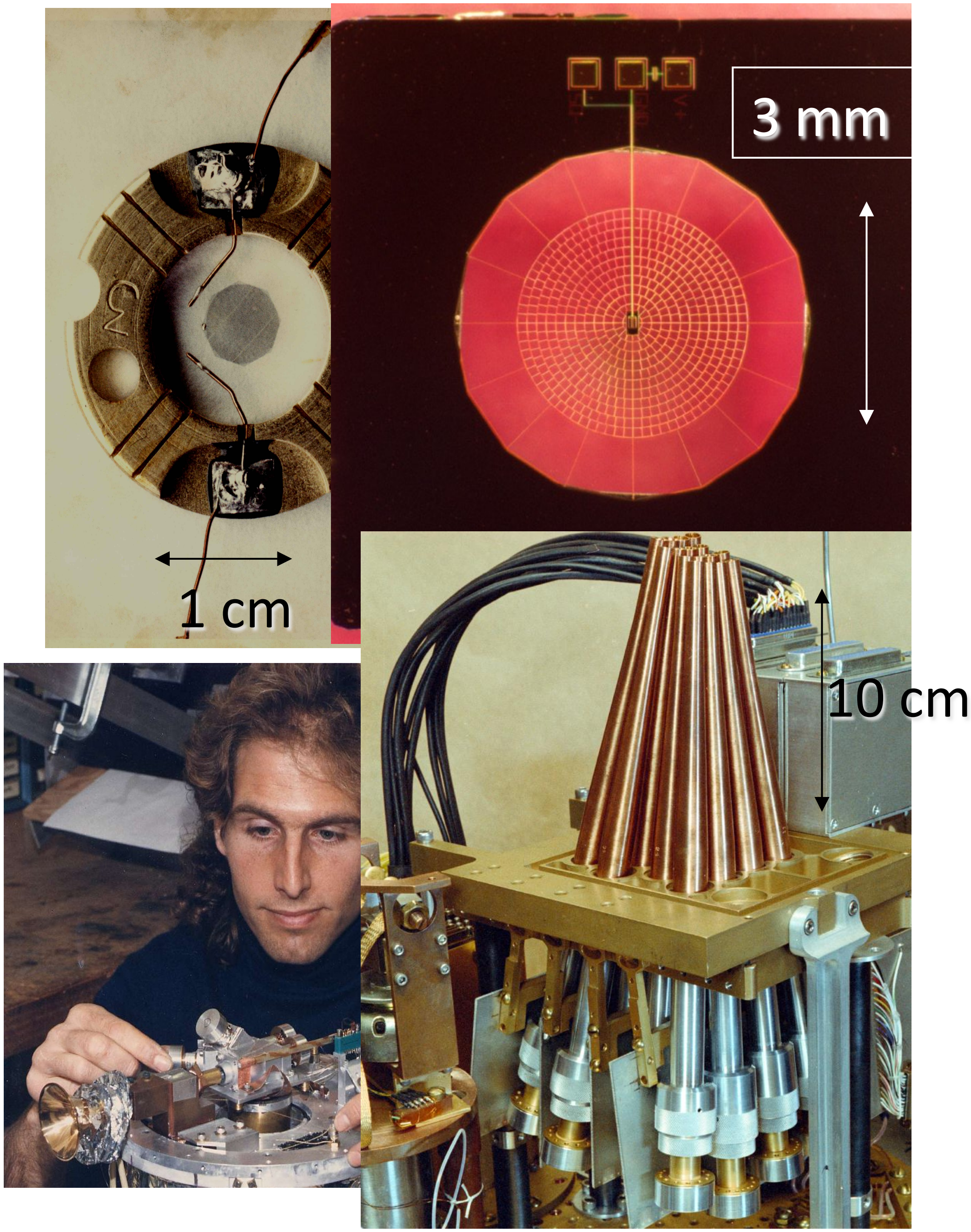
Plot from J. Zmuidzinas

Discovery of CMB

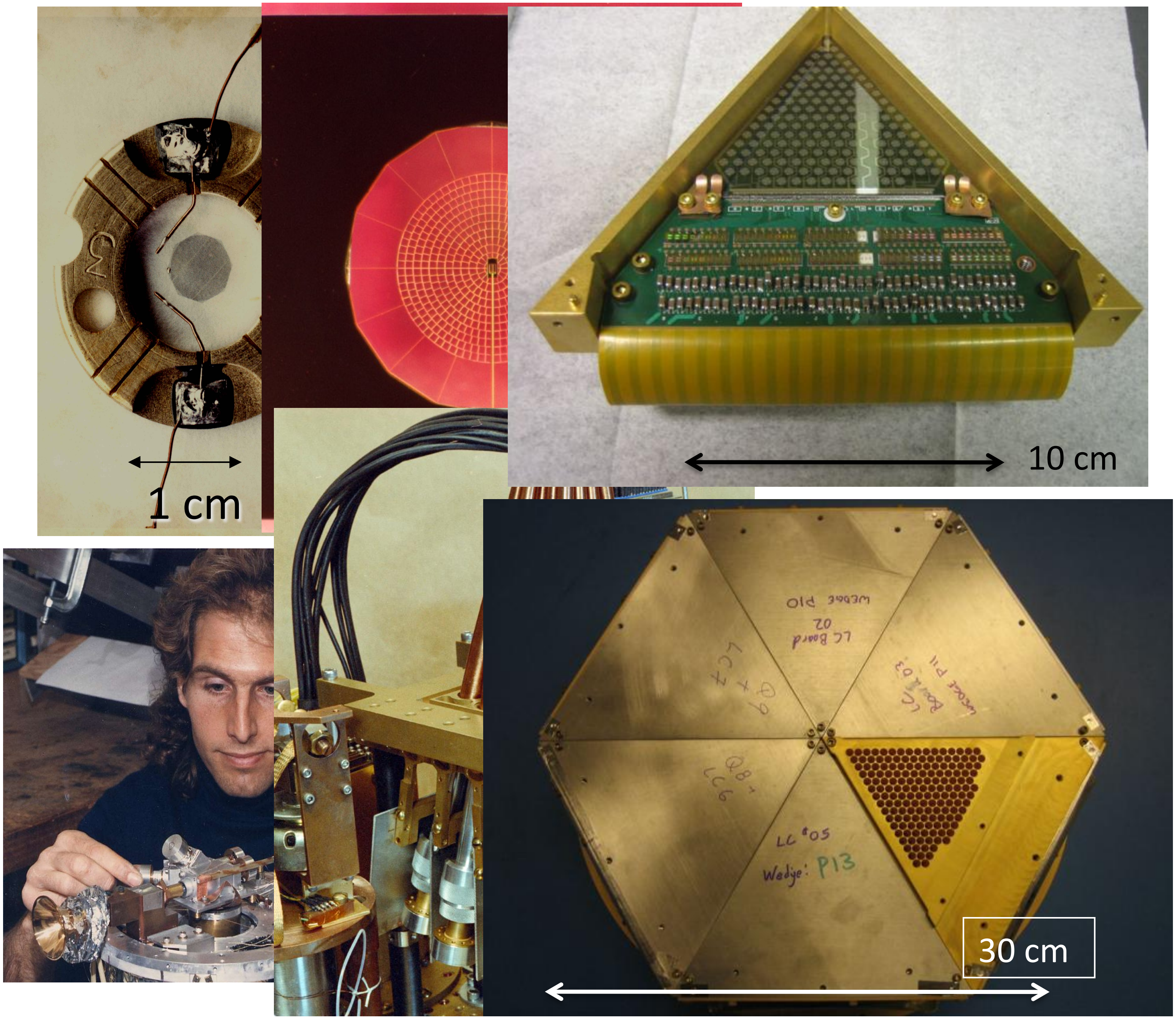




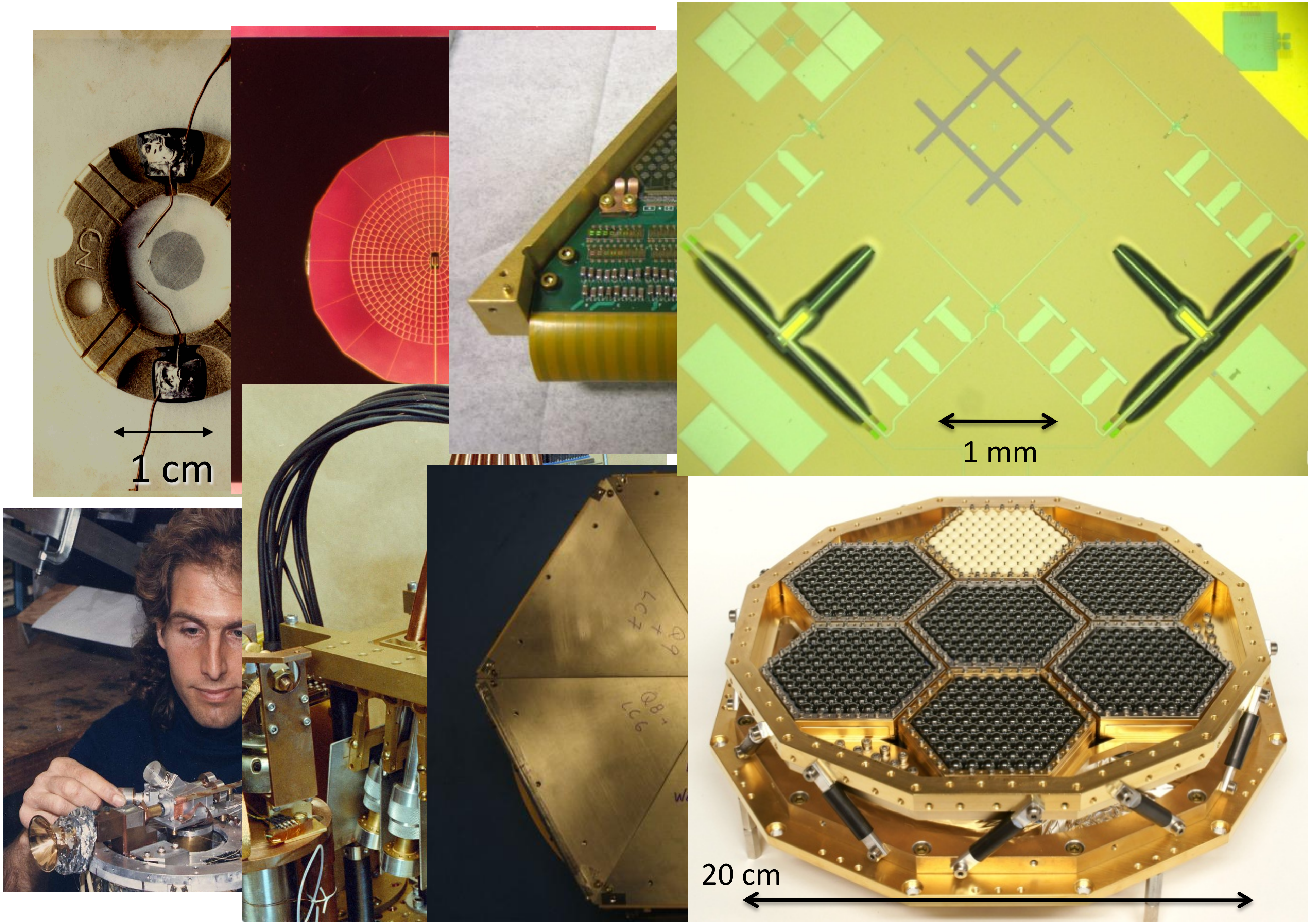
1980’s



1980's 1990's



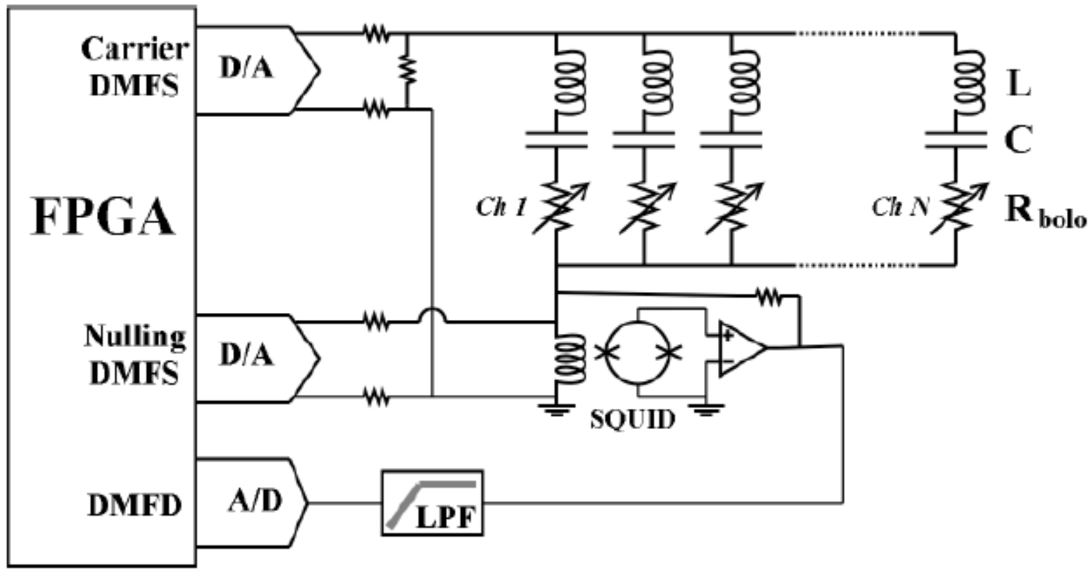
1980's 1990's 2000's



1980's 1990's 2000's 2010's

Readout Multiplexing
Application of ASIC

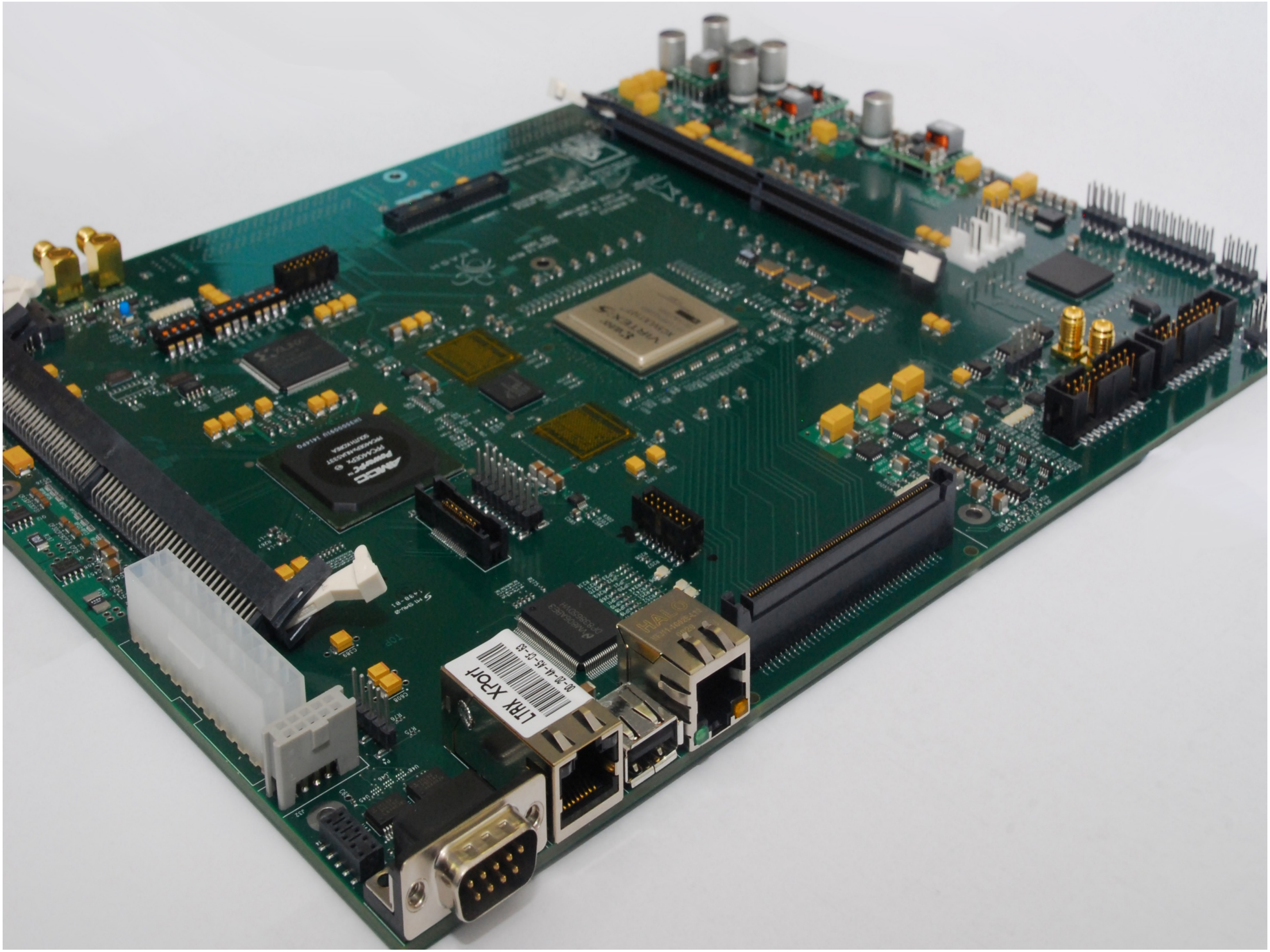
Frequency Domain Multiplexer



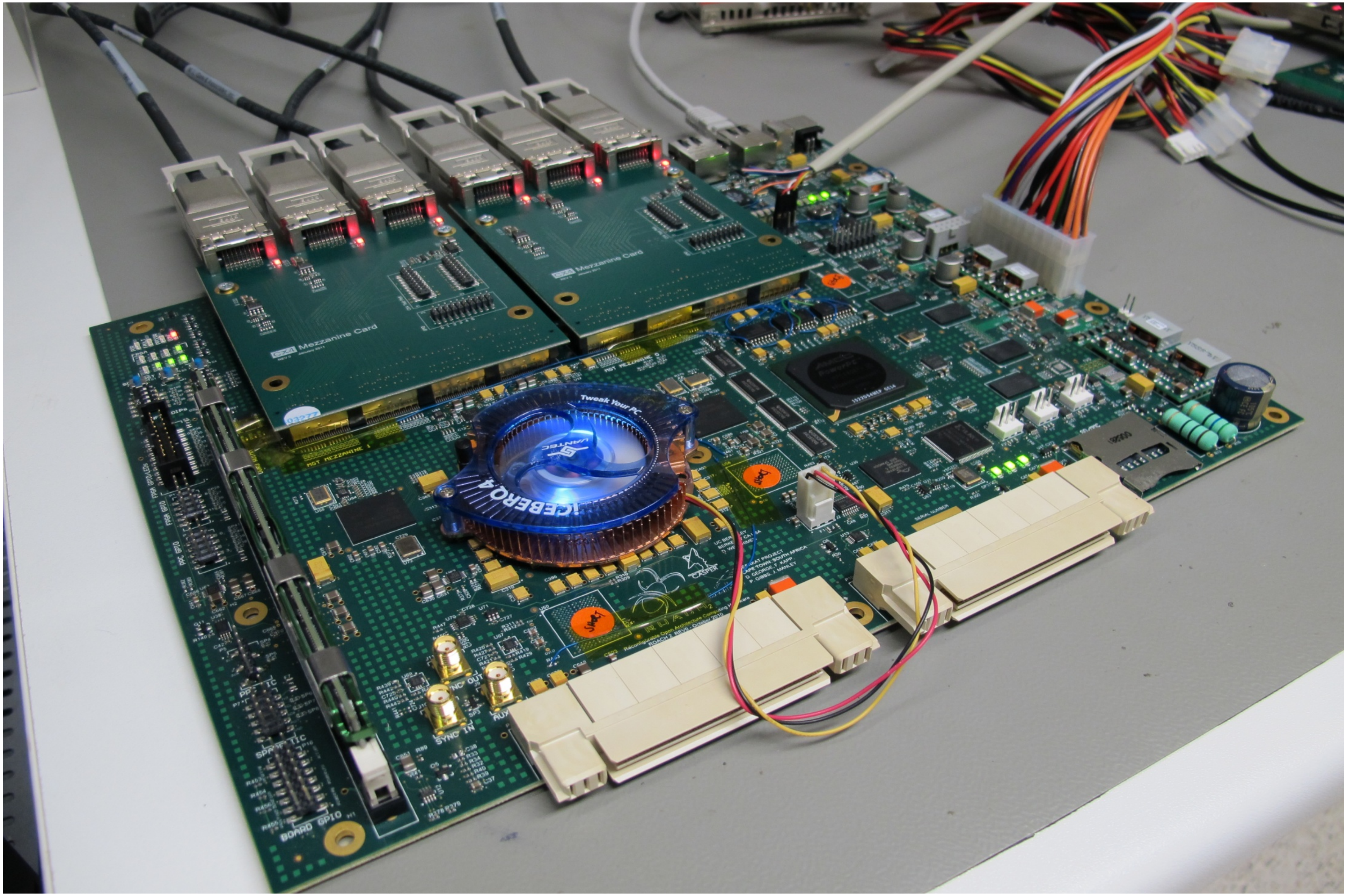
- Current system bandwidth = 1 MHz
  - 16 detectors multiplexed on one readout chain
- 1st year goal: 3 MHz
  - 64-128 detectors
- 2nd year goal: move carriers to 20 MHz
  - Readout components can be integrated into detector wafer

FPGA Implementation Example #1

Dan Werthimer (SSL)
ROACH (Reconfigurable Open Architecture Computing Hardware)


LTRX XPort

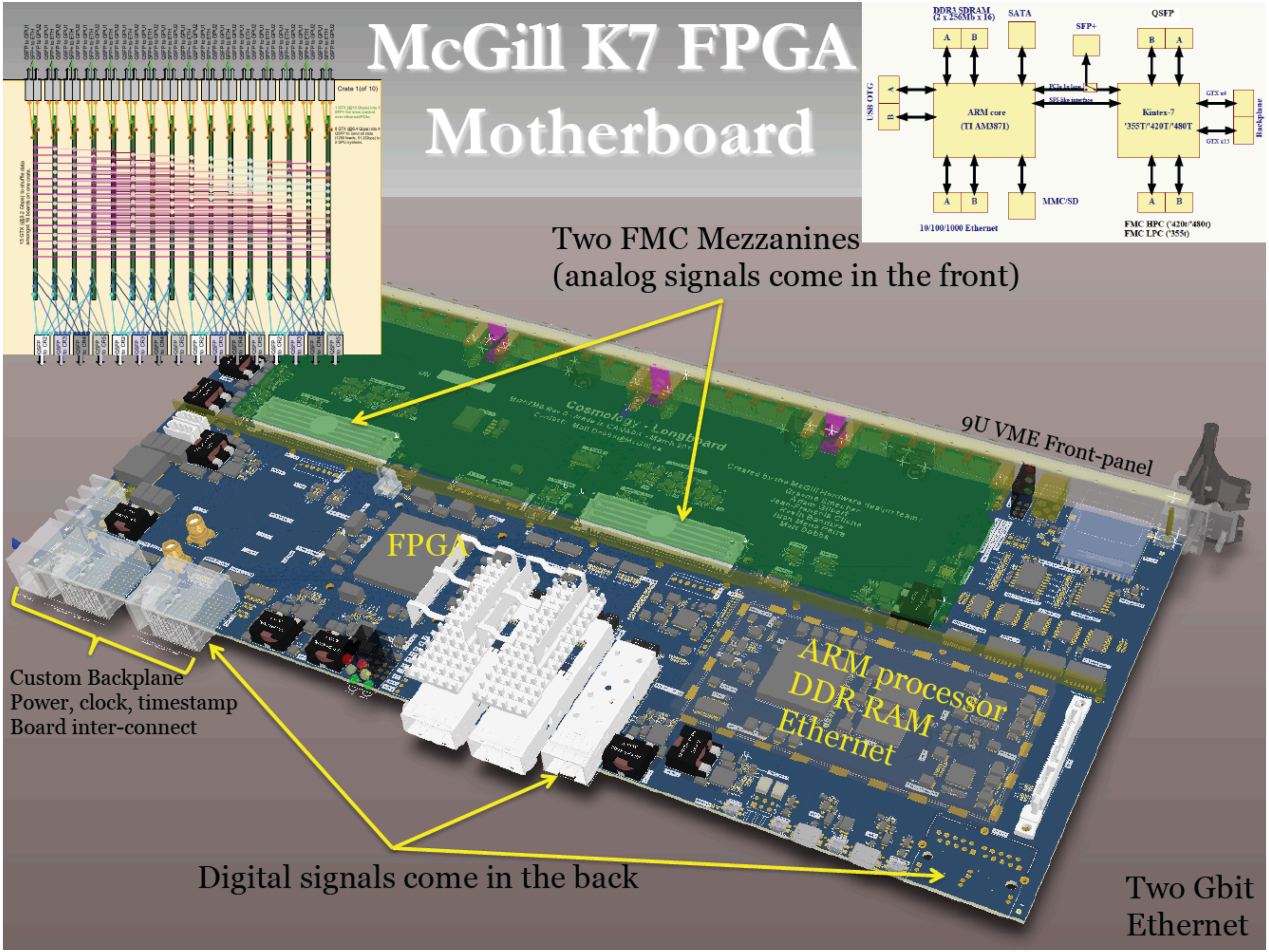
Roach II


Mezzanine Card
Mezzanine Card
Tweak Your PC
SYNC IN
BOARD GPIO

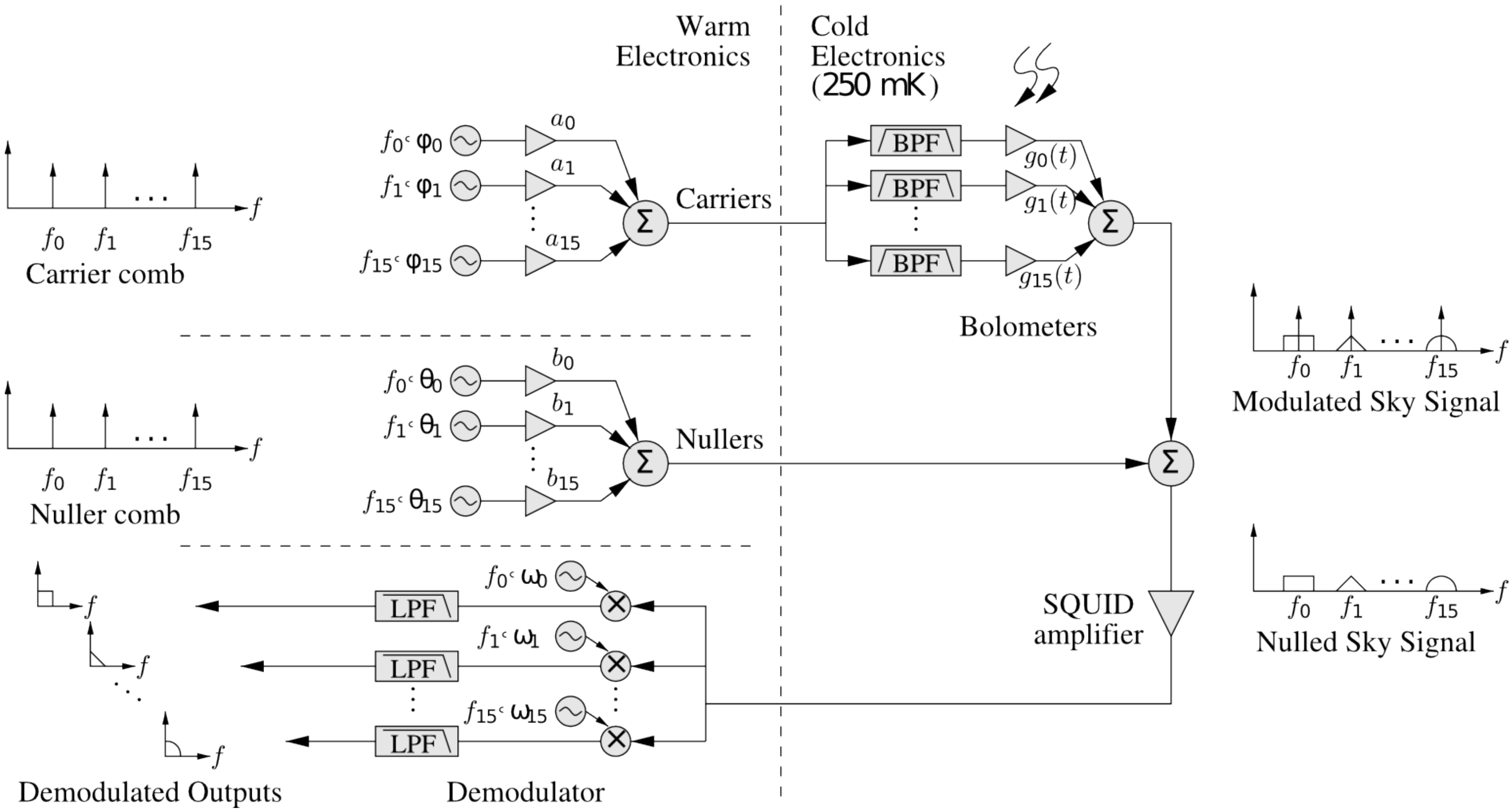
Implementation Example #2

Matt Dobbs (McGill)

"dFMUX"


McGill K7 FPGA Motherboard
DDR3 SDRAM (2 x 256Mb x 16)
SATA
SFP+
QSFP
USB OTG
ARM core (TI AM3871)
Kintex-7 '355T/'420T/'480T
Backplane
MMC/SD
10/100/1000 Ethernet
FMC HPC ('420t/'480t)
FMC LPC ('355t)
Two FMC Mezzanines
(analog signals come in the front)
9U VME Front-panel
FPGA
ARM processor
DDR RAM
Ethernet
Custom Backplane
Power, clock, timestamp
Board inter-connect
Digital signals come in the back
Two Gbit
Ethernet

Signal Path: Overview



(To appear, IEEE Trans. Instrum. Meas.)

ASIC Motivation

- Space Missions
  - LiteBIRD CMB Polarization Mission (JAXA, NASA, CSA, …)
    - Power Dissipation, LiteBIRD => 100 W total budget
    - Radiation Hardness
    - Performance e.g. bit depth -> dynamic range
- Ground Based
  - Cost per channel
    - ~$300 per channel for readout today

LiteBIRD working group

- 64 members (as of Nov. 23, 2012)
- International and interdisciplinary

KEK
Y. Chinone
K. Hattori
M. Hazumi (PI)
M. Hasegawa
N. Kimura
T. Matsumura
H. Morii
R. Nagata
S. Oguri
N. Sato
T. Suzuki
O. Tajima
T. Tomaru
M. Yoshida

SOKENDAI
Y. Akiba
Y. Inoue
H. Ishitsuka
A. Shimizu
H. Watanabe

JAXA
H. Fuke
I. Kawano
H. Matsuhara
K. Mitsuda
T. Nishibori
A. Noda
S. Sakai
Y. Sato
K. Shinozaki
H. Sugita
Y. Takei
N. Yamazaki
T. Yoshida
K. Yotsumoto

Tsukuba U.
M. Nagai
S. Takada

Okayama U.
H. Ishino
A. Kibayashi
S. Mima
Y. Mibe

UC Berkeley
A. Ghribi
W. Holzapfel
A. Lee (US PI)
H. Nishino
P. Richards
A. Suzuki

McGill U.
M. Dobbs

LBNL
J. Borrill

MPA
E. Komatsu

IPMU
N. Katayama

Yokohama NU.
S. Murayama
S. Nakamura
K. Natsume

ATC/NAOJ
K. Karatsu
T. Noguchi
Y. Sekimoto
Y. Uzawa

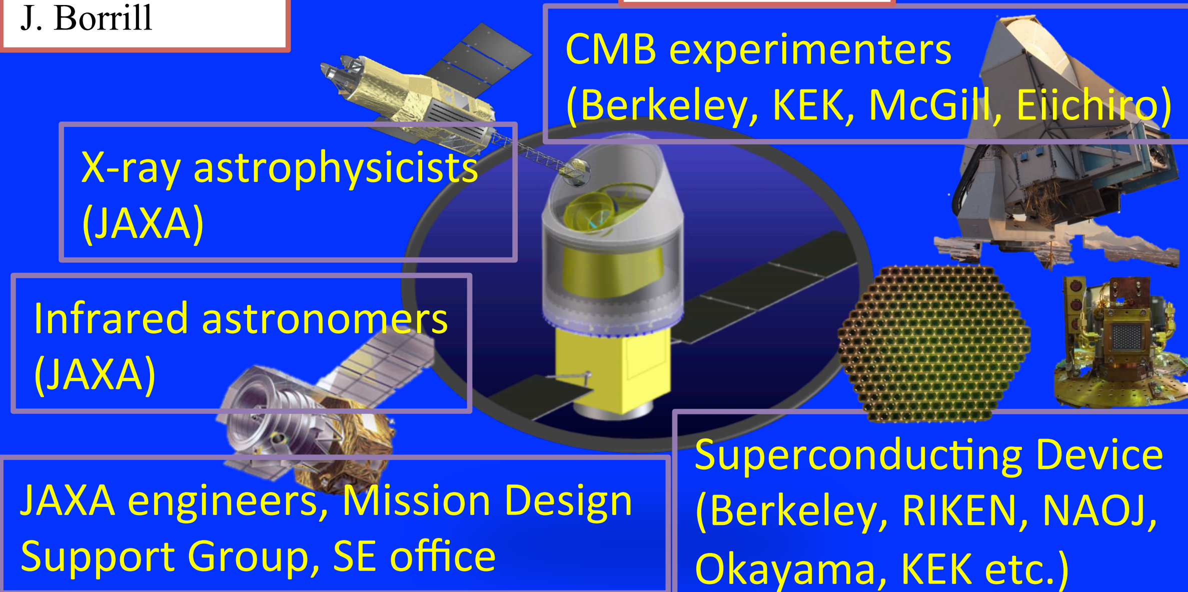
Saitama U.
M. Naruse

Osaka Pref. U.
K. Kimura
H. Ogawa

RIKEN
K. Koga
C. Otani

Tohoku U.
M. Hattori
K. Ishidoshiro

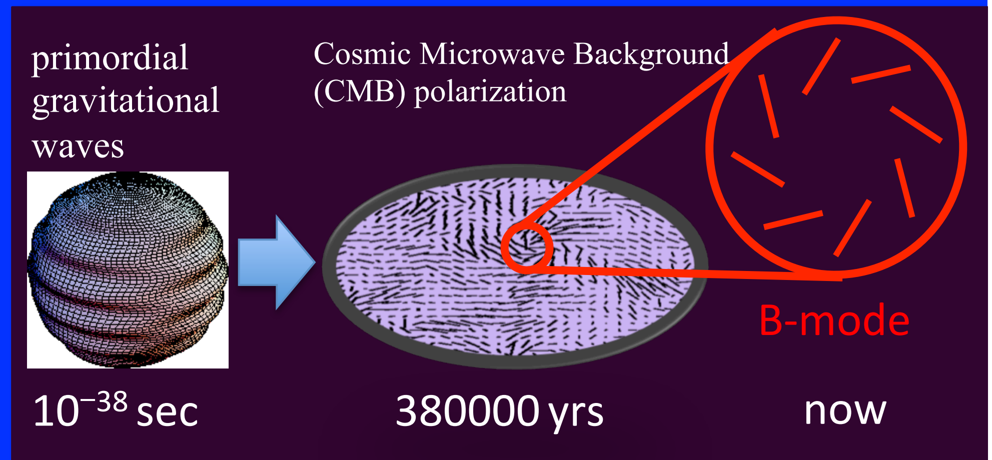
Kinki U.
I. Ohta

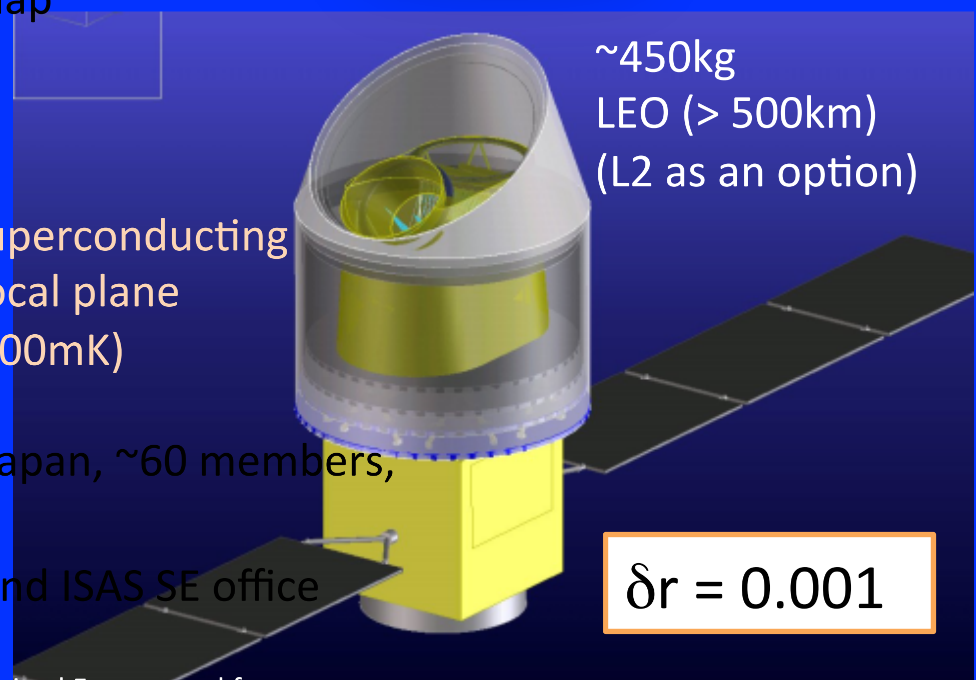


LiteBIRD

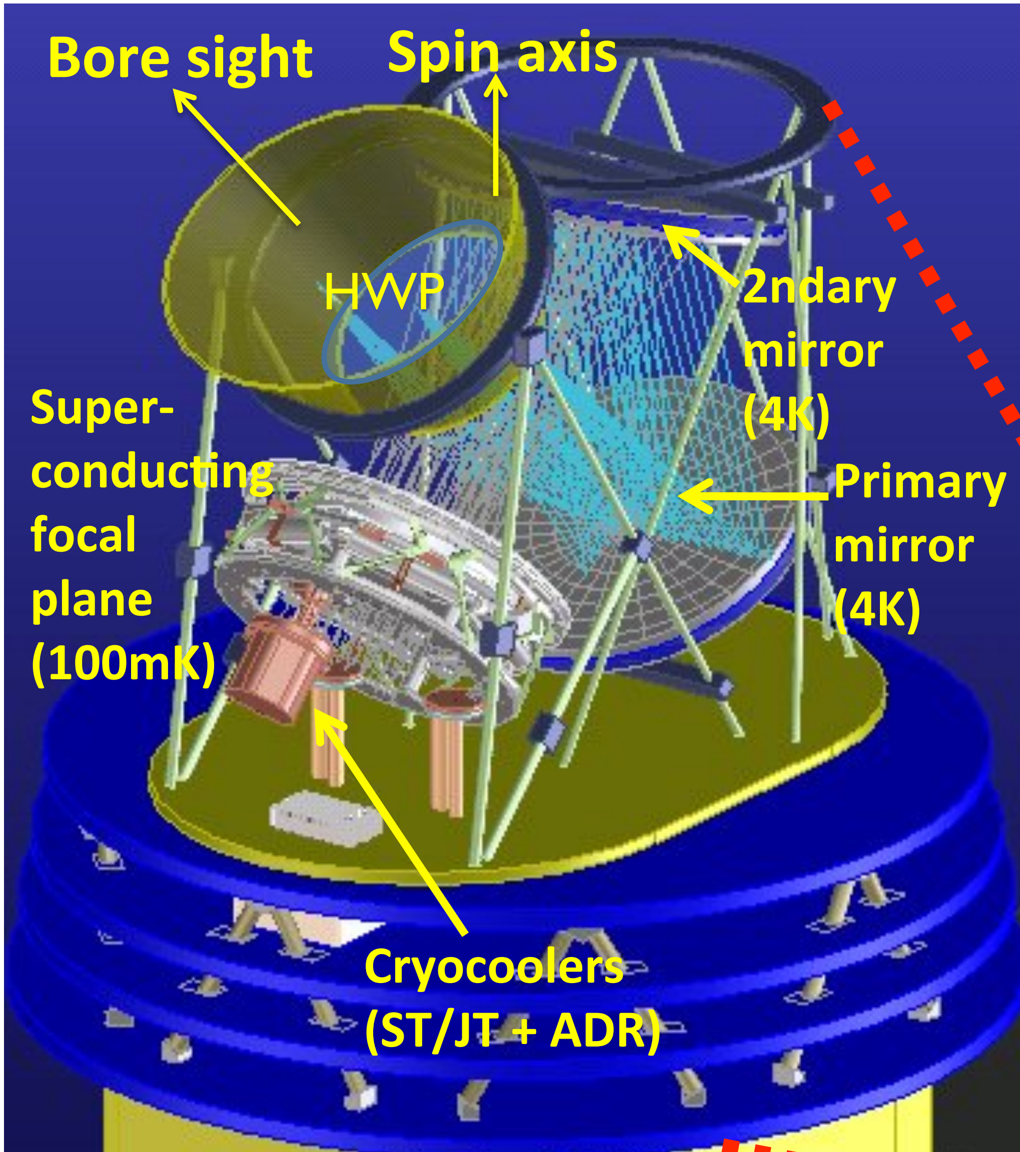
Lite (Light) Satellite for the Studies of B-mode Polarization and Inflation from Cosmic Background Radiation Detection

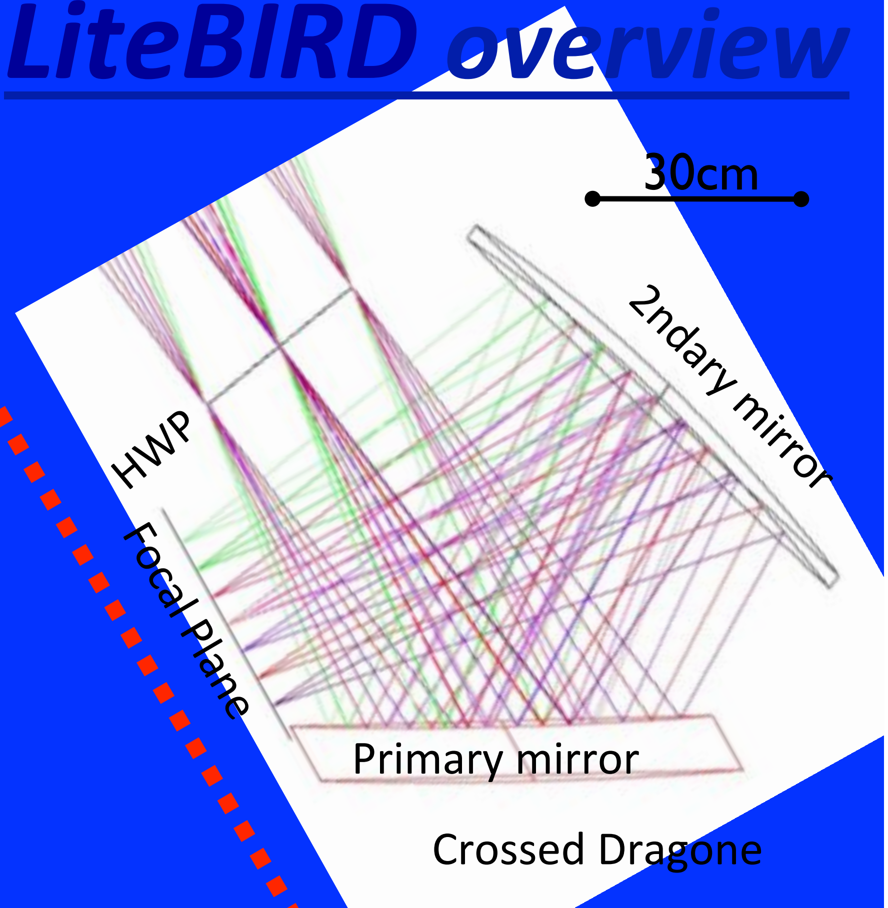
- Scientific objectives
  - Stringent tests of cosmic inflation
  - Tests of quantum gravity theories
- Observations
  - Full-sky CMB polarization survey at a degree scale
  - Detecting primordial gravitational waves imprinted in CMB polarization map
- Strategy
  - Part of technology verification from ground-based projects
  - Synergy with ground-based super-telescopes
- Project status/plans
  - Working group authorized by SCSS in Japan, ~60 members, international and interdisciplinary
  - Technical Support from JAXA's MDSG and ISAS SE office
  - Target launch year ~2020

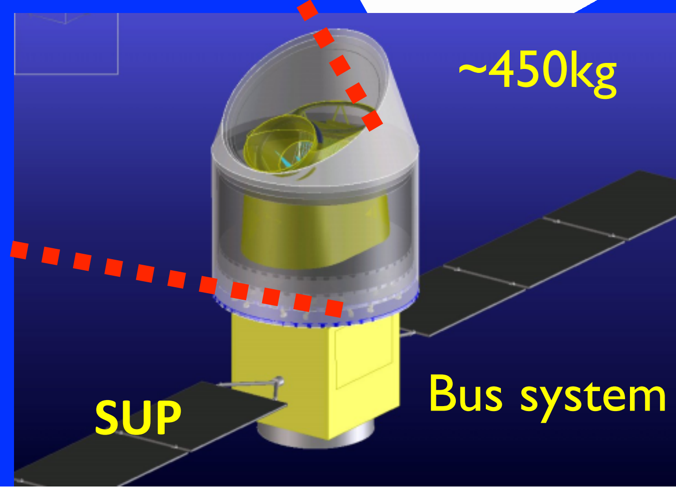




LiteBIRD overview







- Mission Definition Review in 2013
- Target launch year: 2020 (LEO or L2)
- Launch vehicle: H2 or Epsilon
- EPIC-type scan strategy

MPA,

Power Budget

- Total Power for LiteBIRD spacecraft ~ 100W
  - FPGA: ~ 50mW/detector x 2000 detectors ~ 100W

Power Overview

- Current DAN build: Mux factor 16, 4 modules per DfMUX
  - 5.7 W fixed digital power
    - On-board: Ethernet, RAM, serial transceivers
    - On FPGA: MicroBlaze, FPGA leakage
    - Misc: Regulator losses
  - 6.63 W analog
    - 2 Mezzanines
    - 1/2 SQUID controller
  - 3.42 W scaling digital power
    - DSP, DAC/ADC IOs, traffic
    - (Overestimate)
- 250 mW per bolometer (about factor 10 too high)

Power Overview

- Shotgun approach: increase mux factor
  - 5.7 W fixed digital power
    - On-board: Ethernet, RAM, serial transceivers
    - On FPGA: MicroBlaze, FPGA leakage
    - Misc: Regulator losses
  - 6.63 W analog
    - 2 Mezzanines
    - 1/2 SQUID controller
  - 3.42 W scaling digital power
    - DSP, DAC/ADC IOs, traffic
- 128x mux factor, 4 modules per DfMUX: 50.8 mW/bolo

Simple Power Improvements

- Virtex-4 => Virtex-6 or -7 series
  - Low power now intrinsic to silicon, CAD flow
  - > 20% savings for free

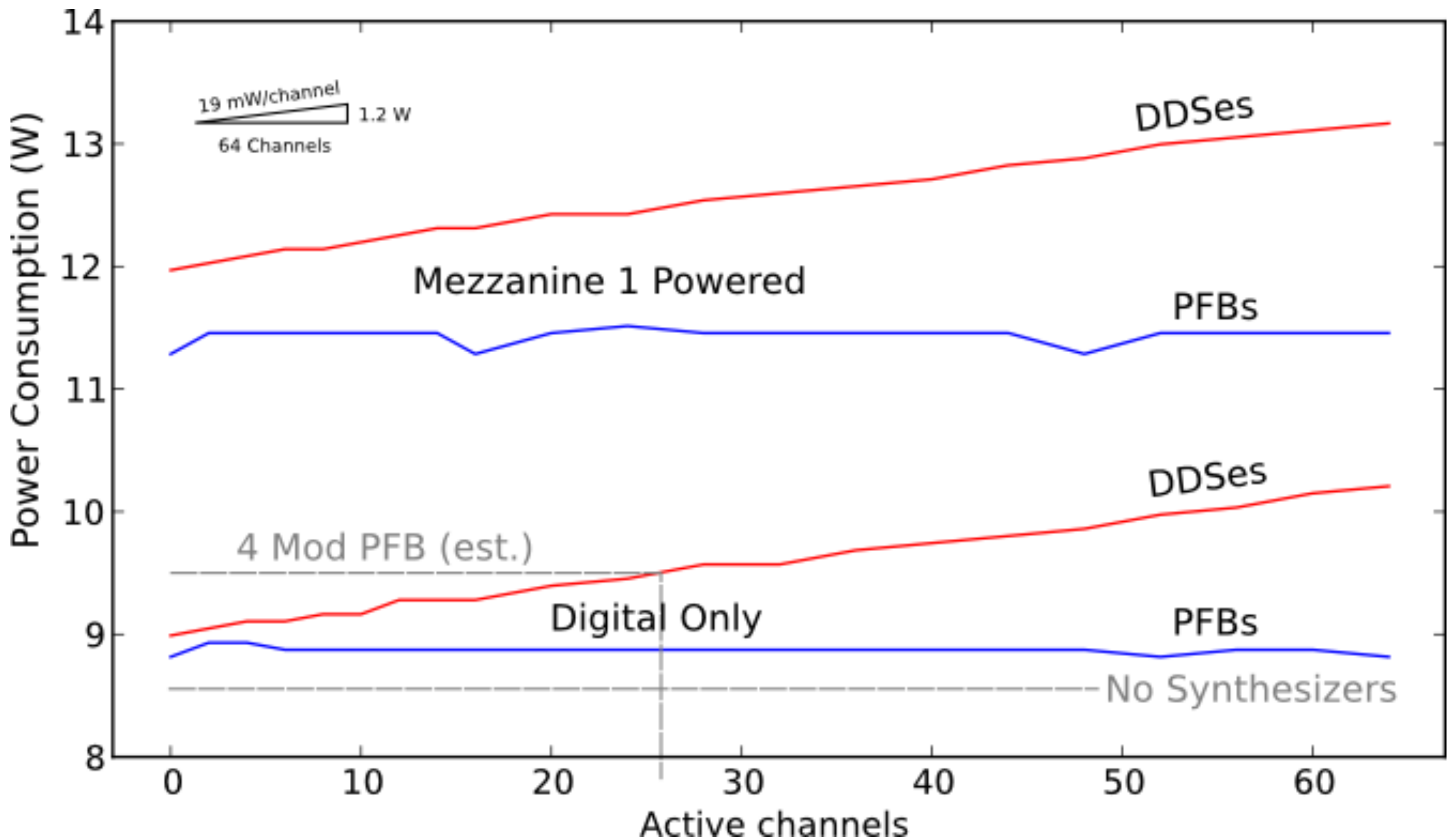
- More, better embedded blocks
  - Higher clock rates, wider multipliers/adders
    - Keeps high-speed crunching off ordinary fabric
    - Intrinsically more power-efficient
  - Memory interfaces, MAC/PHYs, ...
  - Extreme case: Zynq family

- Board-level savings
  - Built-in SQUID controller?
  - Lower-voltage islands (e.g. LPDDR or DDR3?)
  - Narrower RAM (32-bit => 8-bit memory)
  - Trim excess (SystemACE)

Other Interesting Possibilities

- Different signal-processing topologies
    - Polyphase Filter Bank (PFB) DMFS or DDS
    -

Power Scaling with MUX factor



Polyphase Filter Bank and Direct Digital Synthesis

Conclusions

- Possible gains using ASIC
  - Power Dissipation
  - Radiation Hardness
  - Cost per unit (for ground based)
  - Increased performance by removing compromises for lower power in FPGA-based system?
    - E.g. Higher bit depth gives operational flexibility

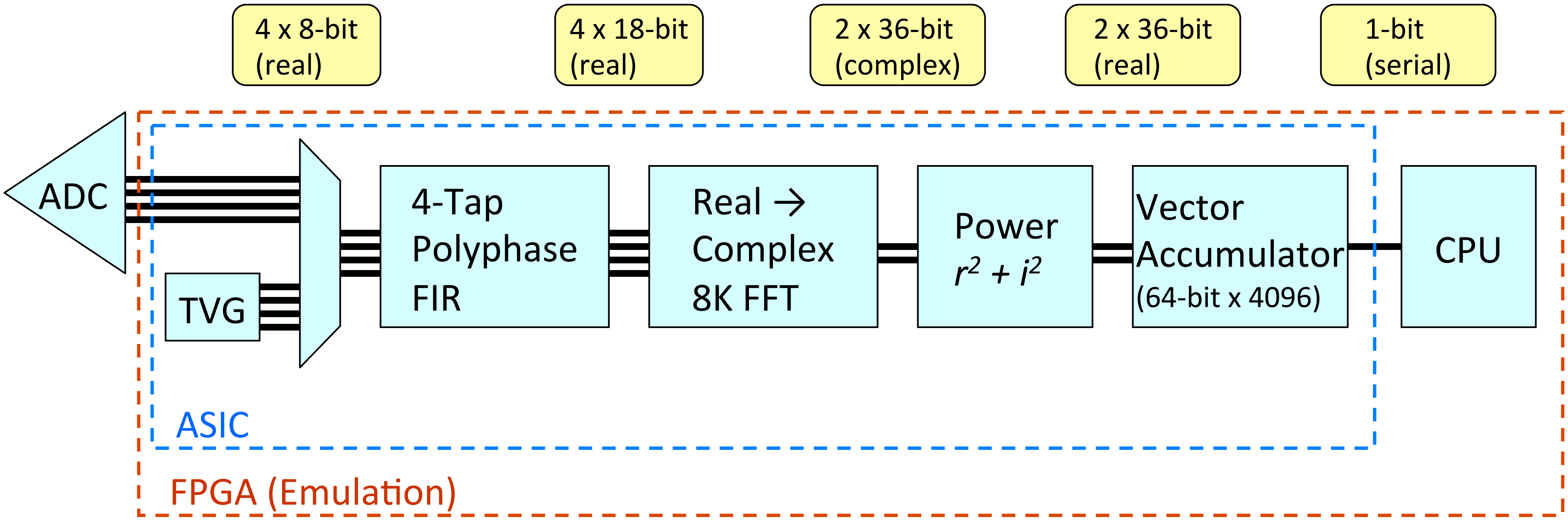
A 1.5GS/s 4096-Point Digital Spectrum Analyzer for Space-Borne Applications

Brian Richards, Nicola Nicolici[*], Henry Chen, Kevin Chao, Robert Abiad[**], Dan Werthimer, and Borivoje Nikolić

Berkeley Wireless Research Center, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley
[*]Department of Electrical and Computer Engineering, McMaster University,
[**]Space Sciences Laboratory, U. C. Berkeley

The authors acknowledge students, faculty and sponsors of BWRC, chip fabrication donation of STMicroelectronics, NSF Infrastructure Grant No. 0403427, C2S2, and support from Robert Jarnot and Paul Stek from NASA and the Jet Propulsion Laboratory

Architecture of the 4096-Point Spectrometer



- Stream-based Datapath:
  - Parallel channels with consecutive 2K packets.
  - Continuous operation: All input samples are used.

4096 channel Mars spectrometer

“Chip in a day” FPGA to ASIC