ICs for Data Transmission in HEP

Jingbo Ye

Physics, SMU

HEPIC2013

Outline

1. Data Transmission Needs and Challenges
2. Copper, Fiber or Free-Space
3. ASICs or COTS
4. ASICs being designed or discussed
5. Issues for future ASIC work
6. Issues of using COTS
7. Summary

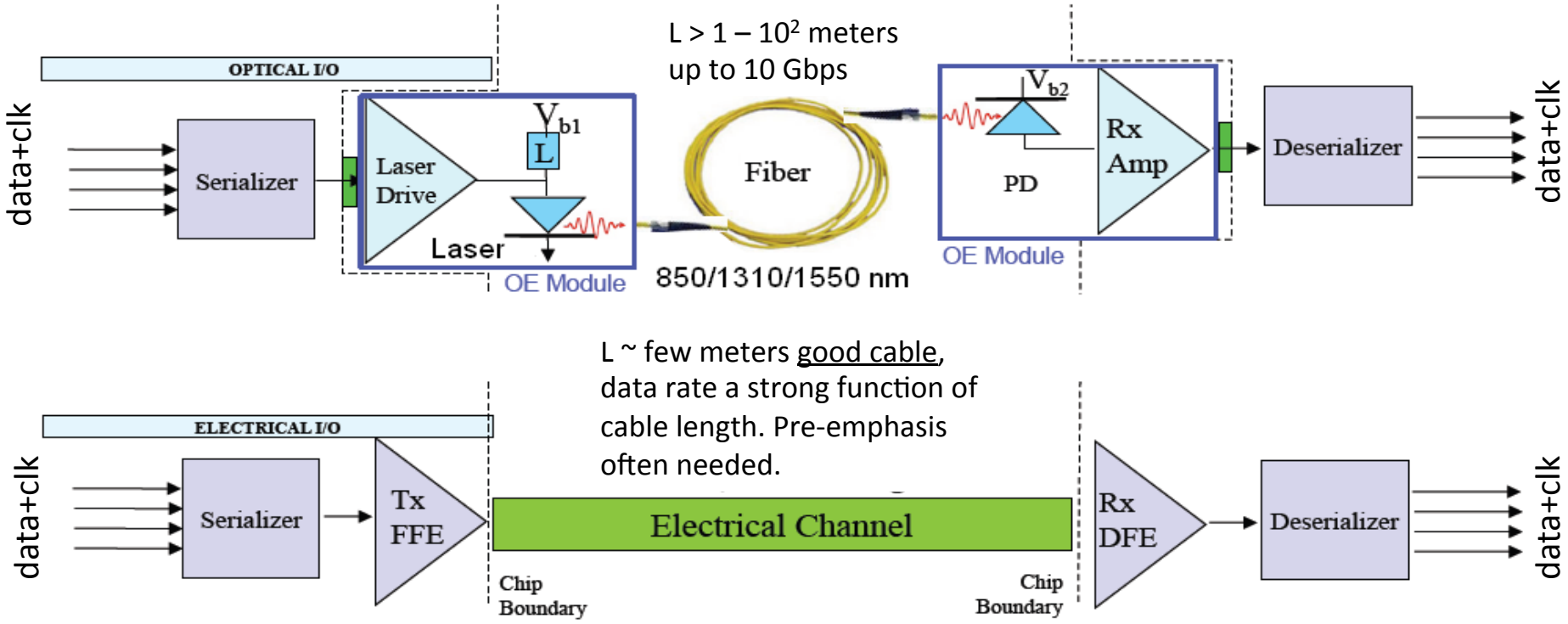
Data Transmission Needs and Challenges

- Some history and (immediately) future
  - Tevatron: Mbits per second, COTS, copper, LED + fiber.
  - LHC: n × 10 – 10^3 Mbits per second, COTS (GLink 1.6 Gbps) and ASIC GOL (1st ASIC in data transmission?). Lesson: need high quality clock for fast serial data transmission: QPLL (a stopgap). EEL(edge emitting laser)/VCSEL + fiber.
  - LHC upgrades: 1 – 10 Gbps, ASICs (GBT, LOC) + FPGAs, need careful board level design and special instruments. EEL but more VCSEL, array optics + fiber.
- Triggering data
  - Low and fixed latency.
  - Low power dissipation (high channel density in a board).
  - Example: ATLAS/LAr: 5.12 Gbps/fiber, 205 Gbps/board, or 40 fibers for 320 detector channels, front-end full (ASIC + transmission protocol) custom design.
- Streaming data
  - Lossless detector data streaming to take advantage of the embedded SerDes + processing power of an FPGA, for the backend (ex. pileup, digital filtering).
  - Desire 10 Gbps due to overall data volume (ATLAS LAr: 1524 FEBs at about 150 Tbits per second for the whole system, prefer front-end custom design).

Data Transmission Needs and Challenges

- Special operational environment (inner tracker, inside LAr)
  - Very high (> 500 krad, > 10^{13} particles/cm^2 fluence) radiation environment.
  - Special requirements on packaging (small form-factor, low mass, nonmagnetic).
  - Cryogenic operational temperature (89K). COTS spec goes from -10 C to 55 C. ASIC needed unless operating COTS outside of the specs. Need R&D on guidelines for “IC in cold”.
- Overall remarks
  - Ultra high reliability (both at component and system level) due to difficulties in or impossible for maintenance and repair of the detector side of the link.
  - Full evaluation of a technology or a design takes years, and should not be rushed.
  - Requirements are different for up-links (detector to counting-room) and down-links (clock, config and control to detector). For example: High data bandwidth and low power for up-links, high reliability (including FEC to mitigate SEUs) for down-links.
  - COTS are usually designed for generic applications and are generally not optimized for applications with high demands as in a HEP experiment. We should also refrain from designing an ASIC into an AGIC (application generic) under the argument of “economy of scale” .

Copper, Fiber or Free-Space



Copper or Fiber? Depends on the application. Should be evaluated case by case.
Using a copper cable, due to fewer components, is usually more reliable. Pre-emphasis may be needed for multi-gigabit per second data rate, leads to high power.
When transmission distance is over 5 meters at a rate of > 5 Gbps, a fiber link is usually better in power consumption, channel density, EMI. A fiber link also breaks the front- and back-end ground loop. When the distance is more than 10 meters, fiber (or optical) link is maybe the only option.

Copper, Fiber or Free-Space

- Compared with Fiber, Free-Space data transmission
  - Save on fiber/connectors, that's about it.
  - Data rate and transmission distances: above LVDS/twist-pairs, below fiber.
  - Maybe good for very special applications such as in an inner tracker, if the VCSELs withstand the radiation.

ASICs or COTS

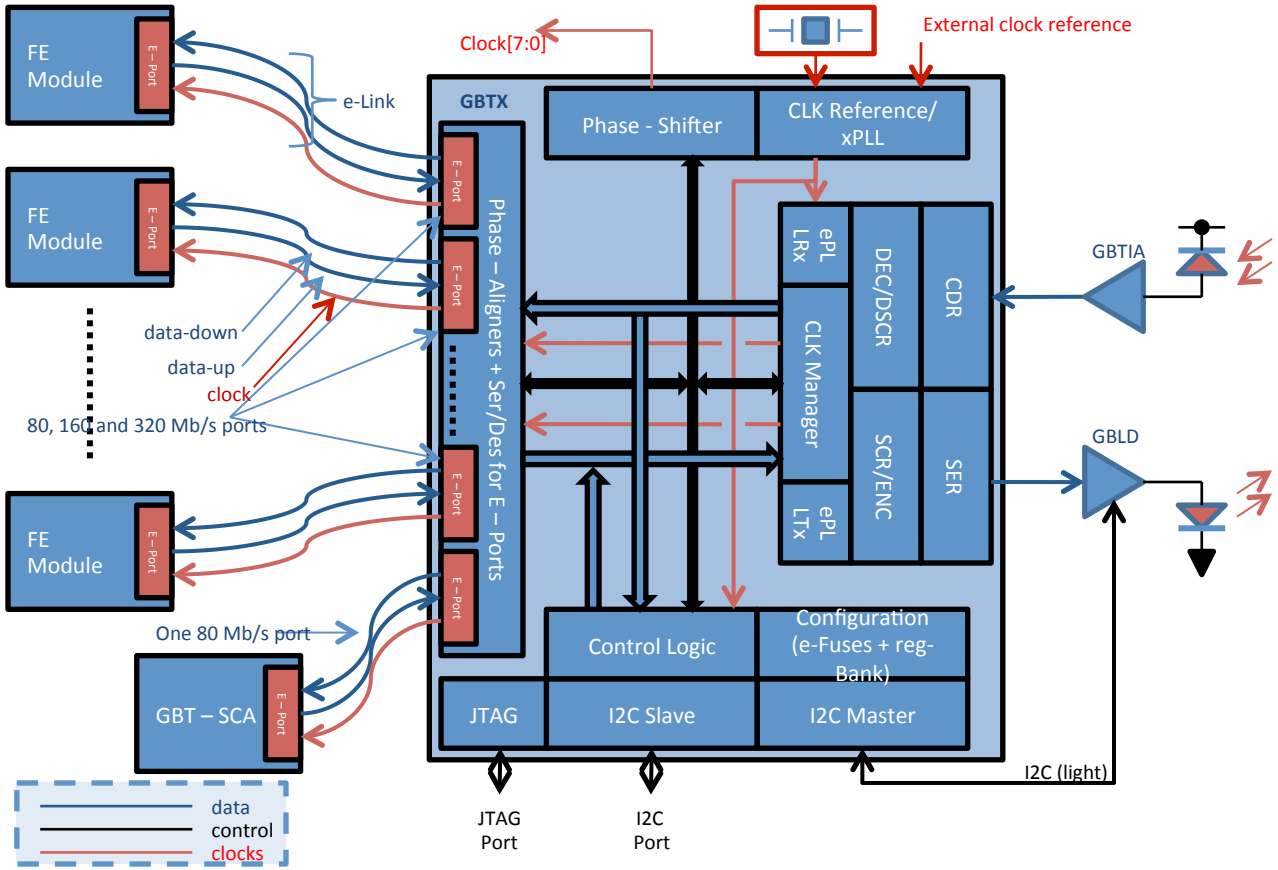
- ASICs (of serial data transmission)
  - TTCrx, 0.8 μm DMILL technology. 80 Mbps, receives TTC signals for the front-end. BiPhase Mark encoding, no error correction for SEUs generated by the p-i-n diode if an optical link is used as the transmission medium. Output clocks not suitable for high-speed serializers.
  - GOL, 0.25 μm CMOS. 16:1 serializer with 800 Mbps or 1.6 Gbps, 8B/10B encoding, CML and VCSEL driver outputs, designed for LHC experiments. Now used in CMS ECAL and other LHC experiments.
  - There are other ASICs, like the SMUX (DMILL, performs 2:1 mux + level shifting) for ATLAS/LAr optical link, developed for data transmissions in LHC experiments.
  - Up front R&D cost and long R&D phase, but clear advantage in radiation tolerance and power, as well as system optimization. An ASIC needs to be designed with a system in mind.

ASICs or COTS

- COTS
  - GLink, Bipolar, proprietary protocol (must use the TX and RX chips in pairs), wide (208 – 1120 Mbps) tuning range. The batch used in ATLAS LAr was pre-screened run at 1.6 Gbps. TTL input, PECL output, high power (1.5W TX and 2.5W RX), about $100 a pair. Manufacturer changed from HP to Agilent in R&D and Construction, and to Avago during maintenance, making part rad-evaluation and spares difficult.
  - The TLK family from TI, SerDes : 2.5 – 10 Gbps, radiation-soft, optimized for Telecom, not for HEP experiments.
  - SerDes embedded in FPGAs (Stratix and Arria,, Virtex and Kentex) 130 – 28 nm, multichannel, 6 – 12 Gbps per channel, with the powerful FPGA this is very suitable for the back-end electronics. It is not suitable for the front-end due to high concentration of transmitting point, power and SEUs. TID is usually not a concern.

ASICs being designed or discussed

- SerDes – GBTx
  - 0.13 µm CMOS. 80, 160 and 320 Mbps e-PORT to be embedded in upstream ASICs, Bi-directional 4.8 Gbps serial data rate, 3 protocols (GBT 3.28 Gbps, 8B/10B 3.52 Gbps, wide-bus 4.48 Gbps), powerful FEC with the GBT protocol, a good (the only?) replacement for TTCrx. Good quality clocks for ADC and high-speed serial data transmission.



Package: 17 mm × 17 mm, 20 × 20 ball array.

Not very suitable for trigger and high data rate (~100 Gbps per board) links.

Power: 2.2 W (all on).

(final) Prototype 2013.

ASICs being designed or discussed

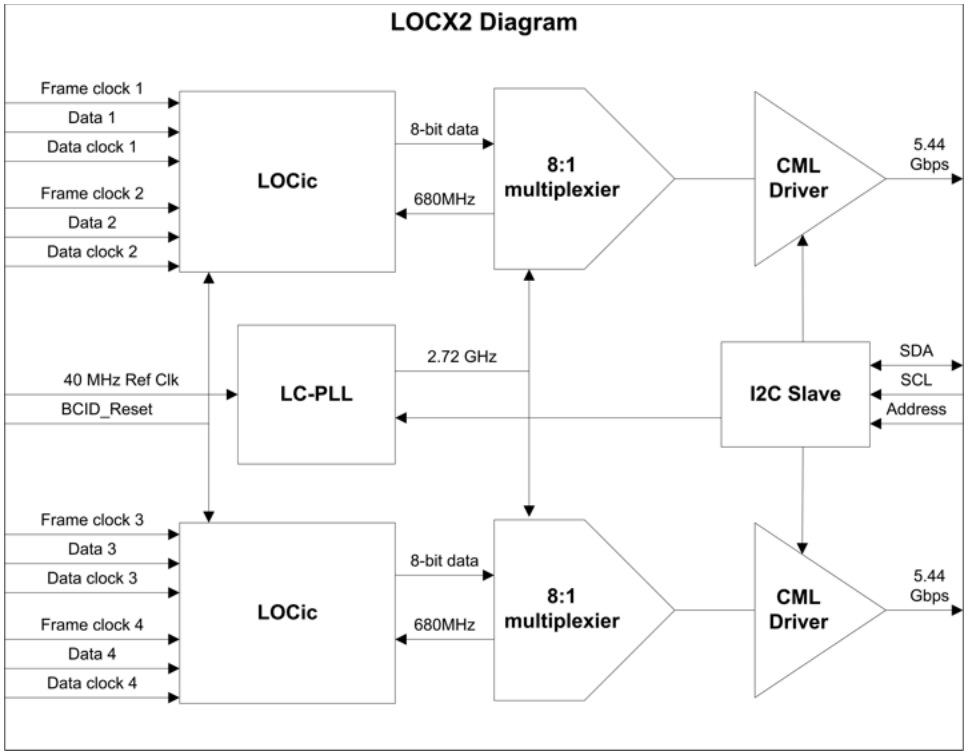
- Serializer – LOCx2
  - 0.25 µm Silicon-on-Sapphire CMOS. No SEL mechanism, low SEU. Designed for ATLAS LAr trigger upgrade. Two-channel sharing one PLL. Low power (1 W). 2 × 5.12 Gbps per chip (user bandwidth 2 × 4.48 Gbps). Best for low latency and high data rate transmission. Package QFN-88 (10 mm × 10 mm)

and designed with the dual optical transmitter. Interfaces to 2 × 8 channels of ADC.

Highly optimized for one (ATLAS/ LAr trigger upgrade) application. Not suitable for any other applications unless the interface part: LOCic, is re-designed.

Prototype in 2013 – 2014. The serializing and CML driver blocks prototyped up to 8 Gbps.

LHC clock + 16 ADC serial outputs

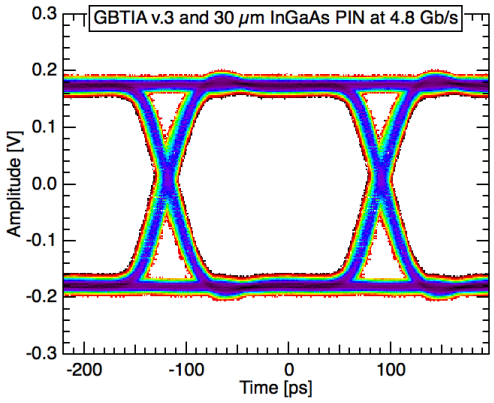


ASICs being designed or discussed

- EEL and VCSEL driver – GBLD
  - Programmable current matches EEL and VCSEL.
  - Pre-emphasis, can be used as a cable driver.
  - Version 4.1 will be production-ready.
- VCSEL driver – LOCld, LpGBLD and LD65
  - LOCld: Designed to match with LOCx2, has two packaging versions: single channel and dual channel (to simplify system implementation). Single channel prototyped 2013. Whole chip prototype is being tested.
  - LpGBLD: a strip-down version of GBLD only for VCSEL to save power. Prototyped 2013. May replace GBLD and become “CERN baseline”.
  - LD65: 65 nmCMOS. Designed and (preliminarily) tested to 10 Gbps at SMU.
- Array VCSEL drivers – LOCld4, and an R&D from OSU
  - LOCld4: a 4-channel VCSEL array driver, open drain, design for 8 Gbps. Under test at SMU. If successful, will move to 12-channel VCSEL driver.
  - The R&D from OSU: mostly based on GBLD, an 8-channel VCSEL driver (0.13 µm CMOS) has been tested at 5 Gbps. A 10 Gbps version is being designed with 65 nm technology.

ASICs being designed or discussed

- GBTIA
  - The only one in our field. No need of an limiting amplifier, making board level implementation very simple.
  - Tested at 5 Gbps.
  - Sensitivity -18 dBm.
  - Dynamic range 12 dB.
  - Currently used in VTRx (Versatile Link common project).
- Config and Control – GBT-SCA
  - Last one in the GBT family to be prototyped (Aug. 2013).
- LpGBT or 10 Gbps GBT
  - 65 nm CMOS
  - Low power mode: 4.8 Gbps bidirectional
  - High speed mode: 9.8 Gbps for the up-line, 4.8 Gbps for the down-link.
  - May be the project after the completion of GBT (2014?).



Issues for future ASIC work

- Technology choice
  - Bulk silicon CMOS, led by CERN: 0.25 µm and 0.13 µm CMOS, 65 nm. TID becomes not an issue, but SEU needs mitigation and R&D.
  - Silicon-on-Sapphire 0.25 µm to 180 nm. Pioneered by a university group but it really needs leadership from national labs.
  - SOI for System on Chip, readout included. Collaboration mostly led by KEK.
- Resources in HEP
  - GBT: CERN led 5 – 6 years development , 17 authors, 2 to 5 iterations.
  - LOC: SMU, 1 to 3 FTEs over 4 – 6 years, 2 to 4 iterations.
  - LpGBT: estimate 14.5 man-year, if it becomes a CERN project.
- Packaging
  - C4-BGA for GBT like chips with Gbps speed and ~ 400 connections.
  - QFN good for Gbps speed with < 100 connections.
- Reliability and QA
  - Not rigorously followed up, usually ad hoc. But good enough so far?
  - Desires more attention and resources, especially when we want to screen each chip and demand a high system reliability. GBT > 50k chips, LOC ~ 10k chips.

Issues of using COTS

- TID and SEU: for digital circuits, as the feature size shrinks, TID becomes a non-issue (verification still needed). SEU becomes an issue that often renders application in detector front-end difficult.
- Laser driver and TIA (trans-impedance amplifier)
  - are available but due to the associated control and config circuits which are usually a micro-processor, they are rather rad-soft and not suitable for detector front-end.
  - The driving part of a driver is usually rad-tol, if the micro-processor config/control circuits can be by-passed.
- SerDes
  - Generic SerDes such as GLink and TLK2501 become obsolete or with few choices.
  - We need to follow up with SerDes embedded in FPGAs, especially for the link back-end.
  - It has become non-trivial to operate these highly complex FPGAs with SerDes embedded, expertise needs to be retained in HEP.

Summary

- Needs in HEP:
  - 5 – 10 Gbps per fiber channel.
  - Small form factor or array optics to meet requirements in 10^2 Gbps per board space/material constraints in inner trackers.
  - Custom design for detector front-end, COTS for the back-end.
- ASICs
  - GOL, GBTx, LOCx2, (Lp)GBLD, GBTIA, LOCld.
  - LpGBT, LOCld4.
  - Technology choices, how many suits our needs and we can afford?
  - Application Specific but common IPs, suitable for “common projects” cross experiments.
- COTS
  - Not “plug&play”, needs to keep the expertise for multi-gigabit per second system development.