Collaborative Efforts For 3D Integrated Circuits In HEP

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For
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Outline

- This talk will provide a quick overview of 3D activities related to HEP
  - Why 3D
  - Early history
  - Collaborative efforts that have evolved
  - A focus on US efforts
    - Processes used
    - Review of major problems
    - Brief summary of 3D circuit designs and tests
  - New and Future developments
- Conclusions
- References
- Appendix with more circuit details and test results

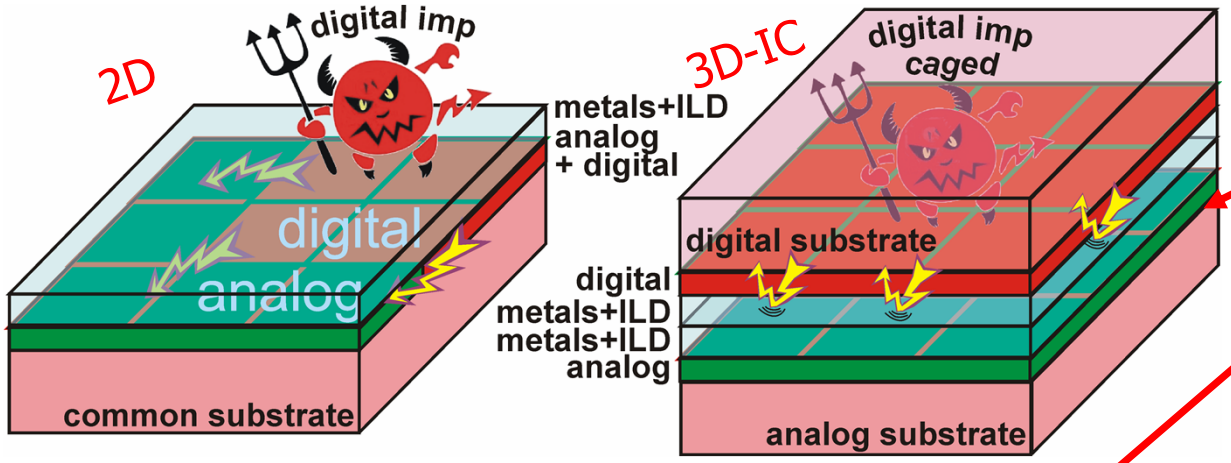
Introduction

- Fermilab began development of the first 3D integrated circuit for HEP in late 2006. The idea was to explore this new technology with a practical application. The first design was a 3 tier pixel readout chip that had an ambitious set of features for the ILC. Although the 3D technologies were in an early stages of development, we thought the R&D effort had significant potential. After our first silicon was received in 2008, our efforts expanded. Over the years the path toward 3D integrated circuit design has divided and grown to include many other participants. There have been some successes but the path forward still has a ways to go before 3D is considered a viable option for HEP

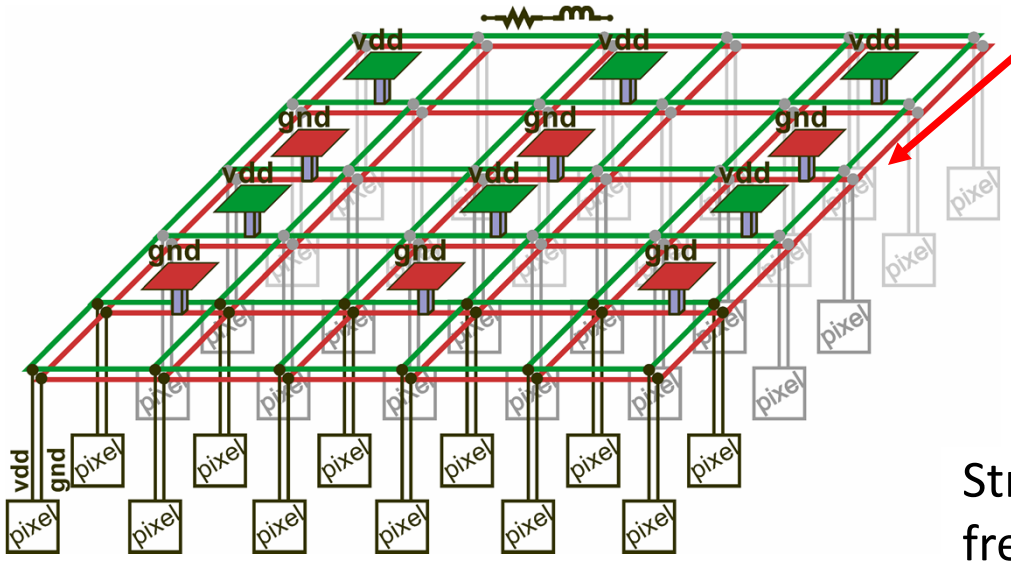
3D-IC: advantages [1]

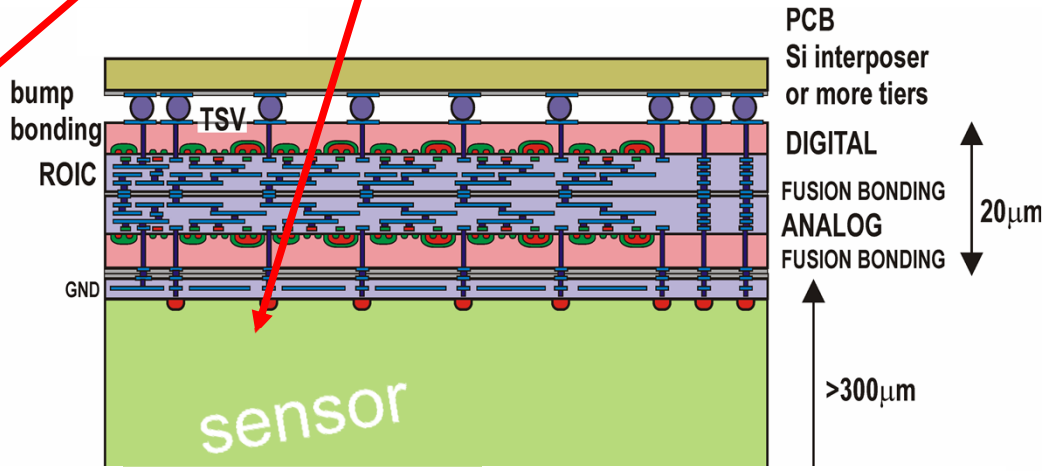
Why?

- 3D-IC offers a transformational change to address current roadblocks in advancing fine-grained detector, and with in-situ processing.



- **3D ROICs - complete separation of digital activity from low-noise analog parts**
- **3D ROICs - uniform distribution of power supply and I/O pads on the back side**
- **ROICs can be integrated with sensors without bump-bonds**

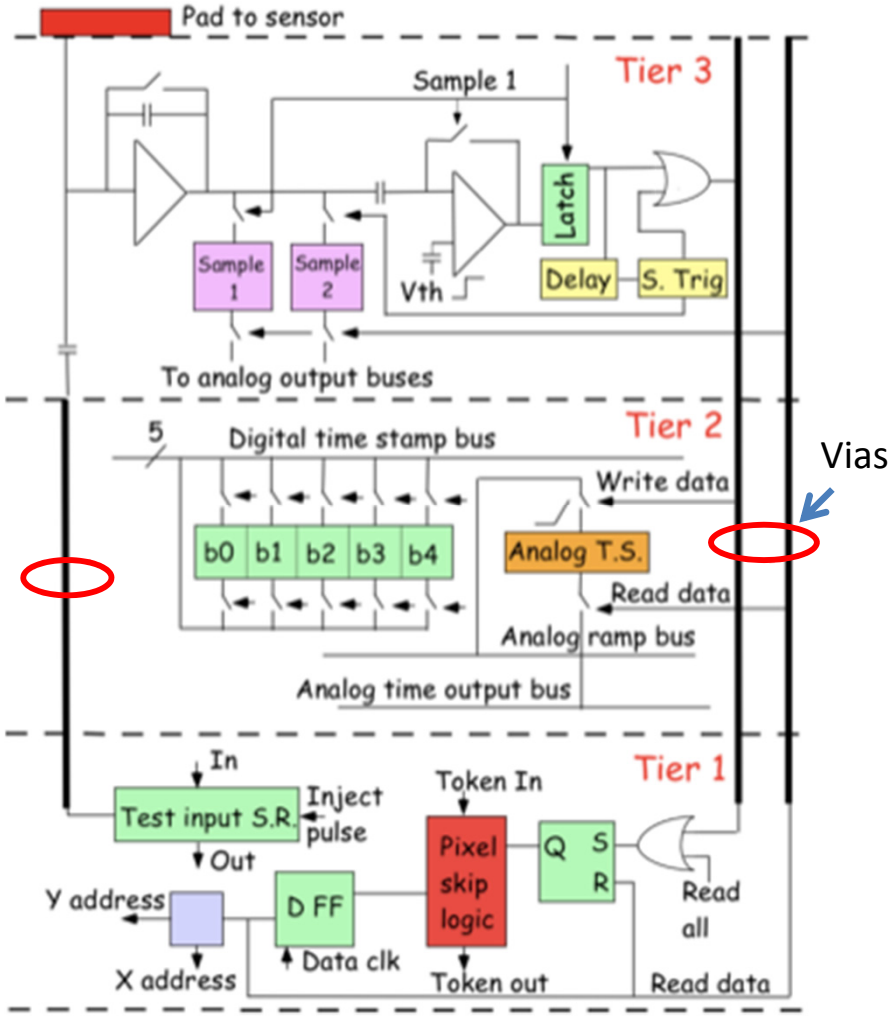




Strategic direction: 4 side buttable, dead-area-free detectors

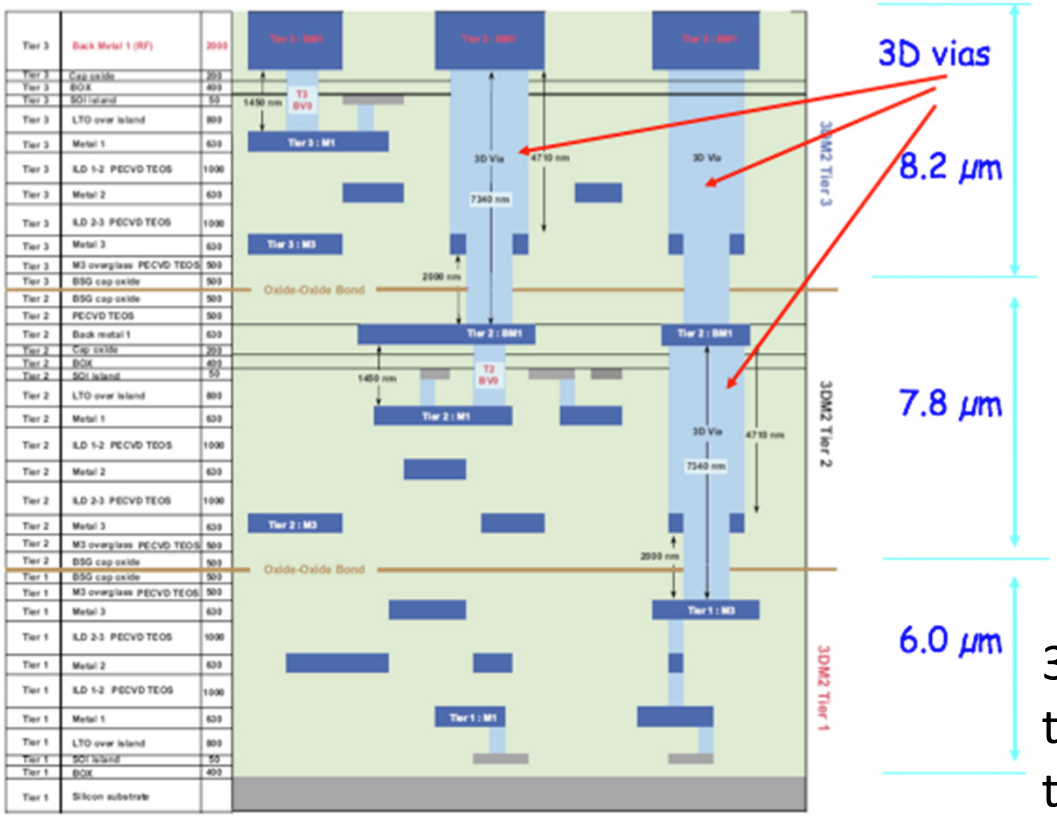
Early History: Design for MIT LL 3D Process

- Joined MIT LL collaboration sponsored by DARPA to investigate 3D IC design in SOI technology
- Our initial 3D design used MIT LL 3D SOI process with 0.18 um features. [2]
- VIP1: First run had serious processing problems resulting in near zero yield.
- VIP2: Design was made more conservative and resubmitted.
- Second submission produced better yield and functioning chips.
- Full function 3-tier chip for ILC pixel detector, main features:
  - 64x64 array
  - 20 um (VIP1), 24 um (VIP2a) pitch
  - Digital and analog time stamp circuitry
  - Data sparsification with high speed look ahead for next hit.
  - Pixel analog information output along with time stamp.

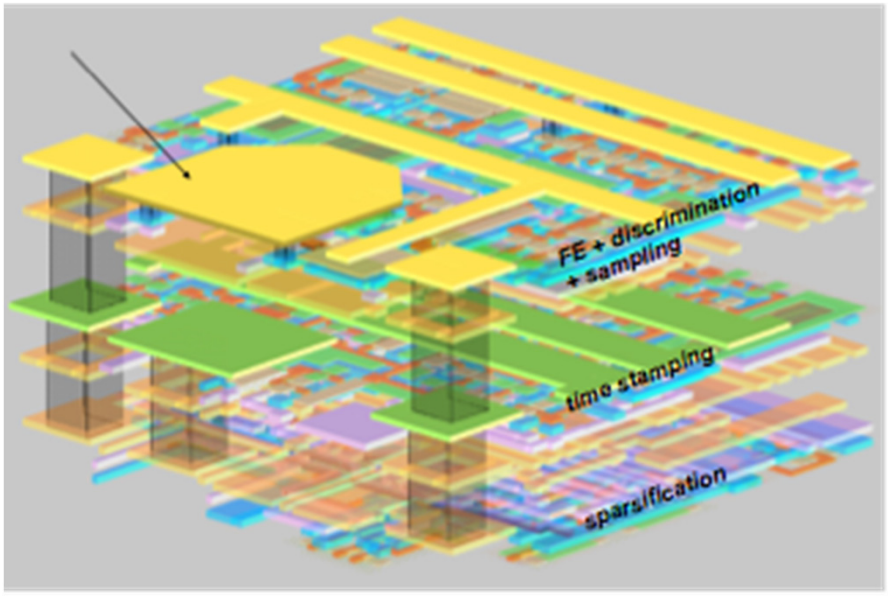


Single ILC pixel schematic divided into 3 tiers

MIT LL 3D Process



Cross-sectional view of MIT process using oxide bonding on a 3 tier assembly. Top 2 layers are about 8 um thick with 1.2 um vias inserted using a via last process (vias inserted after oxide bonding and thinning).



3D view of an ILC pixel cell showing the 3 tiers and the vias between the tiers.

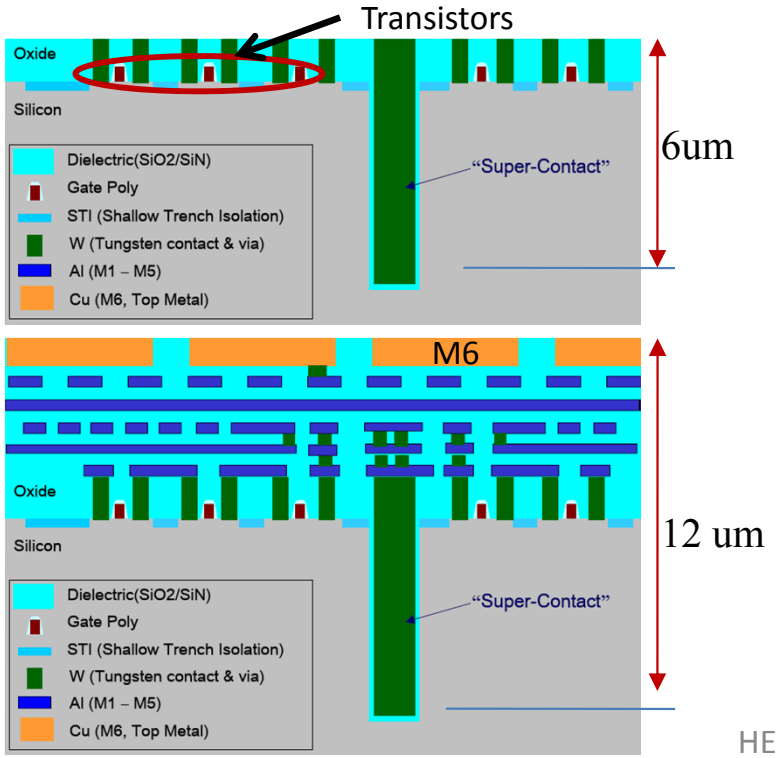
*No problems were identified with the vias or bonding during the testing.
*Further work in this process was stopped due to concern about analog performance in SOI and radiation tolerance in future applications.
However feasibility of 3D for HEP was Demonstrated for first time.

Move to Commercial 0.13 um CMOS Process at Global (Chartered) Foundries

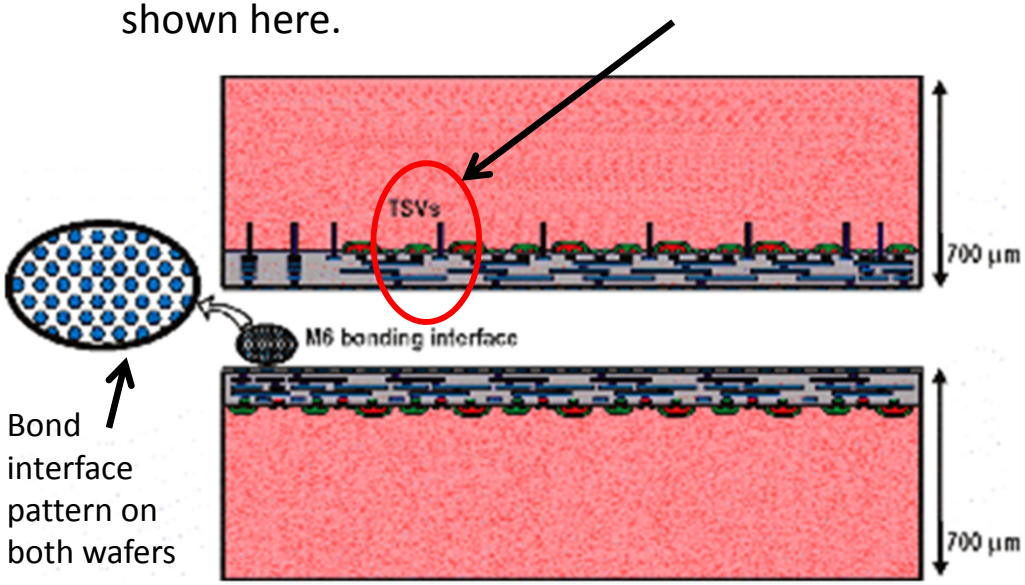
- Access to Global foundry thru Tezzaron
- After fabrication of transistors 1 um dia, 6 um deep, blind vias (super contact) inserted (via middle process).
- Super contact filled with tungsten at same time connections are made to transistors.
- BEOL, M1-M6 completed.
- M6 used to make pads intended for Cu-Cu thermo compression W2W bonding.

After FEOL fabricate 6 um super contact (via)

Complete BEOL processing



- Very regular pattern of M6 copper bond pads is critical for proper bonding.
- Copper bond pitch is about 4 um
- In 2 tier chip, the wafers are bonded face-to-face with vias pointing into the substrate as shown here.



Bond interface pattern on both wafers

Will come back to wafer bonding options with Global wafers later.

3D Collaborations Form

- After beginning to work with Tezzaron, a group of 15 HEP institutions from 5 countries formed a 3D consortium to submit a multi-project run to Chartered/Tezzaron using the via middle process with small (1.2um) vias for a few hundred $K. Jumped directly to design and fabrication of full scale 3D ICs.
- Later in 2011, the European Union formed the AIDA consortium for wafer thinning, etching of vias, planarization, and back metalization leading to wafer bonding and 3D integration. AIDA is funded for 8M euros by the European Commission under FP-7 Research Infrastructures.
- Most recently MOSIS, CMP, and CMC have come together to offer commercial 3D IC fabrication using Tezzaron/Global Foundries. The first multi-project run is due back in June 2013. The first MPW run closely follows the features of the HEP consortium MPW run.

Overview of AIDA Subprojects [3]

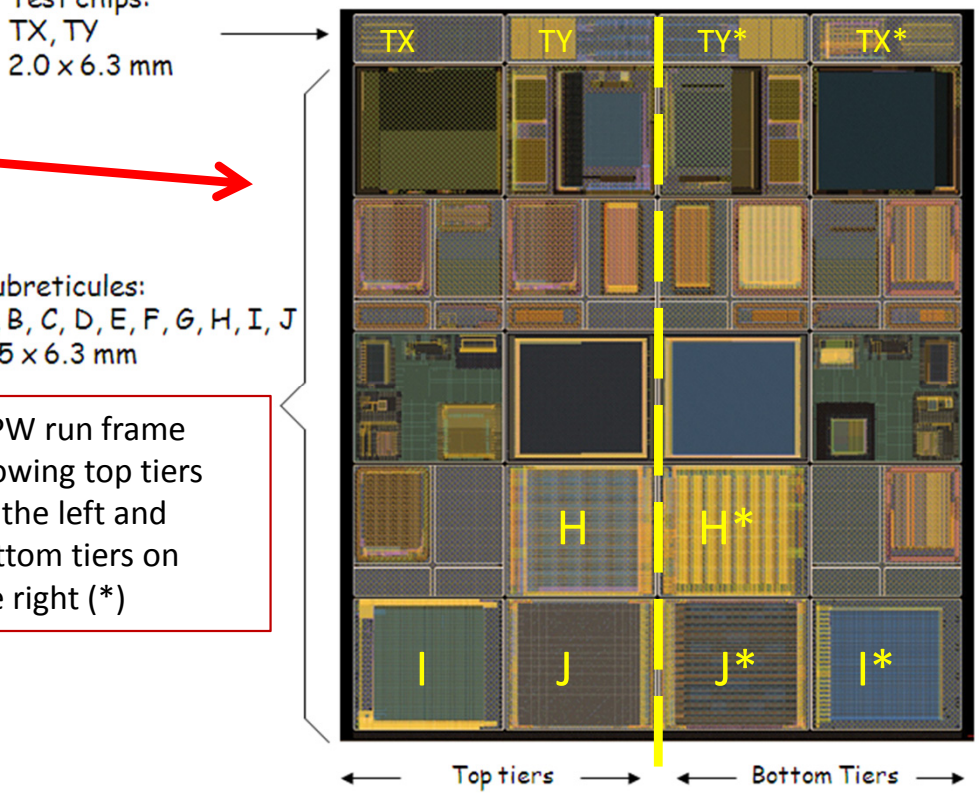
Numerous European institutions investigating 3D processes, generally focusing on via last processes with large vias:

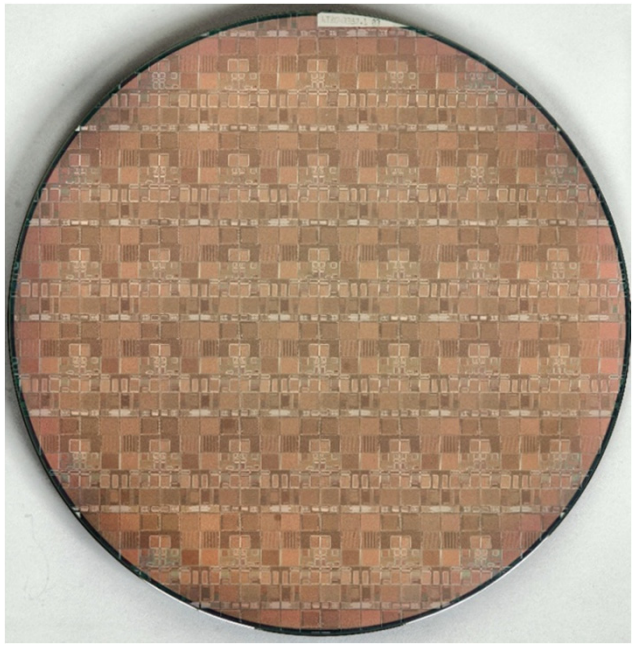
- **Bonn/CPPM:** Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch): The FEI4 wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer),
- **CERN:** Interconnection of MEDIPIX3 chips using the CEA-LETI process: The MEDIPIX3 wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer),
- **INFN/IPHC-IRFU:** Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others). Tezzaron/Chartered offers a via-first technology. Hence no post processing is needed in the first stage of this project. Post processing may become necessary in a later stage preparing the wafers for interconnection (UBM).
- **LAL/LAPP/LPNHE/MPP:** Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process. The wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer).
- **MPP/GLA/LAL/LIV/LPNHE:** Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT. The FEI4 wafers need to be post-processed (thinning, etching of vias and addition of a redistribution layer),
- **UB**: 3D interconnection of 2 layers of Geiger-Mode APD arrays with integrated readout in Tezzaron Chartered technology. This via first approach does not need post-processing.
- **RAL/UPPSALA**: Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV including redistribution of I/O connections to the backside for a 4-side buttable device. The ASIC tiers need to be post-processed (thinning, etching of vias, adding UBM and redistribution layers)

Global foundry Multi-Project Run

- Multi-project HEP run submitted to GF through Tezzaron with numerous designs from 3D consortium.
- One set of masks used for 2 tier 3D circuits.
- Frame divided into 24 subreticules. 12 for top tier and 12 for bottom tier.
- Intended for wafer face to face bonding.
- Produces both normal and reversed designs.
- Designs contributed by France, Italy, Germany, Poland and the US.

Frame show symmetry about center line





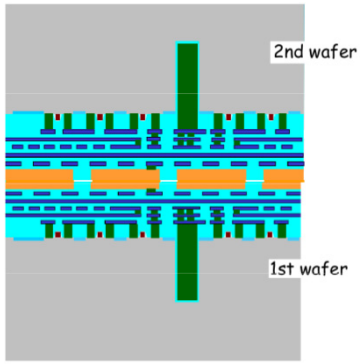
Eight inch wafer

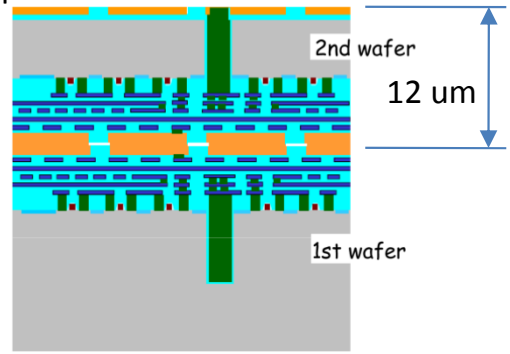
Fermilab designs:
H: VICTR – pixel readout chip mating with two sensors for track trigger in CMS
I: VIP2b – ILC pixel chip with time stamping and sparcification (2 tier version of MIT design)
J: VIPIC – fast frame readout chip for X-ray Photon Correlation Spectroscopy at a light source
TX and TY : test chips

Numerous Challenges Encountered

- Design and submission issues
- Fabrication issues
  - Chartered bought by Global
  - Knowledgeable foundry personnel lost
  - Flip-flopped on decision to stop 3D processing on 130nm
  - Full lot of wafers lost due to improper frame placement (1.2 mm off center)
  - New lot re-fabricated

Tezzaron bond process

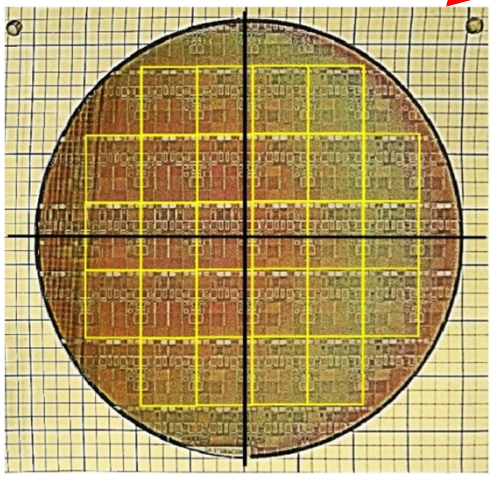




Flip wafer and bond

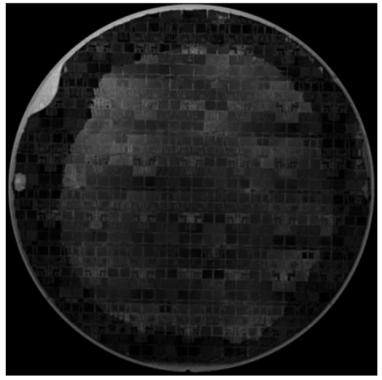
Thin wafer to 12um, add metal

1.2 mm



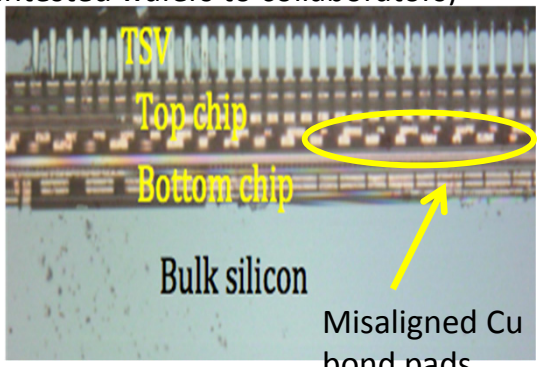
Frames not placed symmetrically about wafer center line – prohibits bonding due to bonder limitations.

First 6 wafers bonded at EVG Tempe, lost due to residual carbon layer



Bonded wafer acoustic image (light sections show poor bonds).Poor bonding may be also due to lack of forming gas in Tempe bonder.

Second 6 wafers bonded at EVG Tempe lost due to misalignment (mistake to send untested wafers to collaborators)



Misaligned Cu bond pads

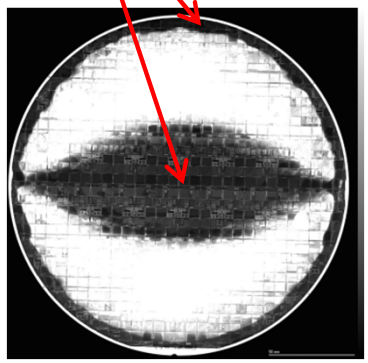
Decision made to bond remaining wafers at EVG Austria due to different wafer alignment process and use of forming gas.

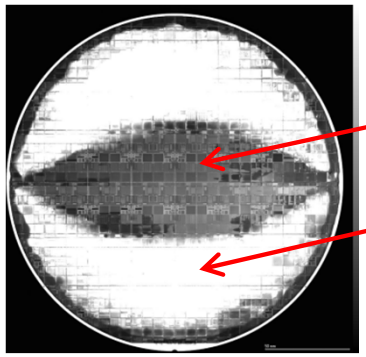
- Bonding started on new lot using Tezzaron Cu-cu bond process
  - Etch surface oxide exposing Cu bond pad (350 nm high)
  - Align for face to face bonding
  - Cu-Cu thermo compression bond
  - Thin one side to expose vias
  - Add metalization for bond pads

Wafer Bonding Results

- Remaining 16 wafers sent to EVG Austria for bonding.
  - Initially 8 wafers would not bond
    - Tried many bond pressures with forming gas.
    - Attributed to larger copper grain boundaries which have been found to develop over time. (Documented by Tezzaron). Wafers were “old”.
  - Next 8 wafers sent to Ziptronix for bond pad processing and then sent back to Austria
    - 1 wafer pair broke in the EVG bonder at high pressure
    - 3 remaining wafer pairs exhibited poor bonding due to trapped gas.
      - Cu bond pads insufficiently exposed during etch process.
      - Oxide bond occurred around rim of wafer trapping gas.

Relatively good bonding





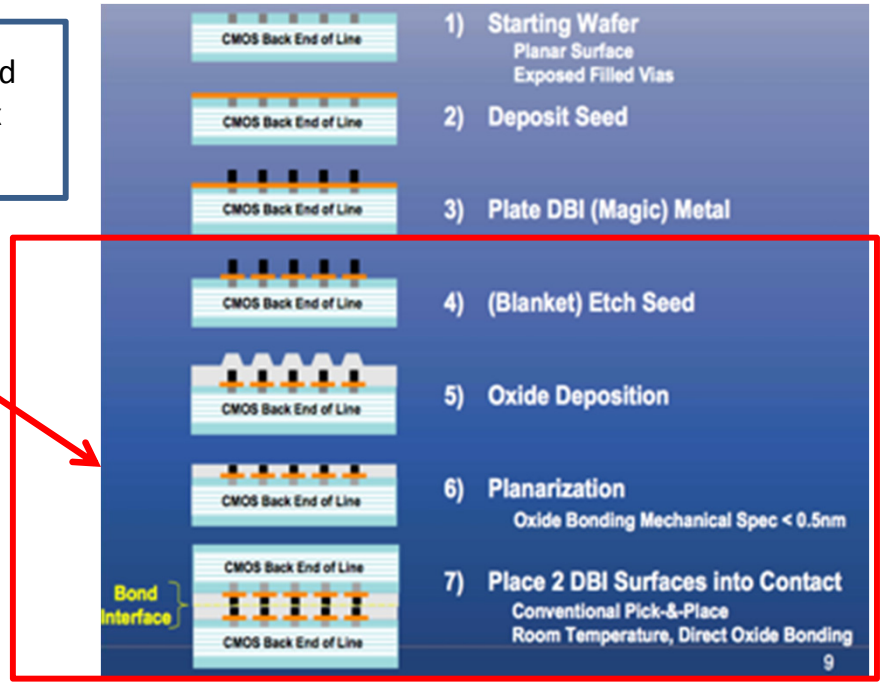
Poor

Bad

Bonded wafer acoustic images, white areas are bad bonding

- Decided to try bonding wafers using Ziptronix DBI (Direct Bond Interface) process with copper.
  - No unused wafers left.
  - Ziptonix separated one pair of poorly bonded Tezzaron wafers from EVG in Tempe
  - Wafers were reprocessed for oxide bonding and bonded at Ziptronix.

Simplified Ziptronix process



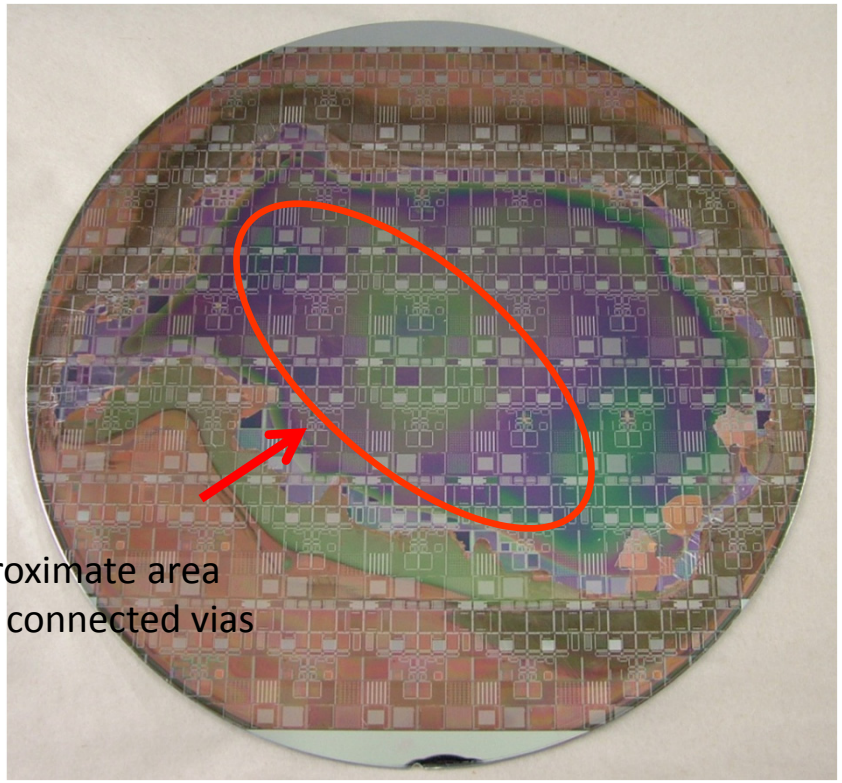
Part of Ziptronix Process used

Ziptonix bonding was not great due to prior history of wafers.

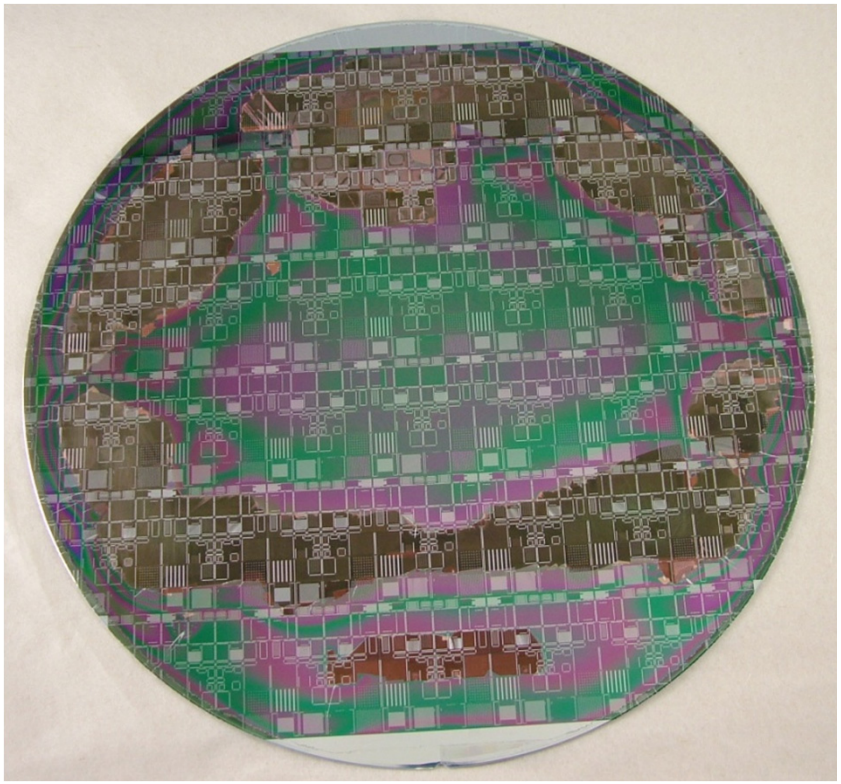
Wafers Diced for Test Parts

- Ziptronix bonded wafer
  - Used refurbished Tezzaron bonded wafers as a test for DBI process
  - Limited number of useable parts for testing
  - Parts distributed to collaborators
  - Fermilab parts
    - VICTR (tested)
    - VIPIC (tested)
    - VIP2b (not tested yet)

- Tezzaron bonded wafer
  - Eye pattern of useable parts (in center)
  - Limited number of useable parts for testing
  - Parts distributed to collaborators
  - Fermilab parts
    - VICTR (tested)
    - VIPIC (tested)
    - VIP2b (not tested yet)



Ziptronix bonded wafer – non-uniformity of Si CMP caused by non-uniform bonded area resulted in right side TSVs being buried and not connected.



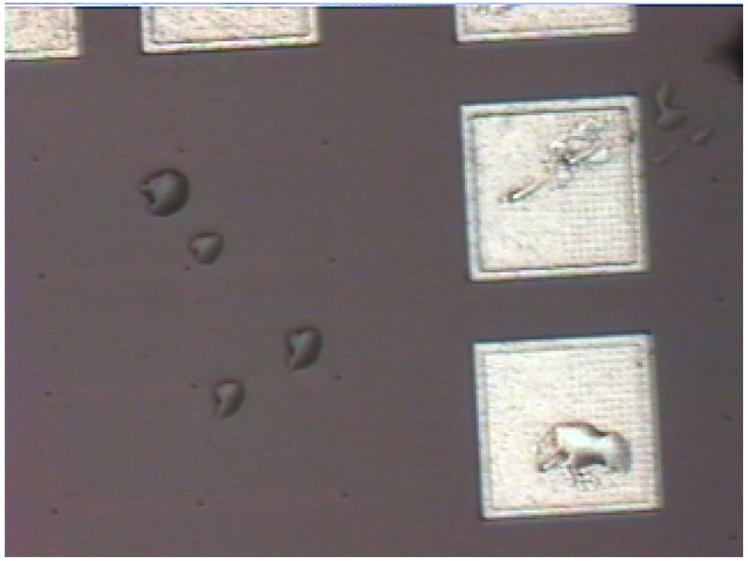
Tezzaron bonded wafer – TSVs appear to connected across the entire bonded area (eye pattern in center).

Preliminary test results

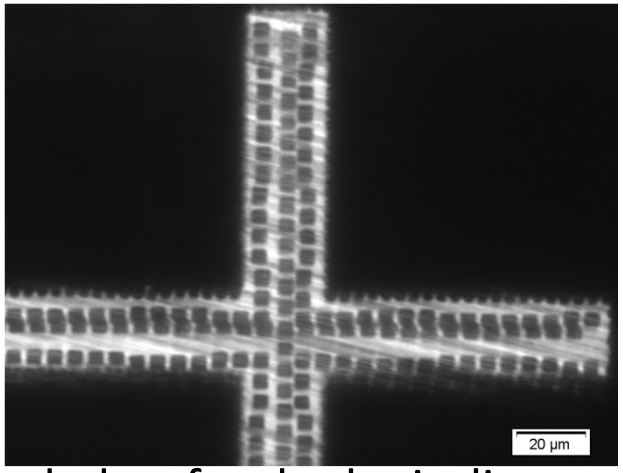
- Although the wafer processing was not good, a few working parts were obtained from both the the Cu-Cu and DBI bonded wafers. [4]
- FNAL Designs
  - VICTR: Vertically Integrated CMS Tracker
    - Chip looks for coincidences between closely spaced detector planes to form a track trigger.
    - Identifies particles with high Pt and provides z and phi resolution
    - Some parts from the Cu-Cu bonded and DBI bonded were found to be fully functional
  - VIPIC: Vertically Integrated Photon Imaging Chip
    - Intended for X-ray Photon Correlation Spectroscopy
    - Designed to quickly count hits in every pixel and read out quickly the hits in a sparsified and dead timeless manner.
    - Operates in 2 modes: Timed readout and imaging mode.
    - A few chips from both the Cu-Cu and DBI bonded wafers are working
  - VIP2b: Veritically Integrated Pixel chip
    - Design is very similar to MIT chip (VIP2a) previously designed and tested
    - Design changed from 3 Tiers (VIP2a) to 2 tiers (VOP2b)
    - Parts are about to be tested
  - Some more information on the design and test results for the chips are available in appendix.
- Similar positive results from different designs on the Cu-Cu and DBI bonded wafers have been reported by other consortium members
    - CPPM Marseilles tested FE-TC4 (ATLAS pixels)
    - University of Bergamo/INFN tested MAPS chips
- Demonstrated the feasibility of 3D for HEP using 2 more 3D bonding processes

New 18 Wafer Lot

- 18 new wafers fabricated at Global to replace wafers lost during assembly (at no cost).
  - No known processing problems
  - Very long (poor) delivery
  - One wafer used for process monitor tests
- 8 wafers bonded in Austria using Cu-Cu bonding.
  - First two bonded pairs showed bubbles near bond pads which were removed by heating.
  - First 2 bonded pairs showed poor alignment
  - Second 2 bonded pairs have better alignment and have just arrived

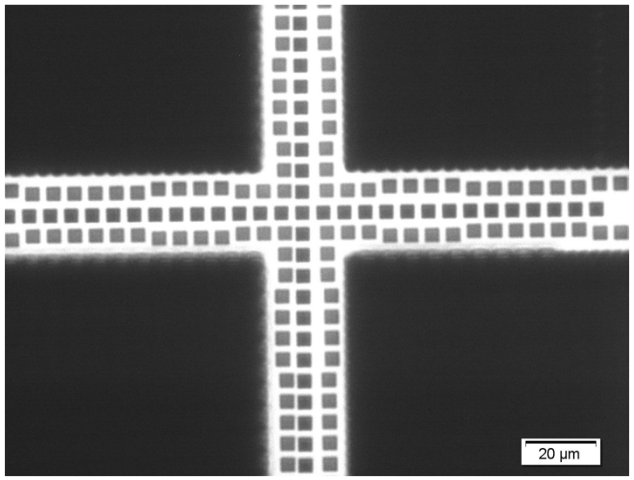


Bubbles under passivation



First bonded wafers had misalignment
(2.5 um vertical misalignment shown here).

Alignment keys with 3.8 um square dots and 2.2 um spaces



Better alignment on 2nd bonded pair

New Wafer lot

- 8 remaining wafers ready for the DBI process at Ziptronix
  - Four completed 3D wafers due back soon.
  - Have requested alignment photos as soon as they are available.
  - Alignment expected to be more consistent and better with the DBI wafers.
  - Hopefully functioning die from these wafers can be distributed to consortium members.

Collaboration Status

- Fermilab consortium has no plans to organize another 3D run at this time. Expect to share results as they develop.
- AIDA will continue its efforts and is funded through 2014.
- MOSIS/CMP/CMC are awaiting return of its first 3D run (due in 3 weeks). MOSIS is committed to offering a 3D process. It does not want to submit another run using Global Foundries. It is awaiting verification of new process flow at Tezzaron. Earliest possible next run is spring 2014.

Major changes at Tezzaron/Novati

- Two major issues were encountered on our first multi-project run
  - Processing of wafers at Global foundry (Tezzaron currently has large backlog at Global)
  - Delays and poor results for bonding and alignment from outside vendors (EVG).
- Tezzaron has moved on several fronts to solve these issues. [5]
  - Purchase of SVTC (formerly Sematech) in October 2012 and formed Novati. Allows via formation alternative and semiconductor processing up to 300 mm wafer processing. Can process 3000 wafers per week. Can also do DBI.
  - Licenced to use the Ziptronix DBI process (Dec 2012). (DBI wafer alignment is better.)
  - Purchased it's own high force bonder for Cu-Cu bonding, due for delivery late this year.

Major changes at Tezzaron/Novati

- Tezzaron is working on 2 alternate processes for via insertion as alternates to Global foundries.
  - Via last processing on wafers from many other foundries, (can eliminate export issues)
    - Cu-Cu or DBI bonding
    - 2 um tungsten vias inserted from thinned back side
    - 7 um pitch
    - 5 um landing pads on metal 1
    - Can work with several different foundries and technologies
  - Via near end of line on wafers from many other foundries, (can eliminate export issues)
    - Cu-Cu or DBI bonding
    - 2 um vias inserted from top side to M4
    - Back end of line M5 and M6 finished at Novati
- Planning 20M capital equipment improvements this year. $100 M sales expected for 2013.
- Novati now claims to be the first open-platform, full-line foundry in the world offering 3D stacking services and test to all its customer's for both 2.5D interposer and 3D designs with true, 3D integration and TSV interconnect.

Conclusion

The 3D activities started by Fermilab expanded to a HEP 3D multi-project run with 15 institutions. In addition, a European consortium with separate funding, and a partnership between 3 commercial silicon brokers to offer 3D circuit fabrication have been formed. The 3D process is still in its development stages. Designers are working to identify the best applications for 3D technologies in HEP and elsewhere. The commercial market will continue to drive 3D development and we can benefit from their investments.

Although we have encountered numerous obstacles, we have been able to design, fabricate, and test working 3D ICs from 3 different assembly processes.

Just as the development of silicon strip ICs, pixel readout chips, and MAPS have taken time to bear fruit, the road to 3D ICs can also be expected to take time. Most importantly, this technology has the potential to provide important new opportunities for HEP detector/readout development.

References

- [1] Deptuch, G. , The 3D integration and SOI pixels, WE-Heraeus Seminar, Bad Honef Germany, May 23-25, 2013.
- [2] Deptuch, G.; Demarteau, M.; Hoff, J.; Lipton, R.; Shenai, A.; Yarema, R.; Zimmerman, T.; , "Pixel detectors in 3D technologies for high energy physics," 3D Systems Integration Conference (3DIC), 2010 IEEE International , vol., no., pp.1-4, 16-18 Nov. 2010.
- [3] H.-G. Moser, Wafer Post Processing (Thinning, TSV), Document identifier AIDA-Del-D3-5, May 7, 2013.
- [4] R. Yarema, G. Deptuch, J. Hoff, F. Khalid, R. Lipton, A. Shenai, M. Trimpl, and T. Zimmerman, Vertically Integrated Circuit Development at Fermilab for Detectors, 2013_JINST_8_C01052
- [5] Conversations with Bob Patti, CTO of Tezzaron.

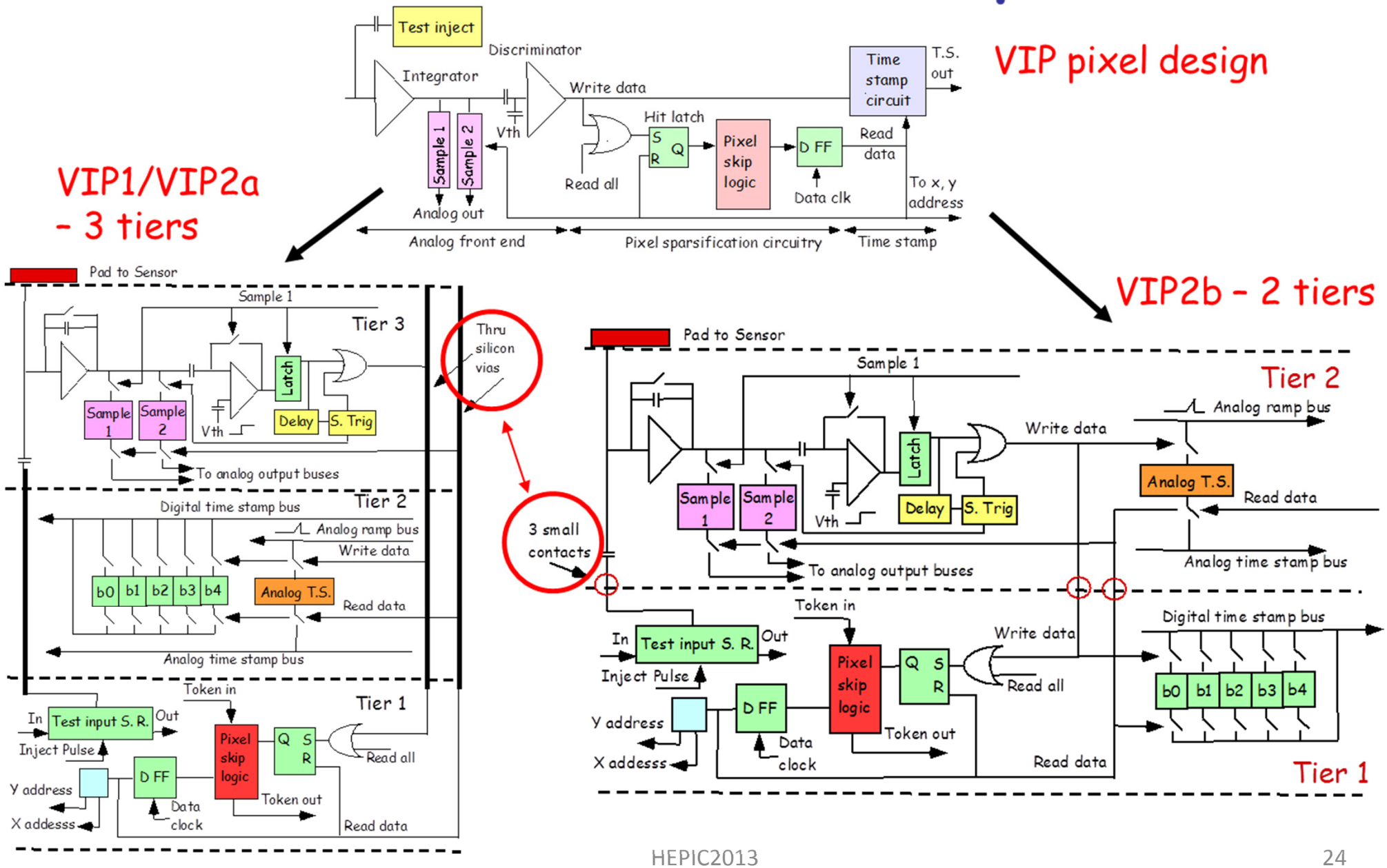
Appendix
Fermilab 3 D designs

- VIP2b - Chips received, test setup being assembled.
- VICTR – Chips received, preliminary tests completed, tests continuing
- VIPIC– Chips received, preliminary tests completed, tests continuing
- VIPRAM – New design, 2D chips have been received in preparation for 3D design

VIP2b design

- VIP2b design essentially the same as VIP2a.
- Because VIP2b is in a CMOS deep sub micron process, the design should be inherently more radiation hard.
- Radiation tolerance of Chartered 0.13 um process has been studied by another group and shown to be quite good.
- Going from 3 layers in 0.18 um technology to 2 layers in 0.13 reduces the pixel size.
- Using the via first process at Global eliminates the wasted area needed for vias in the MIT LL process.
- Global provides fully characterized process and models at commercial foundry along with standard cell libraries.
- VIP2b requires less 3D processing for via insertion than VIP2a

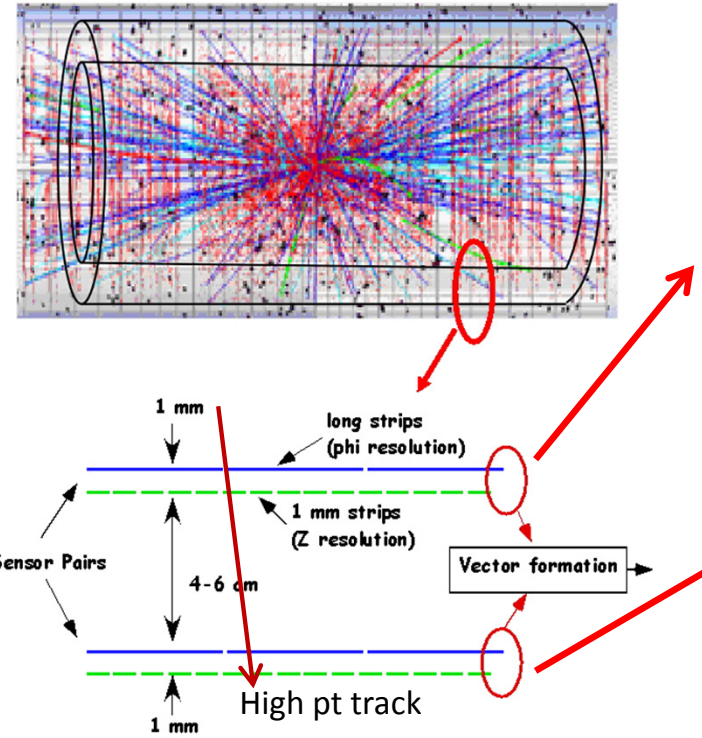
VIP2a and VIP2b Comparison



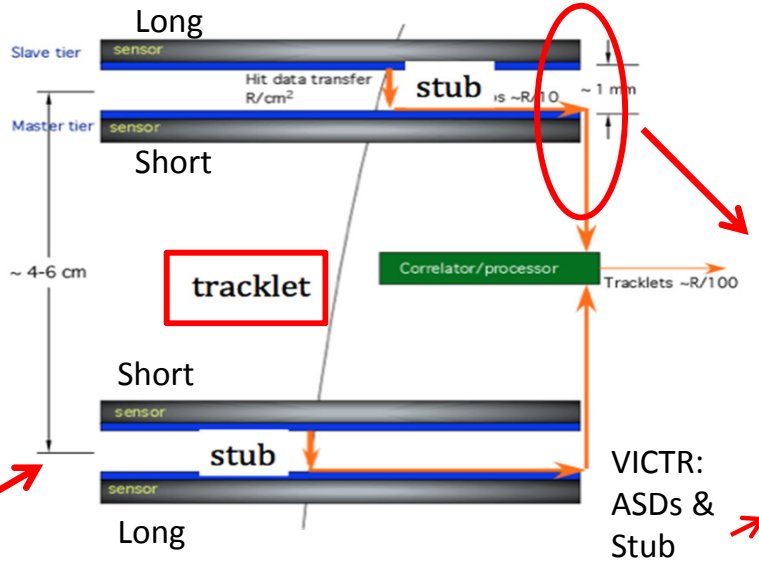
VICTR (Vertically Integrated CMS TRacker)

- High luminosities at the SLHC will require track trigger to reduce hit densities for data readout.
- Track trigger has several functions
  - Identify particles Pt above 2 Gev for data transfer
  - Identify particles with Pt above 15-25 Gev (low curvature tracks)
  - Provide Z resolution of about 1 mm for tracks above 2Gev with short strips
  - Phi resolution provided by long strips

- Our solution is based on assemblies of sensors and 3D readout chips that forms track stubs and tracklets looking for track curvature. [5]
  - Stubs are found locally from sensor pairs
    - Comprised of a top detector (phi) of long strips
    - A 1 mm interposer
    - The VICTR ASIC with 2 tiers
    - A bottom detector (z) comprised of short strips
  - Tracklets found from a pair of stubs
  - Tracks found by precise extrapolation of tracklets to other layers.
- More sophisticated logic to be added to later versions of VICTR

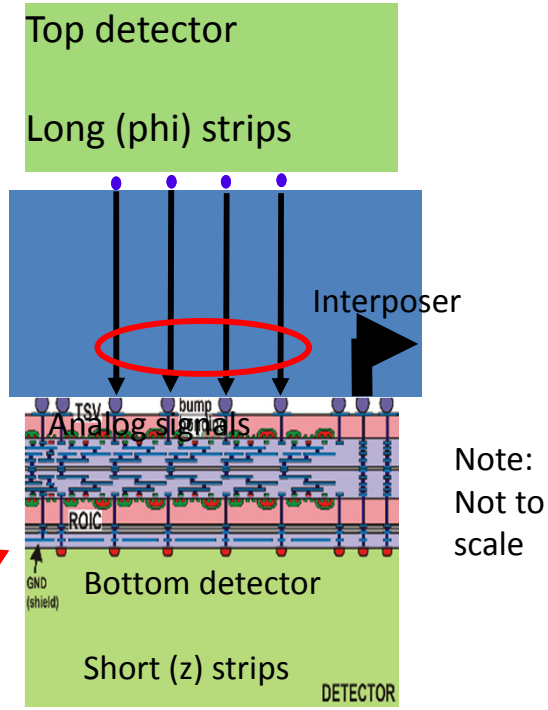


2 layers form a stub



2 stubs form a tracklet

VICTR: ASDs & Stub formation



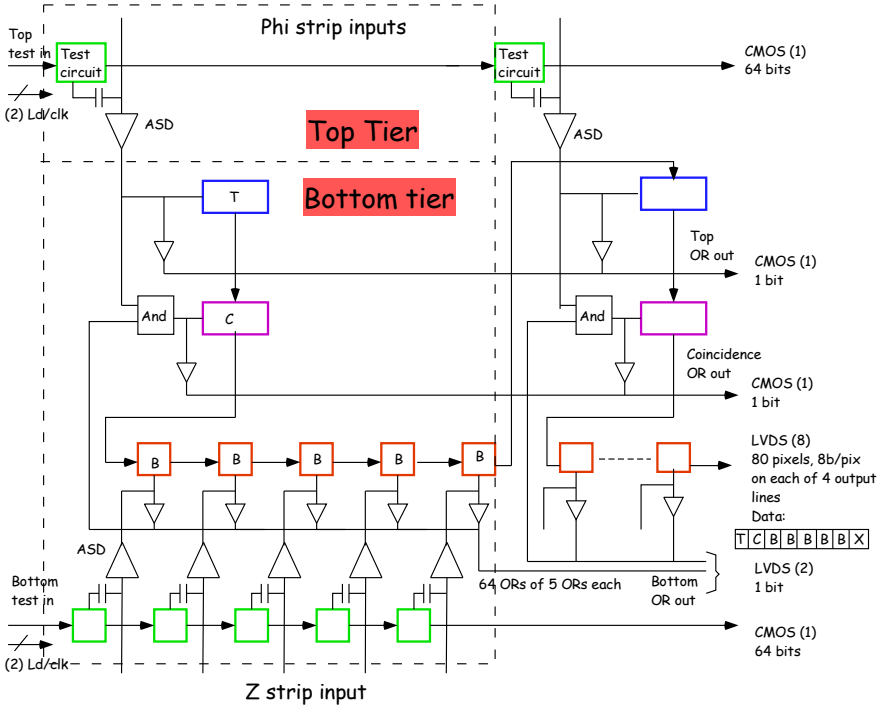
Note: Not to scale

Stub detail

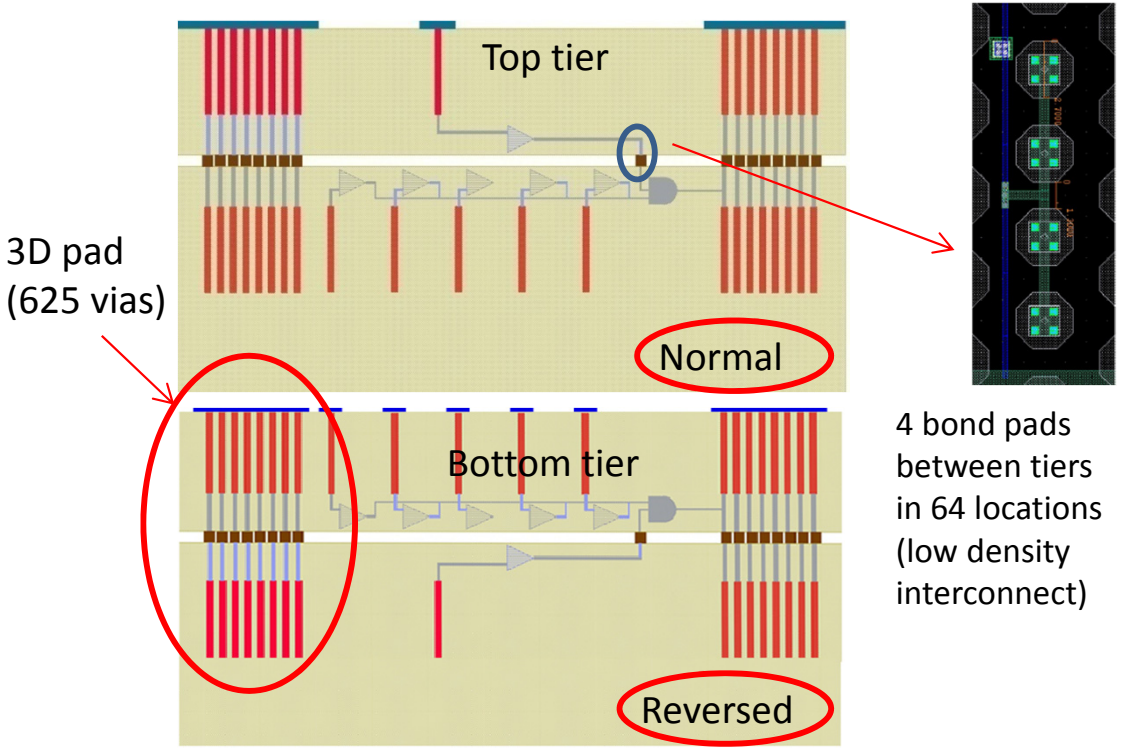
VICTR

- The function of the VICTR chip is to find coincidences between hits on the top strips (phi) and their associated bottom strips (z).
- Features
  - Programmable test input for every strip
  - Fast OR output for Top hits, Coincidence, and Bottom hits.
- Detector arrays for VICTR
  - 64 long strips
  - 5x64 = 320 short strips

- The single mask set wafers provide chips both with the top tier on the surface and the bottom tier on the surface.
- 3D pad connections were incorporated in the VICTR design to allow testing of both versions
  - Top tier, face up is called normal
  - Bottom tier, face up is called reversed.



Top tier to bottom tier coincidence circuit



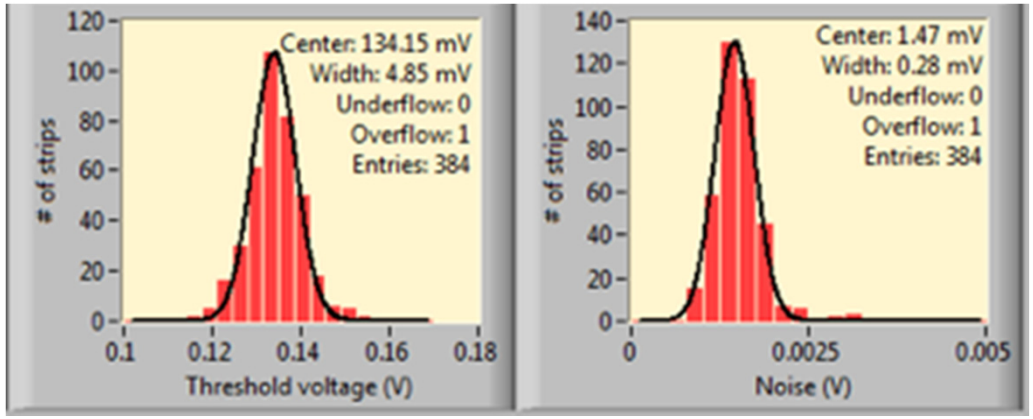
4 bond pads between tiers in 64 locations (low density interconnect)

Two versions of VICTR chip

VICTR

- A small number (11) of VICTR chips were visually inspected and selected for testing from both the Tezzaron and Ziptronix bonded wafers.
- Fully functional chips
  - Ziptronix bonded chips: 3 normal, 1 reversed
  - Tezzaron bonded chips: 1 normal
- Partially working chips
  - Ziptronix: 1 normal
  - Tezzaron: 2 reversed
- No inference should be made regarding process yields
- Functions tested
  - Charge injection to top and/or bottom ASD circuits
  - Masking of hit channels
  - Common threshold adjustment for top and bottom ASDs
  - Readout of top, bottom, and coincidence hits.
  - Power dissipation
  - Threshold dispersion
  - Noise

- In order for chips to work, one ASD signal is passed from the top tier to the bottom tier through 4 parallel copper bond connections.
- All signals are brought onto the chip through bond pads with multiple 1 um TSVs. (normal and reversed chips)
- Work is in progress to bond working chip to a detector



Threshold dispersion Noise

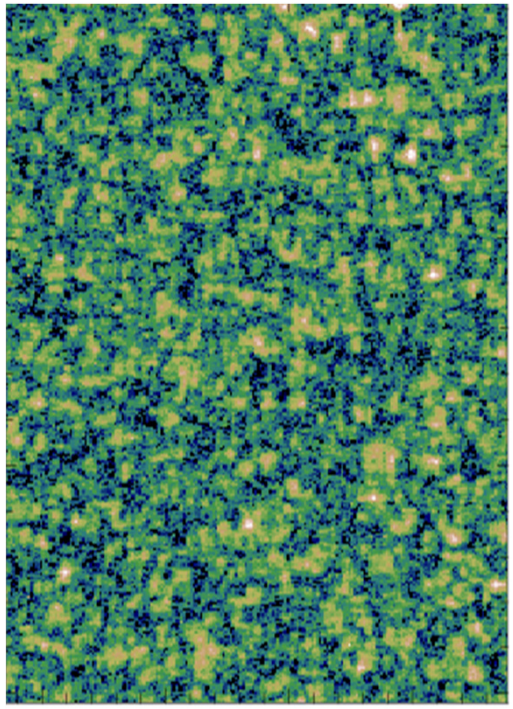
Hit and coincidence map

Random noise hits set by lowering threshold.

Green = hit

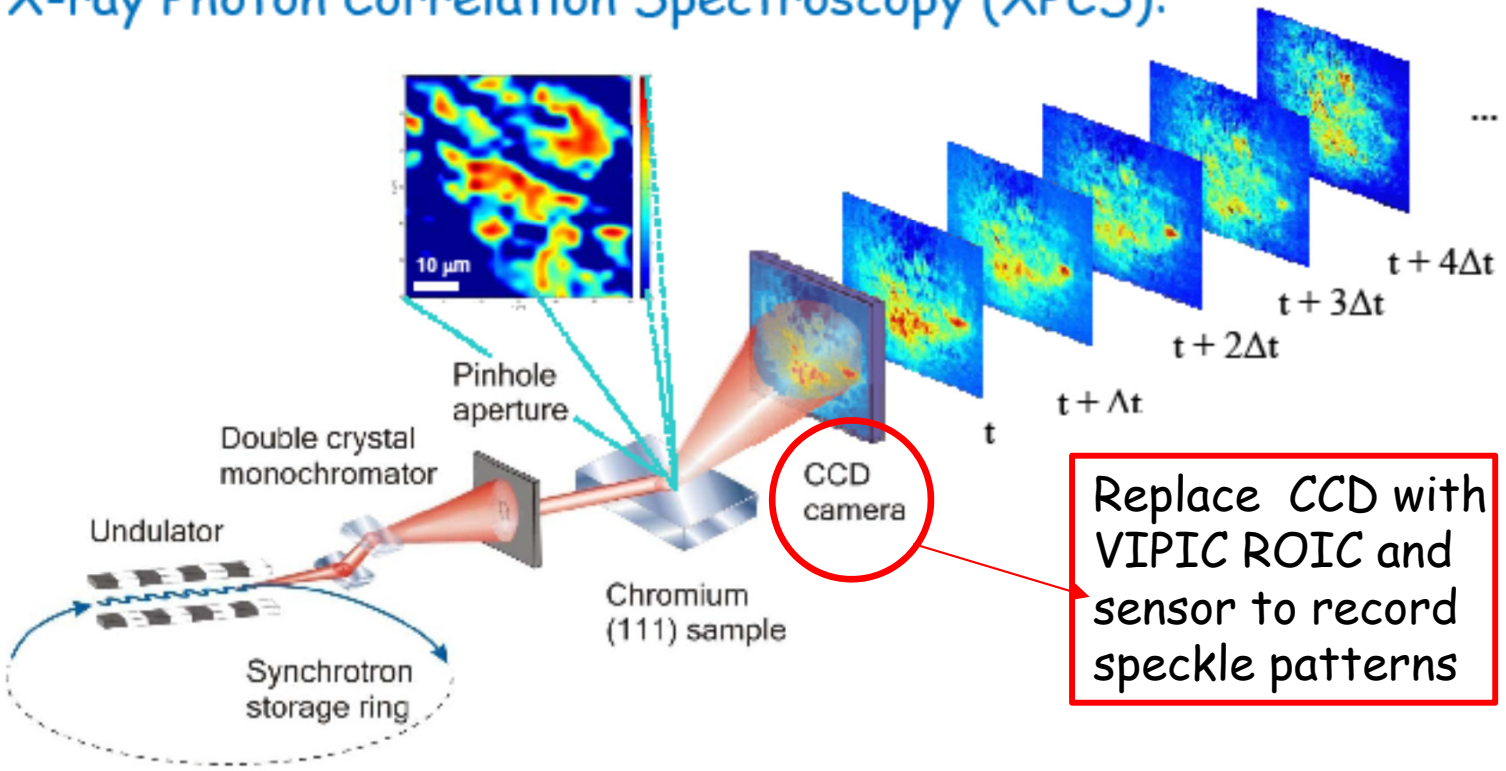
VIPIC for X-ray Photon Correlation Spectroscopy (XPCS)

- XPCS is a novel technique that studies the dynamics of various equilibrium and non-equilibrium processes occurring in condensed matter systems [6] (e.g. gels, colloids, liquid crystals, bio-materials, membranes, metals, oxides, magnets, etc.)
- XPCS is based on the generation of a speckle pattern by the scattering of coherent X-rays from a material where spatial inhomogeneities are present.
- If the state of disorder of the system changes with time, the speckle pattern will change. Thus by studying the time dependence of the scattered intensity, one can study the dynamics of the materials both in or out of thermodynamic equilibrium (e.g. diffusion constants, magnetic domain relaxation times, phase transformations)
- Advantages
  - Observe smaller features sizes
  - Can be used to observe charge, spin, chemical and atomic structure behavior.
  - Works with non-transparent materials

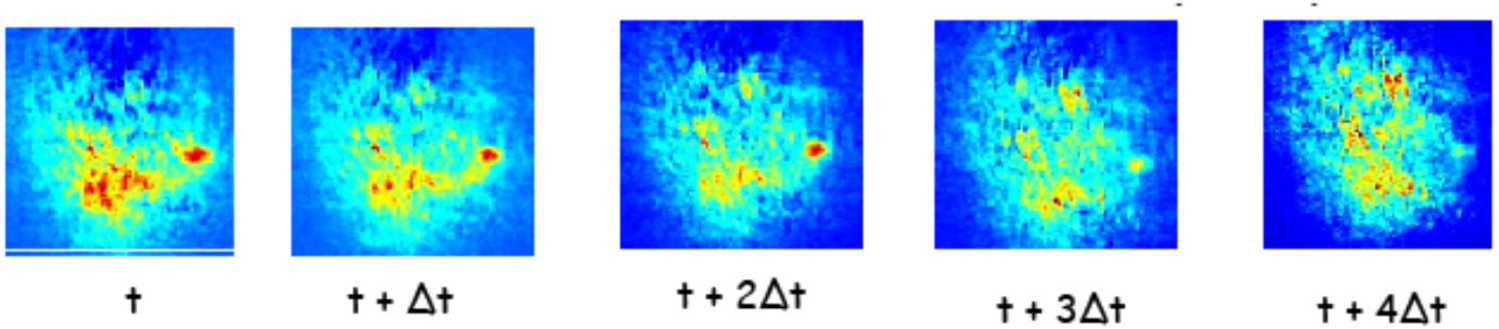


Speckle pattern

X-ray Photon Correlation Spectroscopy (XPCS):



Replace CCD with VIPIC ROIC and sensor to record speckle patterns



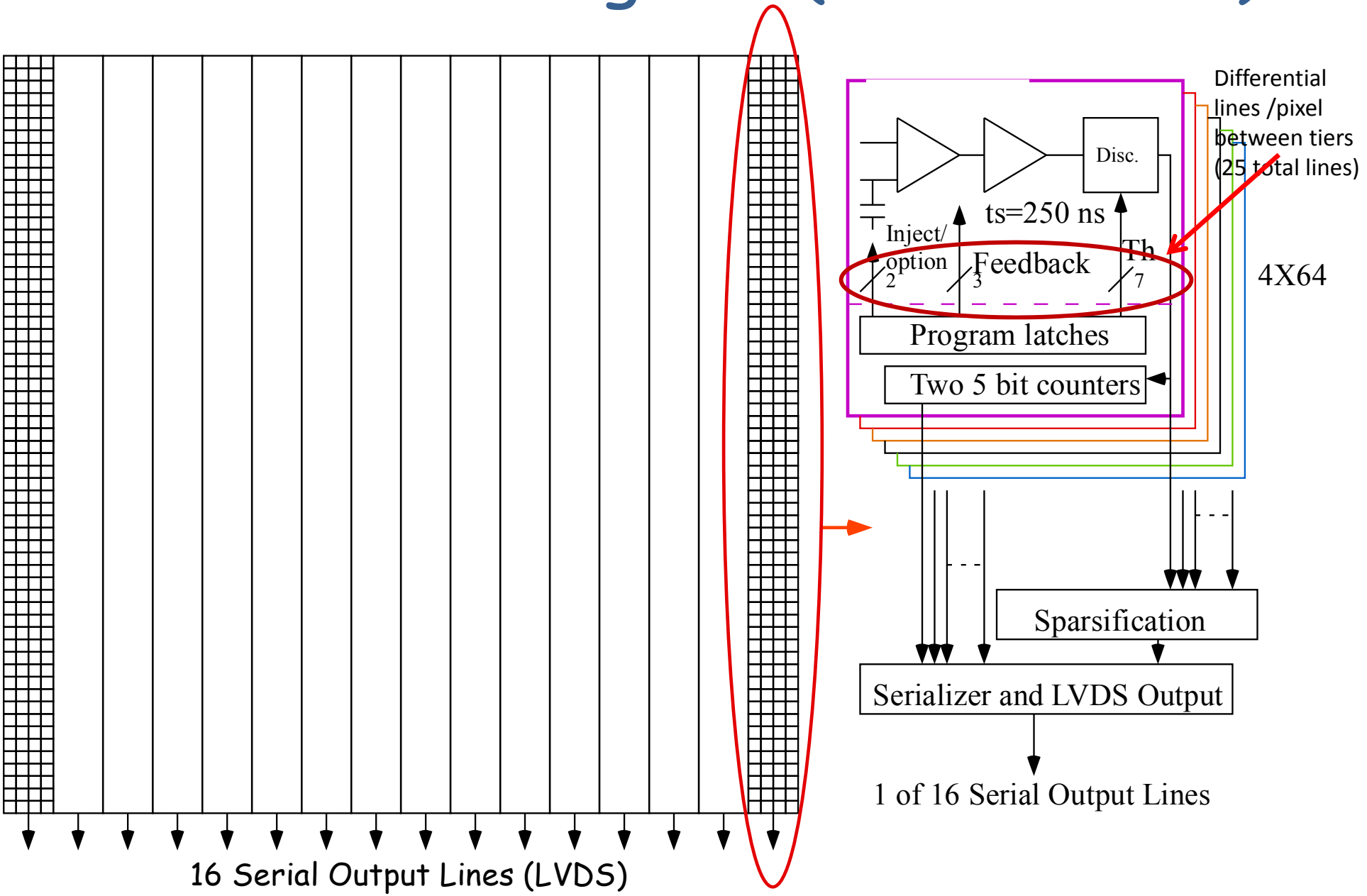
Speckle pattern changes with time

O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

VIPIC (Vertically Integrated Photon Imaging Chip)

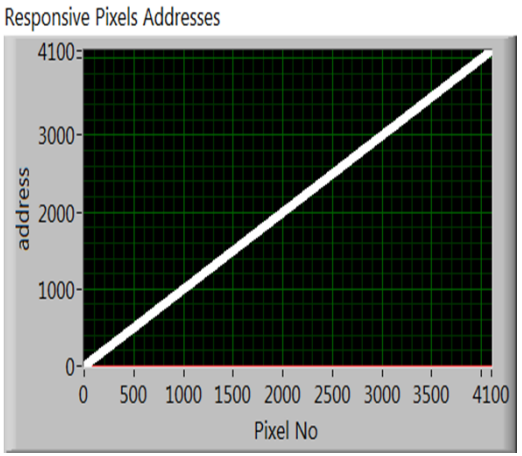
- The VIPIC is designed to quickly count hits in every pixel and read out quickly the hits in a sparsified and dead timeless manner.
- Specifications
  - 64 x 64 array of 80 micron pixels
  - Binary readout (no energy information)
  - Optimized for photon energy of 8KeV
  - Triggerless operation
  - 2 Modes
    - Timed Readout of hits and addresses at low occupancy (10 usec/frame for occupancy ~ 100 photons/cm^2/usec)
    - Imaging – alternating 5 bit counters read out hits in each time slot without addresses but using sparsification
- Relatively complicated communication protocol and a high number of signal lines (25) passed between tiers for every pixel.
- Features (5.5 x 6.3 mm die size)
  - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
  - Sparsified address generated by priority encoder [7]
  - Generates pixel address in 5 ns regardless of hit pixel location
  - Parallel serial output lines
    - 16 serial high speed LVDS output lines
    - Each serial line takes care of 256 pixels
  - 2 tier readout chip with separate analog and digital tiers
  - Adaptable to 4 side butt able X-ray detector arrays

VIPIC Block Diagram (4096 Pixels)

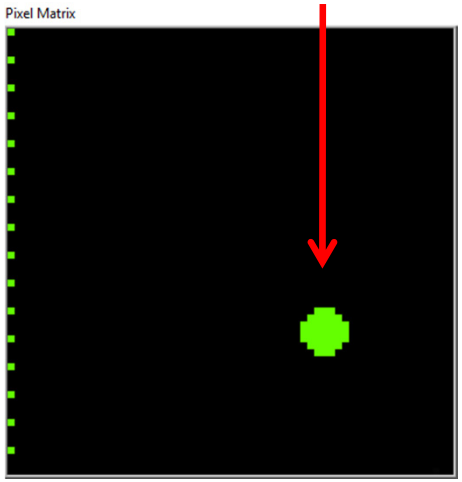


Test Results

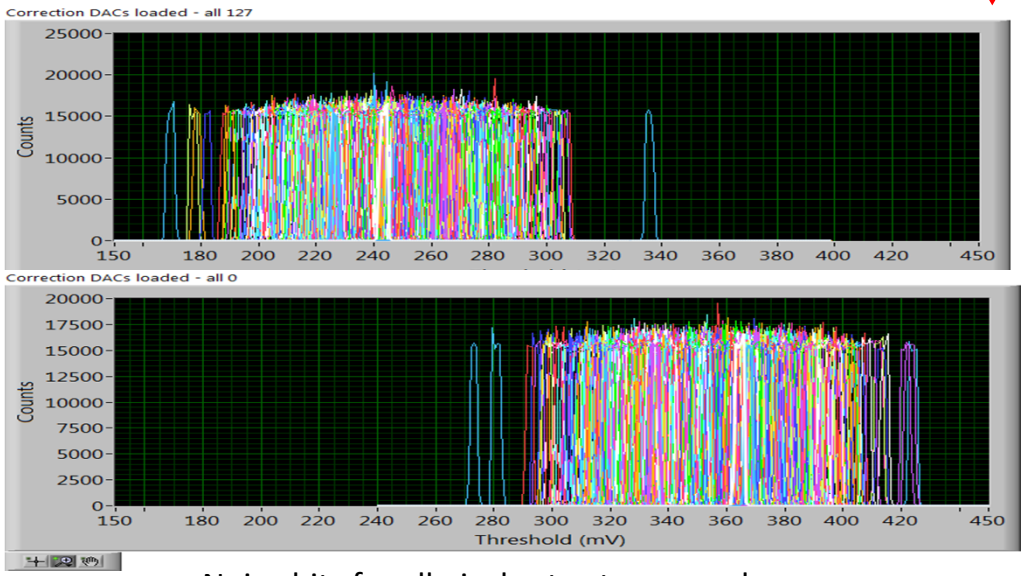
- Bonded 5 chips after visual inspection
  - 1 Tezzaron bonded chip is working
  - 2 Ziptronix bonded chips are working
- Testing confirms operation in both modes [8]
  - Configuration shift registers (up to 49152 bits long) are working.
  - Shifted in 1's to all cells with cal strobe and read out every address in normal readout mode in sequential order.
  - Found address encoder generating proper addresses
  - Thinned analog tier operation closely matches simulated performance. (Power and noise)
  - Reset (kill) all pixels and set pixels in region of interest, found appropriate sparsified addresses
  - Reduced threshold to get noise hits and found pixel counters reading out non-zero values. Chip fully working from input to output
  - Outputs fully functional
    - 16 serializers
    - 16level converters
    - 16 LVDS buffers
  - Changed 7 bit threshold DAC to 2 end values and found appropriate shift in threshold distributions (DAC range wide enough to correct for offsets)
- Future tests: 3 bits for preamp time constant, precise trimming of offsets
- Of the 25 connections/pixel between tiers, 19 appear to be working and 6 haven't been tested yet



Proper sequential address read out when 1's shifted into all cells (using normal read out mode)



Normal array read out with all pixels killed except small area in green (sparsification works)

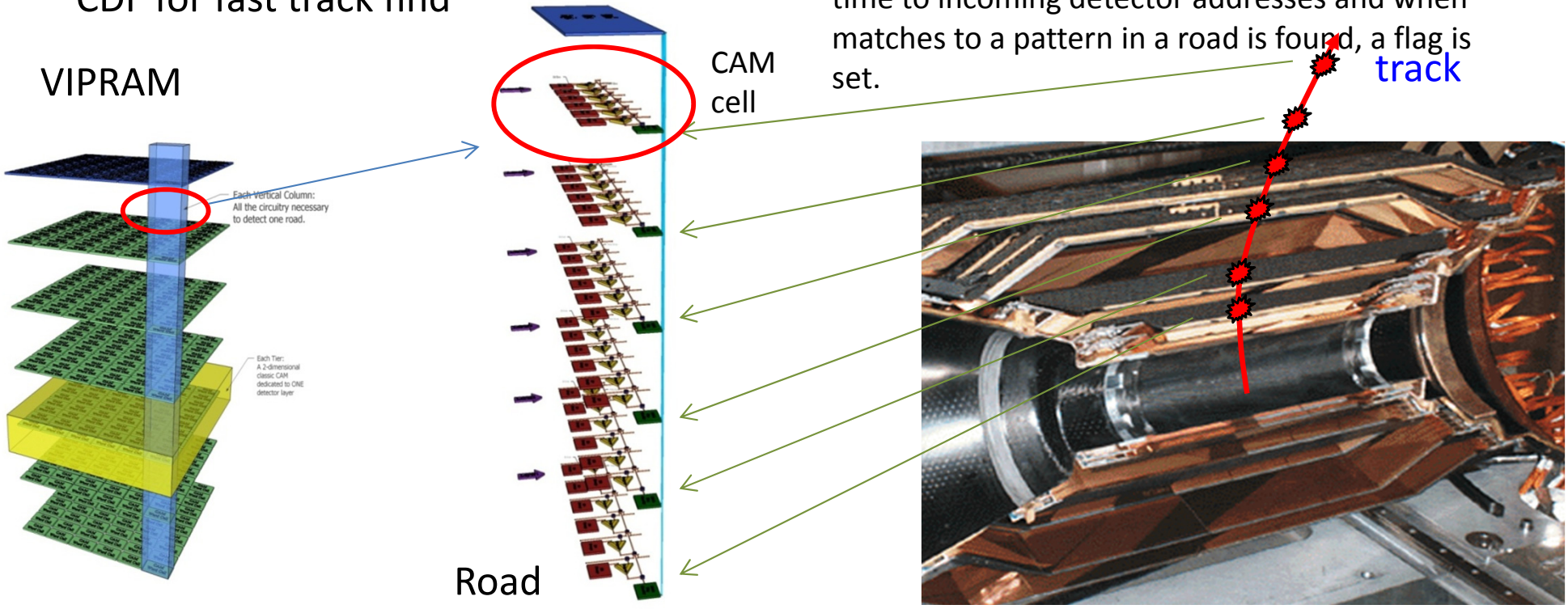


Noise hits for all pixels at extreme end of DAC settings

New 3D Effort: VIPRAM

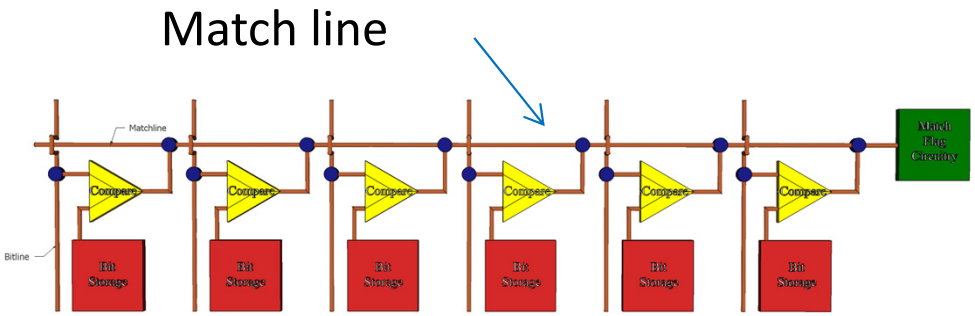
- Particle track reconstruction using fast pattern/track recognition is becoming increasingly more difficult as luminosities increase in HEP experiments
- The Pattern Recognition Associative Memory (PRAM) concept has been successfully used in the AMchip03 at CDF for fast track find

- VIPRAM adds the idea of Vertical Integration to increase pattern density and decrease power. [10]
- Monte Carlo simulations are used to create particle track address patterns in VIPRAM corresponding to possible hits in a number of detector layers.
- The stored patterns are then compared in real time to incoming detector addresses and when matches to a pattern in a road is found, a flag is set.

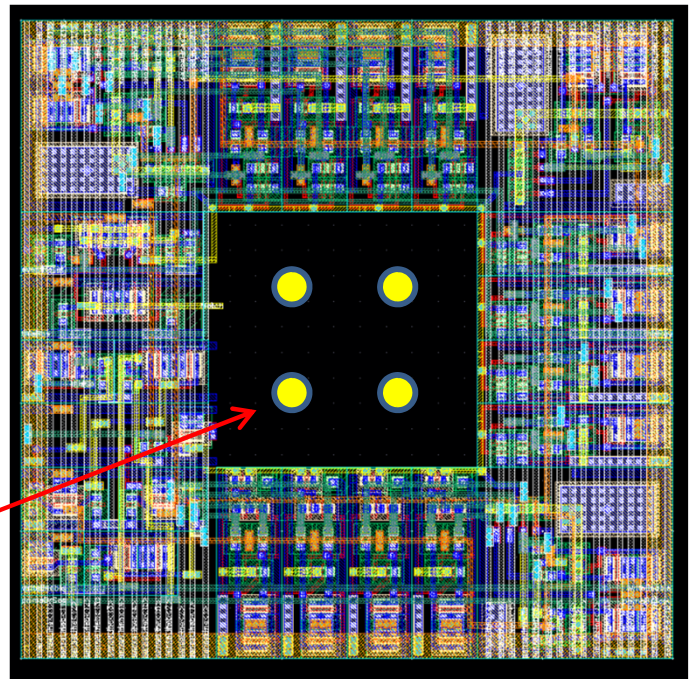


Benefits of 3D to the PRAM Concept

- Traditionally a CAM cell is a linear array of digital comparison and storage circuits with a relatively long match line.
- Several CAMs working together form a PRAM
- 3D allows for a new configuration for the match line and shorter communication to the glue logic which increases speed and lowers power.
- Currently designing a 2D PRAM chip with a 15 bit CAM cell layout in a 128 x 128 array which is easily converted to a 3D stacked assembly
- See poster by Jim Hoff at TWEPP 2012, "Vertically Integrated Pattern Recognition Associated Memory for Track Finding" for more details.



6 bit CAM cell



15 bit CAM cell layout for 2D and 3D