US Workshop on IC Design for High Energy Physics – HEPIC2013

Challenges for electronics for space

David Nelson
djn@slac.stanford.edu

U.S. DEPARTMENT OF ENERGY
Office of Science

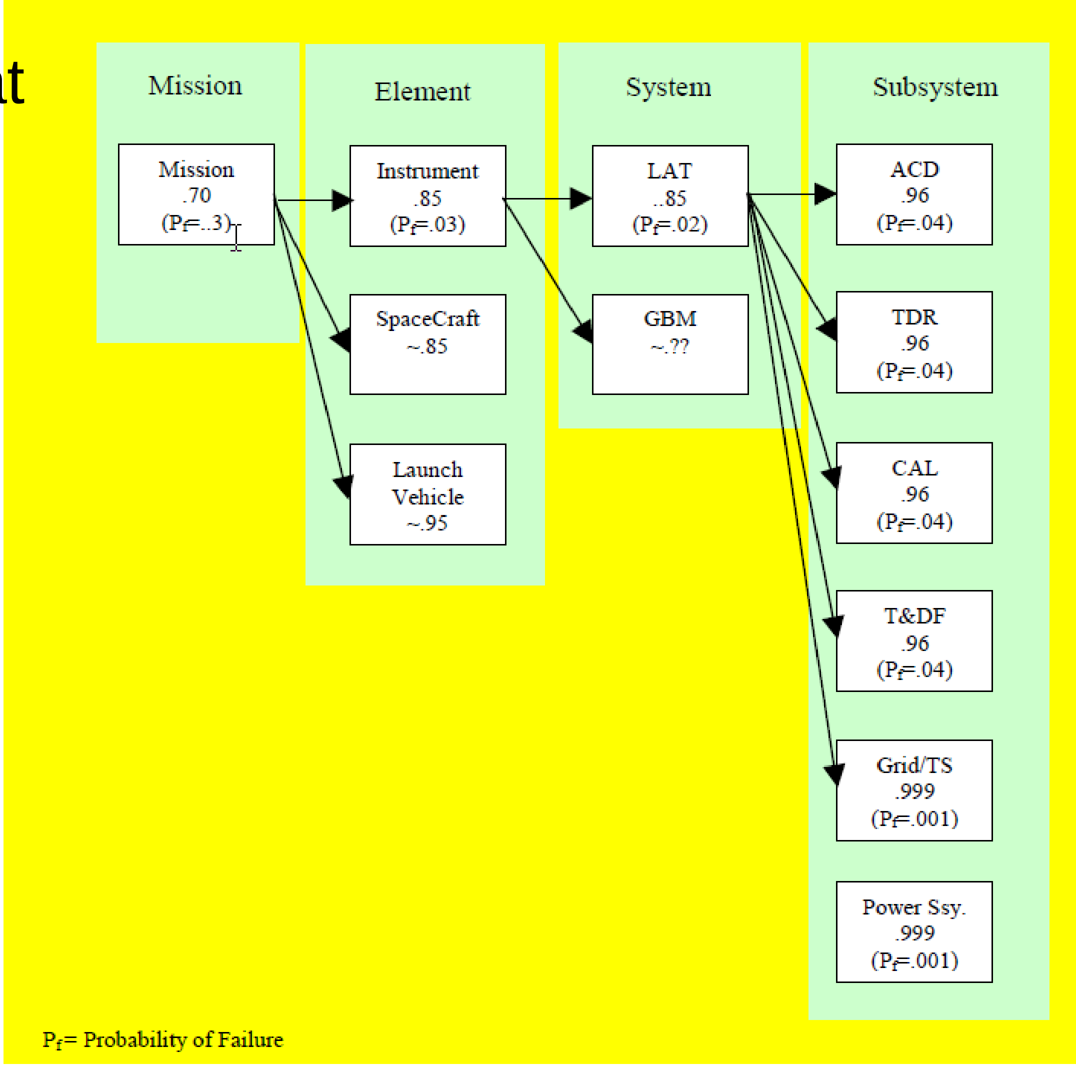
SLAC NATIONAL ACCELERATOR LABORATORY

Content

- General challenges (example: FERMI ASICs) and challenges for future missions

Mission Critical Reliability Flow-Down: Example GLAST/FERMI

- First need to calculate what are reliability requirements for an ASIC to be used
- Mission-> Element-> System-> Subsystem -> component
- Example tracker (TRK) ASICs for GLAST/FERMI



Allowable TKR Failure Rates with insignificant Loss of Mission Objectives, (Example)

Table 1 Allowable TKR Failure Rates with insignificant Loss of Mission Objectives

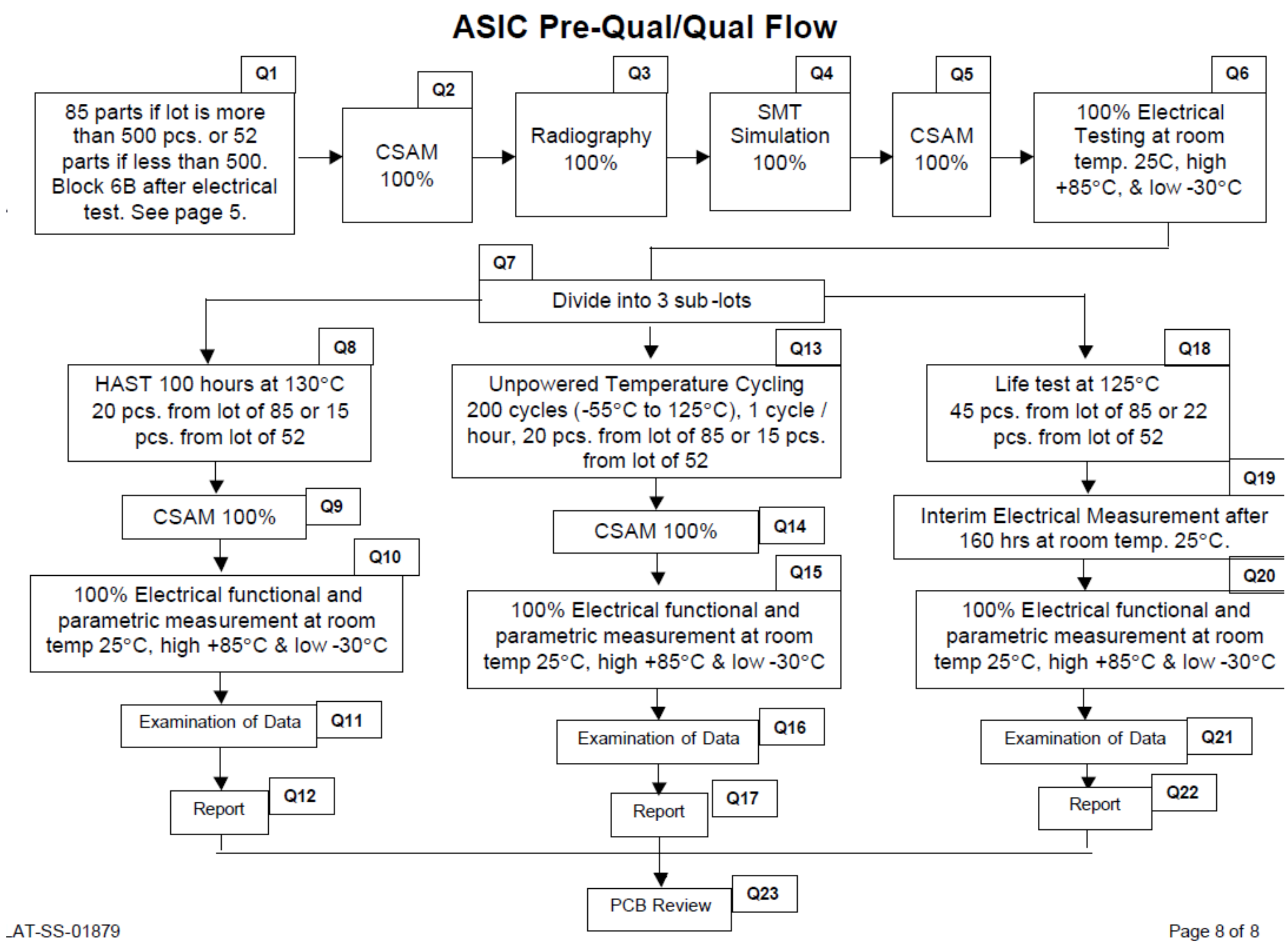
TKR Sub Assemblies	Number	Allowable Failure Rate with insignificant Loss of Mission Objectives (Category 4 or larger)	Observed Failures in BTEM	Remarks
Tower	16 / LAT	None	none	
Tower Cable	2 / side (8 / Tower)	1 / side (4 / Tower)	1 during assembly, none during testing	Redundant pair connects 8 TMCMs
Si Plane /TMCM	36 / Tower	1 / Tower	none	Assumes isolation between different TMCM's.due to Polyswiitches
GTRC ASIC	2 / TMCM (72 / Tower)	1 / TMCM	none	Redundant pair on each TMCM
Si Ladder	144 / Tower	2 / tower	1 during assembly, none during testing	Ladder Bias isolated by resistors
GTFE ASIC	864 per Tower	5 / Tower	none	Readout redundant
Coupling Cap	55926 / Tower	20 / Tower	none	Assumes affects ¼ GTFE
Single Channel	55926 / Tower	500 / Tower	27 mostly during assembly	

Design

- Reliability
  - Supposed not to use new cutting edge process, but process which has been around and also been fabricated at same fabrication plant for a while with track record
  - Make sure all design rules are checked <u>completely</u>
  - Need fabrication monitoring with process-flow paper work

- Radiation (depending on mission requirements)
  - TID, SEL: process (feature size, epi-layer) + design (substrate contacts)
  - SEU: design techniques for memory, FF; use of triple majority logic, etc

Challenge ASIC qualification (each lot)



Radiation Test Plan (each lot)

Table 2a: Screening parameters and acceptance values (after 10kRad TID)

ID	Name	Acceptance value
P	All power lines	< 20% increase in power
N	Error rate	100 % write and read back at 20 MHz, <0.1% error rate (TBD)
M	Timing Margin	100 % write and read back at 22 MHz
S	Data retention	100% data retention

Table 3: Screening parameters and acceptance values (SEE)

Error	Target	Cross section
SEL	All ASICs	$\sigma < 2*10^{-4}$ cm^2 per device
SEU	All ASICs	$\sigma < 1*10^{-4}$ cm^2 per bit

Table 4: Particle type and fluence required for the SEE test.
(For each particle, the fluence will be delivered in two equal steps)

Ion species	Energy [MeV]	LET [MeV·cm^2/mg]	Range [um]	Total fluence [ions/cm^2]	Dose [krad]		
					Total	after 1st half	after 2nd half
^{79}Br	246.84	38.8	31	4×10^6	2.5	1.25	2.5
^{107}Ag	271.88	54.7	28	3×10^6	2.5	3.75	5.0
^{58}Ni	236.13	28.4	34	5×10^6	2.5	6.25	7.5
^{28}Si	161.06	8.6	62	2×10^7	2.5	8.75	10.0

ASIC Screening, (1) (in this case example for packaged ASIC, some screening while assembled on board)

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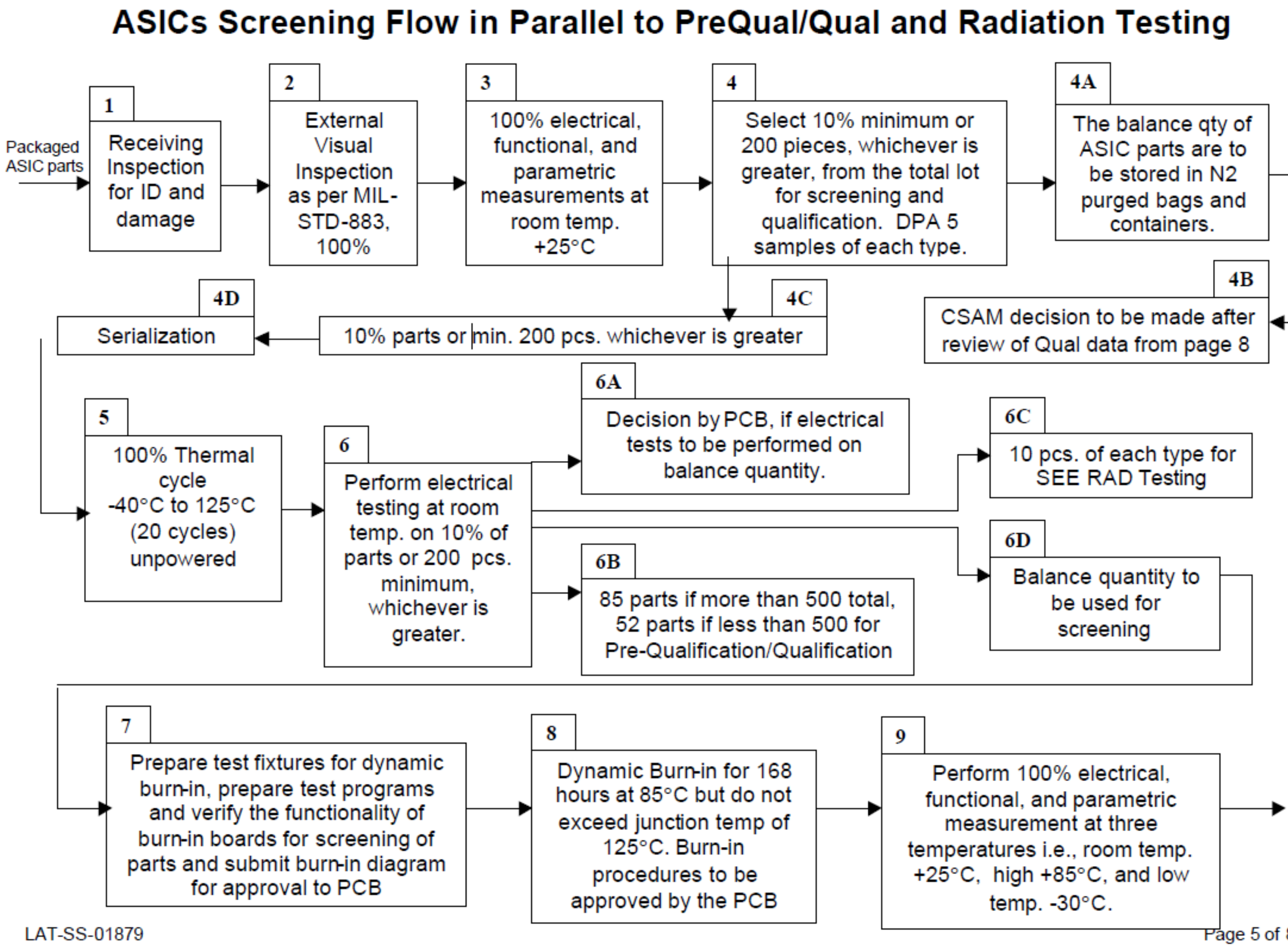

ASIC Screening, (2)

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10 — CSAM (optional) Decision will be made after review of Pre-Qual/Qual Data. See block 4A and 4C for quantity.

11 — Parts Control Board (PCB) to make decision to use the balance parts (block 4A & 4B) after reviewing test data.

11A — Select 10 samples of each type for total dose testing under bias.

12 — Review TID results and if parts are acceptable, bake parts from block 9 and ship the screened parts to ACD and DAQ and store balance quantity in nitrogen purge bags to be used for rework, see block 22.

13 — Verify integrity of bare PWB as per GSFC S-312-P-003, prepare reflow profile, run test boards after assembly as per NASA-STD-8739.2, prepare detailed procedures, certify selected vendor, verify functionality of sample assembled board, submit all procedures to PCB for approval, and conduct flight mount review. Software and procedure to be configuration controlled and all anomalies as recorded

14 — Bake parts from block 4A only if any of the bags have been opened

15 — Assemble flight boards using proven, approved, and configuration controlled documents as defined in block 13. Mandatory inspection points during assembly to be defined by PCB

16 — 100% Visual Inspection of assembled boards as per NASA-STD-8739.2 for surface mount assemblies

17 — 100% electrical verification of flight board at room temp. using configuration controlled and approved test program as per procedure approved by PCB

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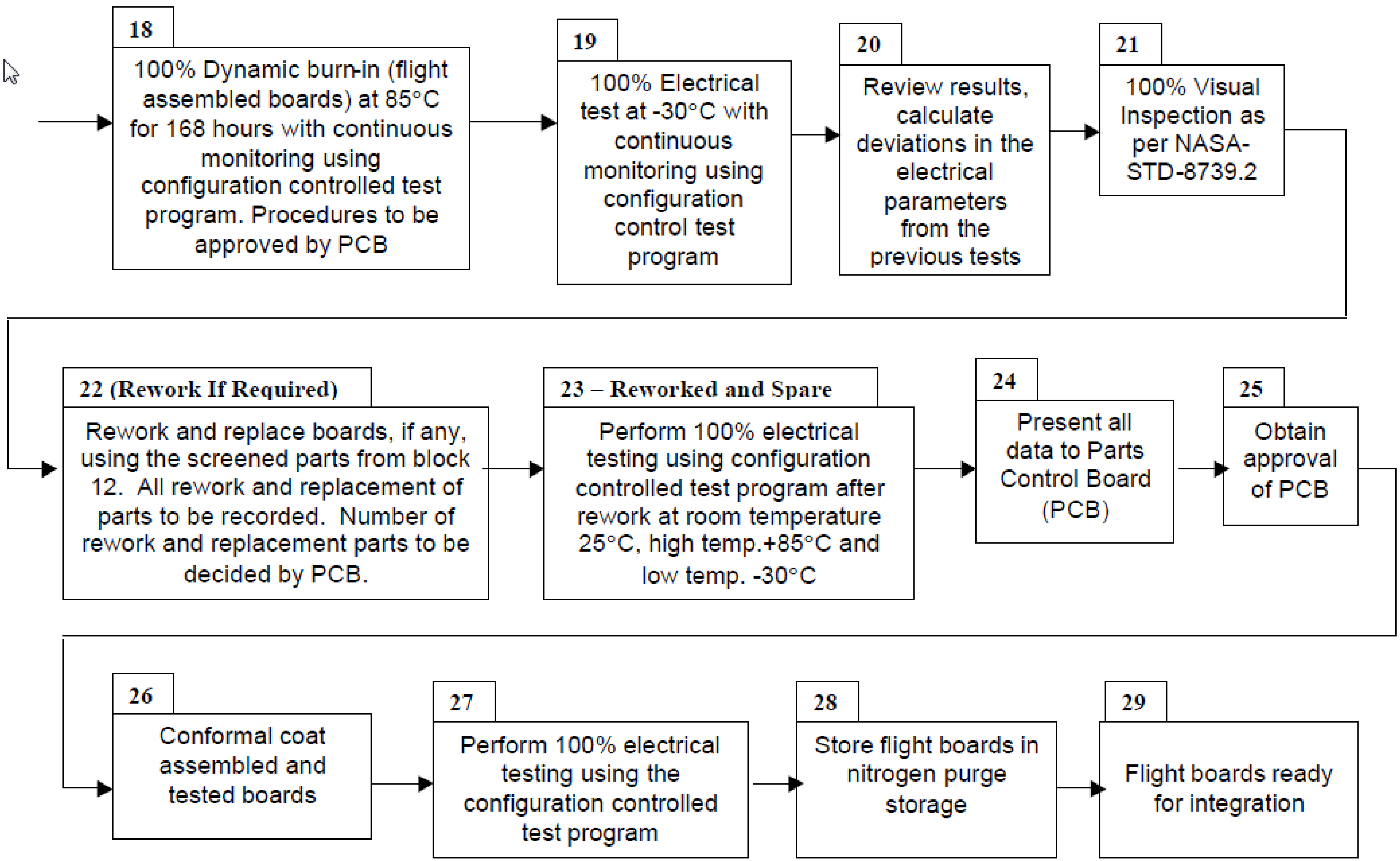
ASIC Screening, (3)



Example: GLAST/FERMI ASICs

Sub-system	Name	Main function	Design Institution	Number of ASICs (about)
TKR	GTFE	mixed (Si-strip readout)	UCSC, SLAC	14,000
TKR	GTRC	digital	SLAC	1152
CAL	GCFE	analog (CsI/diode readout)	SLAC	3,072
CAL	GCRC	digital	SLAC, NRL	256
ACD	GAFE	analog (PMT readout)	SLAC, GSFC	216
ACD	GARC	digital	SLAC, GSFC	12
DAQ	GLTC	mixed	SLAC	36
DAQ	GCCC	digital	SLAC	64
DAQ	GTCC	digital	SLAC	128

- The need for ASICs was required for functionality, physical space & power limitations
- Nine ASICs, all HP 0.5um CMOS (launched ~5 years ago, 10 year mission goal)

GLAST/FERMI Reliability

- ~20,000 ASIC's, 9 types
- No failures in orbit in four years
- No SEU, latch-ups
- One Tracker readout controller ASIC failure before launch
  - Recovered using redundant readout
- Total masked tracker hot strips is 524 out of ~800,000 channels
  - 0.05% dead channels.
- Rate of new hot strips is 10 to 20 per 4-6 months

Challenges for future space missions

- High reliability
  - typically no access for repair, use of redundant system design
- Radiation tolerance
  - depends on mission
- Qualification/screening
  - lot of work plus stacks of documents
- Low power
  - important, not just for supplying power (solar arrays) but also to get rid of heat (radiator size)
    - FERMI ~650W for ~1M channels including triggering/event-building/processing + power conversion/thermal control
- High on-board data reduction (link to ground only 1.5Mb/s)
  - Depends on mission (FERMI up to 4kHz level 1 trigger rate, < 400 Hz to ground)