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Radiation Hardness Challenges

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Introduction

Performance and functionality of integrated circuits continued to increase for the past few decades. Technology scaling (down) has fueled what is known as Moore's law (or is it vice versa?): the number of components per chip roughly doubles every 24 months.

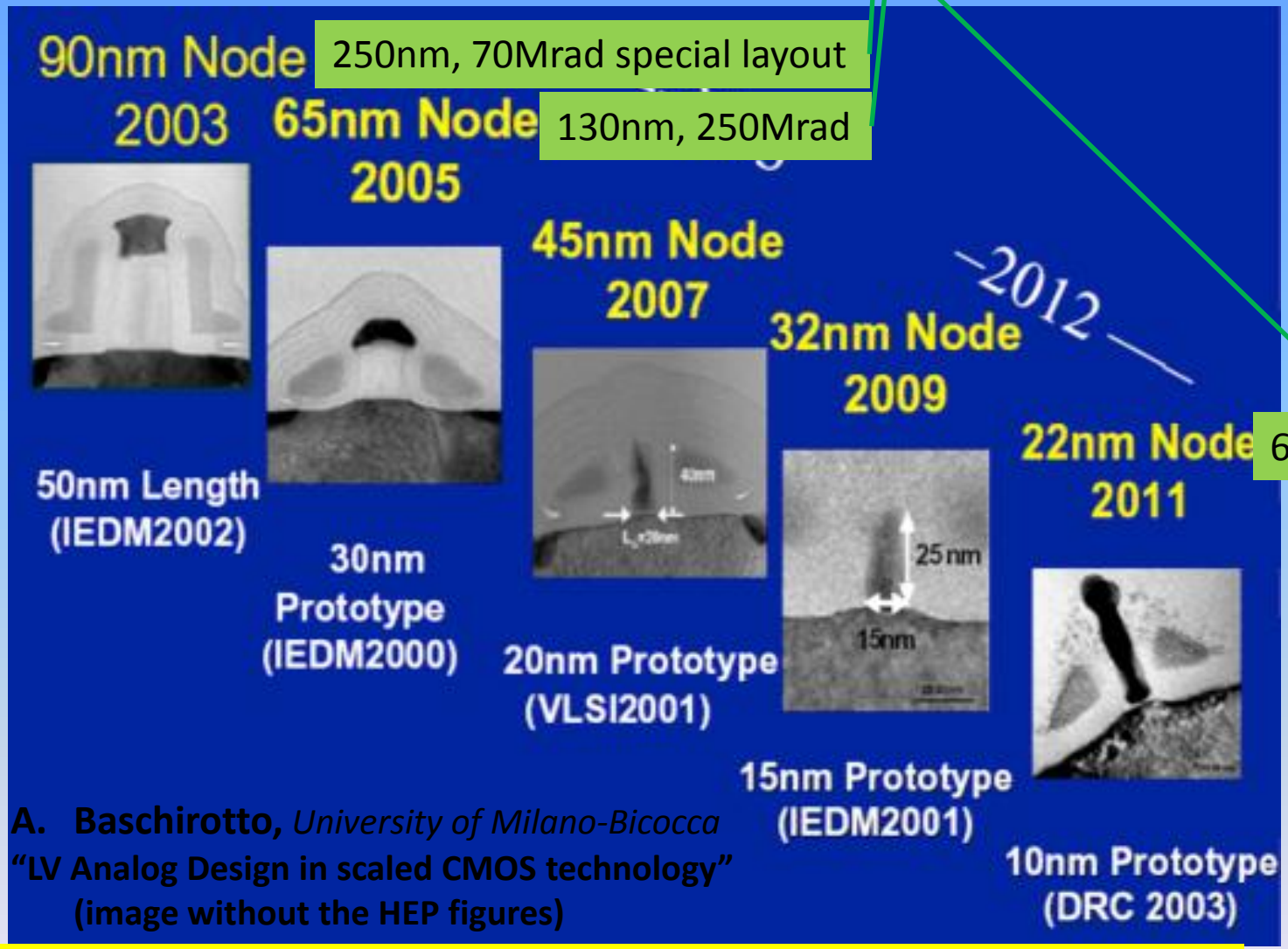
Transistor dimensions (width, length and gate thickness) are continuously decreased and so are the metal pitch while the number of metal levels has been increased. Process optimization for some niche market (like RF) has also led to multi-threshold and multi-supply transistors along with high quality passives.

Without the advances in IC technology, some important HEP projects (at some crucial time) would have been not feasible or would have required specialized low yield low performance high cost processes. The use of the, then, new (for HEP) processes (250 and 130nm nodes) helped address the high radiation tolerance issue with little or no added "cost"

The future will be no different. Complex and challenging instrumentation projects (Upgrades, HL-LHC, new Detector concepts) will require the adoption of the ever more empowering (and more complex) IC technologies.

Radiation hardness required for some of the future projects is unprecedented (>1Grad and >2e16 n/cm2). The question remains whether the commercial advanced technologies are tolerant enough to withstand exposure to high a level of radiation. Some issues related to the subject will be highlighted along with some recent experimental results.

Industry and HEP IC "nodes"



250nm, 70Mrad special layout

130nm, 250Mrad

65nm, >400Mrad

HEP projects, even though lagging mainstream technology, are benefitting from Technology scaling.

ITRS performance RF/Analog roadmap

Year of Production ➔	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*
Supply voltage (V)	1.1	1.05	1.05	1.05	1	0.95	0.95	0.95	0.85	0.85	0.85	0.85	0.75
Tox (nm)	1.2	1.2	1.2	1.2	1.10	1.10	1.10	1.10	1.10	1.00	1.00	0.90	0.90
Gate Length (nm)	38	38	32	29	27	22	18	17	15	14	13	12	11
gm/gds at 5·Lmin-digital	30	30	30	30	30	30	30	30	30	30	30	30	30
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	100	90	80	70	70	60	50	50	40	40	40	30	30
s Vth matching (mV·µm)	5	5	5	5	5	5	5	5	5	5	5	4	4
Ids (µA/µm)	9	9	8	7	7	6	5	4	4	3	3	3	2
Peak Ft (GHz)	240	240	280	310	340	400	480	520	570	630	680	750	820
Peak Fmax (GHz)	290	290	340	380	420	510	610	670	740	820	900	990	1090
NFmin (dB)	0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2

Notice difference between Performance versus precision (next slide)

ITRS key: Yellow=solution known but not optimized. Red= solution not known.

http://www.itrs.net/

ITRS Precision Analog/RF roadmap

Year of Production ➔	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*
Supply voltage (V)	**2.5**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.8**	**1.5**	**1.5**	**1.5**
Tox (nm)	**5**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2.6**	**2.6**	**2.6**
Gate Length (nm)	**250**	**180**	**180**	**180**	**180**	**180**	**180**	**180**	**180**	**180**	**130**	**130**	**130**
gm/gds at 10·Lmin-digital	**220**	**160**	**160**	**160**	**160**	**160**	**160**	**160**	**160**	**160**	**110**	**110**	**110**
1/f Noise (μV²·μm²/Hz)	**1000**	**360**	**360**	**360**	**360**	**360**	**360**	**360**	**360**	**360**	**270**	**270**	**270**
s Vth matching (mV·μm)	**9**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**5**	**5**	**5**
Peak Ft (GHz)	**40**	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**50**	**70**	**70**	**70**
Peak Fmax (GHz)	**70**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**90**	**120**	**120**	**120**

- *Tox decreasing: better TID resistance. Gate rupture? Other problems?*
- *Gm/gds decreasing: Lower gain*
- *1/f noise decreasing.*
- *Matching improving (barely and only for analog devices)*
- *Speed increasing*
- *Supply voltage decreasing: reduced Dynamic range.*
- *Other: gate leakage, off current, variability of non analog transistors …*

ITRS bipolar Roadmap (2 years ago)

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*
1/f-noise (μV²·μm²/Hz)	2	1.5	1.5	1.5	1	1	1	1	1	1	1	1	1
s current matching (%·μm)	2	2	2	2	2	2	2	2	2	2	2	2	2
High Speed NPN (HS NPN) - Common to mmWave Table													
Emitter width (nm)	130	120	110	105	95	90	85	80	75	70	65	65	60
Peak fT (GHz)	265	285	305	325	345	365	385	405	425	445	465	485	505
Peak fMAX (GHz)	310	350	390	430	470	510	550	590	630	670	710	750	790
Maximum Available Gain (dB) @ 60 GHz	12.0	12.9	13.6	14.3	15.0	15.6	16.1	16.6	17.1	17.5	18.0	18.4	18.7
Maximum Available Gain (dB) @ 94 GHz	8.0	8.9	9.6	10.3	11.0	11.6	12.1	12.6	13.1	13.5	14.0	14.4	14.7
NFMIN (dB) @ 60 GHz	2.5	2.0	1.6	1.3	1.1	0.9	0.8	0.7	0.6	0.5	0.5	0.4	0.4
BVCEO (V)	1.7	1.7	1.6	1.6	1.5	1.5	1.4	1.4	1.4	1.3	1.3	1.3	1.2
JC at Peak fT (mA/μm2)	14	15	16	18	19	20	22	23	24	26	27	28	30
High Speed PNP (HS PNP)													
Emitter width (nm)	500	500	300	300	200	200	200	200	200	150	150	150	150
Peak fT (GHz)	25	40	60	80	85	95	105	115	125	135	145	155	165
Peak fMAX (GHz)	40	50	80	90	95	105	115	130	140	150	160	170	180
BVCEO (V)	5.5	4.0	3.0	2.5	2.2	2.0	1.9	1.8	1.7	1.6	1.5	1.4	1.4

For specialized projects. May be the better choice for niche HEP projects/layers.
Breakdown voltage getting lower. Will be worse with irradiation.
Careful radiation (TID and neutron) characterization challenging and costly.

Advanced IC processes are available thru brokers

32 nm	0.9 /1.5	7th generation IBM SOI technology improves energy savings for high-performance servers, printers, storage devices; networking, mobile, consumer, and game applications. Trusted foundry access only.[1]
45 nm	1.0 /0.9	This energy-saving SOI process is suitable for a broader range of consumer electronics, including digital TVs and high-end mobile applications. Trusted foundry access only.[1]
65 nm	1.0 /1.8, 2.5	Excellent for consumer electronics, wireless communications, and other applications requiring high performance or system-on-a-chip. Trusted foundry access only.[1]
	1.2 /2.5	Tailored for power-sensitive applications in wireless communications and consumer electronics. Trusted foundry access only.[1]
90 nm	1.0 /2.5	Ideal for leading-edge microprocessors, communications, and computer data processing applications. Trusted foundry access only.[1]
	1.2 /2.5	Use for low-cost, high performance wireless applications, as cellular handsets, mobile TV, WiMax, UWB and GPS. Trusted
130 nm	1.2 /2.5	Use for low-cost, high performance wireless applications as cellular handsets and GPS.
	1.2 /2.5	Similar to 8RF-DM, but uses LM top metal.

IBM CMOS (mosis)

VDD

40 nm	Low-power logic
65 nm	Standard logic, RPO
	Mixed-mode/RF, RPO, MiM
90 nm	Standard logic, RPO
	Mixed-mode/RF, RPO, MiM
0.13 µm	Standard logic, RPO
	Mixed-mode, RPO, MiM
	Low-power logic, RPO
	Low-voltage logic, RPO

TSMC CMOS (mosis)

Advanced IC processes available thru brokers

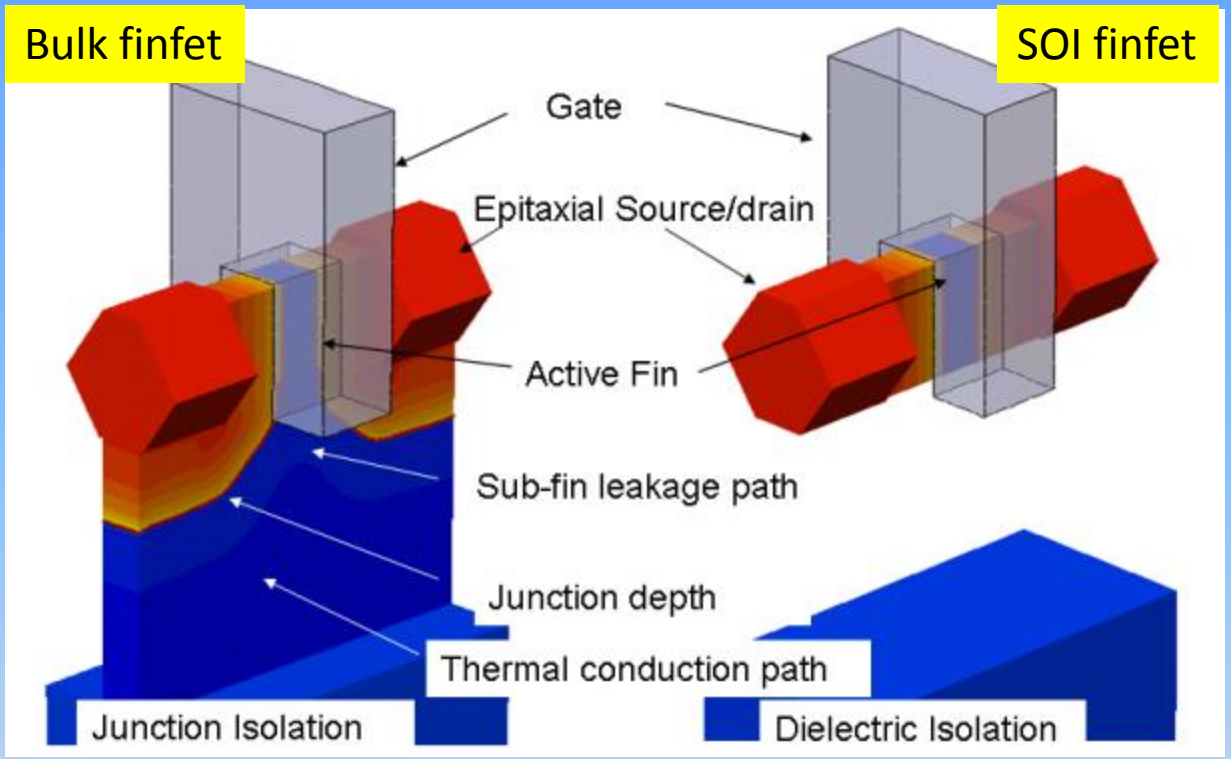
Feature Size	CMOS Vdd [V]	SiGe Ft [GHz] | BVceo(1) [V] HP Ft/BVceo	SiGe Ft [GHz] | BVceo(1) [V] HB Ft/BVceo	Description
				IBM BiCMOS SiGe (mosis)
0.13 µm	1.2, 2.5, 3.3	200 | 1.77	57 | 3.55	5th generation SiGe technology for advanced RADAR and mmWave applications.
	1.2, 2.5, 3.3	103 | 2.4	54 | 4.7	Reduced performance, cost effective technology for wireless applications.
0.18 µm	1.8, 2.5, 3.3	120 | 2.0	20 | 4.75	4th generation SiGe technology best suited for wireless and high-speed switches.
	1.8, 2.5, 3.3	60 | 3.3	29 | 6.0	Reduced performance, yet most cost effective SiGe technology offered.
0.25 µm	2.5, 3.3	47 | 3.3	27 | 5.7	3rd generation SiGe technology.
	2.5, 3.3	60 | 3.2	29 | 6.0	A descendant of 7WL, it integrates 0.25 µm CMOS with the 7WL SiGe NPN.

28 nm CMOS28LP	CMOS 7LM
40 nm CMOS040	CMOS 7LM
65 nm CMOS065	CMOS 7LM
65 nm CMOS065-SOI	SOI 6LM

St Micro CMOS (cmp)

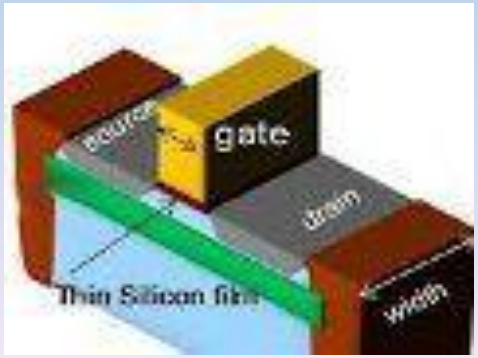
Other less advanced and specialized processes are available thru mosis, cmp, europractice
And others!
http://www.mosis.com
http://cmp.imag.fr/
http://www.europractice-ic.com/

Challenges: keeping up. We necessarily have to follow (by some lag) the market. Is more advanced better?



- ✓Bulk CMOS is becoming very Complex at very advanced nodes
- ✓SOI is being advertized as the natural Moor's law extender (low leakage, better SEU tolerance, higher speed, ….)
- ✓SOI is becoming the technology of the future again (May be for real this time)

http://www.advancedsubstratenews.com



Companies expected to tilt at FDSOI windmill

ST announced last week that it has secured design wins for 28nm FDSOI, which adds to mounting evidence for the emergence of an FDSOI ecosystem. The momentum is slowly but surely building on a global scale, extending from (EE times)

Challenges: keeping up. We necessarily have to follow (by some lag) the market. Is more advanced better?

- *Besides feature size, new "devices", structures, materials, process details at all levels are continuously being introduced to deliver on the promise of "more than Moore".*
- *It is not clear how these will fare as far as very high radiation tolerance is concerned.*
- *Can this community explore these processes with a reasonable lag. Very challenging! Is it even desirable?*
- *Do we know the ultimate limits (with and without design mitigation) of "our" mature technologies (130nm)? Are they really obsolete? Certainly not for every future project.*
- *The consensus is that at this stage 65nm CMOS looks like the most promising (Reachable) process for ATLAS/CMS pixel layers and that systematic collective effort should go into characterizing and qualifying this "node" (more precisely a specific flavor of a specific process from a specific manufacturer @ this node)*
- *Some selected results will be shown for the 65nm CMOS*

Design challenges in advanced CMOS

Gate leakage	Big problem biasing/controlling large number of transistors in parallel (pixels). Current is proportional to gate area: can be problematic for low noise large cap FENDs (wide input transistor)	Be Aware the problem. Can be serious. Realistic simulations is a must. Design Bias DACs to handle the excess current. Use higher voltage devices, if possible. **Radiation effects not known**
Off leakage current	Problem for low current circuits. May lead to higher power (increase operating currents to dwarf leakage)	Use low leakage transistor variants (order of magnitude lower). **Radiation affect this through VTH changes**
Parasitic transistor leakage	Aggravates the sub-threshold leakage problem.	**This is a radiation specific problem. Layout and transistor size dependent. Credible technology characterization is needed**
Low Supply voltage	Reduced Dynamic range. May lead to higher analog power. Problem for high precision/accuracy systems	**Mitigating large VTH shits becomes more difficult. Noise immunity decrease.**
Highly layout dependent device parameters	Makes design more complex. Requires a high quality design kit.	**Radiation Effects can be layout dependent in newer process. Very strict rules (no ELT in 65nm for example)**

Design challenges in advanced CMOS

junction leakage	Problem high for impedance nodes/paths and very low current paths. Junction can be parasitic or functional.	**Need to pay attention (usually we don't). 2e16 n/cm2 could be quite damaging. ESD devices? Temp sensors, Bandgap circuits and other junction based design**
"Parasitic" bipolar transistor issues	Beta degradation (it is very low to start with) and other effects.	**If used need to be characterized. Usually it is not. Bandgap circuits.**
Special devices effects		**Example: special ESD (other than diodes) devices. Rarely characterized.**
Multi Threshold variants	What to use when?	**Nominal, HVT, LVT, MVT transistors, Do they degrade in a similar manner. May be?**
IO transistors	Use them for analog?	**Thicker devices (back to square 1?).**

Insufficient or unreliable radiation effects data
Lack of radiation effects modeling
To reduce risk and cost: inclusion of radiation effects in circuit simulations is needed.

Radiation characterization: Can we do it right?

- *Irradiating at too a high rate: can we validate the results for our operating conditions through rigorous standard procedures? 1Grad in 10 days is ~4000 the real rate. Are these procedures applicable?*
- *Temperature effects (irradiation, testing and operating temps)? Do they affect the conclusions. Do irradiated chips work at operating temperatures?*
- *Irradiation particles and energies(displacement and ionizing damage)*
- *Variability! Are the results consistent run to run, lot to lot ….. Radiation hardness has been always very process specific. When at the limit of tolerable dose, small details matter.*
- *Device hardness does not mean circuit/system hardness. A given complex circuit (front-end chain) can fail earlier or later than predicted by device results.*
- *Can we characterize all the devices (multi-VT MOS, Core and I/O, PN, BIP, ESD, … devices)?*
- *Do we need guard rings (device-device leakage)?*
- *SEU characterization? SEU dependence on TID.*
- *…..*
- *Do we have, collectively, the right expertise? We cannot do everything 100% right but being aware of most issues is very important.*

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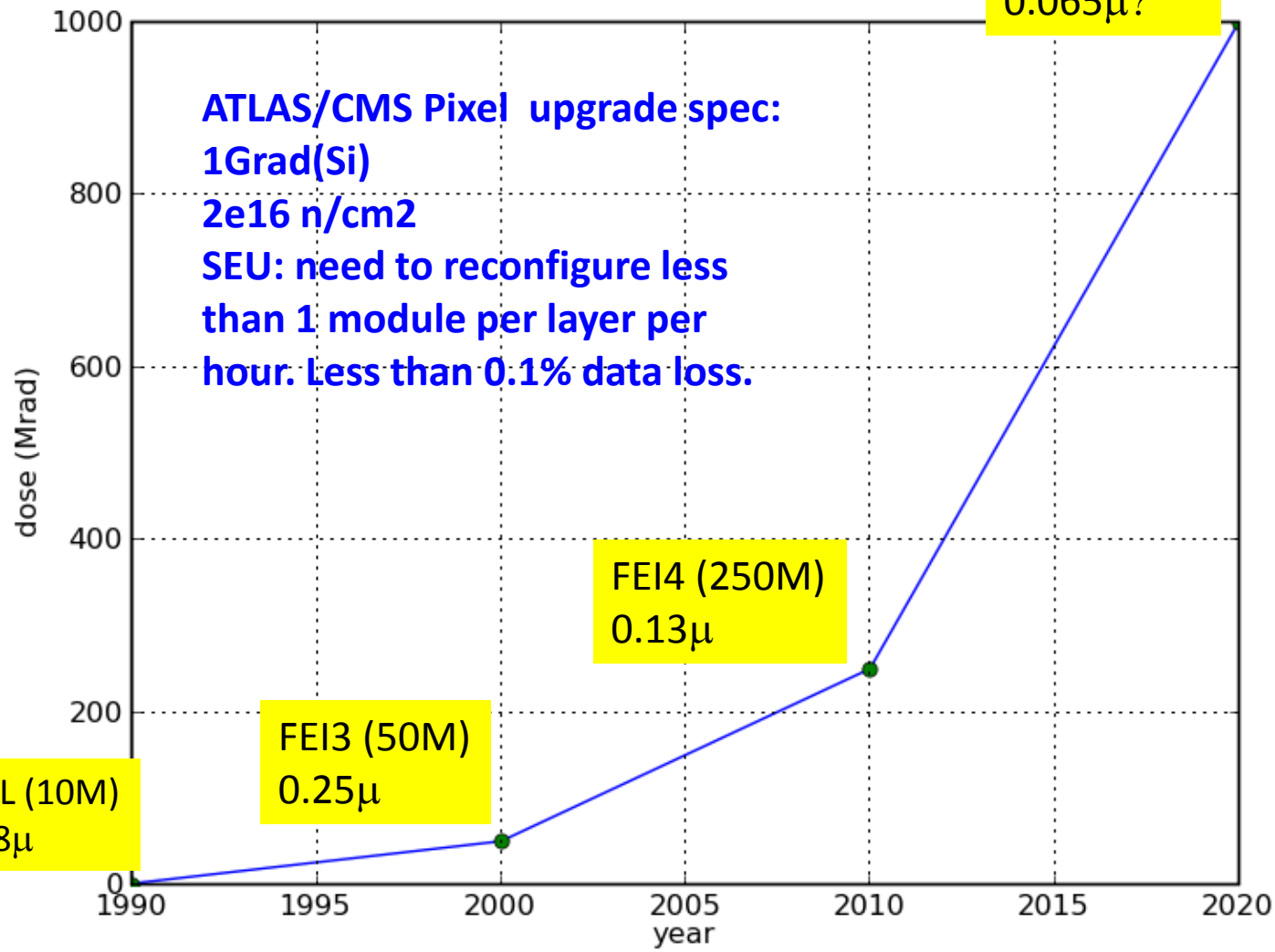
Designing for radiation hardness: Can we do it right?

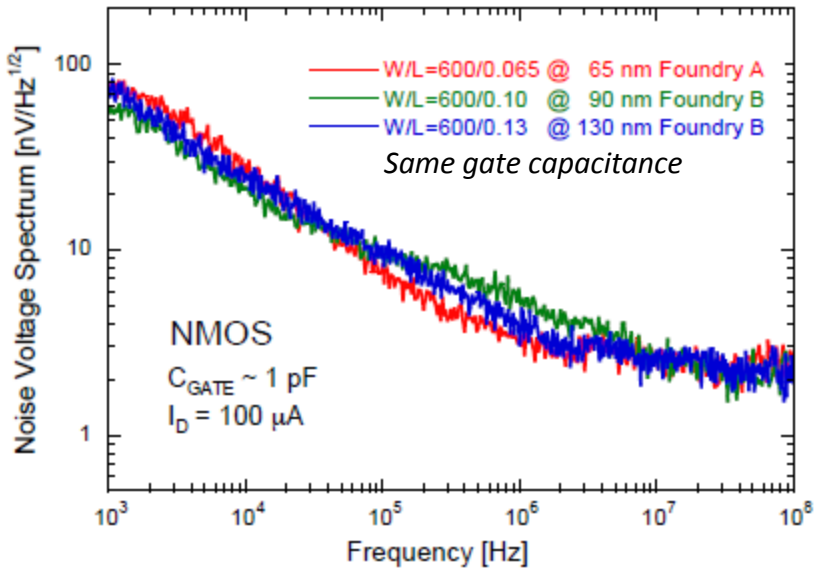
- *Is there any simulations tools available?? Can we feedback irradiation data into our design tools.*
- *Technologies are very expensive designing for hardness is the same as design for process variation. Instead of PVT think PVTR (Process Voltage Temperature Radiation)*
- *Are we simplifying our designs to limit the number of weak links.*
- *Using digital to correct analog is good. But too much configuration bits can turn a blessing into a curse.*
- *Are we building enough redundancy and error correction schemes?*
- *Any layout aware tools to optimize cell placement for optimum SEU tolerance in n-redundant memory cells (latches)*

HEP Radiation levels



Graph data approximate!

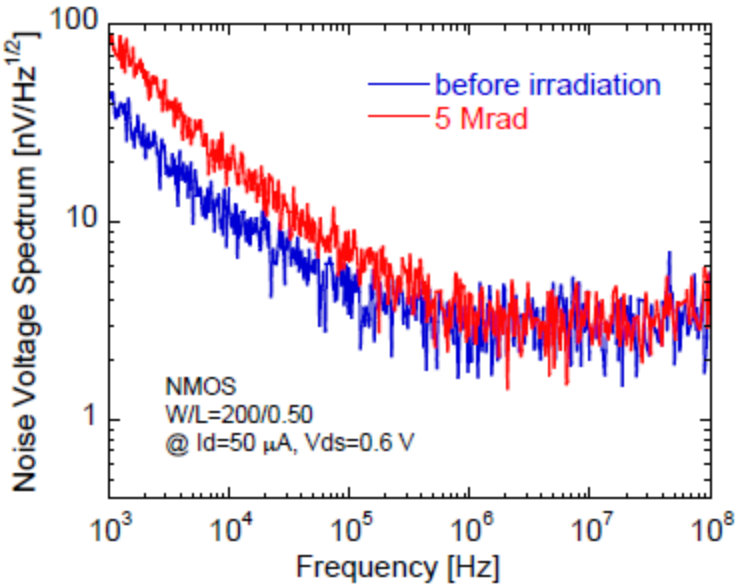
65nm: Some transistor test result (Noise out the way)

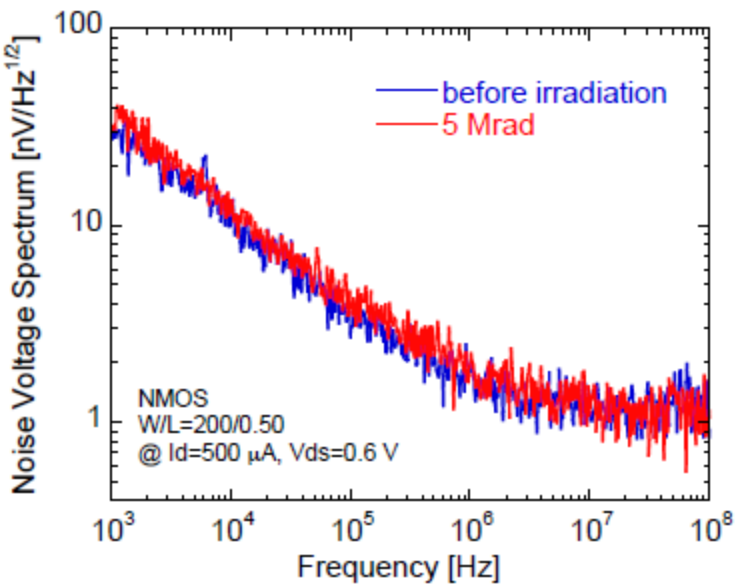


- No noise degradation at lower nodes
- No thermal noise increase with radiation
- No or little 1/f noise increase with radiation

- Very high frequency noise ???
- Increased RTS noise for small structures ???

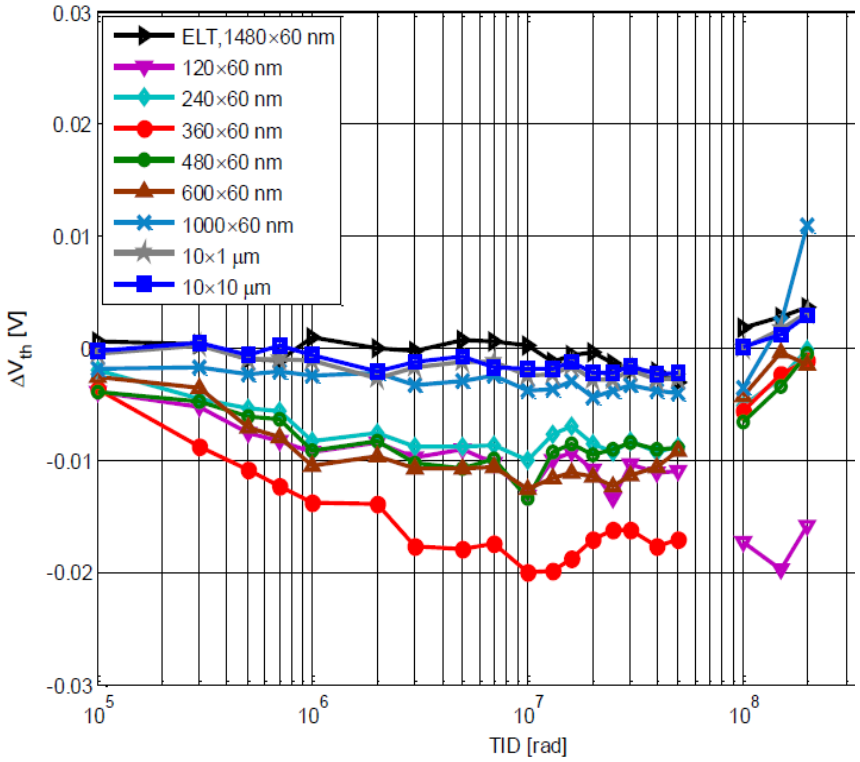
M. Manghisoni et al. TWEPP 2011



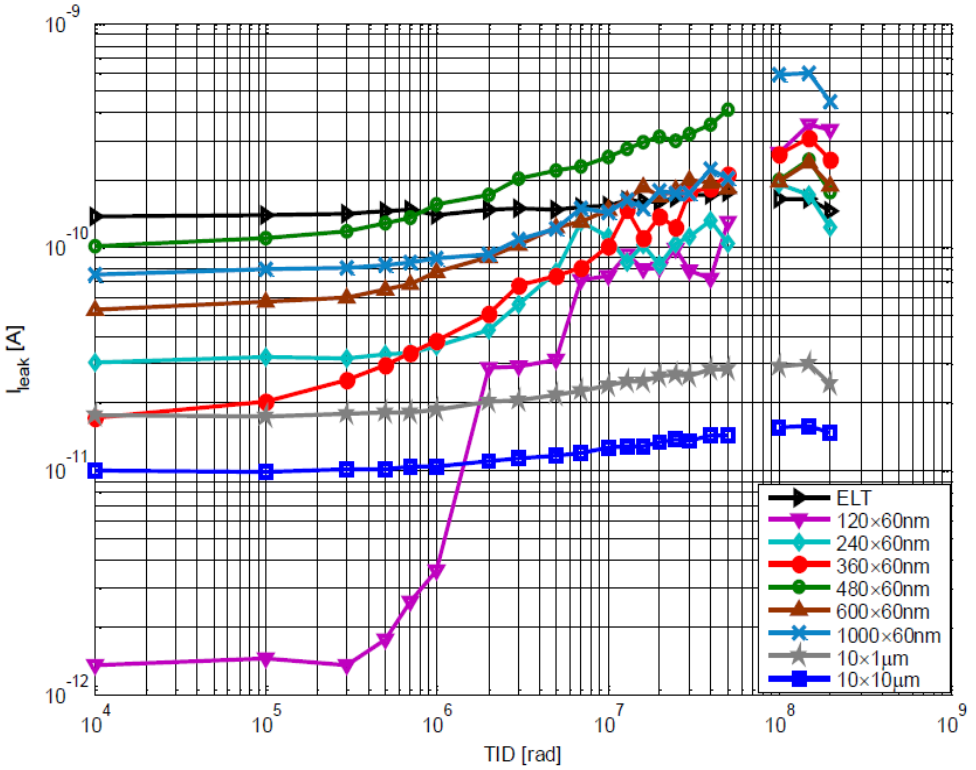


65nm: Some radiation tolerance results

Threshold voltage



Leakage current

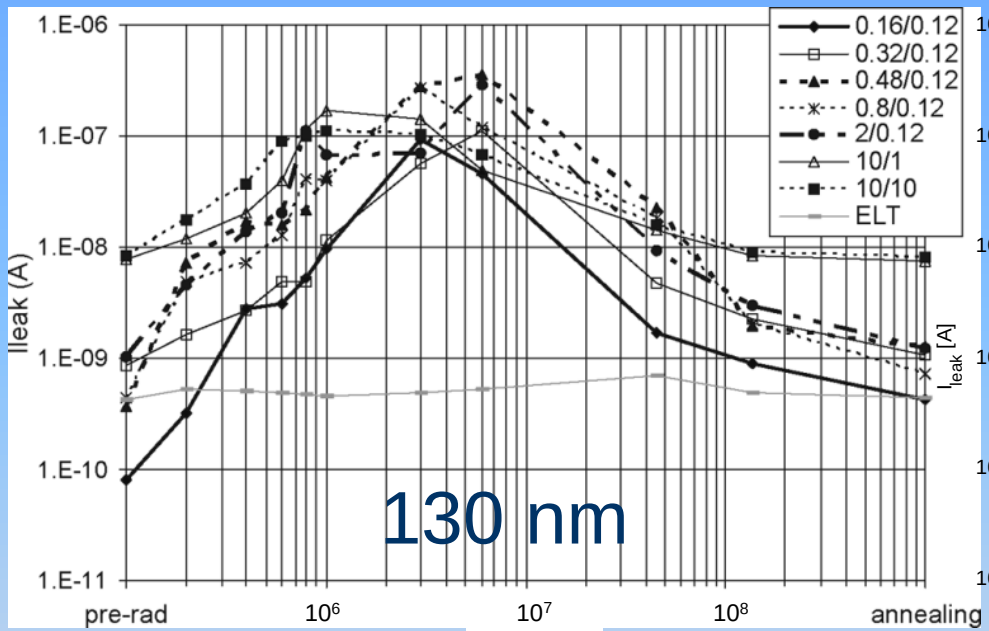


S. Bonacini et al. TWEPP 2011

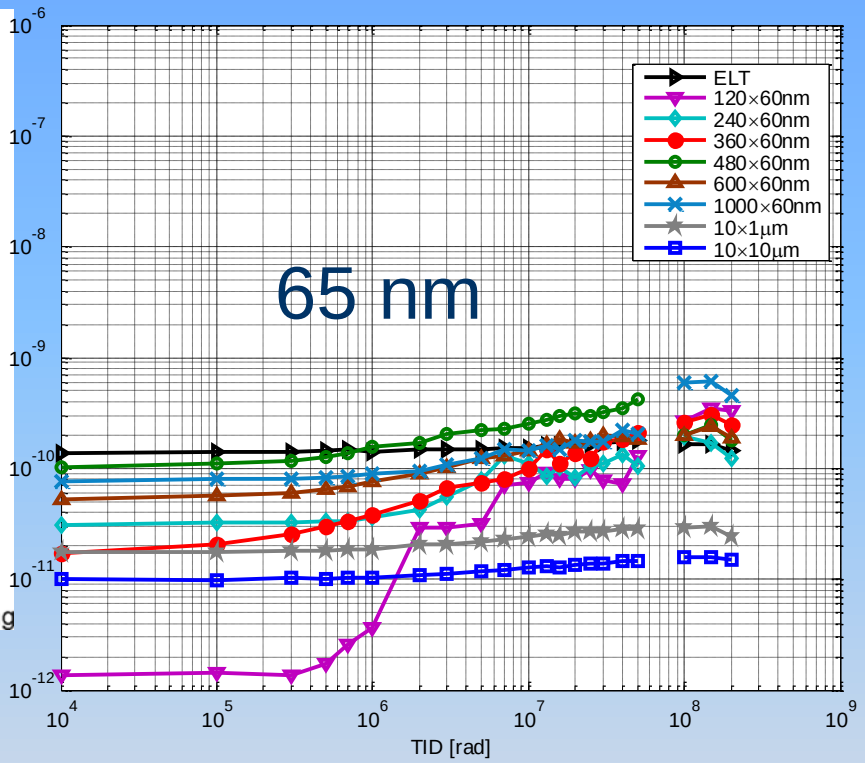
- *65 nm core devices seem to outperform their 130nm (delta VTH=20mV Vs 150mV for 0.13µ)*
- *Some indication that narrow transistors might be more affected*
- *136 Mrad only!*

65nm CORE NMOS Leakage current

Courtesy of Sandro Bonacini, CERN



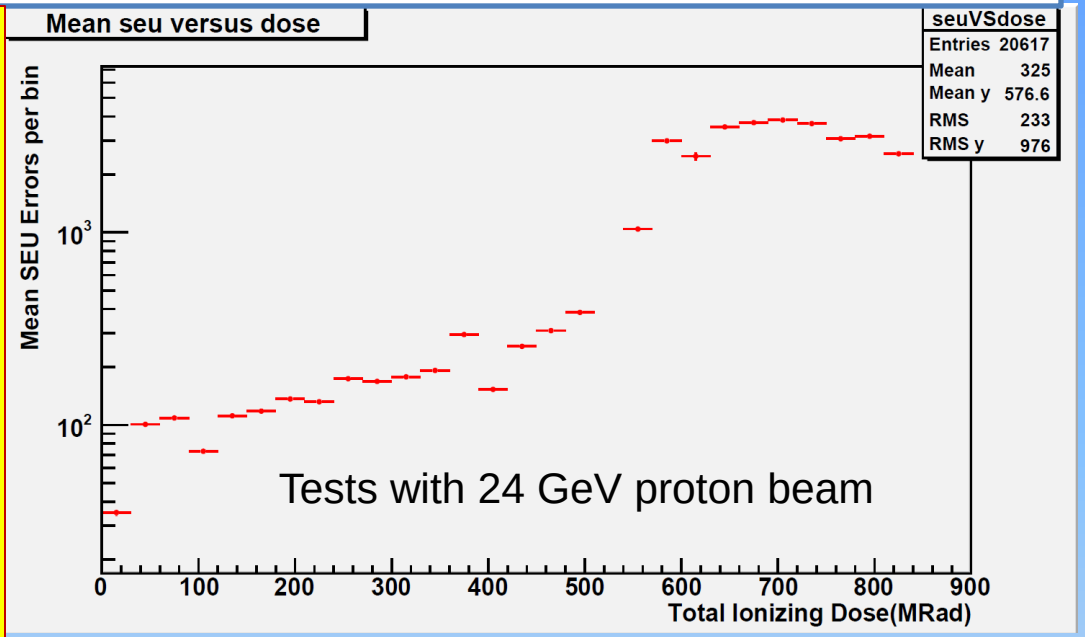
F.Faccio et al., "*Radiation-induced edge effects in deep submicron CMOS transistors*", IEEE Tr. Nucl. Sci. 2005

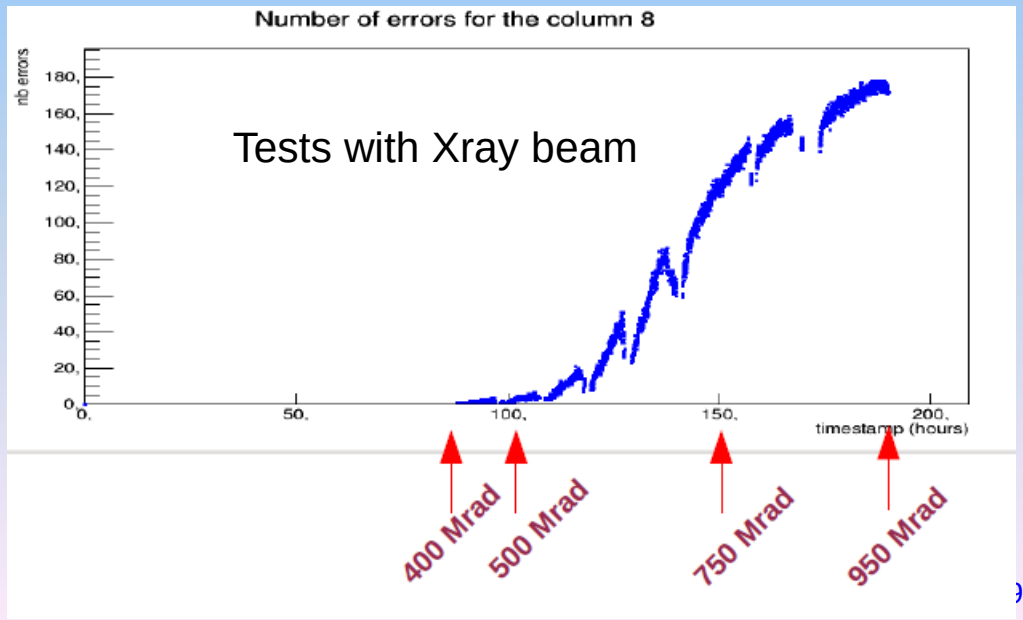


- 65nm has better performance with respect to 130nm: (Plots are in the same scale)
  - a rebound effect is visible in 130 nm:
  - all 130nm devices are peaking at ~100nA
  - Narrow devices increase I_{leak} by 3 orders of magnitude
  - I_{leak} is ~1nA @136 Mrad

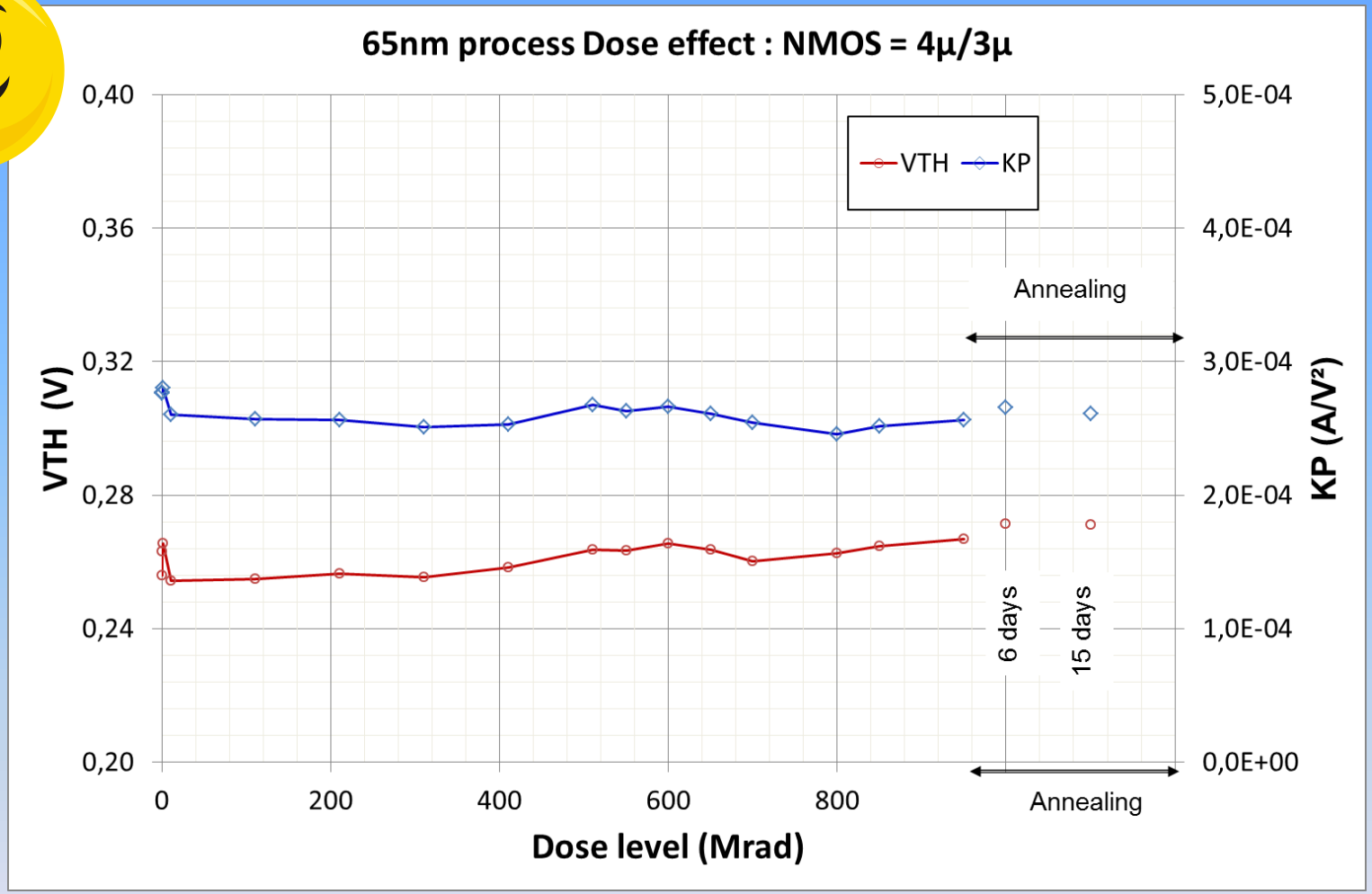
65nm CMOS radiation hardness: Another story

- Latches are triple redundant from the standard library
- SEU at low doses compares favorably with 0.13u custom designed SEU tolerant latches.
- Very high number of errors after 400Mrad
- These are not simple SEU errors.
- The readout output goes from working to working-with-errors to random to stuck.
- We concluded that after some critical cumulated dose the digital gates stop working. Why?
- These and subsequent measurement are from the ATPIX65 chip designed at LBL.
- This chip was not designed with radiation characterization in mind. It is neither thorough nor final.
- All results are courtesy of ***Mohsine Menouni*** from CPPM (France). Thanks



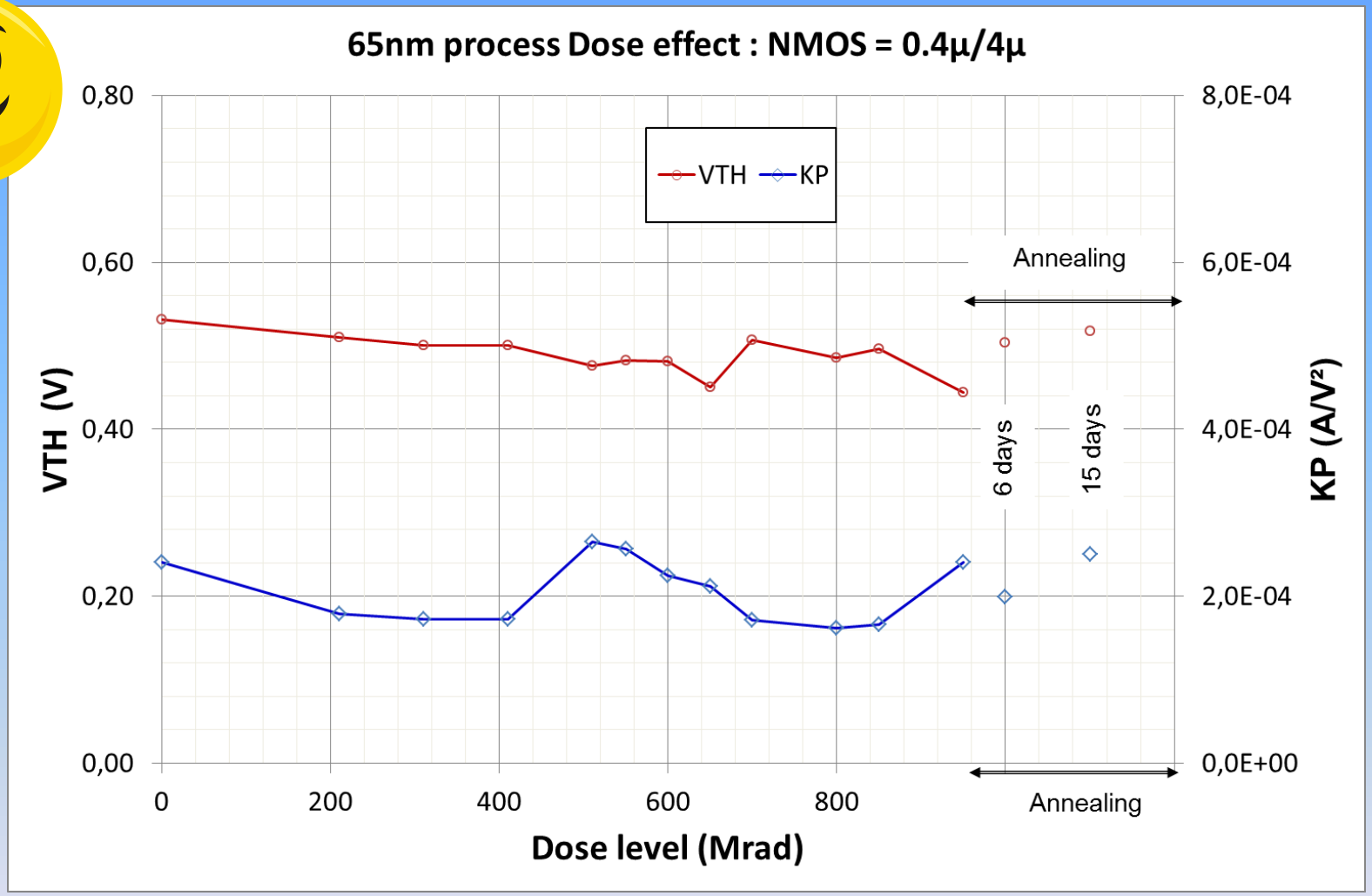


65nm CMOS radiation hardness



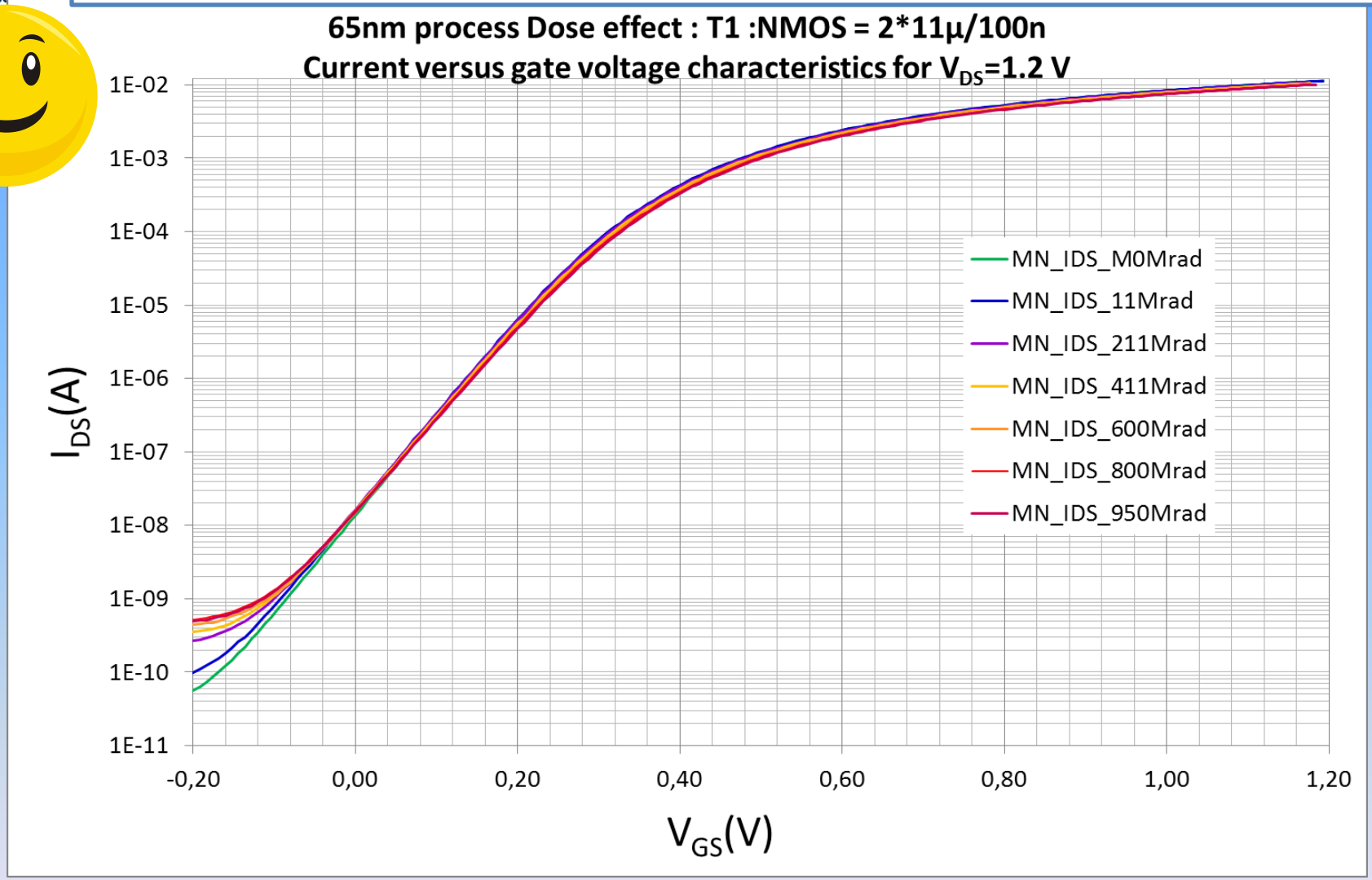
- VTH pre-Irrad = 0.256 V VTH(850 Mrad) = 0.267 V
- VTH maximum shift : -2 mV at 100 Mrad +10 mV at 950 Mrad
- KP maximum variation : 10% from 0 to 950 Mrad

65nm CMOS radiation hardness



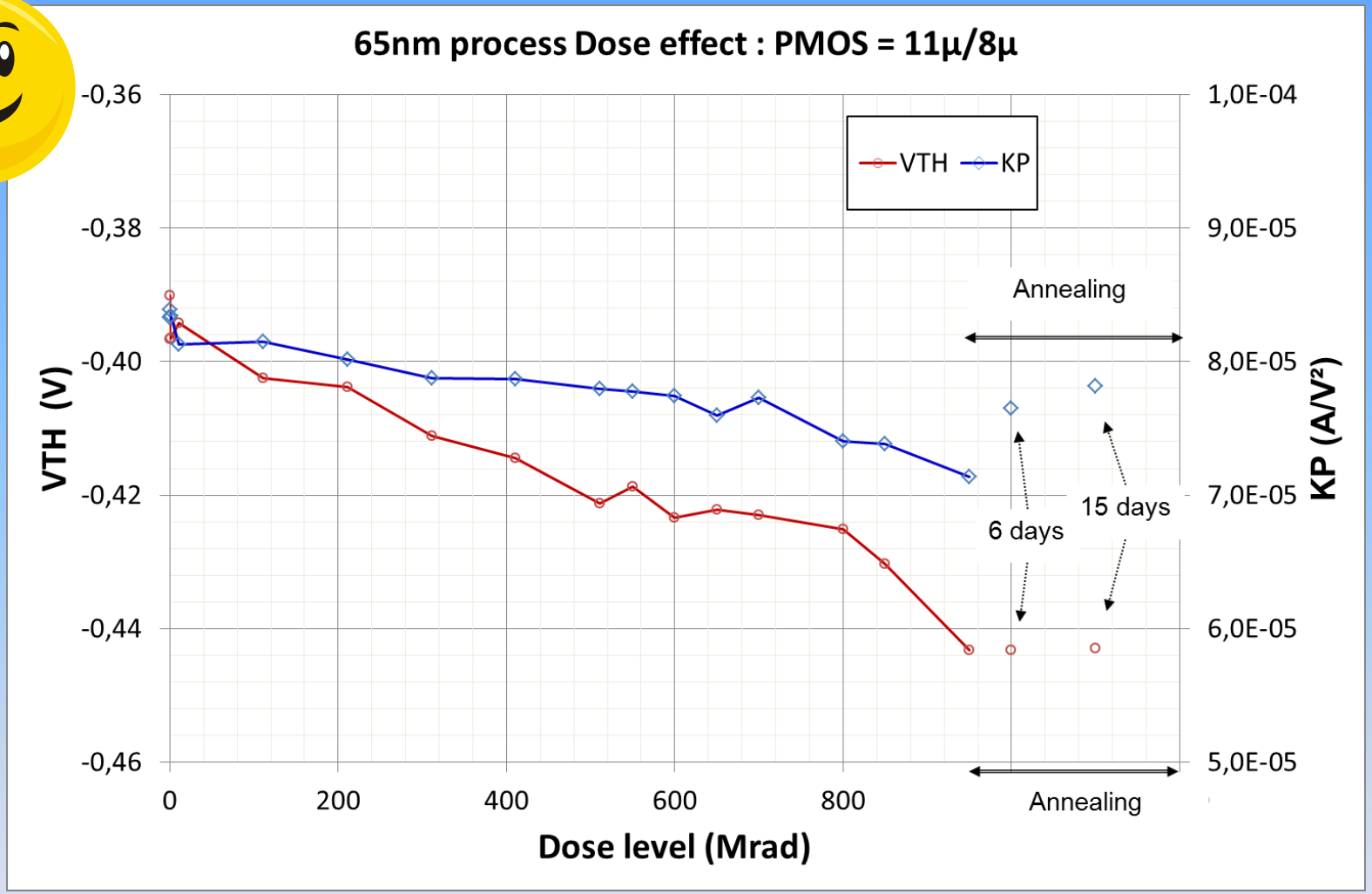
- VTH pre-Irrad = 0.532 V VTH(950 Mrad) = 0.444 V
- VTH shift : -88 mV at 950 Mrad
- KP variation : -30% at 850 Mrad and +10 % at 500 Mrad
- This is not really a narrow transistor.

65nm CMOS radiation hardness



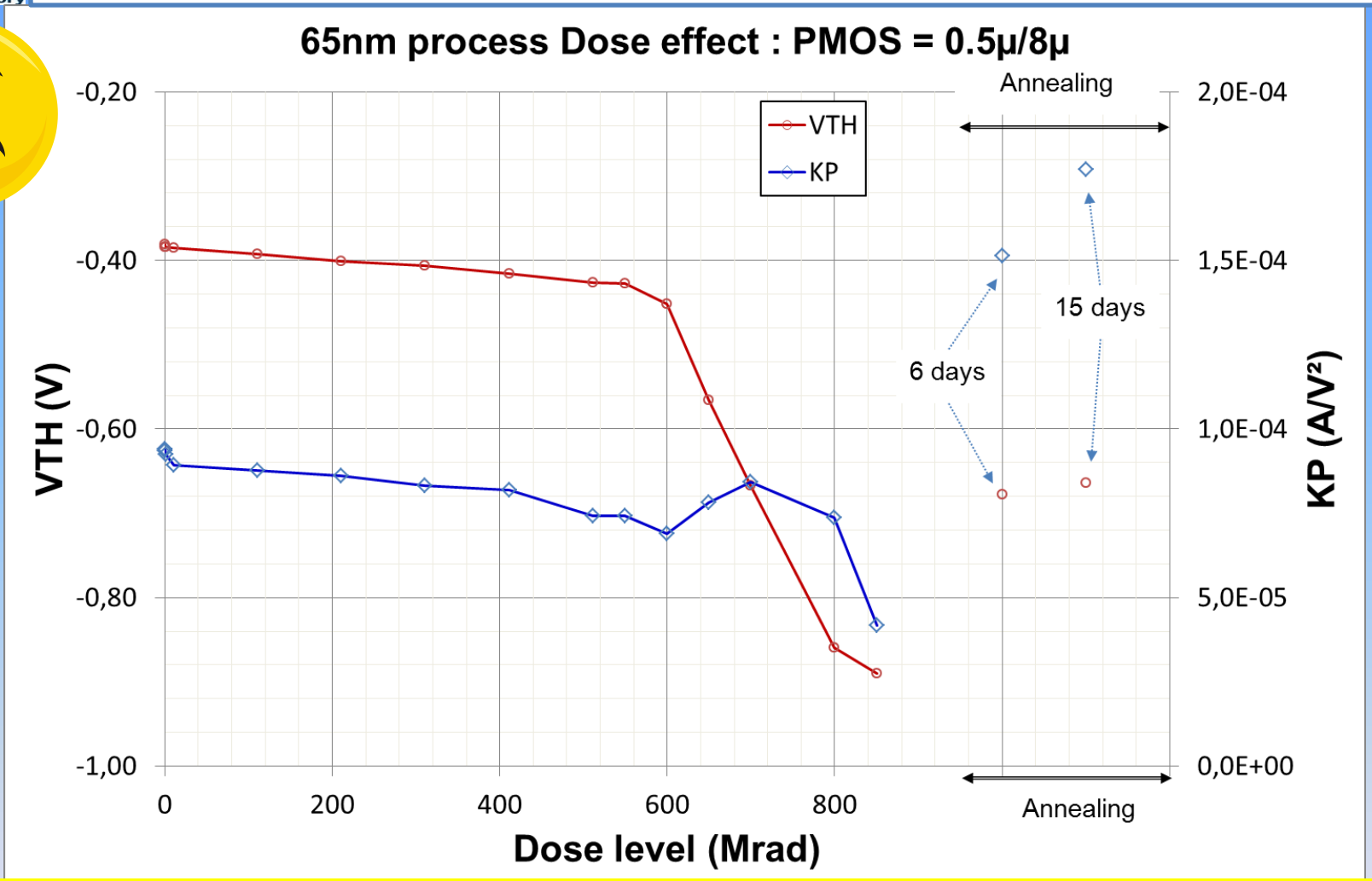
Acceptable leakage current even after 950Mrad.

65nm CMOS radiation hardness



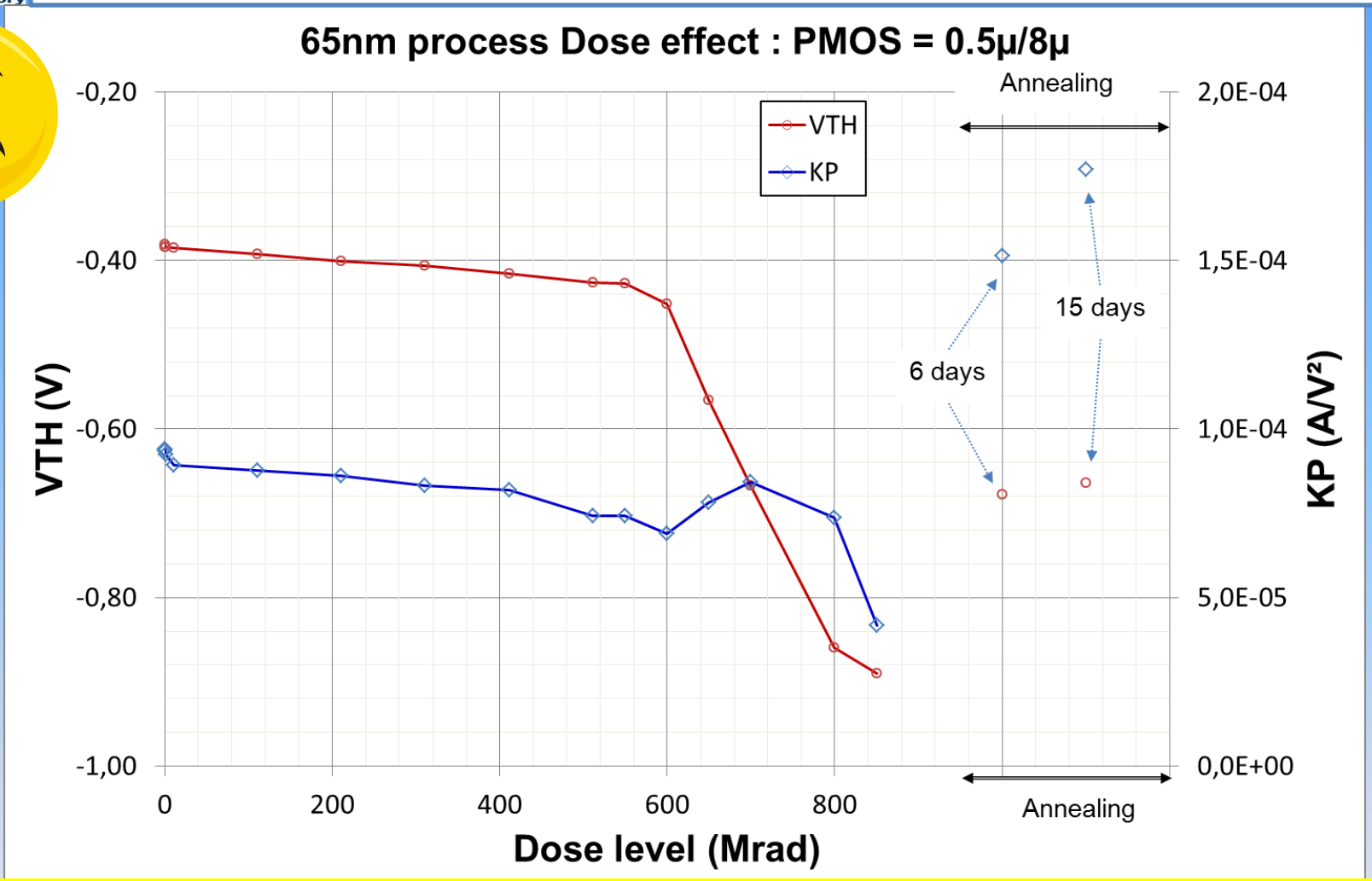
- VTH preIrrad = - 0.39 V VTH(950 Mrad) = -0.443 V
- VTH shift : -14 mV at 200 Mrad -35 mV at -800 Mrad -53 mV at 950 Mrad
- KP shift : -3.8% at 200 Mrad and -14 % at 950 Mrad

65nm CMOS radiation hardness



- VTH shift : -20 mV @ 200 Mrad -509 mV @ 850 Mrad
- KP shift : -8% @ 200 Mrad and -55 % @ 850 Mrad
- Is the annealing data good news ???? (to what extent)
- How about W<0.5u

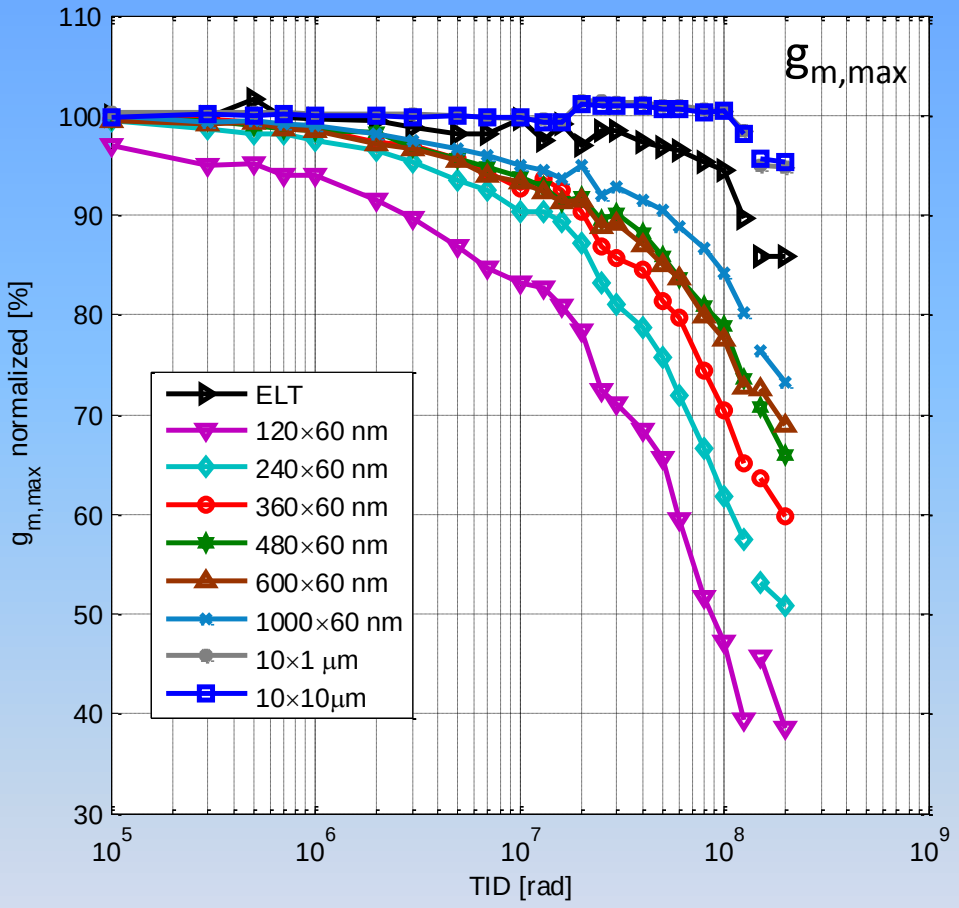
65nm CMOS radiation hardness

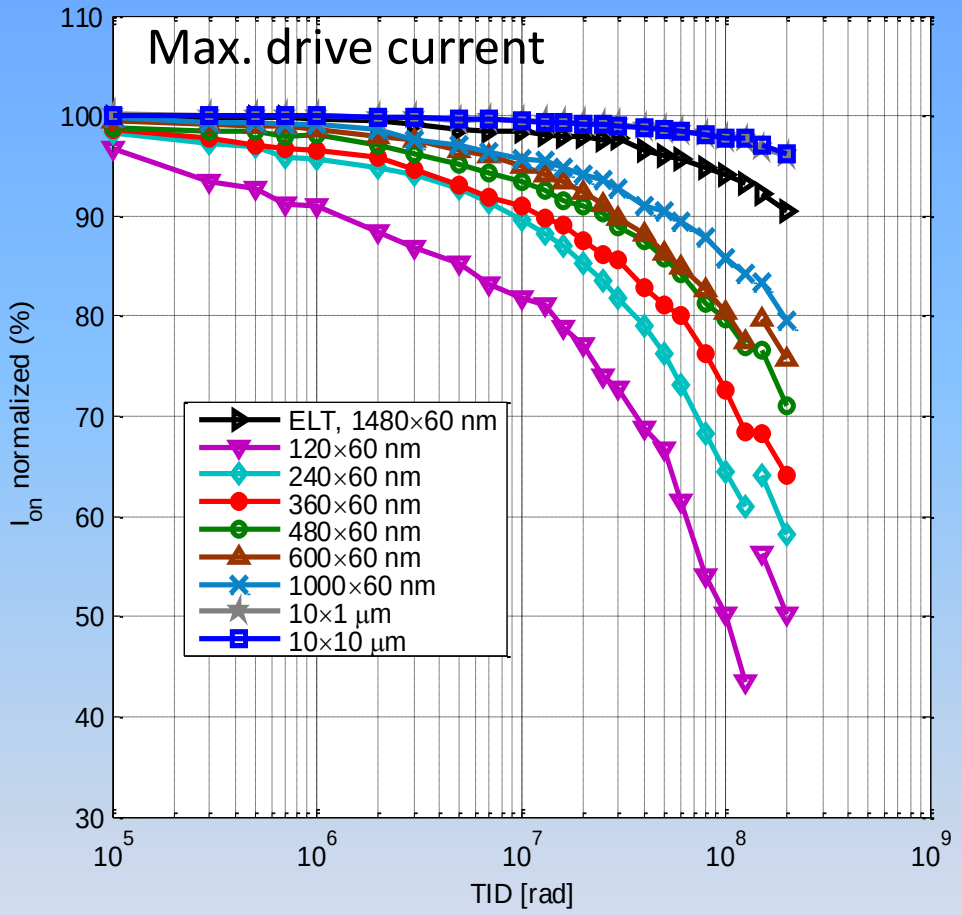


- VTH shift : -20 mV @ 200 Mrad -509 mV @ 850 Mrad
- KP shift : -8% @ 200 Mrad and -55 % @ 850 Mrad
- Is the annealing data good news ???? (to what entent?)
- How about W<0.5u

65nm PMOS problem (CERN's tests)

Courtesy of Sandro Bonacini, CERN





- Radiation kills maximum $g_{m,max}$ (strong inversion)
  - …but not g_m in weak inversion region
- Could influence the speed of digital logic
  - Affects only PMOS

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65nm CMOS radiation hardness: Conclusions

Based on this partial tests indicate that :

- *Overall 65nm CMOS looks very promising for the very high Radiation tolerance*
- *NMOS devices are potentially extremely radiation tolerant (up to 950Mrad).*
- *Wide PMOS transistors are also likely to be tolerant to the same level (arguably)*
- *Narrow PMOS devices are clearly the Achilles' heel for this process. This a very important limitation and need to be addressed.*
- *Standard digital libraries make extensive use of these devices.*
- *What is the minimum allowed????*
- *What is the loss, in terms of integration density, if one has to use a custom "standard" library with the required minimum widths.*
- *Library needs to be designed, and fully characterized, to be used by high level design tools.*
- *Is this a major setback?*
- *Our (CPPM+LBNL) evaluation is limited to the devices available only. To be complete and final the evaluation has to be based on a specially designed chip. (a la CERN +)*
- *A major effort is still needed to fully be comfortable with this process for radiation levels @ the Grad and beyond. Temperature and rate effects need to be addressed!*
- *See CERN's presentations and papers for more about the radiation of the process they characterized*

Hardness of SiGe Bipolar transistors?

	G25H1 Ft=190GHz BVCEO=1.9	SG25H3 Ft=120GHz BVCEO=2.3	SGB25VD Ft=45GHz BVCEO=4
PreIrrad	266	159	199
50Mrad	37	51	61
1Grad	?	?	?

Table I: Transistor gain values @VBE = 0.7 V for gamma irradiations

	G25H1 Ft=190GHz BVCEO=1.9	SG25H3 Ft=120GHz BVCEO=2.3
PreIrrad	137	88
5e14 n/cm2	54	30
1e15 n/cm2	42	25
2e16	?	?

Table 2: Transistor gain values @VBE = 0.7 V for neutron irradiations

M. Ullán et. al., "Radiation Hardness Evaluation of SiGe Technologies for the Front-End Electronics of the ATLAS Upgrade"

Conclusions

Designing reliable high yield ICs is getting more challenging at the advanced technology nodes

Radiation effects add another dimension to this complexity

Fully qualifying modern complex technologies is a major undertaking. Collective multi institution efforts are needed.

Prototyping is very expensive: radiation damage knowledge will reduce the cost of the R/D efforts.

Keeping up with industry is extremely challenging/impossible. It is necessary that the "phase" does not grow with time.

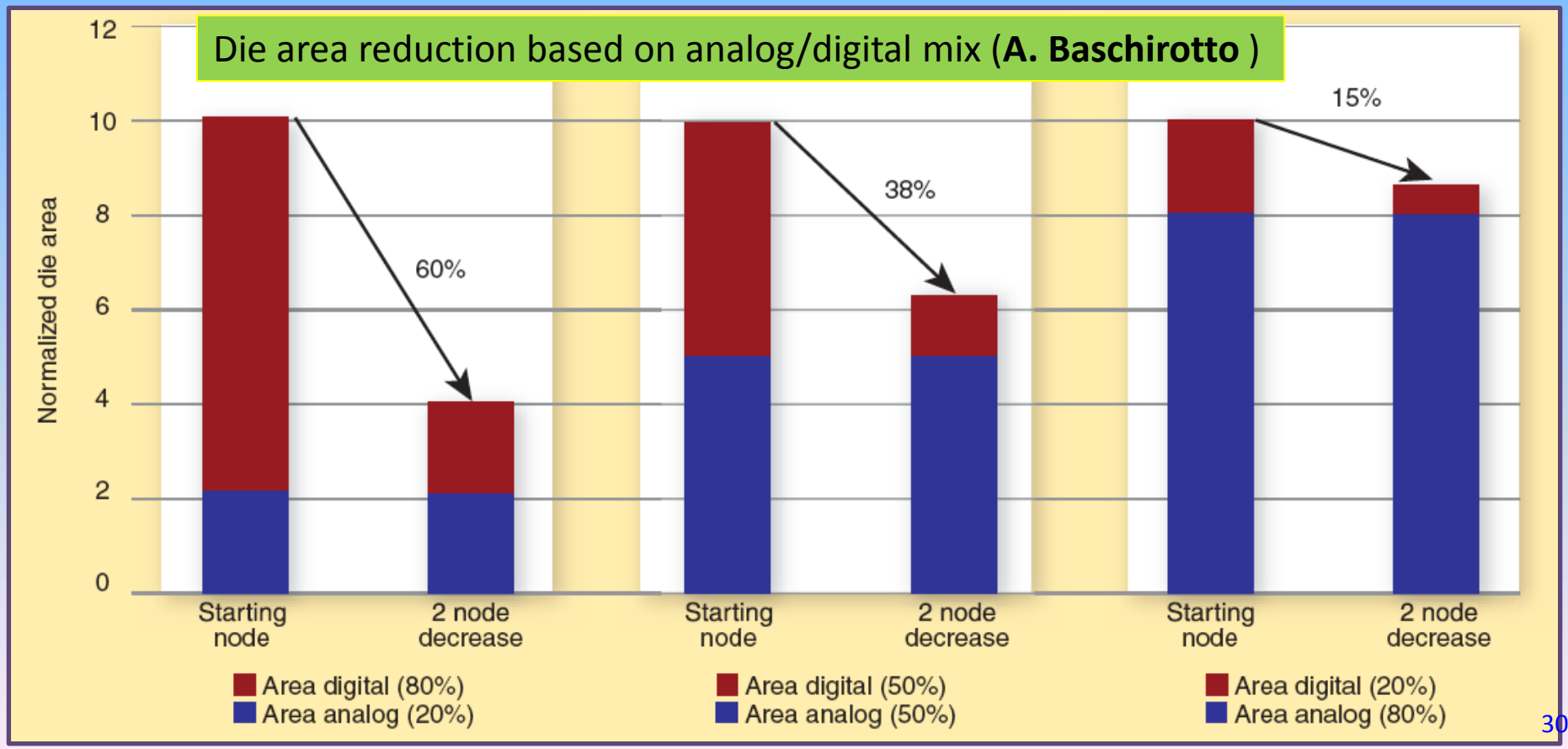
Don't burry the "old" good 0.13μ and Co. For many sub-systems it might just be the optimum process for many systems(personal bias).

Future chips tend to be mostly “digital”

The trend is to reduce analog functionality to the minimum to benefit from the ever increasing integration density in advanced process. Will most likely (not necessarily) increase radiation tolerance of complex chips

(not necessarily): TID effects could be fatal for digital blocks. Analog dies gracefully

Configurability a blessing that should not turn into a curse (too many bits)



65nm ATPIX radiation results

	0 rad (Chip2)	~70 Mrad (chip2)	>600 Mrad (chip3)	
Vbp1 (pmos)	525	474	440	@250 nA
Vbp2 (pmos)	620	609	586	@2 uA
Vbn1 (nmos)	636	623	648	@1uA
Vbn2 (nmso)	238	237	236	@1uA
Vbn3 (nmos)	277	274	276	@0.5uA

- VG of diode connected transistors at fixed current (in mV)
- Different size transistors
- Small/negligible change in threshold voltages of PMOSs/NMOSs
- PMOS threshold variation more pronounced!
- Some measurement errors in the low current regime (meter impedance and esd diodes leakage)

65nm ATPIX radiation results (2)